PF1550

Power management integrated circuit (PMIC) for low power application processors

Rev. 7 — 29 September 2021 Product data sheet

1 General description

The PF1550 is a power management integrated circuit (PMIC) designed specifically for use with i.MX processors on low-power portable, smart wearable and Internet-of-Things (IoT) applications. It is also capable of providing full power solution to i.MX 7ULP, i.MX 6SL, 6UL, 6ULL, and 6SX processors.

With three high-efficiency buck converter, three linear regulators, RTC supply, and battery linear charger, the PF1550 can provide power for a complete battery-powered system, including application processors, memory, and system peripherals.

1.1 Features and benefits

This section summarizes the PF1550 features:

- Input voltage range to PMIC VBUSIN pin via USB bus or AC adapter: 4.1 V to 6.0 V
- Buck converters:
  - SW1, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW2, 1.0 A; 0.6 V to 1.3875 V in 12.5 mV steps, or 1.1 V to 3.3 V in variable steps
  - SW3, 1.0 A; 1.8 V to 3.3 V in 100 mV steps
  - Soft start
  - Quiescent current 1.0 μA in ULP mode with light load
  - Peak efficiency > 90 %
  - Dynamic voltage scaling on SW1 and SW2
  - Modes: forced PWM quasi-fixed frequency mode, adaptive variable-frequency mode
  - Programmable output voltage, current limit, and soft start
- LDO regulators
  - LDO1, 0.75 V to 1.5 V/1.8 to 3.3 V, 300 mA with load switch mode
  - LDO2, 1.8 V to 3.3 V, 400 mA
  - LDO3, 0.75 V to 1.5 V/1.8 V to 3.3 V, 300 mA with load switch mode
  - Quiescent current < 1.5 μA in Low-power mode
  - Programmable output voltage
  - Soft start and ramp
  - Current limit protection

- Battery charger
  - Supports single-cell Lithium Ion/Lithium Polymer batteries
  - Linear charging (10 mA to 1500 mA input limit)
  - Up to 6.5 V input operating range
  - VSYS regulator can withstand transient and DC inputs from 0 V up to +22 V
  - Programmable charge voltage (3.5 V to 4.44 V)
  - Programmable charge current (100 mA to 1000 mA)
  - Programmable charge termination current (5.0 mA to 50 mA)
  - Integrated 50 mΩ battery isolation MOSFET for operation with no/low battery
  - Battery supplement mode
  - Battery discharge overcurrent protection, up to 3.0 A
  - USB_PHY low dropout linear regulator
  - Programmable LED driver (status indicator)
  - JEITA-compliant battery temp sensing and charger control
  - Key charging parameters can be configured and permanently stored in OTP
  - I^2C Control Interface permitting processor control and event detection
- LDO/switch supply
  - RTC supply VSNVS 3.0 V, 2.0 mA
  - Battery backed memory including coin cell charger
- DDR memory reference voltage, VREFDDR, 0.5 V to 0.9 V, 10 mA
- OTP (One time programmable) memory for device configuration
  - User programmable start-up sequence, timing, soft-start, and power-down sequence
  - Programmable regulator output voltages and charger parameters
- I^2C interface
- User programmable Standby, Sleep/Low-power, and Off (REGS_DISABLE) modes
- Ambient temperature range −40 °C to 105 °C

1.2 Applications

- Smart mobile/wearable devices
- Low-power IoT applications
- Wireless game controllers
- Embedded monitoring systems
- Home automation
- POS
- E-Read

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2 Application diagram

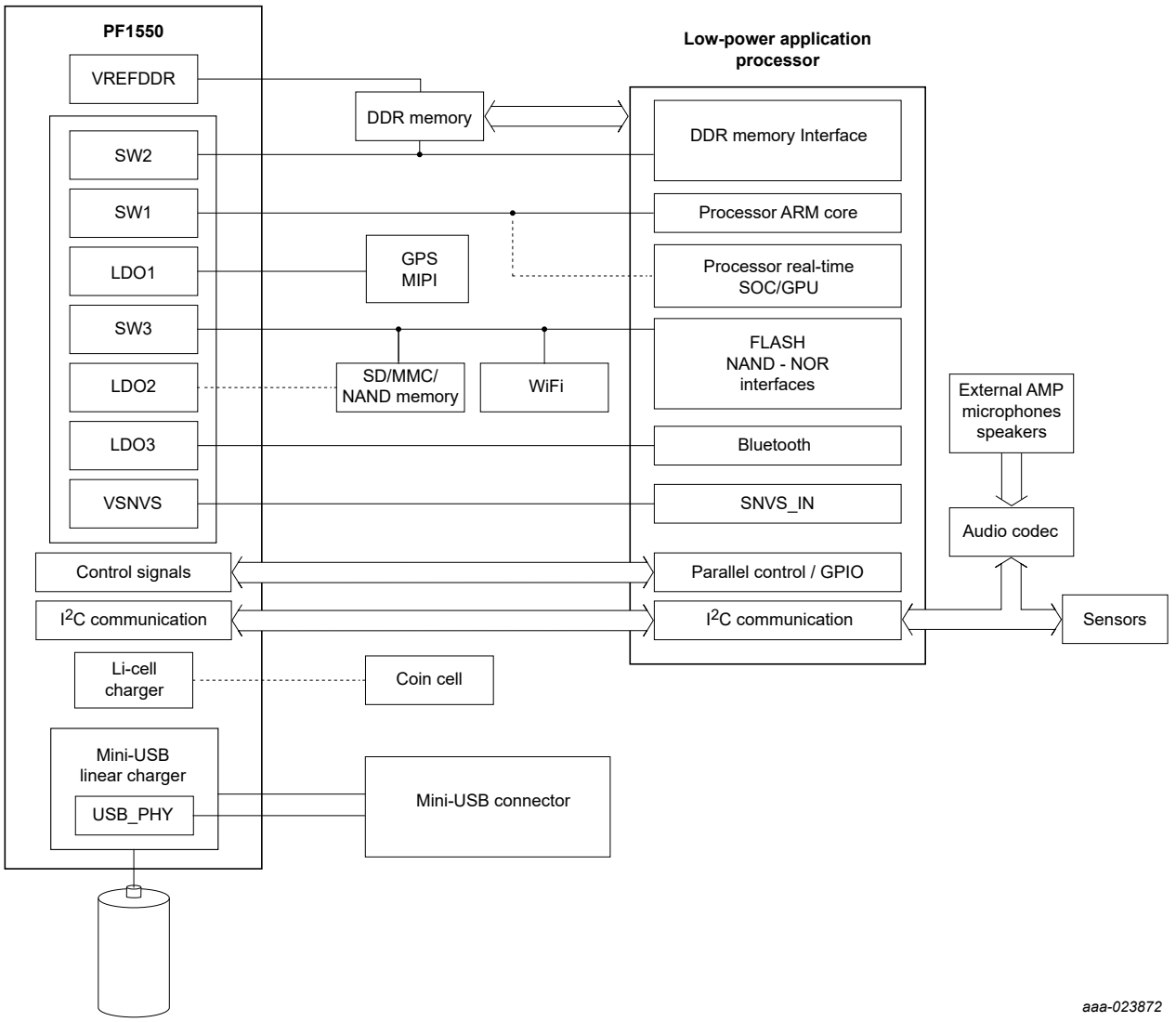

Figure 1. Application diagram

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2.1 Functional block diagram

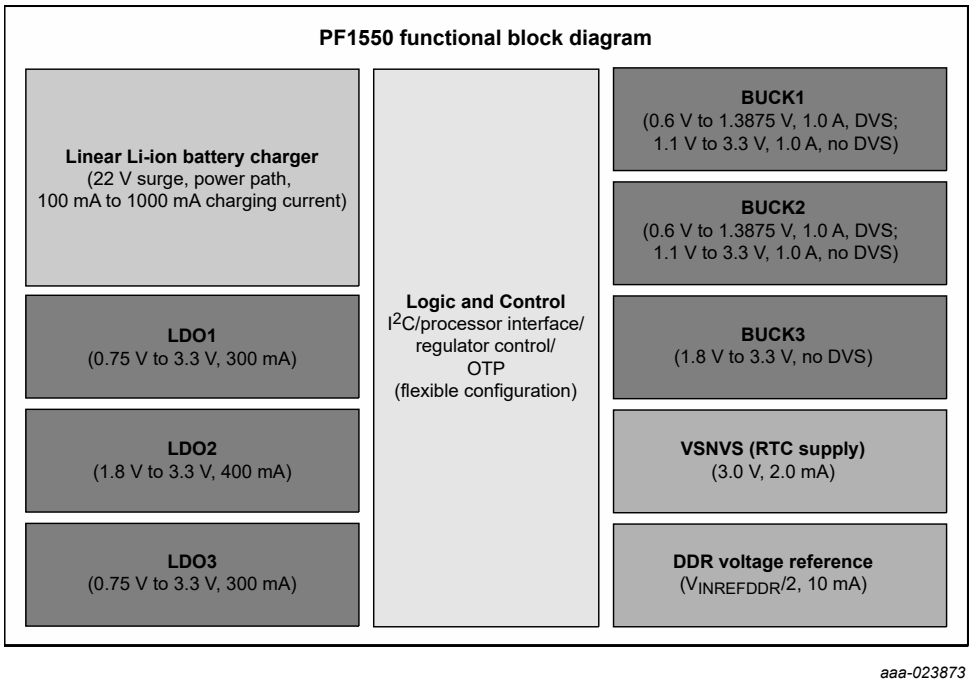

Figure 2. Functional block diagram

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2.2 Internal block diagram

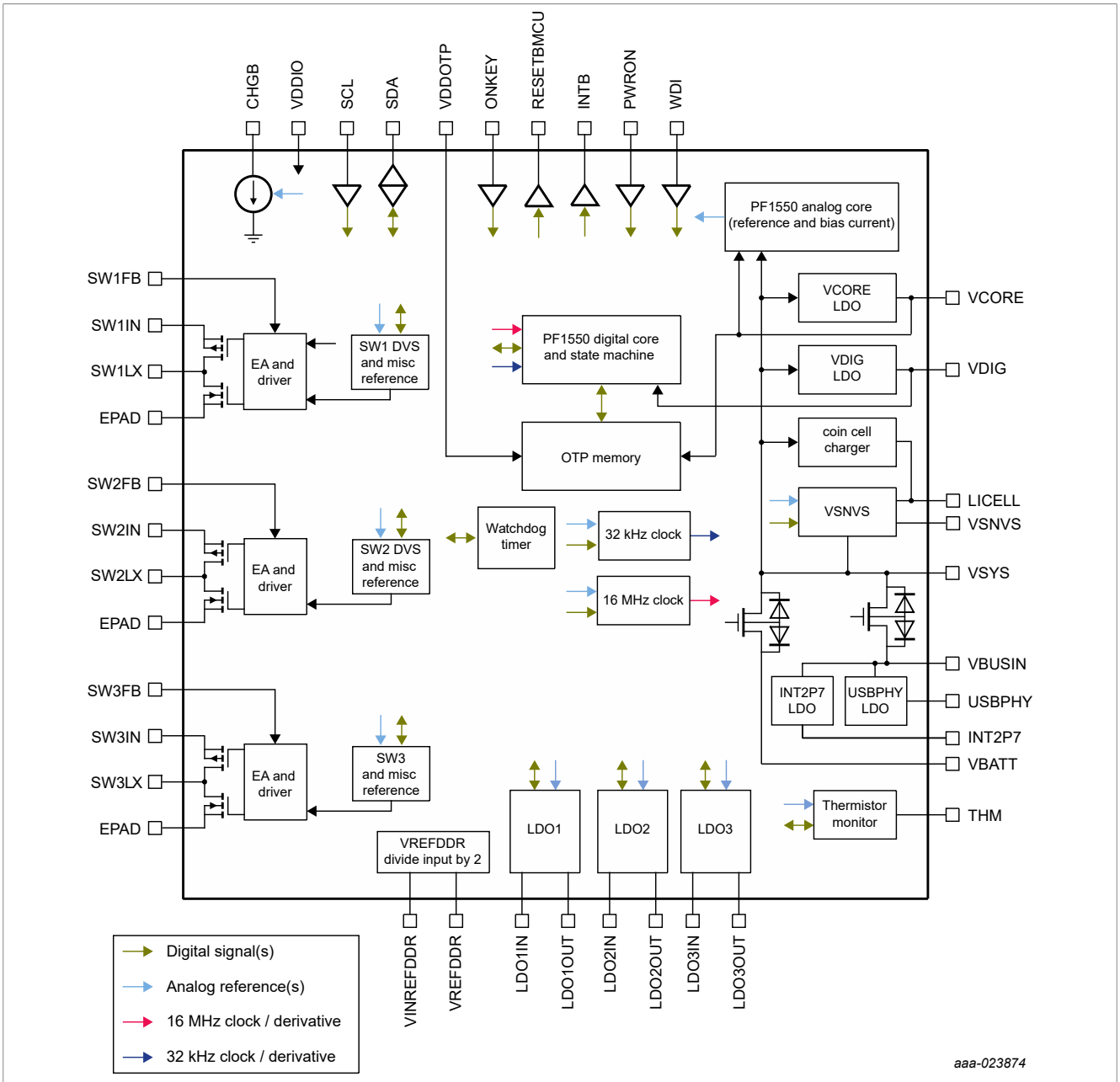

Figure 3. Internal block diagram

3 Orderable parts

The PF1550 is available only with preprogrammed configurations. These preprogrammed devices are identified using the program code from Table 1, which also list the associated NXP reference designs where applicable. Details of the OTP programming for each device can be found in Table 85.

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Table 1. Orderable part variations

Part number[1]	Temperature (T_A)	Package	Programming options
MC32PF1550A0EP	−40 °C to 85 °C (for use in consumer applications)	98ASA00913D, 40-pin QFN 5.0 mm x 5.0 mm with exposed pad	0 - Not programmed
MC32PF1550A1EP			1 (Default)
MC32PF1550A2EP			2 (i.MX 7ULP with LPDDR3) [2]
MC32PF1550A3EP			3 (i.MX 6UL with DDR3L)
MC32PF1550A4EP			4 (i.MX 7ULP with LPDDR3)
MC32PF1550A5EP			5 (i.MX 6UL with DDR3)
MC32PF1550A6EP			6 (i.MX 6ULL with DDR3L)
MC32PF1550A7EP			7 (i.MX 6UL with LPDDR2)
MC32PF1550A8EP			8 (i.MX 6UL with DDR3L, Edge Sensitive)
MC32PF1550A9EP			9 (i.MX RT1050)
MC34PF1550A0EP	−40 °C to 105 °C (for use in industrial applications)		0 - Not programmed
MC34PF1550A1EP			1 (Default)
MC34PF1550A2EP			2 (i.MX 7ULP with LPDDR3) [2]
MC34PF1550A3EP			3 (i.MX 6UL with DDR3L)
MC34PF1550A4EP			4 (i.MX 7ULP with LPDDR3)
MC34PF1550A5EP			5 (i.MX 6UL with DDR3)
MC34PF1550A6EP			6 (i.MX 6ULL with DDR3L)
MC34PF1550A7EP			7 (i.MX 6UL with LPDDR2)
MC34PF1550A8EP			8 (i.MX 6UL with DDR3L, Edge Sensitive)
MC34PF1550A9EP			9 (i.MX RT1050)

[1] For tape and reel, add an R2 suffix to the part number.
[2] For internal validation only

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4 Pinning information

4.1 Pinning

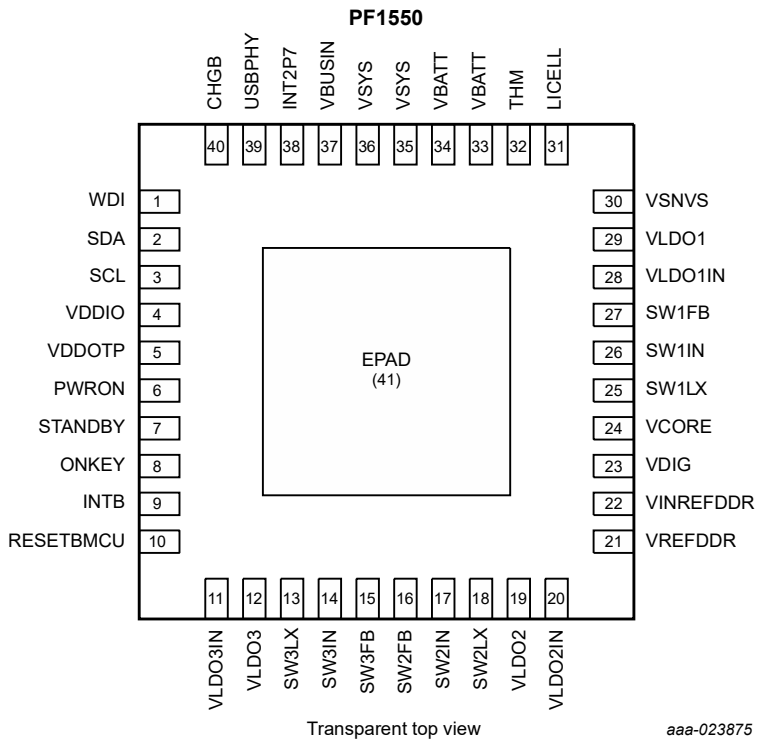

Figure 4. Pinout diagram

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4.2 Pin definitions

Table 2. Pin description

Pin number	Pin name	Block	Description
1	WDI	I/Os	Watchdog input from processor
2	SDA		SDA when used in I^2C mode
3	SCL		SCL when used in I^2C mode
4	VDDIO		I/O supply voltage Connect to voltage rail between 1.7 V and 3.3 V
5	VDDOTP	VDDOTP	Connect to ground in application
6	PWRON	I/Os	PWRON input
7	STANDBY		STANDBY input
8	ONKEY		ONKEY push-button input
9	INTB		INTB open-drain output
10	RESETBMCU		RESETBMCU open-drain output
11	VLDO3IN	LDO3	LDO3 input supply
12	VLDO3		LDO3 output
13	SW3LX	Buck 3	Buck 3 switching node
14	SW3IN		Buck 3 input supply
15	SW3FB		Buck 3 output voltage feedback
16	SW2FB	Buck 2	Buck 2 output voltage feedback
17	SW2IN		Buck 2 input supply
18	SW2LX		Buck 2 switching node
19	VLDO2	LDO2	LDO2 output
20	VLDO2IN		LDO2 input supply
21	VREFDDR	VREFDDR	VREFDDR output
22	VINREFDDR		VREFDDR input supply
23	VDIG	IC core	VDIG regulator output (used within PF1550)
24	VCORE		VCORE regulator output (used within PF1550)
25	SW1LX	Buck 1	Buck 1 switching node
26	SW1IN		Buck 1 input supply
27	SW1FB		Buck 1 feedback input
28	VLDO1IN	LDO1	LDO1 input supply
29	VLDO1		LDO1 output
30	VSNVS	VSNVS	VSNVS regulator output
31	LICELL		Coin cell input
32	THM	CHARGER	Thermistor connection Connect thermistor to ground from this pin
33	VBATT		Battery input
34			
35	VSYS	IC core	Main input voltage to PMIC and output of charger
36			

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Table 2. Pin description...*continued*

Pin number	Pin name	Block	Description
37	VBUSIN	CHARGER	Charger input
38	INT2P7		INT2P7 regulator output (used within PF1550 and as thermistor bias)
39	USBPHY		USBPHY regulator output
40	CHGB		Charger LED input connection Connect LED from VSYS to this pin
41	EPAD	EPAD	Exposed pad Connect to ground

5 General product characteristics

5.1 Thermal characteristics

Table 3. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
THERMAL RATINGS				
T_A	Ambient operating temperature range (industrial) Ambient operating temperature range (consumer)	−40 −40	105 85	°C
T_J	Operating junction temperature range [1]	−40	125	°C
T_{ST}	Storage temperature range	−65	150	°C
T_{PPRT}	Peak package reflow temperature [2] [3]	—	—	°C
QFN40 THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS				
$R_{\Theta JA}$	Junction to ambient thermal resistance, natural convection [4] [5] [6] Four layer board (2s2p) Six layer board (2s4p) Eight layer board (2s6p)	—	 27 20.6 17.8	°C/W
$R_{\Theta JMA}$	Junction to ambient (@200 ft/min) [4] [6] Four layer board (2s2p)	—	 21.4	°C/W
$R_{\Theta JB}$	Junction to board [7]	—	8.8	°C/W
$R_{\Theta JCBOTTOM}$	Junction to case bottom [8]	—	1.4	°C/W
Ψ_{JT}	Junction to package top – Natural convection [9]	—	0.6	°C/W

[1] Do not operate beyond 125 °C for extended periods of time. Operation above 150 °C may cause permanent damage to the IC. See Thermal Protection Thresholds for thermal protection features.
[2] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
[3] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For peak package reflow temperature and moisture sensitivity levels (MSL), go to http://www.nxp.com, search by part number, and enter the core ID to view all orderable parts (for MC33xxxD enter 33xxx), and review parametrics.
[4] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[5] The Board uses the JEDEC specifications for thermal testing (and simulation) JESD51-7 and JESD51-5.
[6] Per JEDEC JESD51-6 with the board horizontal.
[7] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[8] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[9] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

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5.2 Absolute maximum ratings

Table 4. Maximum ratings

Symbol	Description (Rating)	Min	Max	Unit
I/Os				
VDDIO	I/O supply voltage. Connect to voltage rail between 1.7 V and 3.3 V.	−0.3	3.6	V
SCL	SCL when used in I^2C mode. SCLK when used in SPI mode.	−0.3	3.6	V
SDA	SDA when used in I^2C mode. MISO when used in SPI mode.	−0.3	3.6	V
RESETBMCU	RESETBMCU open-drain output	−0.3	3.6	V
PWRON	PWRON input	−0.3	3.6	V
STANDBY	STANDBY input	−0.3	3.6	V
ONKEY	ONKEY push-button input	−0.3	4.8	V
INTB	INTB open-drain output	−0.3	3.6	V
WDI	Watchdog input from processor	−0.3	3.6	V
VDDOTP				
VDDOTP	Connect to ground in the application	−0.3	10	V
BUCK 1				
SW1IN	Buck 1 input supply	−0.3	4.8	V
SW1LX	Buck 1 switching node	−0.3	4.8	V
SW1FB	Buck 1 feedback input	−0.3	3.6	V
BUCK 2				
SW2IN	Buck 2 input supply	−0.3	4.8	V
SW2LX	Buck 2 switching node	−0.3	4.8	V
SW2FB	Buck 2 output voltage feedback	−0.3	3.6	V
BUCK 3				
SW3IN	Buck 3 input supply	−0.3	4.8	V
SW3LX	Buck 3 switching node	−0.3	4.8	V
SW3FB	Buck 3 output voltage feedback	−0.3	3.6	V
LDO1				
VLDO1IN	LDO1 input supply	−0.3	4.8	V
VLDO1	LDO1 output	−0.3	3.6	V
LDO2				
VLDO2IN	LDO2 input supply	−0.3	4.8	V
VLDO2	LDO2 output	−0.3	3.6	V
LDO3				
VLDO3IN	LDO3 input supply	−0.3	4.8	V
VLDO3	LDO3 output	−0.3	3.6	V
VSNVS				
VSNVS	VSNVS regulator output	−0.3	3.6	V

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Table 4. Maximum ratings...*continued*

Symbol	Description (Rating)	Min	Max	Unit
LICELL	Coin cell input	−0.3	3.6	V
CHARGER				
VBATT	Battery input	−0.3	4.8	V
INT2P7	INT2P7 regulator output (used within PF1550 and as thermistor bias)	−0.3	3.6	V
THM	Thermistor connection. Connect thermistor to ground from this pin.	−0.3	3.6	V
VBUSIN	Charger input	−0.3	24	V
USBPHY	USBPHY regulator output	−0.3	5.5	V
CHGB	Charger LED input connection. Connect LED from VSYS to this pin.	−0.3	4.8	V
INPUT/OUTPUT SUPPLY				
VINREFDDR	VREFDDR input supply	−0.3	3.6	V
VREFDDR	VREFDDR output	−0.3	3.6	V
IC CORE				
VSYS	Main input voltage to PMIC and output of charger	−0.3	4.8	V
VDIG	VCOREDIG regulator output (used within PF1550)	−0.3	1.65	
VCORE	VCORE regulator output (used within PF1550)	−0.3	1.65	V
ELECTRICAL RATINGS				
V_{ESD}	ESD ratings			V
	Human body model [1]	—	±2000	
	Charge device model (corner pins)	—	±750	
	Charge device model (all other pins)	—	±500	

[1] Testing is performed in accordance with the human body model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the charge device model (CDM), Robotic (C_{ZAP} = 4.0 pF).

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5.3 Electrical characteristics

5.3.1 Electrical characteristics – Battery charger

All parameters are specified at T_A = −40 °C to 105 °C, VBUSIN = 5.0 V, VSYS = 3.7 V, typical external component values, unless otherwise noted. Typical values are characterized at VBUSIN = 5.0 V, VSYS = 3.7 V and 25 °C, unless otherwise noted.

Table 5. Global conditions

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
CHARGER INPUTS						
V_{BUS}	VBUSIN voltage range	Operating voltage	V_{UVLO}	—	V_{OVLO}	V
$V_{BUS_WITHSTAND}$	VBUSIN maximum withstand voltage rating		—	—	22	V
V_{BUS_OVLO}	VBUSIN overvoltage threshold	Rising	6.0	6.5	7.0	V
V_{OVLO_HYS}	VBUSIN overvoltage threshold hysteresis	Falling	50	150	250	mV
$t_{D\text{-}OVLO}$	VBUSIN overvoltage delay		5.0	10	15	µs
V_{UVLO}	VBUSIN to GND minimum turn on threshold accuracy	VBUS rising	3.8	4.0	4.2	V
$V_{UVLO\text{-}HYS}$	VBUSIN UVLO hysteresis		400	500	600	mV
V_{IN2SYS_50}	VBUSIN to VSYS minimum turn on threshold accuracy	VBUS_LIN rising, 50 mV setting	20	50	80	mV
V_{IN2SYS_175}	VBUSIN to VSYS minimum turn on threshold accuracy	VBUS_LIN rising, 175 mV setting	100	175	250	mV
$V_{BUS_LIN_DPM_REG}$	VBUSIN adaptive voltage regulation threshold	4.4 V setting (default)	4.3	4.4	4.5	V
V_{DPM_REG}	VBUSIN adaptive voltage regulation threshold accuracy	Programmable at 3.9 V to 4.6 V	−100	—	100	mV

Table 6. Input currents

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
VBUSIN INPUT CURRENT LIMIT						
$ILIM_{10}$	Charger input current limit (10 mA settings)	10 mA	6.0	8.5	11	mA
$ILIM_{15}$	Charger input current limit (15 mA settings)	15 mA	10.5	12.75	16	mA
$ILIM_{20}$	Charger input current limit (20 mA settings)	20 mA	14	17	21	mA
$ILIM_{25}$	Charger input current limit (25 mA settings)	25 mA	17.5	21.25	26	mA
$ILIM_{30}$	Charger Input Current Limit (30 mA setting)	30 mA	21	25.5	30	mA
$ILIM_{35}$	Charger input current limit (35 mA settings)	35 mA	24.5	29.75	35	mA
$ILIM_{40}$	Charger input current limit (40 mA settings)	40 mA	28	34	40	mA
$ILIM_{45}$	Charger input current limit (45 mA settings)	45 mA	31.5	38.25	45	mA
$ILIM_{50}$	Charger input current limit (50 mA settings)	50 mA	35	42.5	50	mA
$ILIM_{100}$	Charger input current limit (100 mA settings)	100 mA	85	95	105	mA

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Table 6. Input currents...*continued*

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$ILIM_{150}$	Charger input current limit (150 mA settings)	150 mA	125	137.5	160	mA
$ILIM_{200}$	Charger input current limit (200 mA settings)	200 mA	170	190	210	mA
$ILIM_{300}$	Charger input current limit (300 mA setting)	300 mA	260	285	320	mA
$ILIM_{400}$	Charger input current limit (400 mA settings)	400 mA	345	380	425	mA
$ILIM_{500}$	Charger input current limit (500 mA settings)	500 mA	430	475	530	mA
$ILIM_{600}$	Charger input current limit (600 mA settings)	600 mA	520	570	640	mA
$ILIM_{700}$	Charger input current limit (700 mA settings)	700 mA	610	665	750	mA
$ILIM_{800}$	Charger input current limit (800 mA settings)	800 mA	690	760	850	mA
$ILIM_{900}$	Charger input current limit (900 mA settings)	900 mA	780	855	950	mA
$ILIM_{1000}$	Charger input current limit (1000 mA settings)	1000 mA	855	950	1100	mA
$ILIM_{1500}$	Charger input current limit (1500 mA settings)	1500 mA	1260	1400	1700	mA
R_{INSD}	Input self-discharge resistance		18	30	42	kΩ
$I_{BATTLEAK}$	Leakage current	Leakage current from VBATT to VBUSIN. VBATT = 4.2 V, BATFET closed, VBUSIN = 0 V. Current measured into VBATT pin at 25 °C	0	—	5.0	μA
$I_{Q_CHARGER}$	Charger quiescent current (BATFET enabled, normal mode)	25 °C only; charger in CC state; ICC = 100 mA	0	2.5	5.0	mA
$I_{Q_CHARGER_LQM}$	Charger quiescent current (low power mode, charging enabled, 10 mA to 50 mA input current limit setting, VBATT > 2.8 V and LED driver OFF)	25 °C only; charger in CC state	0	1.5	3.0	mA
T_{SSVBUS_LIN}	Soft start time (VBUSIN = 5.0 V, time between input LDO enabled and VSYS going to 90 % of regulation	No input current limitation event, measured in Normal mode	—	—	30	ms

Table 7. Internal 2.7 V Regulator (INT2P7)

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{GDRV}	Output voltage		2.6	2.7	2.8	V
I_{GDRV}	Output current		5.0	—	—	mA
$V_{DO(GDRV)}$	Dropout voltage		0	—	800	mV

Table 8. Switch impedances and leakage currents

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$R_{VBUS_LIN2SYS}$	VBUSIN to VSYS resistance		100	250	550	mΩ
R_{BATFET_QFN}	VBATT to VSYS resistance		50	75	120	mΩ
I_{SYS}	VSYS leakage current	VSYS = 0 V, VBATT = 4.2 V, SHIP mode	0	0.2	10	μA

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Table 8. Switch impedances and leakage currents*...continued*

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
I_{BATT_OC}	VBATT reverse ILIM quiescent current when VBUSIN = 0 V	VBUSIN = 0 V, VSYS = VBATT = 4.2 V, BATFET enabled, battery overcurrent enabled	—	—	100	µA

Table 9. Linear transients

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{PK-PK}	Load transient peak-to-peak	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	10	400	850	mV
V_{OV_SHT}	Load transient overshoot	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	0	200	500	mV
V_{UND_SHT}	Load transient undershoot	VBUSIN = 5.0 V, VBATT = 3.6 V, I_{CHG} = 500 mA, VSYS load step 1.0 A/µs	0	200	500	mV

Table 10. Charger characteristics

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{CHGCV_RANGE}	CHGCV output voltage range	See register map for constant voltage programmable range	3.5	—	4.44	V
CV_{ACC}	CHGCV output accuracy in normal charging		—	—	±1	%
$V_{SYSMIN0}$	VSYS output voltage (3.5 V option)	VSYSMIN = 0x00 (3.5 V option)	3.395	3.5	3.605	V
$V_{SYSMIN1}$	VSYS output voltage (3.7 V option)	VSYSMIN = 0x01 (3.7 V option)	3.589	3.7	3.811	V
$V_{SYSMIN2}$	VSYS output voltage (4.3 V option)	VSYSMIN = 0x02 (4.3 V option)	4.171	4.3	4.429	V
$V_{SYSMINLOOP0}$	VSYSMIN loop threshold (3.5 V option)		3.0	3.2	3.39	V
$V_{SYSMINLOOP1}$	VSYSMIN loop threshold (3.7 V option)		3.2	3.4	3.585	V
$V_{SYSMINLOOP2}$	VSYSMIN loop threshold (4.3 V option)		3.83	4.0	4.17	V
I_{FC}	Output current range	Constant current programmable range CHG_CC[4:0]	100	—	1000	mA
I_{FCACC1}	Output current accuracy		−10	—	10	%
I_{EOC}	Charger IEOC range		5.0	—	50	mA
$t_{DB(IEOC)}$	Debounce time for charge termination		20	32	44	ms
$I_{EOC_ACC_5mA}$	Charger IEOC accuracy (5.0 mA settings)	I_{EOC} = 5 mA	1.0	5.0	12	mA
$I_{EOC_ACC_10mA}$	Charger IEOC accuracy (10 mA settings)	I_{EOC} = 10 mA	4.0	10	16	mA
$I_{EOC_ACC_50mA}$	Charger IEOC accuracy (50 mA setting)	I_{EOC} = 50 mA	40	50	60	mA
V_{PRECHG}	Precharge threshold	VBATT rising	2.7	2.8	2.9	V
V_{PRECHG_HYS}	Precharge threshold hysteresis		50	100	150	mV
I_{PRECHG}	Precharge current		30	45	60	mA
$I_{PRECHG.LPM}$	Charging current in LPM and 2.8 V < VBATT < 3.1 V		0.75	1.0	1.25	mA

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Table 10. Charger characteristics*...continued*

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$V_{RESTART}$	Charger restart threshold (100 mV settings)	VBATT below CHGCV[5:0]	50	100	150	mV
$V_{RESTART}$	Charger restart threshold (150 mV setting)	VBATT below CHGCV[5:0]	100	150	200	mV
$V_{RESTART}$	Charger restart threshold (200 mV settings)	VBATT below CHGCV[5:0]	150	200	250	mV
$t_{DB(VRCH)}$	Debounce time on $V_{RESTART}$		20	32	44	ms
V_{BATOV}	BATTOVP range		CHGCV x 1.025	CHGCV x 1.05	CHGCV x 1.075	V
V_{BATOV_HYS}	BATTOVP hysteresis	VBATT falling from BATTOVP	CHGCV x 0.015	CHGCV x 0.025	CHGCV x 0.035	V

Table 11. Power-path management

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{SPLM}	Supplement mode voltage threshold	Entering supplement mode when VSYS < VBATT	10	40	75	mV

Table 12. Watchdog timer

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{WD}	Watchdog timer period		—	80	—	s
t_{WDACC}	Watchdog timer accuracy		−20	0	20	%

Table 13. Charger timer

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{PRECHG}	Precharge time (fixed 45 mA)	Applies to low battery prequalification mode, 500 mA settings	—	30	—	min
t_{FC}	Fast charge constant current and constant voltage time	Adjustable from 2 to 14 in 2-hour steps	—	4.0	—	hrs
t_{EOC}	End-of-charge time	Adjustable from 0 to 70 in 10 min steps	—	30	—	min
t_{acc}	Timer accuracy	All timers associated with the charger block	−20	—	20	%
t_{SCIDG}	Charger state change interrupt delay		0	1.0	2.0	ms
t_{INLIM}	VBUS_VOK delay from VDIG ready following VBUSIN insertion (see charger startup diagram)		0	100	200	µs

Table 14. Battery overcurrent protection

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
t_{BOVCR}	Battery overcurrent debounce time	Response time to BATFET open (OTP option)	12.8	16	19.2	ms
t_{BOVCRI}	Battery overcurrent interrupt debounce time	Response time to generate interrupt	2.4	3.0	3.6	ms
I_{BOVCR}	Battery overcurrent threshold range	Programmable from 2.0 A to 4.0 A in three steps	2.0	—	4.0	A

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Table 14. Battery overcurrent protection*...continued*

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$I_{BOVCRACC_2A}$	Battery overcurrent threshold accuracy (2.2 A setting)		1.0	2.2	3.2	A
$I_{BOVCRACC_3A}$	Battery overcurrent threshold accuracy (2.8 A setting)		1.6	2.8	4	A
$I_{BOVCRACC_4A}$	Battery overcurrent threshold accuracy (3.2 A setting)		2.0	3.2	4.6	A
$R_{SYSDISCH}$	SYS self-discharge resistor in SHIP mode		480	600	720	Ω

Table 15. Thermal regulation

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
T_{REG}	Thermal regulation threshold (80 °C setting)	Temperature at which charge current begins to decrease	—	80	—	°C
T_{REG}	Thermal regulation threshold (95 °C Setting)	Temperature at which charge current begins to decrease	—	95	—	°C
T_{REG}	Thermal regulation threshold (110 °C setting)	Temperature at which charge current begins to decrease	—	110	—	°C

Table 16. Battery thermistor monitor

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$V_{NTECREF}$	NTECREF voltage		2.6	2.7	2.8	V
V_{TN10C}	Thermistor threshold (−10 °C settings)	−10 °C	$0.79*V_{NTECREF}$	$0.82*V_{NTECREF}$	$0.85*V_{NTECREF}$	V
V_{T0C}	Thermistor threshold (0 °C settings)	0 °C	$0.71*V_{NTECREF}$	$0.74*V_{NTECREF}$	$0.77*V_{NTECREF}$	V
V_{T10C}	Thermistor threshold (10 °C settings)	10 °C	$0.62*V_{NTECREF}$	$0.65*V_{NTECREF}$	$0.68*V_{NTECREF}$	V
V_{T45C}	Thermistor threshold (45 °C settings)	45 °C	$0.31*V_{NTECREF}$	$0.33*V_{NTECREF}$	$0.35*V_{NTECREF}$	V
V_{T55C}	Thermistor threshold (55 °C settings)	55 °C	$0.25*V_{NTECREF}$	$0.26*V_{NTECREF}$	$0.27*V_{NTECREF}$	V
V_{T60C}	Thermistor threshold (60 °C settings)	60 °C	$0.22*V_{NTECREF}$	$0.23*V_{NTECREF}$	$0.24*V_{NTECREF}$	V
V_{T_HYS}	Battery temperature hysteresis	All settings	0.5	2.5	5.0	°C

Table 17. USBPHY LDO

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{USB_PHY}	Output voltage	I_{OUT} = 10 mA; 3.3 V and 4.9 V settings. VBUSIN = 5.5 V	−5.0	—	5.0	%
I_{USB_PHY}	Maximum output current		60	—	—	mA
USB_{RDIS}	Internal discharge resistance		500	1000	1500	Ω
USB_{CAPSTA}	Output capacitor for stable operation	0 μA < I_{OUT} < 60 mA, MAX ESR = 10 mΩ	0.7	1.0	2.2	μF
I_{QUSB}	Quiescent supply current		—	35	—	μA
$USBPHY_{LDREG}$	DC load regulation	VBUSIN = 5.5 V, 30 μA < I_{OUT} < 60 mA	0	5.0	13	mV
$USBPHY_{DO}$	Dropout voltage	VBUSIN = 5.0 V, I_{OUT} = 60 mA	—	200	350	mV
$USBPHYI_{LIM}$	Output current limit		65	150	200	mA

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Table 17. USBPHY LDO*...continued*

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
$PSRR_{USB_PHY}$	PSRR	VBUSIN = 5.5 V, C_{OUT} = 1.0 µF	55	60	75	dB

Table 18. LED characteristics

Symbol	Parameter	Measurement condition	Min	Typ	Max	Unit
V_{LED}	LED input voltage operating range (anode to ground)		3.5	—	VSYS	V
V_{CHGB_IN}	CHGB input voltage operating range, LED driver enabled		1.0	—	3.0	V
I_{LED}	LED current accuracy		4.0	6.0	8	mA
T_{ON}	LED duty cycle range	Programmable from 10 % to 100 % duty cycle in 10 % steps	10	—	100	%
$TLED_{RUP}$	LED ramp up	Settings depend on duty cycle	50	—	500	ms
$TLED_{RDN}$	LED ramp down	Settings depend on duty cycle	50	—	500	ms
F_{LED}	LED frequency	Programmable from 0.5 Hz to 256 Hz	0.5	—	256	Hz

5.3.2 Electrical characteristics – SW1 and SW2

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = V_{SWxIN} = 2.5 V to 4.5 V, V_{SWx} = 1.2 V, I_{SWx} = 200 mA, typical external component values, f_{SWx} = 2.0 MHz, unless otherwise noted. Typical values are characterized at VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.1 V, I_{SWx} = 100 mA, and 25 °C, unless otherwise noted.

Table 19. SW1 and SW2 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SWxIN}	Operating input voltage	2.5	—	4.5	V
I_{SWx}	Rated output current	1000	—	—	mA
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 0.6 V ≤ V_{SWx} ≤ 1.0 V	−15	—	15	mV
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.0 V < V_{SWx} ≤ 1.3875 V	−2.0	—	2.0	%
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < ISWx < 0.1 A 0.6 V ≤ V_{SWx} ≤ 1.0 V	−30	—	30	mV
V_{SWx}	Output voltage accuracy DVS enabled mode (OTP_SWx_DVS_SEL = 0) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.0 V < V_{SWx} ≤ 1.3875 V	−3.0	—	3.0	%
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.1 V ≤ V_{SWx} ≤ 1.5 V	−45	—	45	mV
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Normal power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 1.0 A 1.8 V ≤ V_{SWx} ≤ 3.3 V	−3.0	—	3.0	%

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Table 19. SW1 and SW2 electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.1 V < V_{SWx} ≤ 1.5 V	−55	—	55	mV
V_{SWx}	Output voltage accuracy DVS disabled mode (OTP_SWx_DVS_SEL = 1) Low-power mode, 2.5 V < V_{SWxIN} < 4.5 V, 0 < I_{SWx} < 0.1 A 1.8 V ≤ V_{SWx} ≤ 3.3 V	−4.0	—	4.0	%
ΔV_{SWx}	Output ripple	—	5.0	—	mV
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ LP/ ULP mode, 1.2 V, 1.0 mA	—	88	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 50 mA	—	90	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 150 mA	—	92	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 400 mA	—	89	—	%
SWxEFF	Efficiency V_{SWxIN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.2 V, 1000 mA	—	83	—	%
$I_{SWxLIMH}$	Current limiter peak (high-side MOSFET) current detection SWxILIM[1:0] = 00 SWxILIM[1:0] = 01 SWxILIM[1:0] = 10 SWxILIM[1:0] = 11	 0.7 0.8 1.0 1.4	 1.0 1.2 1.5 2.0	 1.3 1.6 2.0 2.6	A
$I_{SWxLIML}$	Current limiter low-side MOSFET current detection (sinking current)	0.7	1.0	1.3	A
I_{SWxQ}	Quiescent current (at 25 °C) Low-power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)	 —	 1.0	 —	µA
I_{SWxQ}	Quiescent current (at 25 °C) Low-power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)	 —	 6.0	 —	µA
I_{SWxQ}	Quiescent current (at 25 °C) Normal power mode with DVS disabled (OTP_SWx_DVS_SEL = 1)	 —	 5.5	 —	µA
I_{SWxQ}	Quiescent current (at 25 °C) Normal power mode with DVS enabled (OTP_SWx_DVS_SEL = 0)	 —	 10	 —	µA
V_{SWxOSH}	Startup overshoot (Normal mode) I_{SWx} = 0 mA DVS speed = 12.5 mV/4 µs, VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.35 V	—	—	25	mV
t_{ONSWx}	Turn on time 10 % to 90 % of end value DVS speed = 12.5 mV/4 µs, VSYS = V_{SWxIN} = 3.6 V, V_{SWx} = 1.35 V	—	—	500	µs
$V_{SWxLOTR}$	Transient load regulation (Normal power mode) Transient load = 50 mA to 250 mA, di/dt = 200 mA/µs Overshoot Undershoot	 — —	 25 25	 — —	mV
R_{ONSWxP}	SWx P-MOSFET $R_{DS(on)}$ at V_{SWxIN} = 3.6 V	—	200	—	mΩ
R_{ONSWxN}	SWx N-MOSFET $R_{DS(on)}$ at V_{SWxIN} = 3.6 V	—	150	—	mΩ
R_{SWxDIS}	Turn off discharge resistance	—	500	—	Ω

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5.3.3 Electrical characteristics – SW3

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = V_{SW3IN} = 2.5 V to 4.5 V, V_{SW3} = 1.8 V, I_{SW3} = 200 mA, typical external component values, f_{SW3} = 2.0 MHz, unless otherwise noted. Typical values are characterized at VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V, I_{SW3} = 200 mA, and 25 °C, unless otherwise noted.

Table 20. SW3 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SW3IN}	Operating input voltage	2.5	—	4.5	V
V_{SW3}	Output voltage accuracy (all voltage settings) Normal power mode, 2.5 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 1.0 A	−2.0	—	2.0	%
V_{SW3}	Output voltage accuracy (all voltage settings) Low-power mode, 2.5 V < V_{SW3IN} < 4.5 V, 0 < I_{SW3} < 0.1 A	−3.0	—	3.0	%
ΔV_{SW3}	Output ripple	—	5.0	—	mV
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SW3} = 1.0 µH, DCR = 50 mΩ LP/ ULP Mode, 1.8 V, 1.0 mA	—	88	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 50 mA	—	90	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 mH, DCR = 50 mΩ Normal power mode, 1.8 V, 100 mA	—	91	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 400 mA	—	92	—	%
SW3EFF	Efficiency V_{SW3IN} = 3.6 V, L_{SWx} = 1.0 µH, DCR = 50 mΩ Normal power mode, 1.8 V, 1000 mA	—	83	—	%
$I_{SW3LIMH}$	Current limiter peak (high-side MOSFET) current detection SW3ILIM[1:0] = 00 SW3ILIM[1:0] = 01 SW3ILIM[1:0] = 10 SW3ILIM[1:0] = 11	 0.7 0.8 1.0 1.4	 1.0 1.2 1.5 2.0	 1.3 1.6 2.0 2.6	A
$I_{SW3LIML}$	Current limiter low-side MOSFET current detection (sinking current)	0.7	1.0	1.3	A
I_{SW3Q}	Quiescent current (at 25 °C) Low-power mode	—	1.0	—	µA
V_{SW3OSH}	Start-up overshoot (Normal mode) I_{SW3} = 0 mA VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V	—	—	50	mV
t_{ONSW3}	Turn on time 10 % to 90 % of end value VSYS = V_{SW3IN} = 3.6 V, V_{SW3} = 1.8 V	—	—	500	µs
$V_{SW3LOTR}$	Transient load regulation (Normal power mode) Transient load = 50 mA to 250 mA, di/dt = 200 mA/µs Overshoot Undershoot	 — —	 50 50	 — —	mV
R_{ONSW3N}	SW3 N-MOSFET $R_{DS(on)}$ at V_{SW3IN} = 3.6 V	—	150	—	mΩ
R_{ONSW3P}	SW3 P-MOSFET $R_{DS(on)}$ at V_{SW3IN} = 3.6 V	—	200	—	mΩ
R_{SW3DIS}	Turn off discharge resistance	—	300	—	Ω

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5.3.4 Electrical characteristics – LDO1

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = 2.5 V to 4.5 V, V_{LDOIN1} = 3.6 V, VLDO1[4:0] = 11111, I_{LDO1} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN1} = 3.6 V, VLDO1[4:0] = 11111, I_{LDO1} = 10 mA, and 25 °C, unless otherwise noted.

Table 21. LDO1 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO1IN}	Operating input voltage V_{LDO1} + 250 mV ≤ VSYS ≤ 4.5 V	 1.0	 —	 4.5	V
$V_{LDO1NOM}$	Nominal output voltage	—	See Table 41	—	V
$I_{LDO1MAX}$	Rated output load current, Normal mode	300	—	—	mA
$I_{LDO1MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO1TOL}$	Output voltage tolerance, Normal mode $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0 mA < I_{LDO1} ≤ 300 mA 0.8 V ≤ V_{LDO1} < 1.8 V 1.8 V ≤ V_{LDO1} ≤ 3.3 V $V_{LDO1INMIN}$ < V_{LDO1IN} < 4.5 V, 0 mA < I_{LDO1} < 10 mA (Low-power mode)	 −2.5 −2.5 −4.0	 — — —	 2.5 2.5 4.0	%
$I_{LDO1LIM}$	Current limit I_{LDO1} when V_{LDO1} is forced to $V_{LDO1NOM}$/2	320	—	1000	mA
$I_{LDO1OCP}$	LDO1FAULTI threshold (also used to disable LDO1 when REGSCPEN = 1)	320	—	1000	mA
I_{LDO1Q}	Quiescent current (at 25 °C) No load, change in I_{VSYS} and $I_{VLDOIN1}$ When LDO1 enabled in Normal mode When LDO1 enabled in Low-power mode	 — —	 17 2.5	 — —	µA
$R_{DSON_QFN_LDO1}$	Dropout on resistance	—	—	350	mΩ
$PSRR_{LDO1}$	PSRR I_{LDO1} = 150 mA, 20 Hz to 20 kHz V_{LDO1} = 3.30 V, V_{LDO1IN} = 3.8 V, VSYS = 4.2 V	 —	 56	 —	dB
TR_{VLDO1}	Turn on time 10 % to 90 % of end value $V_{LDO1INMIN}$ < V_{LDO1IN} ≤ 4.5 V, I_{LDO1} = 0.0 mA	 —	 200	 500	µs
$R_{LDO1DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO1OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO1INMIN}$ < V_{LDO1IN} ≤ 4.5 V, I_{LDO1} = 0.0 mA	 —	 1.0	 2.0	%
$V_{LDO1LOTR}$	Transient load response $V_{LDO1INMIN}$ < V_{LDO1IN} ≤ 4.5 V, I_{LDO1} = 10 mA to 200 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.5 Electrical characteristics – LDO2

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = 3.6 V, V_{LDOIN2} = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN2} = 3.6 V, VLDO2[3:0] = 1111, I_{LDO2} = 10 mA, and 25 °C, unless otherwise noted.

Table 22. LDO2 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO2IN}	Operating input voltage 1.8 V ≤ $V_{LDO2NOM}$ ≤ 2.5 V 2.6 V ≤ $V_{LDO2NOM}$ ≤ 3.3 V	 2.8 $V_{LDO2NOM}$ + 0.250	 – –	 4.5 4.5	V

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Table 22. LDO2 electrical characteristics...*continued*

Symbol	Parameter	Min	Typ	Max	Unit
$V_{LDO2NOM}$	Nominal output voltage	—	See Table 43	—	V
$I_{LDO2MAX}$	Rated output load current, Normal mode	400	—	—	mA
$I_{LDO2MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO2TOL}$	Output voltage tolerance $V_{LDO2INMIN} < V_{LDO2IN} < 4.5$ V 10.0 mA ≤ I_{LDO2} < 400 mA 0.0 mA < I_{LDO2} < 10 mA (Low-power mode)	 −2.0 −4.0	 — —	 2.0 4.0	%
$I_{LDO2LIM}$	Current limit I_{LDO2} when V_{LDO2} is forced to $V_{LDO2NOM}/2$	450	750	1050	mA
$I_{LDO2OCP}$	LDO2FAULTI threshold (also used to disable LDO2 when REGSCPEN = 1)	450	—	1050	mA
I_{LDO2Q}	Quiescent Current (25 °C) No load, change in I_{VSYS} and $I_{VLDO2IN}$ When V_{LDO2} enabled in Normal mode When V_{LDO2} enabled in Low-power mode	 — —	 15 1.5	 — —	µA
$R_{DSON_QFN_LDO2}$	Dropout on resistance	—	—	300	mΩ
$PSRR_{VLDO2}$	PSRR I_{LDO2} = 200 mA, 20 Hz to 20 kHz V_{LDO2} = 3.30 V, V_{LDO2IN} = 3.9 V, VSYS = 4.2 V	 —	 60	 —	dB
t_{ONLDO2}	Turn on time 10 % to 90 % of end value $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 0.0 mA	—	200	500	µs
$R_{LDO2DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO2OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 0.0 mA	—	1.0	2.0	%
$V_{LDO2LOTR}$	Transient load response $V_{LDO2INMIN} < V_{LDO2IN} \leq 4.5$ V, I_{LDO2} = 10 mA to 100 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.6 Electrical characteristics – LDO3

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = 2.5 V to 4.5 V, V_{LDOIN3} = 3.6 V, VLDO3[4:0] = 11111, I_{LDO3} = 10 mA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{LDOIN3} = 3.6 V, VLDO3[4:0] = 11111, I_{LDO3} = 10 mA, and 25 °C, unless otherwise noted.

Table 23. LDO3 electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LDO3IN}	Operating input voltage V_{LDO3} + 250 mV ≤ VSYS ≤ 4.5 V	1.0	—	4.5	V
$V_{LDO3NOM}$	Nominal output voltage	—	See Table 41	—	V
$I_{LDO3MAX}$	Rated output load current, Normal mode	300	—	—	mA
$I_{LDO3MAXLPM}$	Rated output load current, Low-power mode	10	—	—	mA
$V_{LDO3TOL}$	Output voltage tolerance, Normal mode $V_{LDO3INMIN} < V_{LDO3IN} < 4.5$ V, 0 mA < I_{LDO3} < 300 mA 0.8 V ≤ V_{LDO3} < 1.8 V 1.8 V ≤ V_{LDO3} ≤ 3.3 V $V_{LDO3INMIN} < V_{LDO3IN} < 4.5$ V, 0 mA < I_{LDO3} < 10 mA (Low-power mode)	 −2.5 −2.5 −4.0	 — — —	 2.5 2.5 4.0	%
$I_{LDO3LIM}$	Current limit I_{LDO3} when V_{LDO3} is forced to $V_{LDO3NOM}/2$	320	—	1000	mA

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Table 23. LDO3 electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
$I_{LDO3OCP}$	LDO3FAULTI threshold (also used to disable LDO3 when REGSCPEN = 1)	320	—	1000	mA
I_{LDO3Q}	Quiescent current (at 25 °C) No load, change in I_{VSYS} and $I_{VLDOIN3}$ When LDO3 enabled in Normal mode When LDO3 enabled in Low-power mode	 — —	 17 2.5	 — —	µA
$R_{DSON_QFN_LDO3}$	Dropout on resistance	—	—	350	mΩ
$PSRR_{LDO3}$	PSRR I_{LDO3} = 150 mA, 20 Hz to 20 kHz V_{LDO3} = 3.30 V, V_{LDO3IN} = 3.8 V, VSYS = 4.2 V	—	56	—	dB
TR_{VLDO3}	Turn on time 10 % to 90 % of end value $V_{LDO3INMIN} < V_{LDO3IN} < 4.5$ V, I_{LDO3} = 0.0 mA	—	200	500	µs
$R_{LDO3DIS}$	Turn off discharge resistance	—	250	—	Ω
$LDO3OUT_{OSHT}$	Start-up overshoot (% of final value) $V_{LDO3INMIN} < V_{LDO3IN} \leq 4.5$ V, I_{LDO3} = 0.0 mA	—	1.0	2.0	%
$V_{LDO3LOTR}$	Transient load response $V_{LDO3INMIN} < V_{LDO3IN} \leq 4.5$ V, I_{LDO3} = 10 mA to 100 mA in 10 µs Overshoot Undershoot	 — —	 50 50	 — —	mV

5.3.7 Electrical characteristics – VREFDDR

T_A = −40 to 105 °C, VSYS = 2.5 V to 4.5 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.35 V and typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, I_{REFDDR} = 0.0 mA, $V_{INREFDDR}$ = 1.35 V, and 25 °C, unless otherwise noted.

Table 24. VREFDDR electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$V_{INREFDDR}$	Operating input voltage range	0.9	—	1.8	V
V_{REFDDR}	Output voltage, 0.9 V < $V_{INREFDDR}$ < 1.8 V, 0 mA < I_{REFDDR} < 10 mA	—	$V_{INREFDDR}/2$	—	V
$V_{REFDDRTOL}$	Output voltage tolerance, as a percentage of $V_{INREFDDR}$, 1.2 V < $V_{INREFDDR}$ < 1.65 V, 0 mA < I_{REFDDR} < 10 mA	49.25	50	50.75	%
$I_{REFDDRQ}$	Quiescent current (at 25 °C)	—	1.1	—	µA
$I_{REFDDRLM}$	Current limit, I_{REFDDR} when V_{REFDDR} is forced to $V_{INREFDDR}/4$	10.5	24	38	mA
$t_{ONREFDDR}$	Turn on time, 10 % to 90 % of end value, $V_{INREFDDR}$ = 1.2 V to 1.65 V, I_{REFDDR} = 0.0 mA	—	—	100	µs

5.3.8 Electrical characteristics – VSNVS

All parameters are specified at T_A = −40 °C to 105 °C, VSYS = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{SNVS} = 3.0 V, I_{SNVS} = 5.0 µA, and 25 °C, unless otherwise noted.

Table 25. VSNVS electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{SNVSIN}	Operating input voltage Valid coin cell range Valid VSYS	 1.8 2.45	 — —	 3.3 4.5	V

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Table 25. VSNVS electrical characteristics*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
I_{SNVS}	Operating load current $V_{SNVSINMIN} < V_{SNVSIN} < V_{SNVSINMAX}$	2000	—	—	μA
V_{TL1}	VSYS threshold (VSYS powered to coin cell powered)	—	UVDET failing	—	V
V_{TH1}	VSYS threshold (coin cell powered to VSYS powered)	—	UVDET rising	—	V
V_{SNVS}	Output voltage (when running from VSYS) 0 μA < I_{SNVS} < 2000 μA Output voltage (when running from LICELL) 0 μA < I_{SNVS} < 2000 μA 2.84 V < V_{COIN} < 3.3 V	−7.0 % VCOIN − 0.20	3.0 —	7.0 % —	V
$V_{SNVSDROP}$	Dropout voltage VSYS = 2.9 V I_{SNVS} = 2000 μA	—	—	220	mV
$I_{SNVSLIM}$	Current limit VSYS > V_{TH1}	5200	—	24000	μA
$V_{SNVSTON}$	Turn on time (load capacitor, 0.47 μF) 10 % to 90 % of final value V_{SNVS} V_{COIN} = 0.0 V, I_{SNVS} = 0 μA	—	—	3.0	ms
$V_{SNVSOSH}$	Start-up overshoot I_{SNVS} = 5.0 μA dVSYS/dt = 50 mV/μs	—	40	70	mV
$R_{DSONSNVS}$	Internal switch $R_{DS(on)}$ V_{COIN} = 2.6 V	—	—	100	Ω

5.3.9 Electrical characteristics – IC level bias currents

All parameters are specified at 25 °C, VSYS = 3.6 V, VBUSIN = 0 V, typical external component values, unless otherwise noted. Typical values are characterized at VSYS = 3.6 V, V_{SNVS} = 3.0 V, and 25 °C, unless otherwise noted.

Table 26. IC level electrical characteristics

Mode	PF1550 conditions	System conditions	Typ	Max	Unit
Coin cell	VSNVS from LICELL All other blocks off VSYS = 0.0 V	No load on VSNVS	1.5	4.0	μA
CORE_OFF	VSNVS from VSYS Wake-up from ONKEY active All other blocks off VSYS > UVDET	No load on VSNVS, PMIC able to wake up	1.5	4.0	μA
Sleep	VSNVS from VSYS Wake-up from PWRON active Trimmed reference active DDR I/O rail in Low-power mode VREFDDR disabled	No load on VSNVS. DDR memories in self-refresh.	12.5	25	μA
Standby/Suspend	VSNVS from either VSYS or LICELL SW1 in ultra Low-power mode SW2 in ultra Low-power mode SW3 in ultra Low-power mode Trimmed reference active VLDO1 is disabled VLDO2 enabled in Low-power mode VLDO3 enabled in Low-power mode VREFDDR enabled	No load on VSNVS. Processor enabled in Low-power mode.	23	46	μA

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Table 26. IC level electrical characteristics*...continued*

Mode	PF1550 conditions	System conditions	Typ	Max	Unit
REGS_DISABLE	VSNVS from VSYS Wake-up from ONKEY active Most other blocks off VSYS > UVDET	No load on VSNVS, PMIC able to wake up	14	20	µA
SHIP	BATFET open, no LICELL connected VSYS = 0 V, only awake from ONKEY enabled		0.45	1.0	µA

6 Detailed description

The PF1550 PMIC features three high efficiency low quiescent current buck regulators, three LDO regulators, a DDR voltage reference to supply voltages for the application processor and peripheral devices.

Additionally, PF1550 incorporates a single cell Li-ion linear battery charger with a USB-PHY regulator.

The buck regulators provide the supply to processor cores and to other low voltage circuits such as I/O and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores for power optimization.

The three LDO regulators are general purpose to power various processor rails, system connectivity devices and/or peripherals. Depending on the system power configuration, the general purpose LDO regulators can be directly supplied from the main system supply VSYS or from the switching regulators to power peripherals, such as audio, camera, Bluetooth, Wireless LAN.

A specific VREFDDR voltage reference is included to provide accurate reference voltage for DDR memories operation.

The VSNVS block behaves as an LDO, or as a bypass switch to supply the SNVS (Secure Non-Volatile Storage) /RTC (Real Time Clock) circuitry on the processor. VSNVS is powered from VSYS or from a coin cell.

To accommodate applications that do not include Li-ion battery, the PF1550 battery charger regulates the input voltage at VBUSIN pin down to maximum of 4.5 V at VSYS through the power path circuit.

Table 27. Voltage regulators

Supply	Output voltage (V)	Programming step size (mV)	Load current (mA)
SW1 / SW2	0.60 to 1.3875 / 1.1 to 3.3	12.5 / variable	1000
SW3	1.80 to 3.30	100	1000
LDO1	0.75 to 1.50 1.80 to 3.30	50 100	300
LDO2	1.80 to 3.30	100	400
LDO3	0.75 to 1.50 1.80 to 3.30	50 100	300
USBPHY	3.3 or 4.9	—	60
VSNVS	3.0	N/A	2
VREFDDR	0.5*VINREFDDR	N/A	10

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6.1 Buck regulators

The PF1550 features three high-efficiency buck regulators with internal compensation. Each buck regulator is capable of meeting optimum power efficiency operation using reduced power variable-frequency pulse skip switching scheme at light loads as well as operating in forced PWM quasi-fixed frequency switching mode at higher loads. The switching regulator controller combines the advantages of hysteretic and voltage mode control which provides outstanding load regulation and transient response, low output ripple voltage, and seamless transition between pulse-skip mode and Active Quasi-fixed frequency switching mode. The control circuitry includes an AC loop which senses the output voltage (at SWxFB pin) and directly feeds it to a fast comparator stage. This comparator sets the switching frequency, which is almost constant for steady state operating conditions. It also provides immediate response to dynamic load changes.

In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors. The transition into and out of low-power pulse-skip switching mode takes place automatically according to the load current to maintain optimum power efficiency. Additionally, further power savings through cutting the buck circuitry quiescent current can be achieved by activating a Low-power mode upon entering either STANDBY or SLEEP PMIC power mode or as commanded via I^2C control bits. In SW1 and SW2. An OTP option enables or disables DVS in the regulators. When DVS is disabled and the low-power bit is set, the regulator enters an Ultra Low Power (ULP) mode that cuts the operating quiescent current even, in order to reach extremely low standby power levels needed for ultra low power processors such as that from Kinetis K and L series.

As indicated above, the buck controller supports PWM (Pulse Width Modulation) mode for medium and high load conditions and low-power variable-frequency pulse skip mode at light loads. During high current mode, it operates in continuous conduction and the switching frequency is up to 2.0 MHz with a controlled on-time variation depending on the input voltage and output voltage. If the load current decreases, the converter seamlessly enters the pulse-skip mode to cut the operating quiescent current and maintain high efficiency down to very light loads. In pulse-skip mode, the switching frequency varies linearly with the load current. Since the controller supports both power modes within one single building block, the transition from normal power mode to lower power pulse-skip mode and vice versa is seamless without dramatic effects on the output voltage.

In the adopted pulse-skip scheme, the device generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a non-switching (pause) period where most of the internal circuits are shut down to achieve a lowest quiescent current. During this time, the load current is supported by the output capacitor. The duration of the pause period depends on the load current and the inductor peak current.

6.2 SW1 and SW2 detailed description

SW1 and SW2 are identical buck regulators designed to carry a nominal load current of 1.0 A. Detailed characteristics and features of SW1 and SW2 are described in this section. Being identical, reference is made only to SWx though the same specifications apply to SW1 and SW2.

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6.2.1 SWx dynamic voltage scaling description

SWx integrates an optional DVS circuit that is enabled via OTP. To reduce overall power consumption, when DVS is enabled SWx output voltage can be varied depending on the mode or activity level of the processor.

- **Normal operation:**
  The output voltage is selected by I^2C bits SWx_VOLT[5:0]. A voltage transition initiated by I^2C is governed by the SWx_DVSSPEED I^2C bit as shown in Table 28.
- **Standby mode:**
  The output voltage can be selected by I^2C bits SWx_STBY_VOLT[5:0]. Voltage transitions initiated by a Standby event are governed by the SWx_DVSSPEED I^2C bit as shown in Table 28. This applies only when DVS is enabled.
- **Sleep mode:**
  The output voltage can be higher or lower than in normal operation, but is typically selected to be the lowest state retention voltage of a given processor; it is selected by I^2C bits SWx_SLP_VOLT[5:0]. Voltage transitions initiated by a turn off event are governed by the SWx_DVSSPEED I^2C bit for SWx as shown in Table 28. This applies only when DVS is enabled.

As shown in Figure 5, during a falling DVS transition, dv/dt of the output voltage depends on the load current. Setting the SWx_FPWM_IN_DVS bit forces the regulator in the FPWM mode during the falling transition allowing it to accurately track the DVS reference, removing the load dependency. The SWx_FPWM_IN_DVS bit is active only when OTP_SWx_DVS_SEL = 0.

Table 28. SWx DVS setting selection

SWx_DVS speed	Function
0	12.5 mV step each 2.0 µs
1	12.5 mV step each 4.0 µs

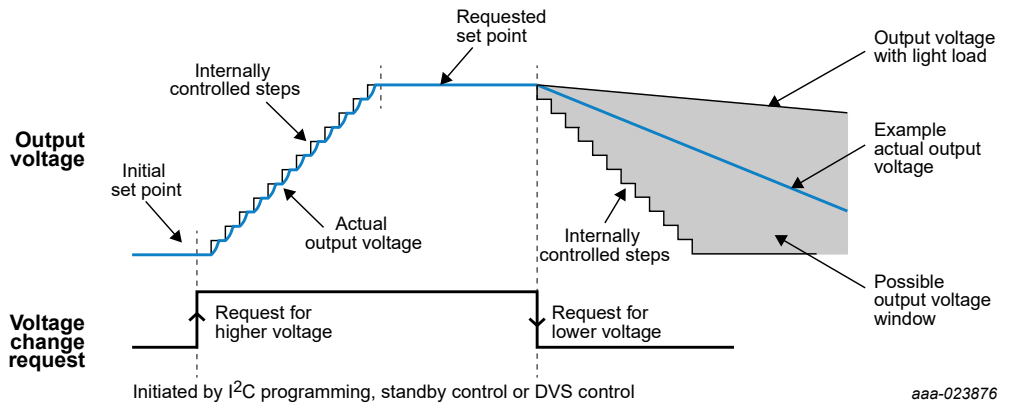

Figure 5. SWx DVS transitions

6.2.2 SWx DVS and non-DVS operation

SWx has two distinct modes of operation selectable via OTP:

- DVS enabled: a DVS reference is activated and output accuracy of the regulator is tight at the cost of slightly higher quiescent current. See Section 5.3 "Electrical characteristics" for details. In Figure 6, **DVS FB** and **DVS REF** are enabled via OTP for this mode of operation.

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- DVS disabled: the regulator operates as a traditional buck converter with a fixed reference and soft-start. The quiescent current in this mode is lower at the cost of output accuracy and transient response. See Section 5.3 "Electrical characteristics" for details. In Figure 6, **VREF FB** and **VREF** are enabled via OTP for this mode of operation.

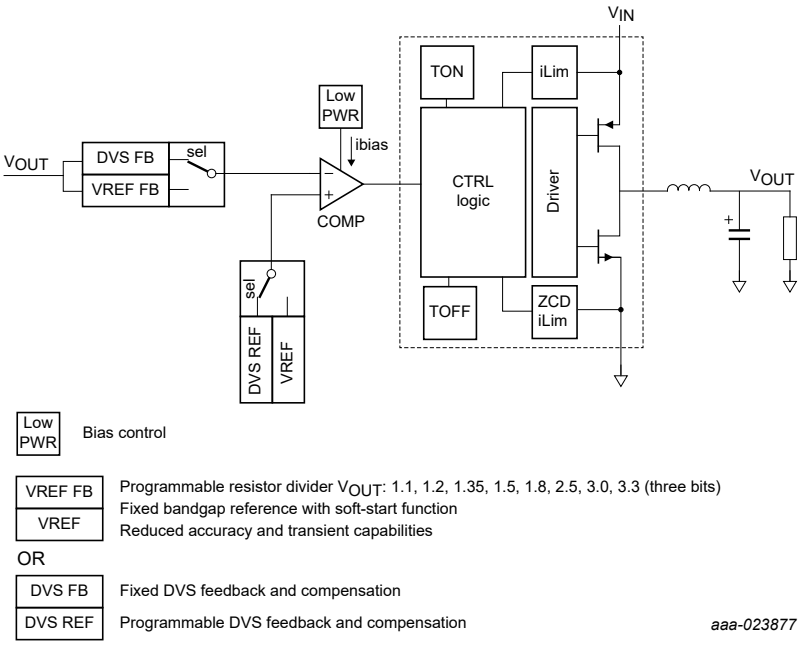

Figure 6. SWx DVS and non-DVS selection

6.2.3 Regulator control

To improve system efficiency, the buck regulators can operate in different switching/ bias modes. The changing between DCM (Discontinuous Conduction Mode) / CCM (Continuous Conduction Mode) takes place automatically based on detecting the load current level. It can be enforced by one of the following means: I^2C programming, exiting/ entering the Standby mode, exiting/entering Sleep/ Low-power mode.

Available modes for buck regulators are presented in Table 29. These switching modes are available with OTP_SWx_DVS_SEL = 0 and OTP_SWx_DVS_SEL = 1. Table 30 shows the bit settings for operating the buck converter is these modes based on the PMIC operating state.

Table 29. Buck regulator operating modes

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged using an internal resistor.
Adaptive	This is the default mode of operation of the buck regulator. In this mode, the regulator operates in a quasi-fixed frequency switching mode at moderate and high loads, with pulse skip (variable switching frequency) scheme at light load for optimized efficiency.
F-PWM	In this mode, the regulator is always in PWM mode operation regardless of load conditions.
Low-power	To further extend power savings when the load current is minimal, this mode cuts the quiescent current of the buck converter by reducing the bias to the comparator. The regulator is operated in Low-power modes (Standby and/or Sleep) with the proper I^2C setting. See Table 30.

The following table shows actions to control different bits for SW1 and SW2.

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Table 30. Buck mode control

PMIC state	SWx_EN	SWx_STBY	SWx_OMODE	SWx_LPWR	SWx_FPWM	SWx operating mode
Run/Standby/Sleep	0	X	X	X	X	SW disabled
Run	1	X	X	0	0	SW enabled. Operates in DCM at light loads
Run	1	X	X	0	1	SW enabled. Forced PWM mode
Run	1	X	X	1	0	SW Enabled. Does not operate in Low-power mode.
Run	1	X	X	1	1	SW enabled. Forced PWM mode – not Low-power mode.
Standby	1	0	X	X	X	SW disabled
Standby	1	1	X	0	0	SW enabled. Operates in DCM at light loads.
Standby	1	1	X	0	1	SW enabled. Forced PWM mode.
Standby	1	1	X	1	0	SW enabled. Operates in Low-power mode.
Standby	1	1	X	1	1	SW enabled. Forced PWM mode – not Low-power mode.
Sleep	1	X	0	X	X	SW disabled
Sleep	1	X	1	0	0	SW enabled. Operates in DCM at light loads.
Sleep	1	X	1	0	1	SW enabled. Forced PWM mode.
Sleep	1	X	1	1	0	SW enabled. Operates in Low-power mode.
Sleep	1	X	1	1	1	SW enabled. Forced PWM mode – not Low-power mode.

6.2.4 Current limit protection

SWx features high and low-side FET current limit. When current through the FETs go above their respective thresholds, the FET is turned-off to prevent further increase in current.

The protection is enabled in a cycle-by-cycle mode. Hitting either current limit sets the corresponding interrupt sense bits. If the faults persist for longer than the 8.0 ms debounce time, the interrupt status bit is set.

6.2.5 Output voltage setting in SWx

Output voltage of SWx is programmable via OTP. During startup (REGS_DISABLE mode to RUN mode), contents of the OTP_SWx_VOLT[5:0] are mapped into the SWx_VOLT[5:0], SWx_STBY_VOLT[5:0], and SWx_SLP_VOLT[5:0] register which set the regulator output voltage during Run, Standby, and Sleep modes respectively.

In the DVS enabled mode (OTP_SWx_DVS_SEL = 0), values of SWx_VOLT[5:0], SWx_STBY[VOLT[5:0], and SWx_SLP_VOLT[5:0] can be changed via I^2C after the PMIC starts up (RESETBMCU is released).

In the DVS disabled mode (OTP_SWx_DVS_SEL = 1), value of SWx_VOLT[5:0], SWx_STBY[VOLT[5:0], and SWx_SLP_VOLT[5:0] are read-only and must not be written to.

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Table 31. SW1 and SW2 output voltage setting

Set point	SWx_VOLT[5:0] SWx_STBY_VOLT[5:0] SWx_SLP_VOLT[5:0]	Output voltage with DVS enabled OTP_SWx_DVS_SEL = 0	Output voltage with DVS disabled OTP_SWx_DVS_SEL = 1
0	000000	0.6000	1.10
1	000001	0.6125	1.20
2	000010	0.6250	1.35
3	000011	0.6375	1.50
4	000100	0.6500	1.80
5	000101	0.6625	2.50
6	000110	0.6750	3.00
7	000111	0.6875	3.30
8	001000	0.7000	3.30
9	001001	0.7125	3.30
10	001010	0.7250	3.30
11	001011	0.7375	3.30
12	001100	0.7500	3.30
13	001101	0.7625	3.30
14	001110	0.7750	3.30
15	001111	0.7875	3.30
16	010000	0.8000	3.30
17	010001	0.8125	3.30
18	010010	0.8250	3.30
19	010011	0.8375	3.30
20	010100	0.8500	3.30
21	010101	0.8625	3.30
22	010110	0.8750	3.30
23	010111	0.8875	3.30
24	011000	0.9000	3.30
25	011001	0.9125	3.30
26	011010	0.9250	3.30
27	011011	0.9375	3.30
28	011100	0.9500	3.30
29	011101	0.9625	3.30
30	011110	0.9750	3.30
31	011111	0.9875	3.30
32	100000	1.0000	3.30
33	100001	1.0125	3.30
34	100010	1.0250	3.30

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Table 31. SW1 and SW2 output voltage setting*...continued*

Set point	SWx_VOLT[5:0] SWx_STBY_VOLT[5:0] SWx_SLP_VOLT[5:0]	Output voltage with DVS enabled OTP_SWx_DVS_SEL = 0	Output voltage with DVS disabled OTP_SWx_DVS_SEL = 1
35	100011	1.0375	3.30
36	100100	1.0500	3.30
37	100101	1.0625	3.30
38	100110	1.0750	3.30
39	100111	1.0875	3.30
40	101000	1.1000	3.30
41	101001	1.1125	3.30
42	101010	1.125	3.30
43	101011	1.1375	3.30
44	101100	1.1500	3.30
45	101101	1.1625	3.30
46	101110	1.1750	3.30
47	101111	1.1875	3.30
48	110000	1.2000	3.30
49	110001	1.2125	3.30
50	110010	1.2250	3.30
51	110011	1.2375	3.30
52	110100	1.2500	3.30
53	110101	1.2625	3.30
54	110110	1.2750	3.30
55	110111	1.2875	3.30
56	111000	1.3000	3.30
57	111001	1.3125	3.30
58	111010	1.3250	3.30
59	111011	1.3375	3.30
60	111100	1.3500	3.30
61	111101	1.3625	3.30
62	111110	1.3750	3.30
63	111111	1.3875	3.30

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6.2.6 SWx external components

Table 32 shows the combination of inductor and capacitor values that work with the SWx regulator.

The design is optimized for a 1.0 µH inductor.

Table 32. Acceptable inductance and capacitance values

Inductance / capacitance	2 x 10 µF
1.0 µH	

Table 33 and Table 34 show example inductor and capacitor part numbers respectively.

Table 33. Example inductor part numbers

Part number	Size (mm)	1.0 µH
DFE201610E	2.0 x 1.6	57 mΩ, 3.6 A
DFE201610P	2.0 x 1.6	70 mΩ, 3.1 A
DFE201210U	2.0 x 1.2	95 mΩ, 3.1 A
DFE160810S	1.6 x 0.8	120 mΩ, 2.0 A
DFE201208S	2.0 x 1.2	86 mΩ, 2.4 A
DFE160808S	1.6 x 0.8	144 mΩ, 1.9 A

Table 34. Example capacitor part numbers

Murata part number	Description
GRM188R60J106ME47D	6.3 V, 10 µF, 0402, X5R
GRM188D70J106MA73	6.3 V, 10 µF, 0402, X7R
GRM188R61A106KE69	10 µF 10 V 10 % X5R 0603 .95 mm
GRM219R61A106KE44	10 µF 10 V 10 % X5R 0805 .95 mm

6.3 SW3 detailed description

SW3 is a buck regulator designed to carry a nominal load current of 1.0 A. The output voltage is programmable from 1.8 V to 3.3 V in 100 mV steps. Dynamic voltage scaling is not supported in this regulator.

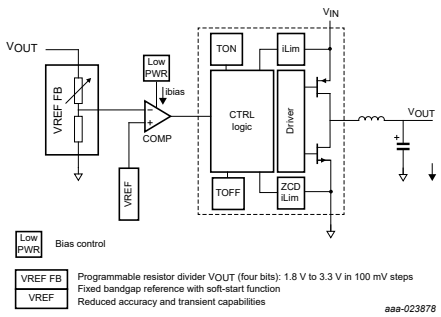

Figure 7. SW3 block diagram

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6.3.1 Regulator control

To improve system efficiency, the buck regulator can operate in different switching/ bias modes. The changing between DCM/CCM takes place automatically based on detecting the load current level. It can be enforced by one of the following means: I^2C programming, exiting/entering the Standby mode, exiting/entering Sleep/ Low-power mode.

Available modes for buck regulators are presented in Table 35 .

Table 36 shows the bit settings for operating the buck converter in these modes based on the PMIC operating state.

Table 35. SW3 buck regulator operating modes

Mode	Description
OFF	The regulator is switched off and the output voltage is discharged using an internal resistor.
Adaptive	This is the default mode of operation of the buck regulator. In this mode, the regulator operates in a quasi-fixed frequency switching mode at moderate and high loads, with pulse skip (variable switching frequency) scheme at light load for optimized efficiency.
F-PWM	In this mode, the regulator is always in PWM mode operation regardless of load conditions.
Low-power	To further extend power savings when the load current is minimal, this mode cuts the quiescent current of the buck converter by reducing the bias to the comparator. The regulator is operated in low power modes (Standby and/or Sleep) with the proper I^2C setting. See Table 36.

Table 36. SW3 buck mode control

PMIC state	SW3_EN	SW3_STBY	SW3_OMODE	SW3_LPWR	SW3_FPWM	SW3 operating mode
Run/Standby/Sleep	0	X	X	X	X	SW disabled
Run	1	X	X	0	0	SW enabled Operates in DCM at light loads
Run	1	X	X	0	1	SW enabled Forced PWM mode
Run	1	X	X	1	0	SW enabled Does not operate in Low-power mode
Run	1	X	X	1	1	SW enabled Forced PWM mode
Standby	1	0	X	X	X	SW disabled
Standby	1	1	X	0	0	SW enabled Operates in DCM at light loads
Standby	1	1	X	0	1	SW enabled Forced PWM mode
Standby	1	1	X	1	0	SW Enabled Operates in Low-power mode
Standby	1	1	X	1	1	SW enabled Forced PWM mode
Sleep	1	X	0	X	X	SW disabled

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Table 36. SW3 buck mode control*...continued*

PMIC state	SW3_EN	SW3_STBY	SW3_OMODE	SW3_LPWR	SW3_FPWM	SW3 operating mode
Sleep	1	X	1	0	0	SW enabled Operates in DCM at light loads
Sleep	1	X	1	0	1	SW enabled Forced PWM mode
Sleep	1	X	1	1	0	SW enabled Operates in Low-power mode
Sleep	1	X	1	1	1	SW enabled Forced PWM mode

6.3.2 Current limit protection

SW3 features high and low-side FET current limit. When current through the FETs go above their respective thresholds, the FET is turned-off to prevent further increase in current.

The protection is enabled in a cycle-by-cycle mode. Hitting either current limit sets the corresponding interrupt sense bits. If the faults persist for longer than the 8.0 ms debounce time, the interrupt status bit is set.

6.3.3 Output voltage setting in SW3

Output voltage of SW3 is programmable via OTP. During start-up (REGS_DISABLE mode to RUN mode), contents of the OTP_SW3_VOLT[5:0] are mapped into the SW3_VOLT[5:0], SW3_STBY_VOLT[5:0], and SW3_SLP_VOLT[5:0] register which set the regulator output voltage during Run, Standby, and Sleep modes respectively.

Values of SW3_VOLT[5:0], SW3_STBY[VOLT[5:0], and SW3_SLP_VOLT[5:0] are read-only and cannot be written to.

Table 37. SW3 output voltage setting

Set point	SW3_VOLT[3:0] SW3_STBY_VOLT[3:0] SW3_SLP_VOLT[3:0]	Output voltage (V)
0	0000	1.80
1	0001	1.90
2	0010	2.00
3	0011	2.10
4	0100	2.20
5	0101	2.30
6	0110	2.40
7	0111	2.50
8	1000	2.60
9	1001	2.70
10	1010	2.80
11	1011	2.90
12	1100	3.00
13	1101	3.10

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Table 37. SW3 output voltage setting...*continued*

Set point	SW3_VOLT[3:0] SW3_STBY_VOLT[3:0] SW3_SLP_VOLT[3:0]	Output voltage (V)
14	1110	3.20
15	1111	3.30

6.3.4 SW3 external components

Table 38 shows the combination of inductor and capacitor values that work with the SW3 regulator.

Table 38. Acceptable inductance and capacitance values

Inductance / capacitance	2 x 10 µF
1.0 µH	

Table 39 and Table 40 show example inductor and capacitor part numbers respectively.

Table 39. Example inductor part numbers

Part number	Size (mm)	1.0 µH
DFE201610E	2.0 x 1.6	57 mΩ, 3.6 A
DFE201610P	2.0 x 1.6	70 mΩ, 3.1 A
DFE201210U	2.0 x 1.2	95 mΩ, 3.1 A
DFE160810S	1.6 x 0.8	120 mΩ, 2.0 A
DFE201208S	2.0 x 1.2	86 mΩ, 2.4 A
DFE160808S	1.6 x 0.8	144 mΩ, 1.9 A

Table 40. Example capacitor part numbers

Murata part number	Description
GRM188R60J106ME47D	6.3 V, 10 µF, 0402, X5R
GRM188D70J106MA73	6.3 V, 10 µF, 0402, X7R
GRM188R61A106KE69	10 µF 10 V 10 % X5R 0603 .95 mm
GRM219R61A106KE44	10 µF 10 V 10 % X5R 0805 .95 mm

7 Low dropout linear regulators, VREFDDR and VSNVS

7.1 General description

This section describes the LDO regulators provided by the PF1550. All regulators use the main band gap as reference.

When a regulator is disabled, the output is discharged by an internal pulldown.

VLDO1 and VLDO3 can be used as load switches by setting the corresponding Load Switch enable bit OTP_VLDOx_LS.

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All general-purpose LDOs have short-circuit protection capability. The short-circuit protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected and REGSCPEN bit is set, the LDO is disabled by resetting its VLDOxEN bit, while at the same time, an interrupt VLDOxFAULTI is generated to flag the fault to the system processor. The VLDOxFAULTI interrupt is maskable through the VLDOxFAULTM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, the regulators are not automatically be disabled upon a short-circuit detection. However, the current limiter continues to limit the output current of the regulator. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators are disabled if an overloaded condition occurs. A fault interrupt, VLDOxFAULTI is generated in an overload condition regardless of the state of the REGSCPEN bit. Each LDO features a Low-power mode where the quiescent current consumed is significantly lower than in regulator operation. In the Low-power mode, load current of each regulator is limited to 10 mA.

7.2 LDO1 and LDO3 detailed description

LDO1 and LDO3 are identical 300 mA low dropout (LDO) regulators that provide output voltage with high accuracy and are programmable through I^2C interface bits. Being identical, reference is made to these LDOs as LDOy.

To support this wide input range, LDOy circuit incorporates a PMOS pass FET as well as an NMOS pass FET. The LDO uses the main band gap as its reference.

The regulator incorporates a soft-start circuit that ramps the internal reference in order to provide smooth output waveform with minimal overshooting during power-up. When the regulator is disabled, the output is discharged by an internal pulldown resistor. Additionally, the LDO can be used as a load switch by setting the corresponding Load Switch enable bit OTP_LDOy_LS.

Moreover, LDOy includes current limit protection with the option to turn off the LDO when an overcurrent is detected.

7.2.1 Features summary

- Input range LDO from 1.0 V to 4.5 V
- Programmable output voltage between 0.75 V to 1.5 V (uses NMOS) or 1.8 V and 3.3 V (uses PMOS) with 2 % accuracy
- Soft-start ramp control during power-up and discharge mechanism during power-down
- Low quiescent current (~ 2.5 μA) at Low-power mode
- Current limit protection
- Configurable into load switch via OTP bit

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7.2.2 LDOy block diagram

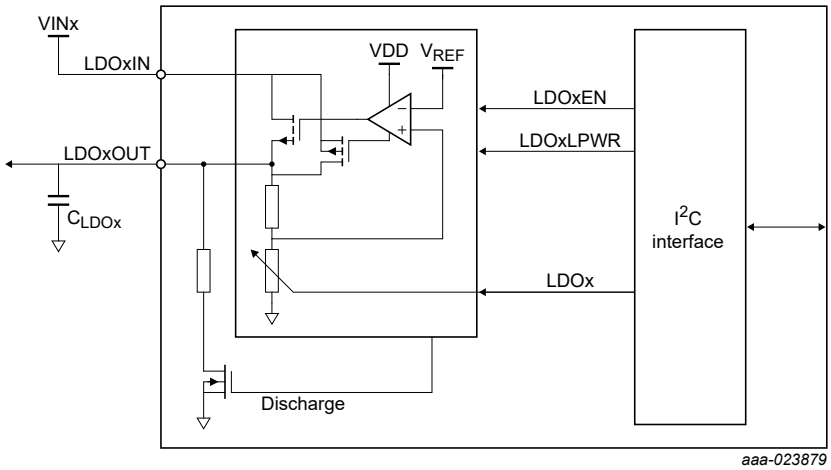

Figure 8. LDOy Block Diagram

7.2.3 LDOy external components

Use a 4.7 µF X5R/X7R capacitor from output to ground with a voltage rating at least 2 times the nominal output voltage.

7.2.4 LDOy output voltage setting

LDOy output voltage is programmed by setting the LDOy[4:0] bits as shown in Table 41.

Table 41. LDOy output voltage setting

Set point	LDOy[4:0]	LDOy output (V)
0	00000	0.7500
1	00001	0.8000
2	00010	0.8500
3	00011	0.9000
4	00100	0.9500
5	00101	1.0000
6	00110	1.0500
7	00111	1.1000
8	01000	1.1500
9	01001	1.2000
10	01010	1.2500
11	01011	1.3000
12	01100	1.3500
13	01101	1.4000
14	01110	1.4500
15	01111	1.5000
16	10000	1.8000
17	10001	1.9000

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Table 41. LDOy output voltage setting...*continued*

Set point	LDOy[4:0]	LDOy output (V)
18	10010	2.0000
19	10011	2.1000
20	10100	2.2000
21	10101	2.3000
22	10110	2.4000
23	10111	2.5000
24	11000	2.6000
25	11001	2.7000
26	11010	2.8000
27	11011	2.9000
28	11100	3.0000
29	11101	3.1000
30	11110	3.2000
31	11111	3.3000

7.2.5 LDOy low-power mode operation

LDOy can operate in a Low-power mode with reduced quiescent current. The Low-power mode can be activated in Standby and Sleep modes by setting the LDOy_LPWR bit as shown in Table 42. Maximum load current is limited to 10 mA when operating in the Low-power mode.

Table 42. LDOy control bits

PMIC state	LDOy_EN	LDOy_STBY	LDOy_OMODE	LDOy_LPWR	LDOy operating mode
Run/Standby/Sleep	0	X	X	X	LDO disabled
Run	1	X	X	X	LDO enabled
Standby	1	0	X	X	LDO disabled
Standby	1	1	X	0	LDO enabled
Standby	1	1	X	1	LDO enabled in Low-power mode
Sleep	1	X	0	X	LDO disabled
Sleep	1	X	1	0	LDO enabled
Sleep	1	X	1	1	LDO enabled in Low-power mode

7.2.6 LDOy current limit protection

LDOy has built in current limit protection. When the load current exceeds the current limit threshold, the regulator goes from a voltage regulation mode to a current regulation mode that limits the available output current.

By setting the REGSCPEN bit, LDOy can be automatically disabled in the event of an overcurrent situation. In the event of an overcurrent, the LDO is disabled by resetting its LDOy_EN bit, while at the same time an interrupt LDOy_FAULTI is generated to flag the fault to the system processor. The LDOy_FAULTI interrupt is maskable through the LDOy_FAULTM mask bit.

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If REGSCPEN is not set, the regulator will not be automatically disabled, but will instead enter the current limit mode. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators will be disabled if an overloaded condition occurs. A fault interrupt, LDOy_FAULTI, is generated in an overload condition regardless of the state of the REGSCPEN bit.

Current limit is not active when LDOy is operated in the load switch mode.

7.2.7 LDOy load switch mode

The LDOy path can be turned into a switch by setting the OTP_LDOy_LS bit. Setting this bit fully turns on the LDO pass FET. This could be useful if power domain partitioning or additional isolation is needed on the system application. Soft-start is engaged during start-up of the load switch to reduce inrush currents.

7.3 LDO2 detailed description

LDO2 is a 400 mA low dropout (LDO) regulator that provides output voltage with high accuracy and programmable through I^2C/ interface bits. To support this wide input range, the LDO circuit incorporates a PMOS pass FET. The LDO uses the main bandgap as its reference.

The regulator incorporates a soft-start circuit that ramps the internal reference in order to provide smooth output waveform with minimal overshooting during power-up. When the regulator is disabled, the output is discharged by an internal pull-down resistor. The pulldown is also activated when RESETBMCU is low.

Moreover, LDO2 includes current limit protection with option to turn off the LDO when an overcurrent is detected.

7.3.1 LDO2 features summary

- Input range LDO from 2.8 V to 4.5 V
- Programmable output voltage between 1.8 V and 3.3 V with 2 % accuracy
- Soft-start ramp control during power-up and discharge mechanism during power-down
- Low quiescent current (~ 1.5 μA) at Low-power mode
- Current limit protection

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7.3.2 LDO2 block diagram

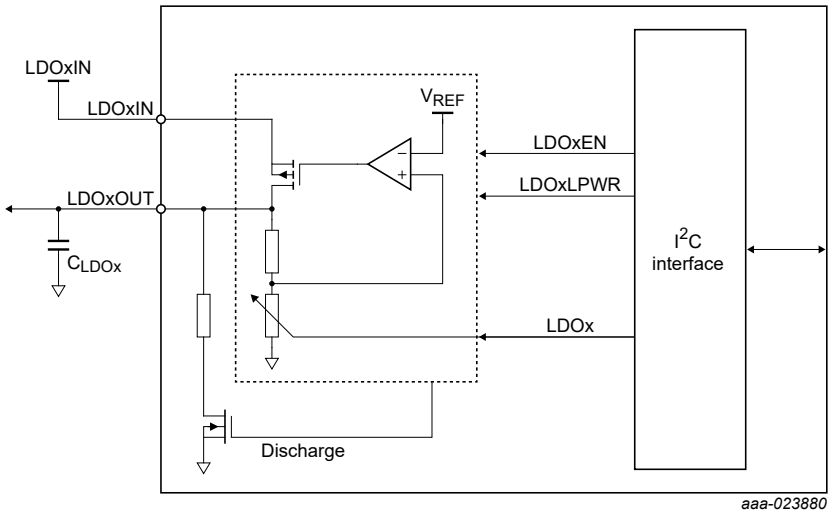

Figure 9. LDO2 block diagram

7.3.3 LDO2 external components

Use a 10 µF X5R/X7R capacitor from output to ground with a voltage rating at least 2 times the nominal output voltage.

7.3.4 LDO2 output voltage setting

LDO2 output voltage is programmed by setting the VLDO2[3:0] bits as shown in Table 43.

Table 43. LDO2 output voltage setting

Set point	VLDO2[3:0]	VLDO2 output (V)
0	0000	1.80
1	0001	1.90
2	0010	2.00
3	0011	2.10
4	0100	2.20
5	0101	2.30
6	0110	2.40
7	0111	2.50
8	1000	2.60
9	1001	2.70
10	1010	2.80
11	1011	2.90
12	1100	3.00
13	1101	3.10
14	1110	3.20
15	1111	3.30

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7.3.5 LDO2 Low-power mode operation

LDO2 can operate in a Low-power mode with reduced quiescent current. The Low-power mode can be activated in Standby and Sleep modes by setting the LDO2LPWR bit as shown in Table 44. Maximum load current is limited to 10 mA when operating in the Low-power mode.

Table 44. LDO2 control bits

PMIC state	LDO2EN	LDO2STBY	LDO2OMODE	LDO2LPWR	LDO2 operating mode
Run	0	X	X	X	LDO disabled
Run	1	X	X	X	LDO enabled
Standby	1	0	X	X	LDO disabled
Standby	1	1	X	0	LDO enabled
Standby	1	1	X	1	LDO enabled in Low-power mode
Sleep	1	X	0	X	LDO disabled
Sleep	1	X	1	0	LDO enabled
Sleep	1	X	1	1	LDO enabled in Low-power mode

7.3.6 LDO2 current limit protection

LDO2 has built in current limit protection. When the load current exceeds the current limit threshold, the regulator goes from a voltage regulation mode to a current regulation mode limiting the available output current.

By setting the REGSCPEN bit, LDO2 can be automatically disabled in the event of an overcurrent situation. In the event of an overcurrent, the LDO is disabled by resetting its VLDO2EN bit, while at the same time an interrupt VLDO2FAULTI is generated to flag the fault to the system processor. The VLDO2FAULTI interrupt is maskable through the VLDO2FAULTM mask bit.

If REGSCPEN is not set, the regulator is not automatically disabled, but instead enters the current limit mode. By default, the REGSCPEN is not set; therefore, at start-up none of the regulators are disabled if an overloaded condition occurs. A fault interrupt, VLDO2FAULTI is generated in an overload condition regardless of the state of the REGSCPEN bit.

7.4 VREFDDR reference

VREFDDR is an internal NMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories.

A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load.

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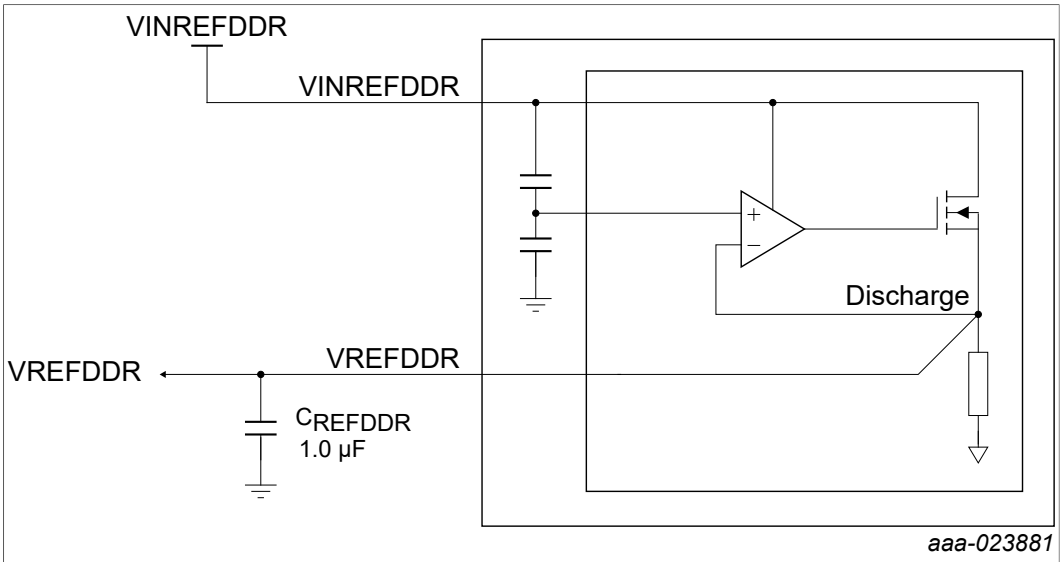

Figure 10. VREFDDR block diagram

7.5 VSNVS LDO/switch

VSNVS powers the low-power SNVS/RTC domain on the processor. It derives its power from either VSYS or a coin cell. When powered by both, VSYS powers VSNVS if VSYS > VTH threshold and LICELL powers VSNVS when VSYS < VTL. When powered by VSYS, VSNVS is an LDO capable of supplying 2.0 mA at 3.0 V. When powered by coin cell, VSNVS output tracks the coin cell voltage with a switch. In this case, the VSNVS voltage is simply the coin cell voltage minus the voltage drop across the switch.

Upon subsequent removal of VSYS, with the coin cell attached, VSNVS changes configuration from an LDO to a switch.

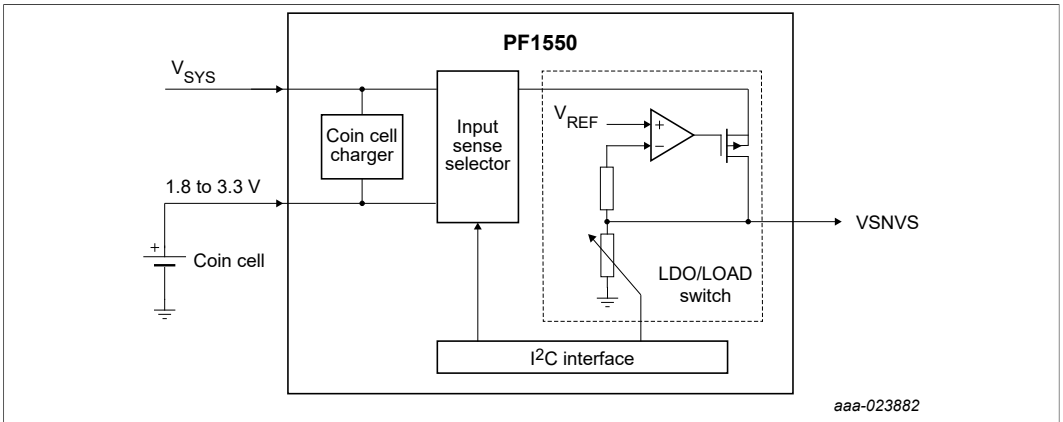

Figure 11. VSNVS block diagram

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8 Battery charger description

The PF1550 charger is an integrated 1-cell Li+ charger with a single VBUS power input and dual path output. All power switches for charging and switching the load between battery and external power are included on chip. No external MOSFETs, blocking diodes or current sense resistors are required.

The VBUS input operates from 4.0 V to 6.5 V with up to 22 V overvoltage protection. The PF1550 internally blocks current from the battery and system back to the inputs when no input supply is present. Other features include precharge battery conditioning and timer, fast charge timer, battery overvoltage protection, charge status and fault outputs, battery thermistor monitor and thermal regulation.

Figure 12 shows a high level internal block diagram of the charger block. The PMIC is powered from the VSYS node in the PF1550.

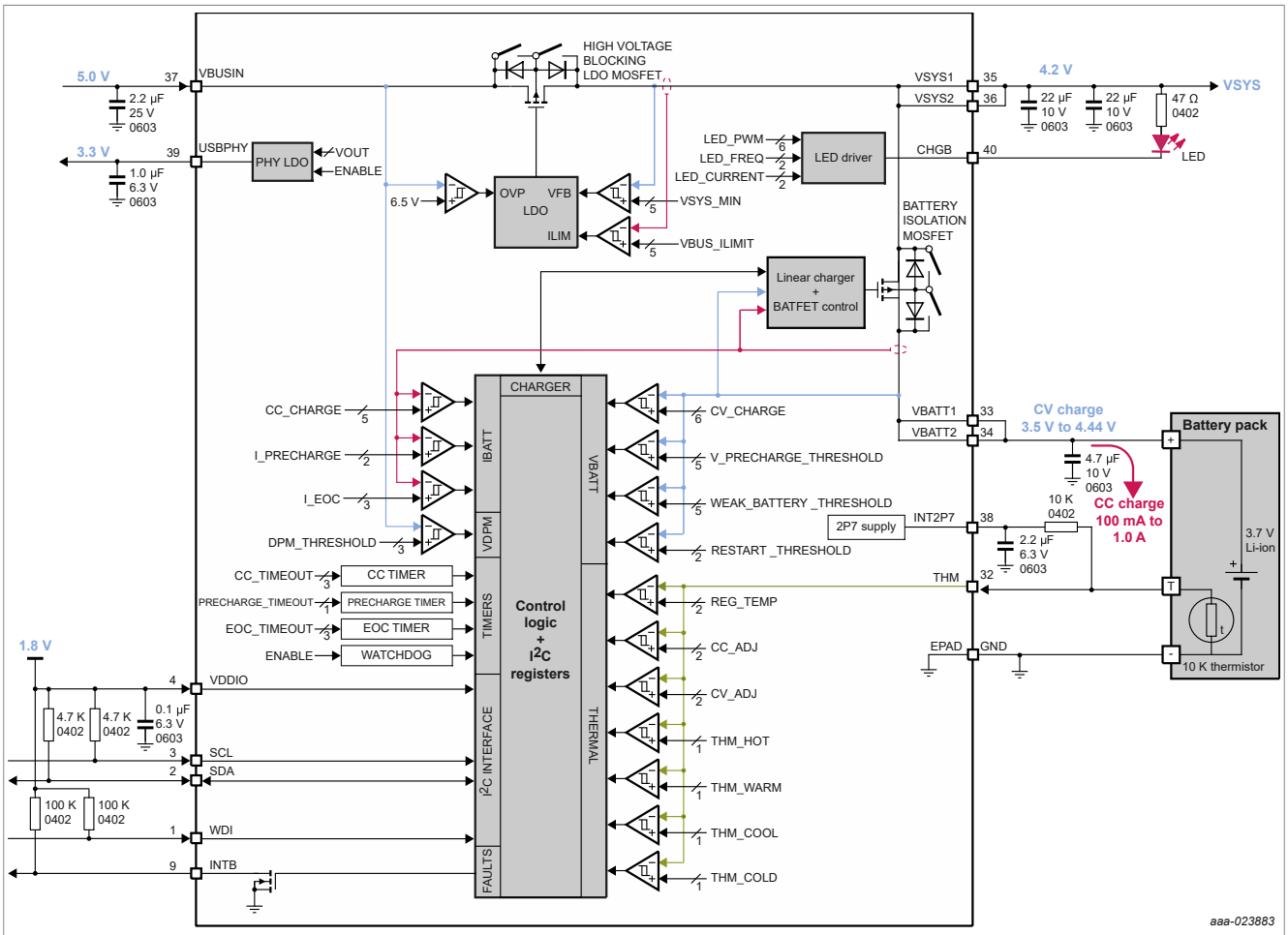

Figure 12. Battery charger internal block diagram

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8.1 Operating modes and behavioral description

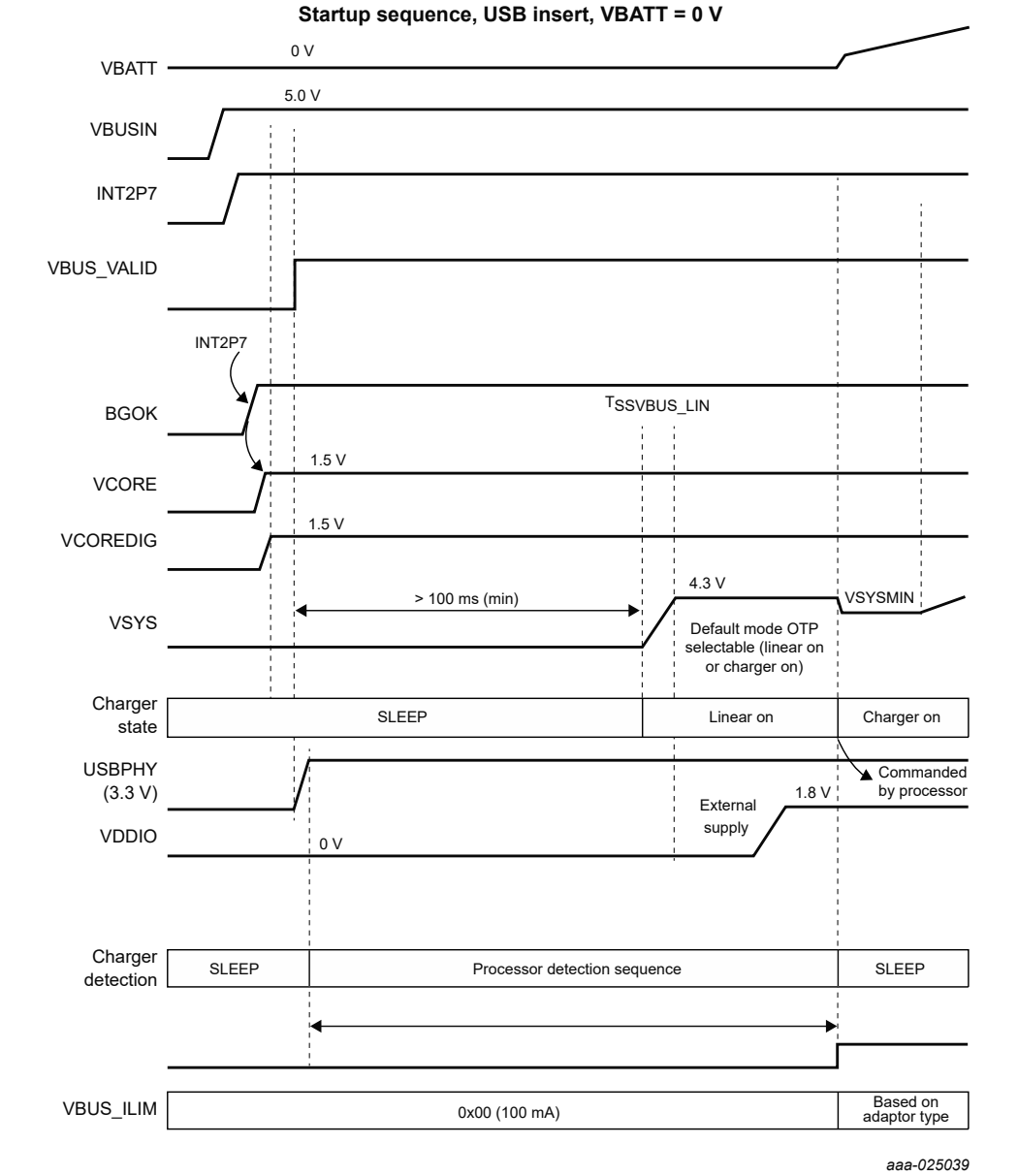

Figure 13. Charger low battery (Startup sequence, USB insert, VBATT = 0 V)

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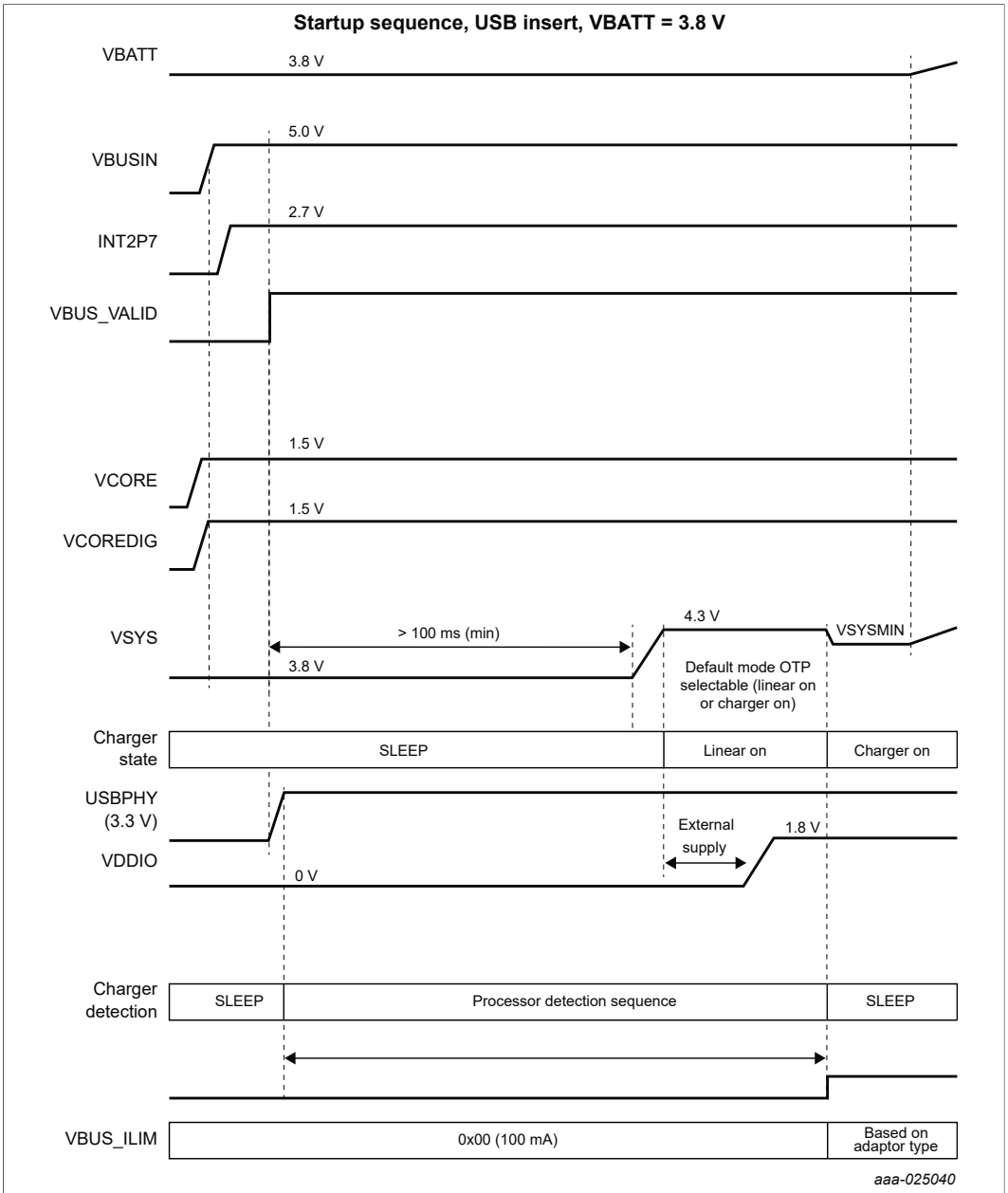

Figure 14. Charger healthy battery (Startup sequence, USB insert, VBATT = 3.8 V)

Table 45. Battery regulation voltage register

BATTERY REGULATION VOLTAGE REGISTER								
ADDR:	0x8F							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	VSYSMIN		CHGCV					
POR:	0	0	1	0	1	0	1	1
ACCESS:								

The $VSYS_{MIN}$ value is programmable via OTP as per the following table.

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Table 46. $VSYS_{MIN}$ setting

VSYSMIN[1:0] setting	$VSYS_{MIN}$ setting (V)
00	3.5
01	3.7
10	4.3
11	Reserved

The $VSYS_{MIN}$ setting is the "normal" regulation point for VSYS. This parameter sets the point where the VSYS loop starts taking control and regulates the output. 4.3 V is the recommended setting to ensure that there is enough headroom before reaching UVDET (PMIC undervoltage detection, 2.9 V typ.).

Selecting lower settings causes the VSYS loop to start regulating, and reduces charging current to lower the VSYS threshold, thus reducing the headroom.

Typically, the VSYS output range can go as low as 300 mV below the $VSYS_{MIN}$ setting. Therefore, the recommended setting for the VSYS output should be between 4.0 V to 4.3 V.

8.2 Charger input source detection

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three characteristics to be valid:

- VBUS must be above V_{UVLO} (4.2 V max.) to be valid
- VBUS must be below its overvoltage lockout threshold (V_{OVLO} (6.0 V min.))
- VBUS must be above the system voltage by V_{IN2SYS} (50 mV / 175 mV programmable via OTP)

The VBUS input generates an input interrupt when its status changes. The input status can be read with VBUS_OK and VBUS_SNS registers. Interrupts can be masked with VBUS_M register.

Note: *Adaptor removal is defined as VBUS < V_{UVLO}.*

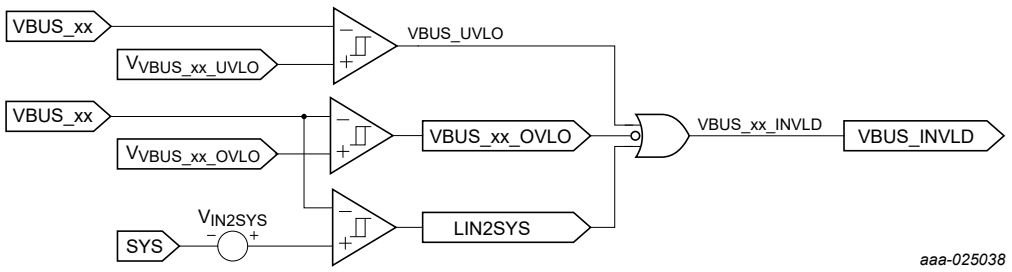

Figure 15. Input source detection delay

8.3 Input self-discharge for reliable charger input interrupt

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed the input voltage decays below the UVLO threshold in a reasonable time.

A 2.2 µF input capacitance charged up to the maximum OVLO threshold (V_{OVLO}) decays down to the minimum UVLO threshold within 300 ms (t_{INSD}). The input self-discharge is

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implemented by with a 30 kΩ resistor (R_{INSD}) from VBUSIN input to ground. The input self-discharge resistor is deactivated in the low-power mode to reduce total quiescent current.

8.4 Charger state diagram

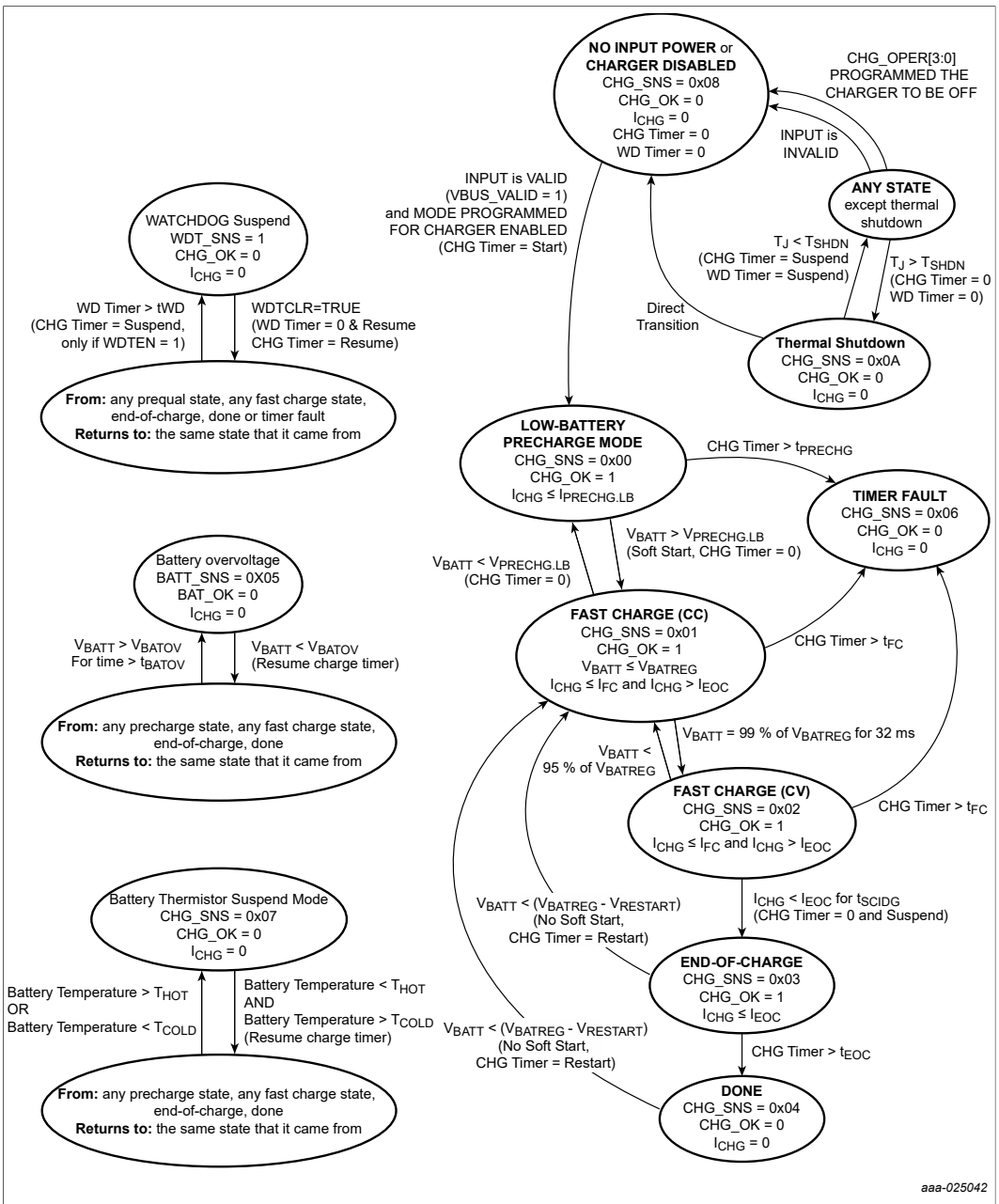

Figure 16. Charger state diagram

8.5 Charging profile

The battery is charged in three modes. Linear control of the BATFET has two subset modes (Trickle and Linear constant current mode).

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- Linear control of BATFET
  - Trickle (programmable from 55 mA/100 mA based on battery voltage)
  - Linear constant current mode from 100 mA to 1000 mA
- Constant current (CC)
- Constant voltage (CV)

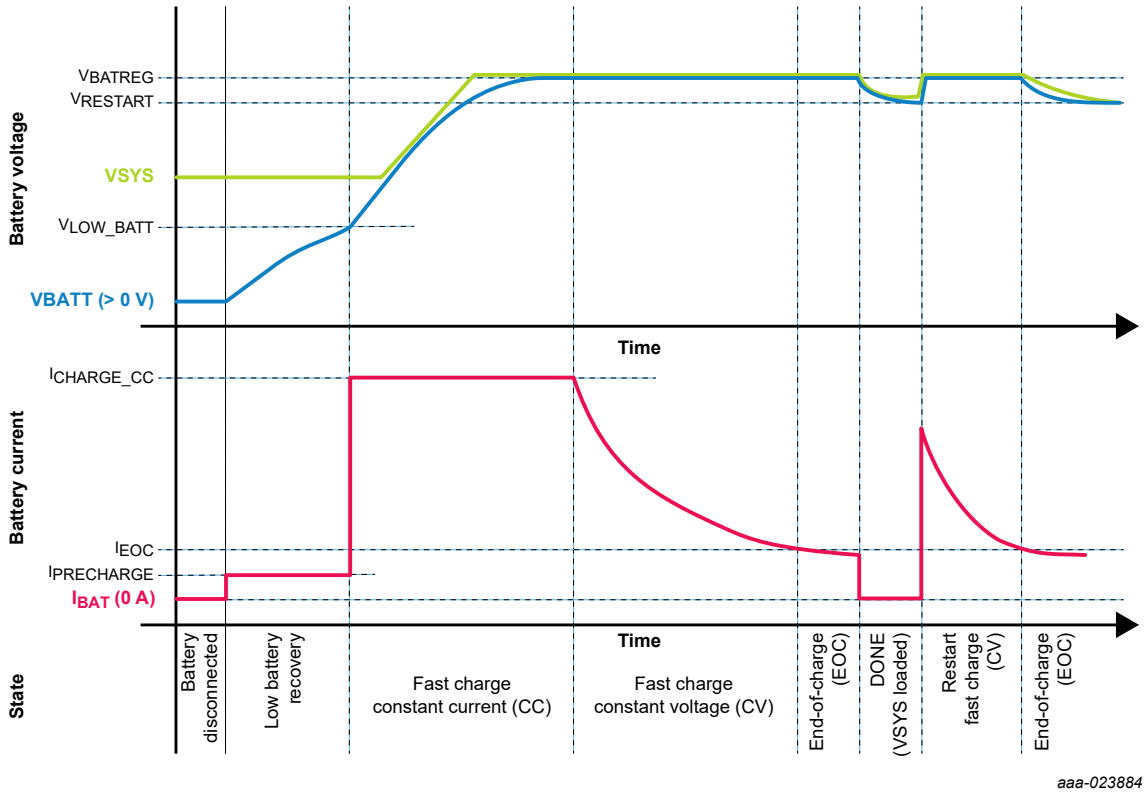

Figure 17. Charging profile

8.5.1 Precharge state

The precharge state is entered when the main-battery voltage is less than $V_{PRECHG.LB}$ which is precharge (low battery) charging voltage threshold set by PRECHGLB_THRS[6:5]. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK bit is set, and CHG_SNS register is set to 0x00. In the precharge state, the charge current into the battery is equal or lower than $I_{PRECHG.LB}$ (45 mA typ).

Following events causes the state machine to exit this state:

1. When the main battery voltage rises above $V_{PRECHG.LB}$, the charger enters the next state in the charging cycle: “Fast-Charge Constant Current" state.
2. If the battery charger remains in this state for longer than t_{PRECHG}, the charger state machine transitions to the “Timer Fault” state.
3. If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note: *The precharge state works with battery voltages down to 0 V.*

The low 0 V operation typically allows this battery charger to revive batteries that have an “open” internal pack protector. Typically, the pack internal protection circuit isolates the Lithium-ion cell if the battery pack has detected an overcurrent, undervoltage, or

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overvoltage. When a battery with an “open” internal pack protector is used with this charger, the low-battery precharge mode forces a small current into the 0 V battery. This current raises the pack’s terminal voltage above the pack revive threshold, causing the internal pack protection switch to reconnect the Lithium-ion cell.

A normal battery pack typically could stay in the low-battery precharge state for several minutes. If a battery pack stays in low-battery precharge for longer than t_{PRECHG}, it may be defective.

8.5.2 Fast charge constant current state

The fast-charge constant current (CC) state occurs when the main-battery voltage is greater than the precharge threshold and less than the battery regulation threshold ($V_{PRECHG.LB} < V_{BATT} < V_{CHGCV}$). In the fast-charge CC state, the current into the battery is less than or equal to I_{FC} (excluding accuracy I_{FCACC}).

Charge current may be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The system load is consuming adapter current. When the voltage drop between VBUS and VSYS is below the VIN2SYS threshold, charging stops and charge current drops down to 0 A.

Note: *The system load always gets priority over the battery charge current.*

The system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the main battery voltage rises above V_{BATREG}, the charger enters the next state in the charging cycle: "Fast Charge (CV)".
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the "Timer Fault" state.
- If the watchdog timer is not serviced, the charger state machine transitions to the "Watchdog Suspend" state.

The battery charger dissipates the most power in the fast-charge constant current state. This power dissipation causes the internal die temperature to rise. If the die temperature exceeds the threshold set by REGTEMP[1:0], I_{FC} is reduced. This is covered in Section 8.8.1 "Thermal regulation".

Table 47. Charger current control register

CHARGER CURRENT CONTROL REGISTER								
ADDR:	0x8E							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	RESERVED	PRECHGLB_THRESHOLD		CHG_CC				
POR:	0	0	0	0	0	0	0	0
ACCESS:	—							

The fast charge current is programmable via I^2C using the bits in Table 48.

Table 48. Constant current charge settings

CHG_CC[4:0] setting	I_{FC} current (mA)
00000	100
00001	150

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Table 48. Constant current charge settings...*continued*

CHG_CC[4:0] setting	I_{FC} current (mA)
00010	200
00011	250
00100	300
00101	350
00110	400
00111	450
01000	500
01001	550
01010	600
01011	650
01100	700
01101	750
01110	800
01111	850
10000	900
10001	950
10010	1000
10011	1050 (Reserved)
10100	1100 (Reserved)
10101	1150 (Reserved)
10110	1200 (Reserved)
10111	1250 (Reserved)
11000	1300 (Reserved)
11001	1350 (Reserved)
11010	1400 (Reserved)
11011	1450 (Reserved)
11100	1500 (Reserved)
11101	1550 (Reserved)
11110	1600 (Reserved)
11111	1650 (Reserved)

To insure proper operation, the maximum CC current selected must be one setting below input current limit (in charger normal mode).

In normal mode, when $V_{SYS} < V_{SYSMINLOOPx}$ ($V_{SYSMINLOOPx} = V_{SYSMINx} - 300$ mV), digital logic automatically controls maximum CC current (one setting lower than charger input current limit I_{LIM} setting). If 100 mA input current limit is selected, the charge current is forced to 50 mA to allow enough current for VSYS.

The Charger Low-power mode (CLPM) is entered automatically when the 50 mA input current limit setting, or lower, is selected and when VBATT > 2.8 V.

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8.5.3 Fast charge constant voltage state

The fast-charge constant voltage (CV) state occurs when the battery voltage rises to V_{BATREG} from the fast-charge CC state.

In the fast-charge CV state, the battery charger maintains V_{BATREG} across the battery and the charge current is less than or equal to I_{FC}. Charger current decreases exponentially in this state as the battery becomes fully charged.

The BATFET control circuitry may reduce the charge current for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The system load is consuming adapter current. The system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below I_{EOC} for t_{SCIDG}, the charger enters the next state in the charging cycle: “End-of-Charge”.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note: *During the CC to CV transition, the charge current can be momentarily higher than I_{FC}. This current is safe and does not result in over charging the battery. After this transition, the charge current decays and is less than or equal to I_{FC}.*

Table 49. Battery regulation voltage register

BATTERY REGULATION VOLTAGE REGISTER								
ADDR:	0x8F							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	VSYSMIN		CHGCV					
POR:	0	0	1	0	1	0	1	1
ACCESS:								

The CV setting is programmable via I^2C using the bits in Table 50.

Table 50. CV settings

CHGCV[5:0]	Output voltage (V)
000000	3.50
000001	3.50
000010	3.50
000011	3.50
000100	3.50
000101	3.50
000110	3.50
000111	3.50
001000	3.50
001001	3.52
001010	3.54

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Table 50. CV settings...*continued*

CHGCV[5:0]	Output voltage (V)
001011	3.56
001100	3.58
001101	3.60
001110	3.62
001111	3.64
010000	3.66
010001	3.68
010010	3.70
010011	3.72
010100	3.74
010101	3.76
010110	3.78
010111	3.80
011000	3.82
011001	3.84
011010	3.86
011011	3.88
011100	3.90
011101	3.92
011110	3.94
011111	3.96
100000	3.98
100001	4.00
100010	4.02
100011	4.04
100100	4.06
100101	4.08
100110	4.10
100111	4.12
101000	4.14
101001	4.16
101010	4.18
101011 [1]	4.20
101100	4.22
101101	4.24
101110	4.26
101111	4.28
110000	4.30
110001	4.32
110010	4.34

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Table 50. CV settings...*continued*

CHGCV[5:0]	Output voltage (V)
110011	4.36
110100	4.38
110101	4.40
110110	4.42
110111	4.44
111000	4.44
111001	4.44
111010	4.44
111011	4.44
111100	4.44
111101	4.44
111110	4.44
111111	4.44

[1] Default setting

Table 51. Charger timers register

CHARGER TIMERS REGISTER								
ADDR:	0x8A							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	TPRECHG	RESERVED	EOCTIME			FCHGTIME		
POR:	0	0	0	0	1	0	1	0
ACCESS:		—						

The fast charge timer is programmable via I^2C through the bits in Table 52:

Table 52. Fast charge timer settings

FCHGTIME[2:0] setting	Fast charge timer duration (Hours)
000	Disable
001	2
010	4
011	6
100	8
101	10
110	12
111	14

The fast charge timer fault can occur in the fast charge mode, the system draws current such that the charger state machine is technically in the "fast charge" state but the battery is not really in "fast charge". This can happen if the current available from the charger input is not sufficient to provide system load as well as charge the battery. It is up to the processor to react to the timer fault accordingly. It can decide to restart charging (via CHG_OPER), or accept it as an actual timer fault.

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8.5.4 End-of-charge state

The end-of-charge state can only be entered from the fast-charge CV state when the charger current decreases below I_{EOC} for t_{SCIDG}. After being in the top-off state for t_{SCIDG} + $t_{DB(EOC)}$, an interrupt is generated, CHG_OK is set and CHG_SNS = 0x03. In the end-of-charge state, the battery charger tries to maintain V_{CHGCV} across the battery and typically the charge current is less than or equal to I_{EOC}.

The BATFET control circuitry may reduce the charge current lower than the battery may otherwise consume for any of the following reasons:

- The charger input is in input current limit
- The charger input voltage is low
- The system load is consuming adapter current. The system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the end-of-charge time (t_{EOC}), the charger enters the next state in the charging cycle: “DONE”.
- If $V_{BATT} < V_{BATREG} – V_{RESTART}$, the charger goes back to the “FAST CHARGE (CC)” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Table 53. Charger EOC configuration register

CHARGER EOC CONFIGURATION REGISTER								
ADDR:	0x8D							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	EOC_MODE	IEOC			EOC_EXIT	FRC_ BATT_ISO	CHG_RESTART	
POR:	0	1	0	0	0	0	0	1
ACCESS:								

The EOC current value is programmable per the following table:

Table 54. EOC current thresholds

IEOC[2:0] setting	I_{EOC} current (mA)
000	5
001	10
010	20
011	30
100	50
101	Reserved
110	Reserved
111	Reserved

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Table 55. Charger timers register

CHARGER TIMERS REGISTER								
ADDR:	0x8A							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	TPRECHG	RESERVED	EOCTIME			FCHGTIME		
POR:	0	0	0	0	1	0	1	0
ACCESS:		—						

The EOC State timer is programmable per the following table:

Table 56. EOC state timer settings

EOCTIME[2:0] setting	EOC timer duration (Minutes)
000	0 (16 seconds debounce)
001	10
010	20
011	30
100	40
101	50
110	60
111	70

8.5.5 Done state

The battery charger enters its done state after the charger has been in the end-of-charge state for t_{EOC}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated, CHG_OK is cleared and CHG_SNS = 0x04.

The following events cause the state machine to exit this state:

- If $V_{BATT} < V_{BATREG} – V_{RESTART}$, the charger goes back to the "FAST CHARGE (CC)" state
- If the watchdog timer is not serviced, the charger state machine transitions to the "Watchdog Suspend" state

In the done state, the charge current into the battery (I_{CHG}) is 0 A. In the done state, the charger presents a very light load to the battery. If the system load presented to the battery is low (<<100 µA), then a typical system can remain in the done state for many days.

If left in the done state long enough, the battery voltage decays below the restart threshold ($V_{RESTART}$) and the charger state machine transitions back into the fast-charge CC state. There is no soft start (di/dt limiting) during the done state to fast-charge state transition. In the done state, the BATFET is fully closed. The correct way to trigger restart feature is to pull loading from VSYS, in order to discharge VBATT.

8.6 Battery supplement mode

The Battery supplement mode is a powerful feature of the PF1550 charger, allowing the device to temporarily suspend charging, and draw supplemental current from the battery to maintain power to the system when the load demands more current than the VBUS supply can deliver. This provides more flexibility when architecting their system. The

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battery capacity can be chosen to handle periods of peak loading, which may be currents higher than supported by the VBUS supply.

If the system load current exceeds the VBUS input current limit, the VSYS supply current is no longer be able to support the load demand and the VSYS output voltage decreases. When VSYS falls below VBATT, the PF1550 suspends charging and enters the Battery supplement mode. In this mode, the battery provides current to support the VSYS load demand.

If the load demand on VSYS now decreases, the VSYS output voltage recovers, and begins to rise. When VSYS rises above VBATT, the PF1550 exits the Battery supplement mode and resumes charging the battery in the CC charging phase.

When VBATT decreases lower than the restart threshold, the part enters CC state from DONE. Then if the loading on VSYS decreases and VSYS > VBATT, charger starts to charge from the CC state.

8.7 Power path features

8.7.1 VSYS regulation

In the case of a low battery, the LDO path regulates VSYS to either 3.5 V, 3.7 V, or 4.3 V. This allows the system to power up with a low battery while the battery gets charged. See Table 46.

8.7.2 Input current limit

The default settings of the VBUSIN and CHG_OPER control bits are such that when a charge source is applied to VBUSIN, the PF1550 turns on its linear regulator in LINEAR-ON or CHARGE-ON (via OTP), and limits the charge current to 100 mA (via OTP).

See Section 12 "Register map" for the default values for specific registers/bits.

The input current limit works by monitoring the current being drawn from the input and comparing it to the programmed current limit. The current limit should be set based on the current-handling capability of the input adapter. Generally, this limit is chosen to optimally fulfill the system-power requirements while achieving a satisfactory charging time for the batteries. If the adapter current exceeds its output capability, the charger responds by reducing the charger current, thus keeping the current drawn from the adapter within its capability.

There is a precision current sense circuitry that monitors the input current whenever internal INT_2P7 is asserted. The input current limit logic signal is used to reduce quiescent current when the charger is not plugged in by turning off the current sense amplifier. The input current limit should include current consumed by the charger block.

There is a low-power mode for the linear regulator where it consumes less than 2.5 mA bias current at 25 °C. This is useful for the 10 mA to 50 mA input current limit settings.

The input current limit also includes a second control which is voltage-based. When it drops below the desired input, it generates an interrupt to decrease the fast-charge current. This is further covered in input voltage regulation mode.

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Table 57. VBUS input current limit register

VBUS INPUT CURRENT LIMIT REGISTER								
ADDR:	0x94							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	VBUS_LIN_ILIM					RESERVED		
POR:	0	1	1	0	1	0	0	0
ACCESS:	R/W	R/W	R/W	R/W	R/W	—		

The table below shows valid input current limit settings.

Table 58. Input current limit settings

VBUS_LIN_ILIM[4:0] setting	VBUS input current limit (mA)
00000	10
00001	15
00010	20
00011	25
00100	30
00101	35
00110	40
00111	45
01000	50
01001	100
01010	150
01011	200
01100	300
01101	400
01110	500
01111	600
10000	700
10001	800
10010	900
10011	1000
10100	1500
10101 to 11101	Reserved
11110	Reserved
11111	Reserved

8.7.3 Battery thermistor

Thermistor is not supported when there is no valid charger inserted. A bank of comparators monitors the thermistor to provide battery temperature information for the battery charger. The comparator thresholds are based on the recommended NTC NCP15XH103F03RC (10 K) from Murata or equivalent. Each comparator has 3 ℃ hysteresis. There are I^2C selections for the T_{HOT} and T_{COLD} temperature threshold.

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8.7.4 BATFET soft start

When the battery is first plugged into the PF1550, BATFET features an internal soft-start that prevents high inrush currents into the capacitors at the VSYS node.

Note: *This feature must be tested during lab validation for functionality. It is not required to cover this in production as there are no critical pass/fail criteria for this feature.*

8.8 Thermal

8.8.1 Thermal regulation

Thermal regulation maximizes the battery charge current while regulating the PF1550 junction temperature. The target charge current reduction is achieved with a digital control loop. As shown in the following figure, when the die temperature exceeds the value programmed by REGTEMP[1:0], a thermal limiting circuit reduces the battery charger's target current.

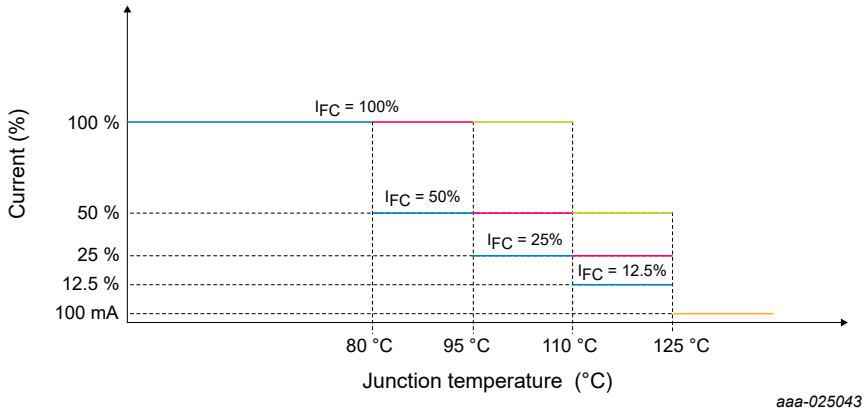

Figure 18. Thermal regulation

Table 59. Thermal regulation

REGTEMP[1:0]	50 % CC Thermal regulation set point (T_{JREG0})	25 % CC Thermal regulation set point (T_{JREG1})	12.5 % CC Thermal regulation set point (T_{JREG2})	100 mA CC Thermal regulation set point (T_{JREG3})
00	80 °C	95 °C	110 °C	125 °C
01	95 °C	110 °C	N/A	125 °C
10	110 °C	N/A	N/A	125 °C
11	N/A	N/A	N/A	125 °C

As shown in the following figure, a hysteresis mechanism is implemented.

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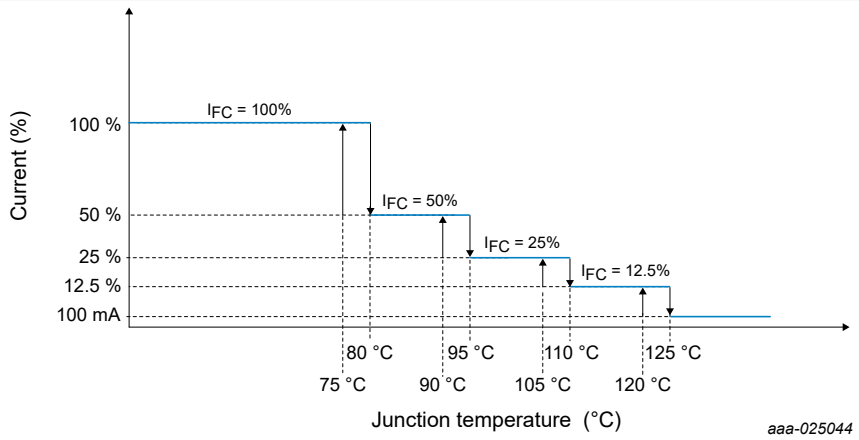

Figure 19. Thermal regulation (Current versus Temp, example with REGTEMP[1:0] = 00 and hysteresis

When thermal regulation changes state, a THM_I interrupt is generated. This is to allow time for the system's microprocessor to read the status of the thermal regulation loop via the TREG_SNS status bit.

This following diagram shows an example of the thermal regulation over time. The green arrows represent when the CHG_I interrupt is generated.

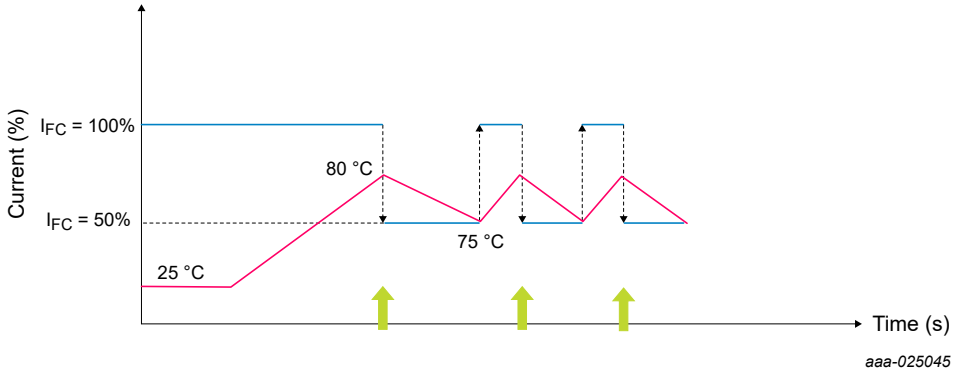

Figure 20. Thermal regulation (Current, Temp versus Time, example with REGTEMP[1:0] = 00 and hysteresis

The thermal regulation does not affect the CHG_OK bit (only information contained within CHG_SNS affects CHG_OK).

8.8.2 Thermal foldback

The thermal foldback function reduces max. charging current which goes into the battery when the charger junction temperature (T_{JREGx}) reaches a pre-defined temperature set by REGTEMP[1:0]. Thermal foldback loop being active is not considered to be an abnormal condition.

After the temperature reaches T_{JREG0}, the charging current is reduced to 50 % of the final CC charging current value.

After the charger temperature rises above T_{JREG0}, if the charger temperature falls back below T_{JREG0} −5 °C, charging current reverts to 100 % of the final CC charging current value.

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If the charger temperature rises and reaches T_{JREG1} but below 125 °C, charging current is reduced to 25 % of the final CC charging current value.

After the charger temperature rises above T_{JREG1}, if the charger temperature falls back below T_{JREG1} −5 °C, charging current reverts to 50 % of the final CC charging current value.

If the charger temperature rises and reaches T_{JREG2} but below 125 °C, charging current is reduced to 12.5 % of the final CC charging current value.

After the charger temperature rises above T_{JREG2}, if the charger temperature falls back below T_{JREG2} −5 °C, charging current reverts to 25 % of the final CC charging current value.

If the charger temperature reaches 125 °C, charging current is reduced to 100 mA.

After the charger temperature rises above 125 °C, if the charger temperature falls back below 120 °C, charging current reverses back to 12.5 % of the final CC charging current value.

The thermal foldback function is not available for LPM.

At charger junction temperature above T_{JREGx}, if the charger current is already set to 100 mA, the thermal foldback function keeps the current 100 mA. The final charging current min. out of the fold back function is clamped at 100 mA.

Table 60. Temperature regulation control register

TEMPERATURE REGULATION CONTROL REGISTER								
ADDR:	0x92							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	TEMP_FB_EN	RESERVED	THM_HOT	THM_COLD	REGTEMP		THM_CONFIG	
POR:	0	0	0	0	0	1	0	1
ACCESS:		—						

The following table shows the different thermal regulation set point:

Table 61. Thermal regulation settings

REGTEMP[1:0] setting	Thermal regulation set point (°C)
00	80
01	95
10	110
11	Reserved

8.8.3 Input voltage regulation mode

An input-voltage regulation loop allows the charger to be well behaved when it is attached to a poor quality power source. The loop improves performance with relatively high-resistance charge sources that exist when long cables are used or devices are charged with non-compliant USB hub configurations. Additionally, this input-voltage regulation loop improves performance with current limited adapters. If the input current limit is programmed above the current limit threshold of given adapter, the input voltage loop allows regulation at the current limit of the adapter. Finally, the input-voltage regulation loop allows the charger to perform well with adapters that have poor transient load response times.

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The input-voltage regulation loop automatically reduces the input current limit in order to keep the input voltage at $V_{VBUS_DPM_REG}$. Once VBUS drops to the 4.5 V threshold (this threshold itself is selectable via the VBUS_DPM_REG[2:0] bits), the charging current is scaled back and this brings back the VBUS voltage higher. The Dynamic Power Management (DPM) loop then regulates the charging current (indirectly by reducing input current limit) dynamically to maintain VBUS at the DPM threshold. An interrupt is generated after the debounce time to notify the processor of the DPM event.

In the following figure, VBUS starts to drop as the charging current increases.

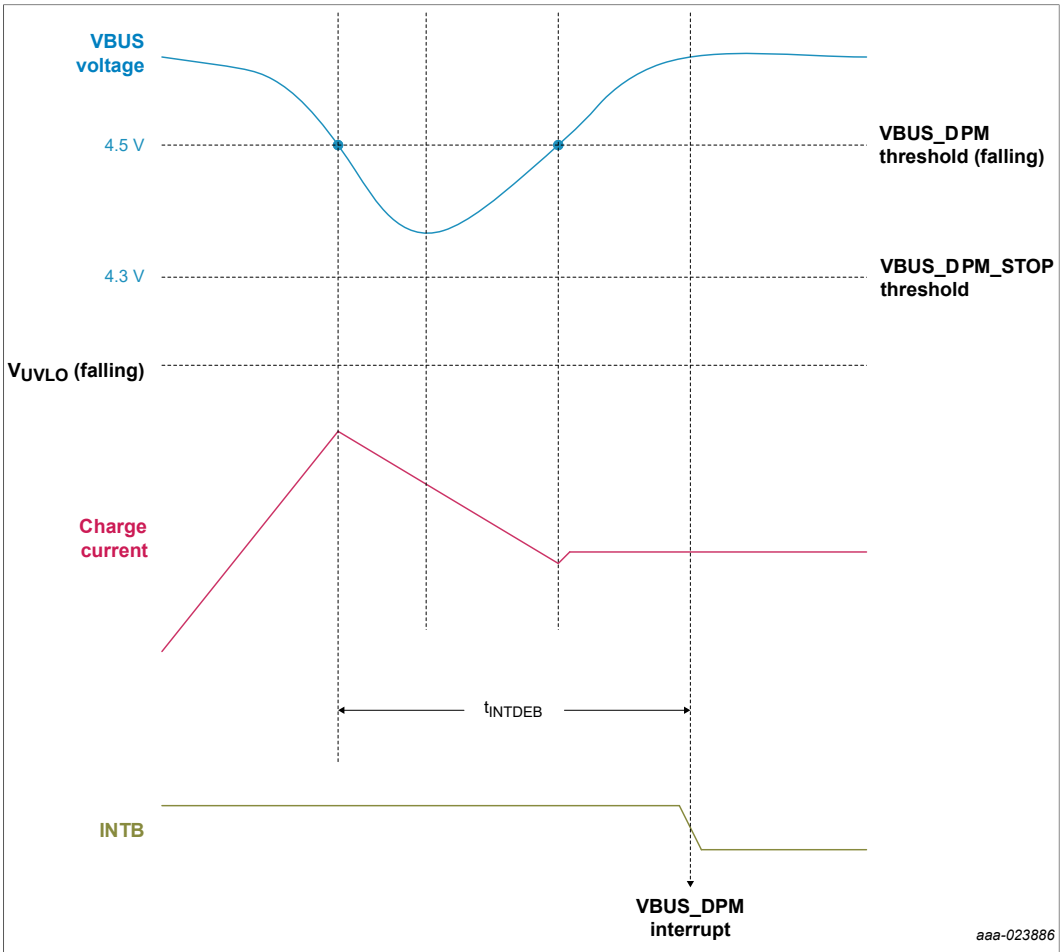

Figure 21. Response to input voltage droop during charging

The following figure describes a more stringent event.

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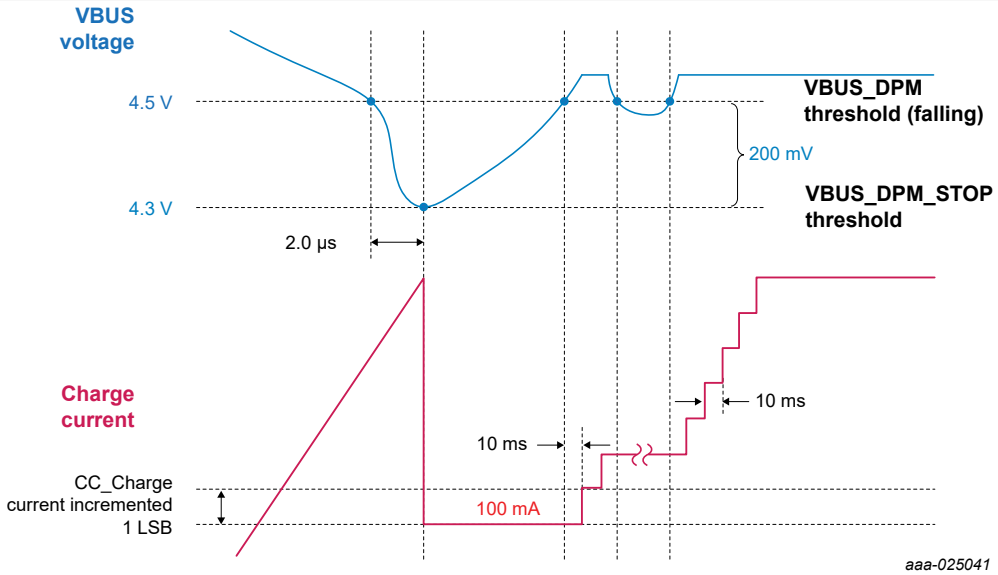

Figure 22. DPM function

There is a second comparator in the DPM loop which is set 200 mV below the VBUS_DPM_REG threshold. As seen in the second figure above, if the VBUS voltage continues to drop and hits the threshold of the second comparator, the charging current is immediately brought to the 100 mA setting to recover from the input voltage droop. At this point, the VBUS voltage should recover (assuming current drawn from VSYS is not causing the VBUS collapse).

Now, the charging current is stepped up slowly (every 10 ms) to arrive at the maximum value that allows regulation of VBUS to or slightly above the DPM threshold. At every incrementing step, the digital logic monitors if the VBUS voltage is above the 4.5 V comparator. The incrementing continues only if it is.

Table 62. VBUS linear dynamic input voltage register

VBUS LINEAR DYNAMIC INPUT VOLTAGE REGISTER								
ADDR:	0x95							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	RESERVED		VIN_DPM_STOP	PRECHGDBATT_THRESHOLD		VBUS_DPM_REG_VOLTAGE		
POR:	0	0	0	0	0	0	0	0
ACCESS:	—							

The input DPM voltage regulation set point is selected by writing to the VBUS_REG register.

Table 63. Input voltage regulation thresholds

VBUS_REG[2:0] setting	VBUS DPM REG voltage setting (V)
000	3.9
001	4.0
010	4.1
011	4.2
100	4.3
101	4.4
110	4.5

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Table 63. Input voltage regulation thresholds*...continued*

VBUS_REG[2:0] setting	VBUS DPM REG voltage setting (V)
111	4.6

8.8.4 JEITA thermal control

The PF1550 includes a temperature control function that conforms to the recommendations specified in the Japan Electronics and Information Technology Industries Association (JEITA) guidelines for improving the safety when charging of lithium-ion batteries.

The JEITA specification establishes five temperature zones, COLD, COOL, NORMAL, WARM, and HOT, with four temperature thresholds partitioning the zones. Battery temperature is monitored using an NTC thermistor, in close proximity of the cell, and the charger is carefully controlled as shown in the following table:

Table 64. JEITA thermal control

Zone	JEITA control function
COLD	Charging inhibited
COOL	Charger CC current and CV voltage adjusted
NORMAL	No JEITA control
WARM	Charger CC current and CV voltage adjusted
HOT	Charging inhibited

JEITA thermal control is enabled by selecting bits THM_CNFG[1:0] in the Temperature Regulation and Control Register 0x92.

Table 65. Temperature regulation control register

TEMPERATURE REGULATION CONTROL REGISTER								
ADDR:	0x92							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	TEMP_FB_EN	RESERVED	THM_HOT	THM_COLD	REGTEMP		THM_CONFIG	
POR:	0	0	0	0	0	1	0	1
ACCESS:		—						

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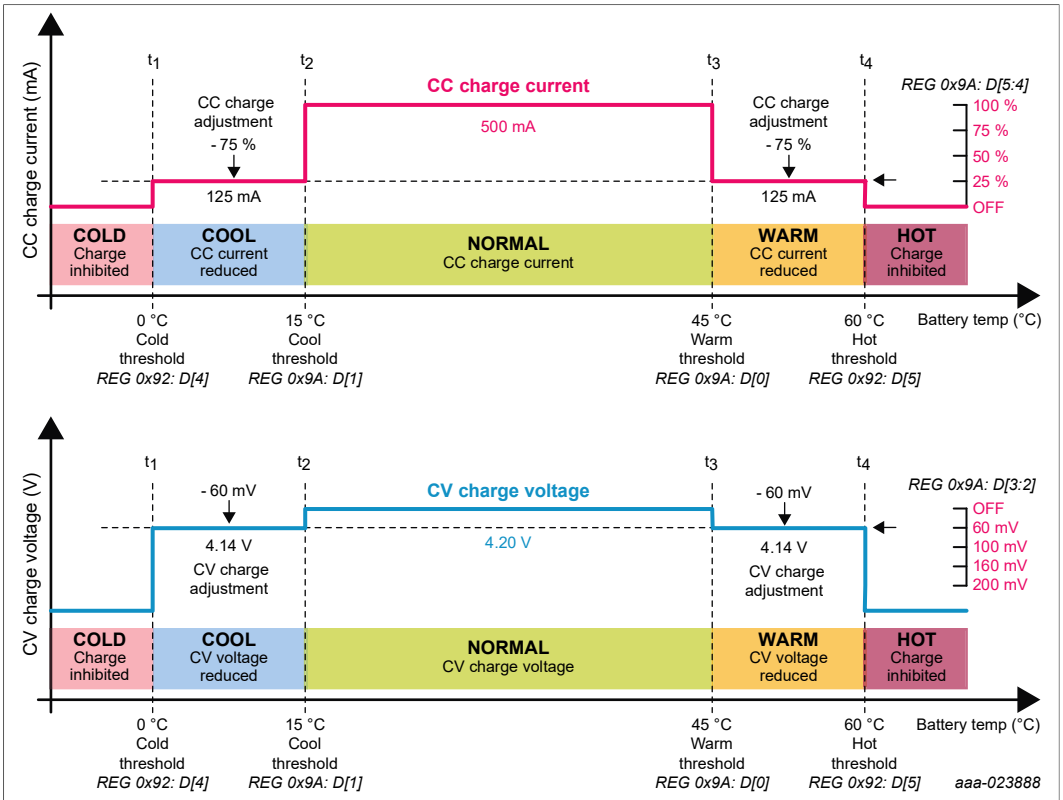

Figure 23. CC charge current and CV charge voltage adjustment

When the THM_CNFG[1:0] is set to 0x02, the charging current and CV voltage are adjusted based on CC_ADJ[1:0] and CV_ADJ[1:0] respectively whenever T_{COOL} and T_{WARM} thresholds are crossed.

When the THM_CNFG[1:0] is set to 0x03, and when the battery temperature rises above warm temp or goes below T_{COOL}, only the charging current is changed based on CC_ADJ[1:0]. CV voltage is not changed.

This feature can be disabled if THM_CNFG[1:0] is set to 0x01.

During THM_CNFG[1:0] =0x01, JEITA compliance can still be achieved but through software.

The PF1550 helps with this implementation by providing an interrupt at the T_{COOL} and T_{WARM} threshold when THM_CNFG[1:0] = 0x01.

The charger parameters must not be locked by OTP to use this software function.

If the thermistor functionality is not needed, THM_CNFG[1:0] can be set 0x00.

Table 66. JEITA temperature control register

JEITA TEMPERATURE CONTROL REGISTER								
ADDR:	0x9A							
	D7	D6	D5	D4	D3	D2	D1	D0
BITS:	RESERVED		CC_ADJ		CV_ADJ		THM_COOL	THM_WARM
POR:	0	0	0	0	0	0	0	0
ACCESS:								

CV_ADJ[1:0] has four settings, see Table 168 and register map:

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Table 67. CV voltage adjustment settings

CV_ADJ[1:0]	CV voltage adjustment (mV)
00	60
01	100
10	160
11	200

CC_ADJ[1:0] has four settings, see Table 168 and register map:

Table 68. CC current adjustment settings

CC_ADJ[1:0]	CC current adjustment (%)
00	25 %
01	50 %
10	75 %
11	100 %

THM_HOT[0]	THM_HOT setting (℃)
0	60
1	55

THM_COLD[0]	THM_COLD setting (℃)
0	0
1	-10

8.9 Fault states

8.9.1 Timer fault state

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging.

The charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in each of its pre-qualification states is t_{PRECHG}.

The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC} which is programmable with FCHGTIME.

Finally, the time that the charger is in the end-of-charge state is t_{EOC} which is programmable with EOCTIME bits. Upon entering the timer fault state, a CHG_I interrupt is generated without a delay, CHG_OK is cleared and CHG_SNS = 0x06.

In the timer fault state, the charger is off. The charger can exit the timer fault state by programming the charger to be off and then programming it to be on again through the CHG_OPER bits. Alternatively, the charger input can be removed and reinserted to exit the timer fault state.

VSYS should continue to regulate while in the Timer fault state.

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8.9.2 Watchdog timer state

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. The watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly.

The watchdog timer is disabled by default with WDTEN = 0. To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally.

Reset the watchdog timer by programming WDTCLR = 0x01. As long as WDTEN = 1, the timer continues to run and the processor continues to clear the register before the timer expires.

The system processor clears the WDTEN bit to stop the timer.

If the watchdog timer expires while the charger is in precharge mode, fast charge CC or CV, end-of-charge, done, or timer fault, the charging stops, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_SNS = 0x0B and indicates that the charger is off because the watchdog timer has expired.

Once the watchdog timer has expired, the charger is restarted by programming WDTCLR=0x01. The VSYS node is supported by the battery and/or the adapter through the Linear regulator while the watchdog timer is expired.

8.9.3 Thermal shutdown state

The thermal shutdown state occurs when the battery charger is in any state and the junction temperature (T_J) exceeds the device's thermal shutdown threshold (T_{SHDN}), typical 140 °C.

When T_J is close to T_{SHDN} the charger folds back the charging current to 0 A, so the charger is effectively off. Upon entering this state, CHG_I interrupt is generated without a delay, CHG_OK is cleared. In the thermal shutdown state, the charger is off and timers are suspended.

CHG_SNS = 0x0A and CHG_OK = 0 in the thermal shutdown state. The charger exits the temperature suspend state and returns to the state it came from once the die temperature has cooled. The timers resume once the charger exits this state. VSYS continues to regulate while in the thermal shutdown state.

8.9.4 Battery overvoltage state

A battery overvoltage fault occurs in any state when the battery voltage exceeds to V_{BATOV} threshold.

In this state, BATT_SNS = 0x05 and BAT_OK = 0. A BATT_I interrupt is generated in this state. In the event of a battery overvoltage state, the BATFET is opened and VSYS is regulated using the linear path. Once the battery overvoltage condition clears, the charger exits the battery overvoltage state and returns to the state it came from.

8.9.5 Charger fault priority

Some of the charger fault states occur at the same time. For example, battery overvoltage and thermal shutdown occur at the same time. In this section, which failure states take priority is discussed.

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In any given state, non-recoverable faults such as battery overcurrent timer fault take the highest priority. Recoverable faults such as a thermistor suspend, or battery overvoltage take lower priority.

8.9.6 Battery overcurrent limit

The VBATT to VSYS detector (BATFET) generates an overcurrent (OVRC) and provides the signal to the PMIC on/off controller.

This feature protects the battery and the system from potential damage due to excessive battery discharge current. Excessive battery discharge current may occur for several reasons such as exposure to moisture, a software problem, a device failure, or mechanical failure that causes a short-circuit.

The battery overcurrent protection feature is enabled with BATFET_OC[1:0] bit.

Disabling this feature reduces the main battery current consumption. When the battery current to system exceeds the programmed overcurrent threshold for at least t_{BOVCRI}, a BAT2SOC_I interrupt is generated and BATTOC_SNS bit reports an overcurrent condition.

If the overcurrent persists for t_{BOVCR}, the VBATT to VSYS MOSFET is disabled or kept alive depending on the BOVRC_DISBATFET OTP bit. Typically, when the system's processor detects this overcurrent interrupt, it executes a housekeeping routine that tries to mitigate the overcurrent situation. There is an OTP option (via BOVRC_DISBATFET bit) to either disable the BATFET after completion of housekeeping routine or remain on.

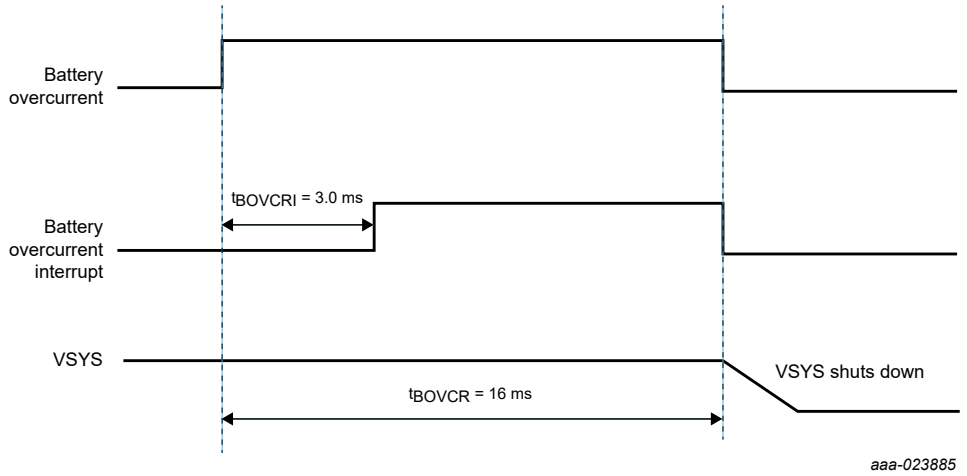

Figure 24. Response to battery overcurrent

The following table shows the different overcurrent threshold settings:

Table 69. Battery overcurrent thresholds

BATFET_OC[1:0] setting	VBATT to VSYS overcurrent threshold (A)
00	Disabled
01	2.2
10	2.8
11	3.2

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8.10 LED indicator

CHGB is a 6.0 mA LED current sink with programmable blink timing. Blink period and on-time are programmable with 2-bits. The LED has indicator depending on the charger state as shown in the LED modes table. Blink frequency is programmable for 0.5 Hz, 1.0 Hz, 8.0 Hz or 256 Hz. Blink duration is programmable from 0/32 duty cycle to 32/32 duty cycle in 1/32 increments.

The LED_CFG bit allows the LEDs to operate in two modes as shown in the following table. With LED_CFG=0, the LEDs behave as follows: charging (on), fault (flashing), and charge complete (off). When LED_CFG = 1, the LED's have the following behavior, charging (flashing), fault (on), and charge complete (off). The LEDs are activated automatically when charging is started and remain under control of the state machine. Software can take control over the charge LED's by setting the LEDOVRD = 1. When LEDOVRD = 1 the LEDs are totally controlled by software, therefore the state machine no longer has control. With LEDOVRD = 0 software cannot force the LED's on but can still set the current.

The charging LED drivers include ramp up and ramp down patterns implemented in hardware. The ramp itself is generated by increasing or decreasing the PWM duty cycle with a 1/32 step every 1/64 seconds. The ramp time is therefore a function of the initial set PWM cycle and the final PWM cycle. As an example, starting from 0/32 and going to 32/32 takes 500 ms whereas going to from 8/32 to 16/32 takes 125 ms.

The ramp function is executed upon every change in PWM cycle setting. If a PWM change is programmed via I^2C when LED_RAMP = 0, then the change is immediate rather than spread out over a PWM sweep. In addition, programmable blink rates are provided. Blinking is obtained by lowering the PWM repetition rate of each of the drivers through LED_FREQ[1:0] while the on period is determined by the duty cycle setting. To avoid high frequency spur coupling in the application, the switching edges of the output drivers are softened.

Table 70. LED modes

Condition	LED_CFG = 1	LED_CFG = 0 (default)	Current (mA)
Charger off	Off	Off	6
Charging	Flashing 1.0 Hz 50 % duty cycle	On steady 100 % duty cycle	6
Charging fault	On steady 100 % duty cycle	Flashing 1.0 Hz 50 % duty cycle	6
Charge complete	Off	Off	6

Table 71. LED enable conditions

LED_EN	CHGB	LEDOVRD
0 (default)	Auto	0
1	On	1
0	Off	1

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Table 72. LED frequency setting

LED_FREQ[1:0]	Frequency	Units
00 (default)	1	Hz
01	0.5	Hz
10	256	Hz
11	8	Hz

9 Control and interface signals

The PF1550 PMIC is fully programmable via the I^2C interface. Additional communication is provided by direct logic interfacing including interrupt and reset pins as well as pins for power buttons.

9.1 PWRON

PWRON is an input signal to the IC that acts as an enable signal for the voltage regulators in the PF1550.

The PWRON pin can be configured as either a level sensitive input (OTP_PWRON_CFG = 0), or as an edge sensitive input (OTP_PWRON_CFG = 1).

As a level sensitive input, an active high signal turns on the part and an active low signal turns off the part, or puts it into Sleep mode.

As an edge sensitive input, such as when connected to a mechanical switch, a falling edge turns on the part and if the switch is held low for greater than or equal to 4.0 seconds, the part turns off or enters Sleep mode.

Table 73. PWRON pin OTP configuration options

OTP_PWRON_CFG	Mode
0	PWRON pin HIGH = ON PWRON pin LOW = OFF or Sleep mode
1	PWRON pin pulled LOW momentarily = ON PWRON pin LOW for 4.0 seconds = OFF or Sleep mode

Table 74. PWRON pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
PWRON	V_{IL}	—	0.0	0.4	V
	V_{IH}	—	1.4	3.6	V

When OTP_PWRON_CFG = 1, PWRON pin pulled low momentarily takes the system from REGS_DISABLE/SLEEP to RUN mode. There is no effect if PWRON is pulled low momentarily while in RUN or STANDBY modes. Only an interrupt is generated.

PWRON pin low for 4.0 seconds with PWRONRSTEN bit = 1: Enters REGS_DISABLE or Sleep mode.

See Section 10 "PF1550 state machine" for detailed description.

In this configuration, the PWRON input can be a mechanical switch de-bounced through a programmable de-bouncer, PWRONDBNC[1:0], to avoid a response to a very short key press. The interrupt is generated for both the falling and the rising edge of the PWRON

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pin. By default, a 31.25 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONDBNC[1:0]. The interrupt is cleared by software, or when cycling through the REGS_DISABLE mode.

Table 75. PWRONDBNC settings

Bits	State	Turn on debounce (ms)	Falling edge INT debounce (ms)	Rising edge INT debounce (ms)
PWRONDBNC[1:0]	00	31.25	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

9.2 STANDBY

STANDBY is an input signal to the IC. When it is asserted the part enters standby mode and when deasserted, the part exits standby mode. STANDBY can be configured as active high or active low using the STANDBYINV bit.

Table 76. Standby pin polarity control

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
0	0	Not in Standby mode
0	1	In Standby mode
1	0	In Standby mode
1	1	Not in Standby mode

Table 77. STANDBY pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
STANDBY	V_{IL}	—	0	0.4	V
	V_{IH}	—	1.4	3.6	V

Since STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes. A programmable delay is provided to hold off the system response to a Standby event. This allows the processor and peripherals some time after a standby instruction has been received to terminate processes to facilitate seamless entering into Standby mode. When enabled (STANDBYDLY = 01, 10, or 11), STANDBYDLY delays the Standby initiated response for the entire IC, until the STBYDLY counter expires. An allowance should be made for three additional 32 kHz cycles required to synchronize the Standby event.

9.3 RESETBMCU

RESETBMCU is an open-drain, active low output configurable via OTP for two modes of operation.

In its default mode, it is deasserted at the end of the start-up sequence. In this mode, the signal can be used to bring the processor out of reset (POR), or as an indicator that all supplies have been enabled; it is only asserted during a turn off event.

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When configured for its fault mode, RESETBMCU is deasserted after the startup sequence is completed only if no faults occurred during start-up. At any time, if a fault occurs and persists for 1.8 ms typically, RESETBMCU is asserted low.

The PF1550 is turned off if the fault persists for more than 100 ms typically. The PWRON signal restarts the part, if the fault persists, the sequence described above is repeated. To enter the fault mode, set bit OTP_PWRGD_EN to 1.

The time from the last regulator in the start-up sequence to when RESETBMCU is deasserted is programmable between 2.0 ms and 1024 ms via OTP_POR_DLY[2:0] bits.

Table 78. RESETBMCU pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
RESETBMCU	V_{OL}	−2.0 mA	0	0.2 * VDDIO	V
	V_{OH}	Open drain	0.8 * VDDIO	3.6	V

9.4 INTB

INTB is an open-drain, active low output. It is asserted when any interrupt occurs, if the interrupt is unmasked. INTB is deasserted after the fault interrupt is cleared by software, which requires writing a “1” to the interrupt bit.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the INTB pin does not go low. A masked interrupt can still be read from the interrupt status register. This gives the processor the option of polling for status from the IC.

The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the INTB pin goes low after unmasking. The sense registers contain status and input sense bits so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Table 79. INTB pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
INTB	V_{OL}	−2.0 mA	0	0.2 * VDDIO	V
	V_{OH}	Open drain	0.8 * VDDIO	3.6	V

9.5 WDI

WDI is an input signal to the IC. It is typically connected to the watchdog output of the processor. When the WDI pin is pulled low, the PMIC enters the “REGS_DISABLE” mode where all the regulators are turned off. The WDI acts as a hard reset input from the processor.

During PMIC startup (REGS_DISABLE to RUN mode), the WDI pin is masked until RESETBMCU is deasserted.

Table 80. WDI pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
WDI	V_{IL}	—	0	0.2 * VDDIO	V
	V_{IH}	—	0.8 * VDDIO	3.6	V

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9.6 ONKEY

ONKEY is an input pin to the IC and is typically connected to a push-button switch. The ONKEY pin is pulled high when the switch is depressed, and is pulled low when the switch is pressed.

Pressing the switch generates interrupts which the processor uses to initiate PMIC state transitions. Pressing the ONKEY for longer than the delay programmed by OTP_TGRESET[1:0] (ranges from 4.0 s to 16 s), forces the PMIC into the REGS_DISABLE state.

Table 81. ONKEY pin logic level

Pin name	Parameter	Load condition	Min	Max	Unit
ONKEY	V_{IL}	—	0	0.4	V
	V_{IH}	—	1.4	4.8	V

Table 82. ONKEYDBNC settings

Bits	State	Turn On debounce (ms)	Falling edge INT debounce (ms)	Rising edge INT debounce (ms)
ONKEYDBNC[1:0]	00	31.25	31.25	31.25
	01	31.25	31.25	31.25
	10	125	125	31.25
	11	750	750	31.25

The ONKEY input can be a mechanical switch debounced through a programmable debouncer, ONKEYDBNC[1:0], to avoid a response to a very short (unintentional) keypress. The interrupt is generated during the rising edge of the ONKEY pin.

The falling edge debounce timing can be extended with ONKEYDBNC[1:0] as defined Table 82. The interrupt is cleared by software, or when cycling through the REGS_DISABLE mode.

See Section 12 "Register map" for detailed description of the ONKEY interrupt registers.

9.7 Control interface I^{2}C block description

The PF1550 contains an I^{2}C interface port which allows access by a processor, or any I^{2}C master, to the register set. Via these registers, the resources of the IC can be controlled. The registers also provide status information about how the IC is operating.

The SCL and SDA lines should be routed away from noisy signals and planes to minimize noise pickup. To prevent reflections in the SCL and SDA traces from creating false pulses, the rise and fall times of the SCL and SDA signals must be greater than 20 ns. This can be accomplished by reducing the drive strength of the I^{2}C master via software.

9.7.1 I^{2}C device ID

I^{2}C interface protocol requires a device ID for addressing the target IC on a multi-device bus. The PF1550 I^{2}C device address is 0x08.

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9.7.2 I²C operation

The I²C mode of the interface is implemented generally following the fast mode definition which supports up to 400 kbits/s operation (exceptions to the standard are noted to be 7-bit only addressing and no support for general call addressing). Timing diagrams, electrical specifications, and further details can be found in the I²C specification, which is available for download at:

http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and each byte is sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to and from the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device responds to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NACK is received, the host should terminate the current transaction and retry the transaction.

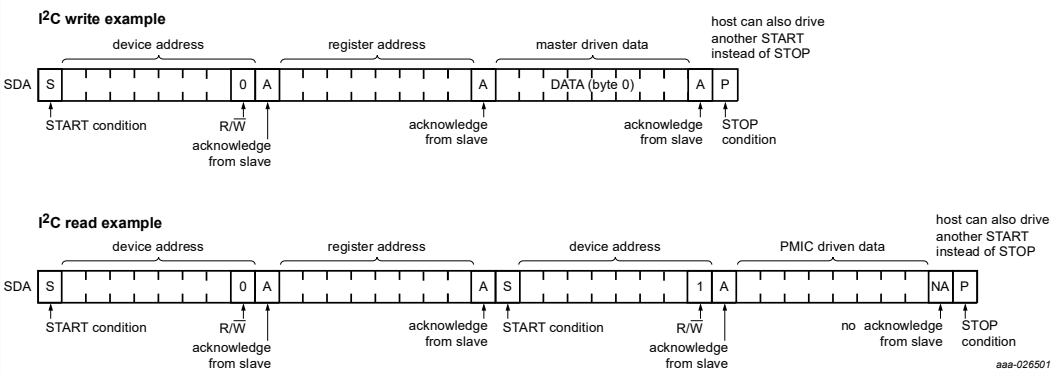

Figure 25. I²C sequence

10 PF1550 state machine

The PMIC part of the PF1550 can operate in a number of states as shown in Figure 26.

The states can be split into two categories:

1. “System On” that includes the RUN, STANDBY, and SLEEP modes
2. “System Off” that includes the REGS_DISABLE, CORE_OFF, and SHIP modes

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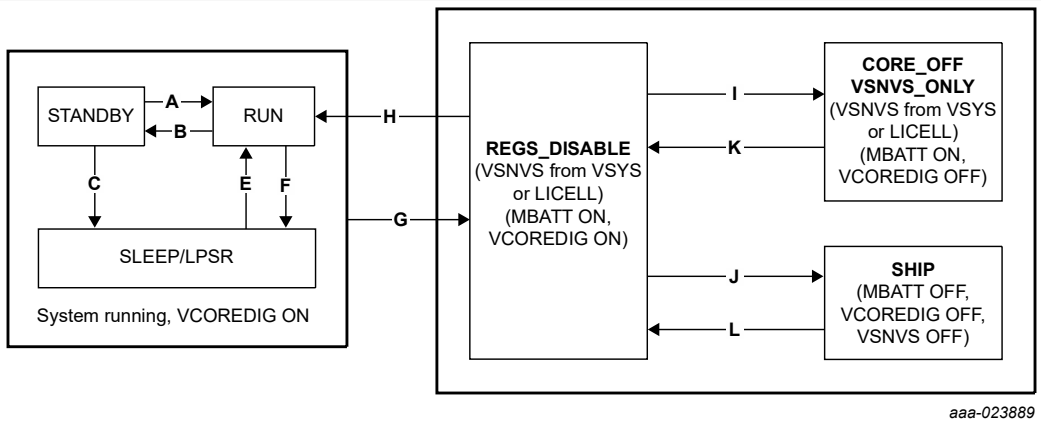

Figure 26. PMIC state machine

In the “System On” modes, some or all of the PMIC regulators are powered and in general the system processor is powered.

In the “System Off” modes, all (or all regulators except VSNVS) are powered off. In general, the system processor is powered off during these states. In the REGS_DISABLE and CORE_OFF modes, the VSNVS supply remains enabled keeping the system RTC running.

The only way to transition from “System Off” to “System On” and vice versa is through the REGS_DISABLE mode. From the REGS_DISABLE mode, the only exit into a “System On” state is into the “Run” mode. Transition from the REGS_DISABLE mode to the Run mode requires a Turn On event. See Section 10.3 "Turn on events".

Transition from any of the “System On” modes to the REGS_DISABLE state is allowed. This transition is referred to as a Turn Off event. See Section 10.4 "Turn off events".

10.1 System ON states

10.1.1 Run state

In this state, the PMIC regulators are enabled and the system is powered up. RESETBMCU is de-asserted in this state.

This mode can be entered in several ways:

1. From REGS_DISABLE through a Turn On Event: During this transition, the PMIC regulators are powered up as per their programmed start-up sequence. After all the regulators are powered, the RESETBMCU pin is de-asserted.
2. From STANDBY by using the STANDBY pin
3. From SLEEP mode by using the PWRON pin: Typically, some of the regulators are turned off in the SLEEP mode compared to the RUN mode. In the SLEEP mode, some of the buck regulator output voltages are set lower than those in the RUN mode. While transitioning from the SLEEP to the RUN mode, regulators that were turned off in the SLEEP mode are turned back on in the RUN mode following the same sequence as the programmed OTP sequence. Output voltage transitions during transition from the SLEEP to the RUN mode also occurs at the same OTP sequence time slot. RESETBMCU is de-asserted through this state transition.

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10.1.2 STANDBY state

This state is entered by controlling the logic level of the STANDBY pin. It can be entered only from the RUN mode.

The STANDBY pin polarity is programmable through the STANDBYINV I^2C bit. By default, STANDBYINV = 0 and a logic high on the STANDBY pin moves the state machine from the RUN state to the STANDBY state. When STANDBYINV = 1, a logic low moves the state machine from the RUN state to the STANDBY state.

Regulator output voltage may be changed, or regulator outputs could be disabled while entering the STANDBY state and vice versa.

For details on the power-down sequence, see Section 10.7 "Regulator power-down sequencer". While exiting STANDBY state into the RUN mode, regulator output voltage changes and regulator enables follow the power-up sequence.

It is possible to exit STANDBY state and enter the SLEEP state. SLEEP state is generally a lower power system state compared to the STANDBY state. Exiting STANDBY into the SLEEP state follows the power-down sequence.

RESETBMCU is de-asserted in the STANDBY state.

10.1.3 SLEEP state

This state is entered from either the RUN state or the STANDBY state by controlling the PWRON pin. The exact condition required for this transition depends on the OTP configuration of the PWRON pin. For details see Section 9.1 "PWRON".

The power-down sequence is followed while entering this state and the power-up sequence is followed while exiting this state into the RUN state.

RESETBMCU is de-asserted in the SLEEP state.

10.2 System OFF states

RESETBMCU is asserted (low) in all the System Off states.

10.2.1 REGS_DISABLE

This state can be considered the ‘home state’ for the state machine. In this state, the state machine waits for appropriate commands to proceed to other states.

REGS_DISABLE can be entered from one of the “System On” state through a turn off event.

REGS_DISABLE can be entered from the CORE_OFF and SHIP mode by a charger attach event.

In the REGS_DISABLE state, the PMIC core circuitry is active. VSNVS is a best-of-supply output of VSYS and LICELL.

10.2.2 CORE_OFF

This state is entered in two ways:

1. From the REGS_DISABLE mode by pressing and holding the ON_KEY button low > T_{greset}
2. From the REGS_DISABLE mode if the GOTO_CORE_OFF bit is set

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This state cannot be entered if a charger is plugged in.

In this state, the internal core of the PMIC is turned off to reduce quiescent current. VSNVS is the only regulator that is supplied to external loads.

10.2.3 SHIP

In this mode, the MBATT switch between VSYS and VBATT is opened. All the PMIC supplies including VSNVS are turned off.

The SHIP mode is entered if the GOTO_SHIP bit is set in the REGS_DISABLE state.

The only way to exit from this mode is by a charger attach event. The state machine exits to the REGS_DISABLE state when this happens. A battery reattach can also be used to exit SHIP mode.

10.3 Turn on events

A turn on event takes the PMIC from the REGS_DISABLE state to the RUN state (transition H in Figure 26).

The turn on events are:

1. PWRON logic high with PWRON_CFG = 0
2. PWRON H -> L with PWRON_CFG = 1

VSYS > $UVDET_{rising}$ and $T_J < T_{SHDN_fall}$ are preconditions for a turn on event to occur.

The turn on is to be completed after the RESETBMCU pin is deasserted. The WDI pin is masked till the RESETBMCU pin is deasserted.

10.4 Turn off events

A turn off event takes the PMIC state machine from one of the “System On” states (RUN, STANDBY, or SLEEP) to the REGS_DISABLE state. The power-down sequence is followed during all of the turn off events.

The turn off events are:

1. Thermal Shutdown ($T_J > T_{SHDN_rise}$)
2. PWRON logic low with OTP_PWRON_CFG = 0
3. PWRON low > 4.0 s with OTP_PWRON_CFG = 1 && PWRONRSTEN = 1
4. WDI = 0. This occurs when the processor watchdog expires and pulls the WDI pin low to create a hard reset.
5. ON_KEY pressed low > T_{greset} && ON_KEY_RST_EN = 1. This facilitates creating a hard reset when pressing the ON_KEY button without processor intervention.
6. GOTO_SHIP = 1. This is used to initiate the device to go into the SHIP mode. When GOTO_SHIP bit is set to 1, the state machine proceeds from one of the “System On” states to the REGS_DISABLE mode to the SHIP mode.

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10.5 State diagram and transition conditions

Table 83. State transition table

Transition	Description	PWRON_CFG = 0 (Level sensitive)	PWRON_CFG = 1 (Edge sensitive)
A	Standby to Run	(STANDBY pin = 0 && STANDBYINV bit = 0) OR (STANDBY pin = 1 && STANDBYINV bit = 1)	(STANDBY pin = 0 && STANDBYINV bit = 0) OR (STANDBY pin = 1 && STANDBYINV bit = 1)
B	Run to Standby	(STANDBY pin = 1 && STANDBYINV bit = 0) OR (STANDBY pin = 0 && STANDBYINV bit = 1)	(STANDBY pin = 1 && STANDBYINV bit = 0) OR (STANDBY pin = 0 && STANDBYINV bit = 1)
C	Standby to Sleep	(PWRON = 0) && (Any SWxOMODE = 1 || Any LDOxOMODE = 1)	(PWRON High to Low and PWRON = 0 > 4s) && (PWRONRSTEN = 1) && (Any SWxOMODE = 1 || Any LDOxOMODE = 1)
E	Sleep to Run	PWRON = 1	PWRON High to Low to High [1]
F	Run to Sleep	(PWRON = 0) && (Any SWxOMODE = 1 || Any LDOxOMODE = 1)	(PWRON High to Low and PWRON = 0 > 4s) && (PWRONRSTEN = 1) && (Any SWxOMODE = 1 || Any LDOxOMODE = 1)
G	Run/Standby/ Sleep to REGS_ DISABLE	(Thermal shutdown) OR (GOTO_SHIP = 1) OR (PWRON = 0 && All SWxOMODE = 0 && All LDOxOMODE = 0) OR (WDI = 0) [2] OR (ONKEY High to Low and ONKEY = 0 > Tgreset && ONKEY_RST_EN = 1) OR (VSYS < UVDET_Fall) [3][4]	(Thermal shutdown) OR (GOTO_SHIP = 1) OR (PWRON High to Low and PWRON = 0 > 4s && PWRONRSTEN = 1 && All SWxOMODE = 0 && All LDOxOMODE = 0) OR (PWRON High to Low and PWRON = 0 > 4s when in Sleep state) OR (WDI = 0) [2] OR (ONKEY High to Low and ONKEY = 0 > Tgreset and ONKEY_RST_EN = 1) OR (VSYS < UVDET_Fall) [3]

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Table 83. State transition table*...continued*

Transition	Description	PWRON_CFG = 0 (Level sensitive)	PWRON_CFG = 1 (Edge sensitive)
H	REGS_DISABLE to Run (Only if VSYS > UVDET and T_J < T_{SHDN_fall})	(PWRON = 1)	(PWRON High to Low) OR (If entered REGS_DISABLE via long press on PWRON && RESTARTEN = 1 && PWRON stays Low > 1.0s) OR (Charger attach) [5] [6]
I	REGS_DISABLE to CORE_OFF (Only if VBUS_INVALID = 1)	(GOTO_CORE_OFF = 1 && ONKEY = 1) OR (ONKEY High to Low and ONKEY = 0 > Tgreset && ONKEY_RST_EN = 1) [7][8]	(GOTO_CORE_OFF = 1 && ONKEY = 1) OR (ONKEY High to Low and ONKEY = 0 > Tgreset && ONKEY_RST_EN = 1) [7][9]
J	REGS_DISABLE to SHIP	GOTO_SHIP = 1 && VBUS_INVALID = 1 [10]	GOTO_SHIP = 1 && VBUS_INVALID = 1 [10]
K	CORE_OFF to REGS_DISABLE	(ONKEY High to Low and ONKEY = 0 > 1000 ms) OR (Charger attach)	(ONKEY High to Low and ONKEY = 0 > 1000 ms) OR (Charger attach)
L	SHIP to REGS_DISABLE	(Charger attach) OR (Battery reattach)	(Charger attach) OR (Battery reattach)

[1] This low period is < 4.0s. If it is longer than 4.0s, it transitions to G
[2] PWRON pin is pulled low by processor after WDI = 0.
[3] Follows regulator power-down sequence for this transition
[4] REGS_DISABLE is a transitionary state when GOTO_SHIP = 1. The state machine does not stay at G when GOTO_SHIP = 1
[5] WDI pin is masked until RESETBMCU is deasserted.
[6] Debounce on PWRON programmable via PWRONDBNC[1:0]
[7] PWRON pin is pulled low by processor after ONKEY = 0 > Tgreset.
[8] GOTO_CORE_OFF is set by user when system is ON. For other products, a secondary processor is used to set this bit while in REGS_DISABLE
[9] GOTO_CORE_OFF must be set by user when system is ON
[10] VBUSIN pin voltage < 1.0 V

10.6 Regulator power-up sequencer

Start-up sequence of all the switching and linear regulators in the PF1550 is programmable. VSNVS's sequence is not programmable but is always the first regulator to power up when the PF1550 is powered up via a cold start (from no input to valid input). When SYS is first applied to the PF1550 (either by applying a battery, or by plugging in a charger), VSNVS comes up first.

The switching and linear regulators power up based on their programmed OTP sequence using the respective OTP_XX_SEQ[2:0] when transitioning from REGS_DISABLE to the RUN state.

RESETBMCU is pulled low from VCOREDIG POR until the end of the power-up sequencer.

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RESETBMCU is pulled high 2.0 ms to 1024 ms after the last regulator powers up. This delay is OTP programmable through the OTP_POR_DLY[2:0] bits.

When transitioning from STANDBY mode to RUN mode, the power-up sequencer is activated only if any of the regulators turn back on during this transition.

The power-up sequencer ends as soon as the last regulator powers up, rather than waiting for a fixed time.

The power-up sequencer is always activated when transitioning from Sleep to Run modes. The sequencer ends as soon as the last regulator powers up, rather than waiting for a fixed time.

The PWRUP_I interrupt is set to indicate completion of transition from STANDBY to RUN and SLEEP to RUN.

The PWRUP_I interrupt is set while transitioning from STANDBY to RUN even if the sequencers were not used. This is used to indicate that the transition is complete.

10.7 Regulator power-down sequencer

The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0], VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence.

The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0].

When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default power-down is a mirror of the power-up sequence.

In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once. During transition from Run to Standby, the power-down sequencer is activated if any of the regulators are turned off during this transition.

If regulators are not turned off during this transition, the power-down sequencer is bypassed and the transition happens at once (any associated DVS transitions still take time).

During transition from Run to Sleep, the power-down sequencer is always activated. However, if all XXX_PWRDN_SEQ[2:0] = 0, the transition happens immediately.

The PWRDN_I interrupt is set during transition from Run to Sleep and Run to Standby even if regulators are not turned off during these transitions.

11 Device start up

11.1 Startup timing diagram

The startup timing of the regulators is programmable through OTP, Figure 27 shows the startup timing of the regulators as determined by their OTP A4 sequence.

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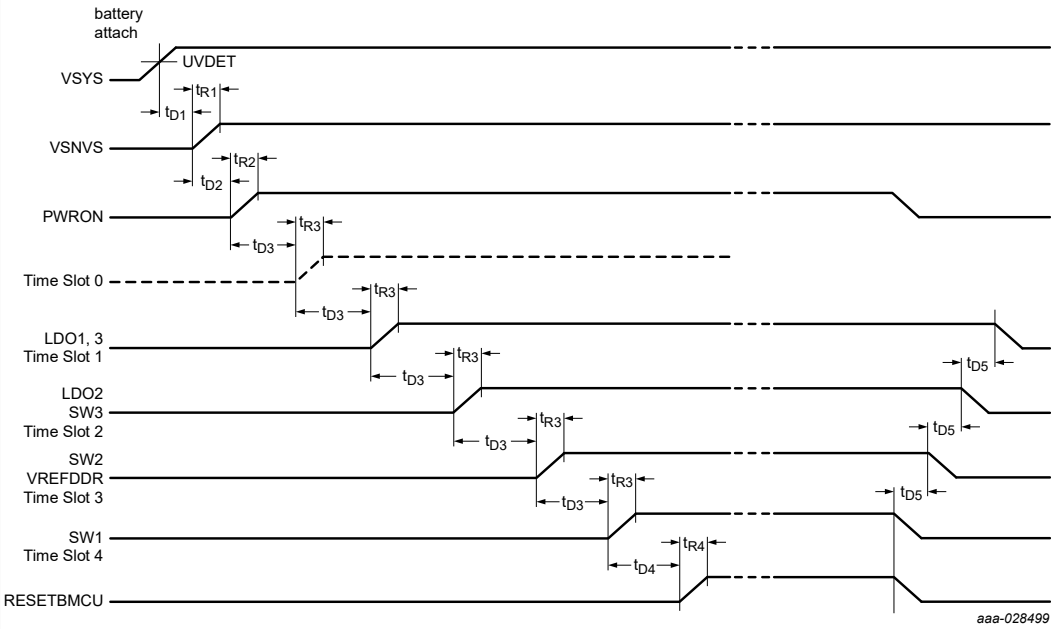

Figure 27. A4 startup and power down sequence

Table 84. A4 startup and power down sequence timing

Parameter	Description [1]	Min.	Typ.	Max.	Unit
t_{D1}	Turn-on delay of VSNVS	—	0.6	—	ms
t_{R1}	Rise time of VSNVS	—	0.1	—	ms
t_{D2}	User determined delay	—	—	—	ms
t_{R2}	Rise time of PWRON	—	[2]	—	ms
t_{D3}	Power up delay between regulators • OTP_SEQ_CLK_SPEED = 0 • OTP_SEQ_CLK_SPEED = 1 [3]	 — —	 0.5 2.0	 — —	ms
t_{R3}	Rise time of regulators [4]	—	0.2	—	ms
t_{D4}	Turn-on delay of RESETBMCU	—	2.0	—	ms
t_{R4}	Rise time of RESETBMCU	—	0.2	—	ms
t_{D5}	Power down delay between regulators	—	2.0	—	ms

[1] All regulators avoid drop-out mode at startup
[2] Depends on the external signal driving PWRON
[3] A4 configuration
[4] Rise time is a function of slew rate of regulators and nominal voltage selected.

11.2 Device start up configuration

Table 85. PF1550 start up configuration

	Pre-programmed OTP configuration								
Registers	A1	A2	A3	A4	A5	A6	A7	A8	A9
Default I^2C address	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08	0x08
OTP_VSNVS_VOLT[2:0]	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V	3.0 V
OTP_SW1_VOLT[5:0]	1.1 V	1.0 V	1.3875 V	1.1 V	1.3875 V	1.275 V	1.3875 V	1.3875 V	3.3 V
OTP_SW1_PWRUP_SEQ[2:0]	1	5	3	4	3	3	3	3	3
OTP_SW2_VOLT[5:0]	1.1 V	1.2 V	1.35 V	1.2 V	1.5 V	1.35 V	1.2 V	1.35 V	3.3 V
OTP_SW2_PWRUP_SEQ[2:0]	2	5	3	3	3	3	3	3	3

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Table 85. PF1550 start up configuration*...continued*

	Pre-programmed OTP configuration								
Registers	**A1**	**A2**	**A3**	**A4**	**A5**	**A6**	**A7**	**A8**	**A9**
OTP_SW3_VOLT[5:0]	1.8 V	1.8 V	3.3 V	1.8 V	3.3 V	3.3 V	1.8 V	3.3 V	3.0 V
OTP_SW3_PWRUP_SEQ[2:0]	3	1	3	2	3	3	3	3	3
OTP_LDO1_VOLT[4:0]	1.0 V	1.8 V	1.8 V	3.3 V	1.8 V	1.8 V	3.3 V	1.8 V	2.8 V
OTP_LDO1_PWRUP_SEQ[2:0]	4	1	3	1	3	3	3	3	3
OTP_LDO2_VOLT[3:0]	2.5 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
OTP_LDO2_PWRUP_SEQ[2:0]	4	1	2	2	2	2	2	2	3
OTP_LDO3_VOLT[4:0]	1.0 V	1.8 V	3.3 V	1.8 V	3.3 V	3.3 V	3.3 V	3.3 V	1.8 V
OTP_LDO3_PWRUP_SEQ[2:0]	5	1	3	1	3	3	3	3	3
OTP_VREFDDR_PWRUP_SEQ[2:0]	5	5	3	3	3	3	3	3	3
OTP_SW1_DVS_SEL	Non-DVS mode	DVS mode							Non-DVS mode
OTP_SW2_DVS_SEL	DVS mode	Non-DVS mode		DVS mode	Non-DVS mode				Non-DVS mode
OTP_LDO1_LS_EN	LDO Mode								
OTP_LDO3_LS_EN	LS Mode	LDO Mode							
OTP_SW1_RDIS_ENB	Enabled								
OTP_SW2_RDIS_ENB	Enabled								
OTP_SW3_RDIS_ENB	Enabled								
OTP_SW1_DVSSPEED	12.5 mV step each 4.0 µs								Non-DVS mode
OTP_SW2_DVSSPEED	12.5 mV step each 2.0 µs	12.5 mV step each 4.0 µs							Non-DVS mode
OTP_SWx_EN_AND_STBY_EN	SW1, SW2, SW3 Enabled in RUN and STANDBY								
OTP_LDOx_EN_AND_STBY_EN	LDO1, LDO2, LDO3, VREFDDR Enabled in RUN and STANDBY								
OTP_PWRON_CFG	Level Sensitive							Edge Sensitive	Level Sensitive
OTP_SEQ_CLK_SPEED	0.5 ms Time Slots	2 ms Time Slots							
OTP_TGRESET[1:0]	4 secs Global Reset Timer								
OTP_POR_DLY[2:0]	2 ms RESETBMCU Power-Up Delay								
OTP_UVDET[1:0]	Rising 3.0 V; Falling 2.9 V								
OTP_I2C_DEGLITCH_EN	I2C Deglitch Filter Disabled								
OTP_CHGR_OPER[1:0]	Charger = ON, Linear = ON	Charger = OFF, Linear = ON	Charger = ON, Linear = ON	Charger = ON, Linear = ON	Charger = ON, Linear = ON	Charger = OFF, Linear = ON	Charger = ON, Linear = ON	Charger = ON, Linear = ON	Charger = OFF, Linear = ON
OTP_CHGR_TPRECHG	Pre-charge timer = 30 minutes								
OTP_CHGR_EOCTIME[2:0]	End-Of-Charge Debounce = 16 secs								
OTP_CHGR_FCHGTIME[2:0]	Fast-Charge Timer Disabled								
OTP_CHGR_EOC_MODE	Linear ON in the DONE state								
OTP_CHGR_CHG_RESTART[1:0]	100 mV below CHGCV								
OTP_CHGR_CHG_CC[4:0]	CC = 100 mA			CC = 500 mA	CC = 100 mA				
OTP_CHGR_VSYSMIN[1:0]	VSYSMIN = 4.3 V					VSYSMIN = 3.7 V	VSYSMIN = 4.3 V		VSYSMIN = 3.7 V
OTP_CHGR_CHGCV[5:0]	CV = 4.2 V								
OTP_CHGR_VBUS_LIN_ILIM[4:0]	VBUS ILIM = 500 mA	VBUS ILIM = 1500 mA							
OTP_CHGR_VBUS_DPM_REG[2:0]	3.9 V	3.9 V	3.9 V	4.5 V	3.9 V	3.9 V	3.9 V	3.9 V	3.9 V
OTP_CHGR_USBPHYLDO	USBPHY LDO Disabled	USBPHY LDO Enabled							
OTP_CHGR_USBPHY	USBPHY = 3.3 V								
OTP_CHGR_ACTDISPHY	USBPHY Active Discharge Disabled	USBPHY Active Discharge Enabled							

12 Register map

12.1 Specific PMIC Registers (Offset is 0x00)

The following pages contain description of the various registers in the PF1550.

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Table 86. Register DEVICE_ID - ADDR 0x00

Name	Bit	R/W	Default	Description
DEVICE_ID	2 to 0	R	100	Loaded from fuses **000 —** Devices with "00" at the end of the part number, such as "PF1500" **001 —** Future use **010 —** Future use **011 —** Future use **100 —** Devices with "50" at the end of the part number, such as "PF1550" **101 —** Future use **110 —** Future use **111 —** Future use
FAMILY	7 to 3	R	01111	Identifies PMIC **01111 —** 0b0_1111 for "15" used to denote the "PF1550"

Table 87. Register OTP_FLAVOR - ADDR 0x01

Name	Bit	R/W	Default	Description
UNUSED	7 to 0	R	0x00	Blown by ATE to indicate flavor of OTP used **0x00 —** OTP not burned **0x01 —** A1 **0x02 —** A2 **0x03 —** A3 continues...

Table 88. Register SILICON_REV - ADDR 0x02

Name	Bit	R/W	Default	Description
METAL_LAYER_REV	2 to 0	R	001	Unused
FULL_LAYER_REV	5 to 3	R	010	Unused
FAB_FIN	7 to 6	R	00	Unused

Table 89. Register INT_CATEGORY - ADDR 0x06

Name	Bit	R/W	Default	Description
CHG_INT	0	R	0	This bit is set high if any of the charger interrupt status bits are set **0 —** No charger interrupt bit is set, cleared, or did not occur **1 —** "OR" function of all charger interrupt status bit
SW1_INT	1	R	0	This bit is set high if any of the Buck 1 interrupt status bits are set **0 —** SW1 interrupts cleared or did not occur **1 —** Any of the SW1 interrupt status bits are set
SW2_INT	2	R	0	This bit is set high if any of the Buck 2 interrupt status bits are set **0 —** SW2 interrupts cleared or did not occur **1 —** Any of the SW2 interrupt status bits are set
SW3_INT	3	R	0	This bit is set high if any of the Buck 3 interrupt status bits are set **0 —** SW3 interrupts cleared or did not occur **1 —** any of the SW3 interrupt status bits are set

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Table 89. Register INT_CATEGORY - ADDR 0x06*...continued*

Name	Bit	R/W	Default	Description
LDO_INT	4	R	0	This bit is set high if any of the LDO interrupt status bits are set. This includes LDO1, LDO2, and LDO3. **0 —** LDO interrupts cleared or did not occur **1 —** Any of the LDO interrupt status bits are set
ONKEY_INT	5	R	0	This bit is set high if any of the interrupts associated with ONKEY push-button are set. **0 —** ONKEY related interrupts cleared or did not occur **1 —** Any of the ONKEY interrupt status bits are set
TEMP_INT	6	R	0	This bit is set if any of the interrupts associated with the die temperature monitor are set **0 —** PMIC junction temperature related interrupts cleared or did not occur **1 —** any of the PMIC junction temperature interrupts status bits are set
MISC_INT	7	R	0	This bit is set if interrupts not covered by the above mentioned categories occur **0 —** Other interrupts (not covered by categories above) cleared, or did not occur **1 —** Status bit of other interrupts (not covered by categories above) is set

Table 90. Register SW_INT_STAT0 - ADDR 0x08

Name	Bit	R/W	Default	Description
SW1_LS_I	0	RW1C[1]	0	SW1 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
SW2_LS_I	1	RW1C	0	SW2 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
SW3_LS_I	2	RW1C	0	SW3 low-side current limit interrupt status. This bit is set if the current limit fault persists for longer than the debounce time. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 3	—	—	Unused

[1] Read or Write 1 to clear the bit

Table 91. Register SW_INT_MASK0 - ADDR 0x09

Name	Bit	R/W	Default	Description
SW1_LS_M	0	RW	1	SW1 low-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.

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Table 91. Register SW_INT_MASK0 - ADDR 0x09*...continued*

Name	Bit	R/W	Default	Description
SW2_LS_M	1	RW	1	SW2 low-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
SW3_LS_M	2	RW	1	SW3 low-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 3	—	—	Unused

Table 92. Register SW_INT_SENSE0 - ADDR 0x0A

Name	Bit	R/W	Default	Description
SW1_LS_S	0	R	0	SW1 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce). **0 —** Fault removed **1 —** Fault exists
SW2_LS_S	1	R	0	SW2 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce). **0 —** Fault removed **1 —** Fault exists
SW3_LS_S	2	R	0	SW3 low-side current limit interrupt sense. Sense is high as long as fault persists (post-debounce) **0 —** Fault removed **1 —** Fault exists
UNUSED	7 to 3	—	—	Unused

Table 93. Register SW_INT_STAT1 - ADDR 0x0B

Name	Bit	R/W	Default	Description
SW1_HS_I	0	RW1C [1]	0	SW1 high-side current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
SW2_HS_I	1	RW1C	0	SW2 high-side current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
SW3_HS_I	2	RW1C	0	SW3 high-side current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 3	—	—	Unused

[1] Read or Write 1 to clear the bit

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Table 94. Register SW_INT_MASK1 - ADDR 0x0C

Name	Bit	R/W	Default	Description
SW1_HS_M	0	RW	1	SW1 high-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
SW2_HS_M	1	RW	1	SW2 high-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
SW3_HS_M	2	RW	1	SW3 high-side current limit interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 3	—	—	Unused

Table 95. Register SW_INT_SENSE1 - ADDR 0x0D

Name	Bit	R/W	Default	Description
SW1_HS_S	0	R	0	SW1 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle. **0 —** Fault removed **1 —** Fault exists
SW2_HS_S	1	R	0	SW2 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle. **0 —** Fault removed **1 —** Fault exists
SW3_HS_S	2	R	0	SW3 high-side current limit interrupt sense. This bit should not toggle within a switching cycle (at buck switching frequency), but report the sense status within the switching cycle. **0 —** Fault removed **1 —** Fault exists
UNUSED	7 to 3	—	—	Unused

Table 96. Register SW_INT_STAT2 - ADDR 0x0E

Name	Bit	R/W	Default	Description
SW1_DVS_DONE_I	0	RW1C[1]	0	Interrupt to indicate SW1 DVS complete. This interrupt should occur every time regulator output voltage is changed (either via I^2C within a given state, or if there is change in voltage when transitioning states, Run to Standby, for example). **0 —** DVS not complete and/or bit cleared **1 —** DVS complete
SW2_DVS_DONE_I	1	RW1C	0	Interrupt to indicate SW2 DVS complete. This interrupt should occur every time regulator output voltage is changed (either via I^2C within a given state, or if there is change in voltage when transitioning states, Run to Standby, for example). **0 —** DVS not complete and/or bit cleared **1 —** DVS complete

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Table 96. Register SW_INT_STAT2 - ADDR 0x0E*...continued*

Name	Bit	R/W	Default	Description
UNUSED	7 to 2	—	—	Unused

[1] Read or Write 1 to clear the bit

Table 97. Register SW_INT_MASK2 - ADDR 0x0F

Name	Bit	R/W	Default	Description
SW1_DVS_DONE_M	0	RW	1	Mask for interrupt that indicates SW1 DVS complete **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
SW2_DVS_DONE_M	1	RW	1	Mask for interrupt that indicates SW2 DVS complete **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 2	—	—	Unused

Table 98. Register SW_INT_SENSE2 - ADDR 0x10

Name	Bit	R/W	Default	Description
SW1_DVS_S	0	R	0	Indicates DVS in progress for SW1 **0 —** DVS not in progress **1 —** DVS in progress
SW2_DVS_S	1	R	0	Indicates DVS in progress for SW2 **0 —** DVS not in progress **1 —** DVS in progress
UNUSED	7 to 2	—	—	Unused

Table 99. Register LDO_INT_STAT0 - ADDR 0x18

Name	Bit	R/W	Default	Description
LDO1_FAULTI	0	RW1C[1]	0	LDO1 current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
LDO2_FAULTI	1	RW1C	0	LDO2 current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
LDO3_FAULTI	2	RW1C	0	LDO3 current limit interrupt **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 3	—	—	Unused

[1] Read or Write 1 to clear the bit

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Table 100. Register LDO_INT_MASK0 - ADDR 0x19

Name	Bit	R/W	Default	Description
LDO1_FAULTM	0	RW	1	LDO1 current limit fault interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
LDO2_FAULTM	1	RW	1	LDO2 current limit fault interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
LDO3_FAULTM	2	RW	1	LDO3 current limit fault interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 3	—	—	Unused

Table 101. Register LDO_INT_SENSE0 - ADDR 0x1A

Name	Bit	R/W	Default	Description
LDO1_FAULTS	0	R	0	LDO1 fault interrupt sense **0 —** Fault removed **1 —** Fault exists
LDO2_FAULTS	1	R	0	LDO2 fault interrupt sense **0 —** Fault removed **1 —** Fault exists
LDO3_FAULTS	2	R	0	LDO3 fault interrupt sense **0 —** Fault removed **1 —** Fault exists
UNUSED	7 to 3	—	—	Unused

Table 102. Register TEMP_INT_STAT0 - ADDR 0x20

Name	Bit	R/W	Default	Description
THERM110I	0	RW1C[1]	0	Die temperature crosses 110 °C interrupt. Bidirectional interrupt. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	1	—	—	Unused
THERM125I	2	RW1C	0	Die temperature crosses 125 °C interrupt. Bidirectional interrupt. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 3	—	—	Unused

[1] Read or Write 1 to clear the bit

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Table 103. Register TEMP_INT_MASK0 - ADDR 0x21

Name	Bit	R/W	Default	Description
THERM110M	0	RW	1	Die temperature crosses 110 °C interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
UNUSED	1	—	—	Unused
THERM125M	2	RW	1	Die temperature crosses 125 °C interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 3	—	—	Unused

Table 104. Register TEMP_INT_SENSE0 - ADDR 0x22

Name	Bit	R/W	Default	Description
THERM110S	0	R	0	110 °C interrupt sense **0 —** Die temperature below 110 °C **1 —** Die temperature above 110 °C
UNUSED	1	—	—	Unused
THERM125S	2	R	0	125 °C interrupt sense **0 —** Die temperature below 125 °C **1 —** Die temperature above 125 °C
UNUSED	7 to 3	—	—	Unused

Table 105. Register ONKEY_INT_STAT0 - ADDR 0x24

Name	Bit	R/W	Default	Description
ONKEY_PUSHI	0	RW1C [1]	0	Interrupt to indicate a push of the ONKEY button. Goes high after debounce. **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared. Interrupt occurs whenever ONKEY button is pushed low for longer than the falling edge debounce setting. Interrupt also occurs whenever ONKEY button is released high for longer than the rising edge debounce setting, provided it went past the falling edge debounce time. In other words, this interrupt occurs whenever a change in status of the ONKEY_PUSHS sense bit occurs.
ONKEY_1SI	1	RW1C	0	Interrupt after ONKEY pressed for > 1 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_2SI	2	RW1C	0	Interrupt after ONKEY pressed for > 2 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_3SI	3	RW1C	0	Interrupt after ONKEY pressed for > 3 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared

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Table 105. Register ONKEY_INT_STAT0 - ADDR 0x24*...continued*

Name	Bit	R/W	Default	Description
ONKEY_4SI	4	RW1C	0	Interrupt after ONKEY pressed for > 4 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
ONKEY_8SI	5	RW1C	0	Interrupt after ONKEY pressed for > 8 s **0 —** Interrupt cleared or did not occur **1 —** Interrupt occurred and/or not cleared
UNUSED	7 to 6	—	—	Unused

[1] Read or Write 1 to clear the bit

Table 106. Register ONKEY_INT_MASK0 - ADDR 0x25

Name	Bit	R/W	Default	Description
ONKEY_PUSHM	0	RW	1	Interrupt mask for ONKEY_PUSH_I **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_1SM	1	RW	1	Interrupt mask for ONKEY_1SI **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_2SM	2	RW	1	Interrupt mask for ONKEY_2SI **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is NOT pulled low if corresponding interrupt status bit is set.
ONKEY_3SM	3	RW	1	Interrupt mask for ONKEY_3SI **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_4SM	4	RW	1	Interrupt mask for ONKEY_4SI **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
ONKEY_8SM	5	RW	1	Interrupt mask for ONKEY_8SI **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 6	—	—	Unused

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Table 107. Register ONKEY_INT_SENSE0 - ADDR 0x26

Name	Bit	R/W	Default	Description
ONKEY_PUSHS	0	R	0	Push interrupt sense **0 —** ONKEY not pushed low. This bit follows debounced version of the ONKEY button being released. **1 —** ONKEY pushed low. This follows the ONKEY button after the debounce circuit (debounce is programmable).
ONKEY_1SS	1	R	0	1 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_2SS	2	R	0	2 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_3SS	3	R	0	3 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_4SS	4	R	0	4 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
ONKEY_8SS	5	R	0	8 s interrupt sense or cleared after ONKEY button is released **0 —** ONKEY not pushed low for >1 s or cleared after ONKEY button is released. **1 —** ONKEY pushed and being held low > 1 s. This bit is cleared when ONKEY_PUSHS goes back to 0 when the push-button is released.
UNUSED	7 to 6	—	—	Unused

Table 108. Register MISC_INT_STAT0 - ADDR 0x28

Name	Bit	R/W	Default	Description
PWRUP_I	0	RW1C[1]	0	Interrupt to indicate completion of transition from STANDBY to RUN and from SLEEP to RUN **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
PWRDN_I	1	RW1C	0	Interrupt to indicate completion of transition from RUN to STANDBY and from RUN to SLEEP **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
PWRON_I	2	RW1C	0	Power on button event interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred

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Table 108. Register MISC_INT_STAT0 - ADDR 0x28*...continued*

Name	Bit	R/W	Default	Description
LOW_SYS_WARN_I	3	RW1C	0	LOW_SYS_WARN threshold crossed interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
SYS_OVLO_I	4	RW1C	0	SYS_OVLO threshold crossed interrupt **0 —** Interrupt cleared or has not occurred **1 —** Interrupt has occurred
UNUSED	7 to 5	—	—	Unused

[1] Read or Write 1 to clear the bit

Table 109. Register MISC_INT_MASK0- ADDR 0x29

Name	Bit	R/W	Default	Description
PWRUP_M	0	RW[1]	1	Mask for Interrupt to indicate completion on transition from STANDBY to RUN and from SLEEP to RUN **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
PWRDN_M	1	RW	1	Mask for Interrupt to indicate completion on transition from RUN to STANDBY and from RUN to SLEEP **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
PWRON_M	2	RW	1	Power on button event interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
LOW_SYS_WARN_M	3	RW	1	LOW_SYS_WARN threshold crossed interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
SYS_OVLO_M	4	RW	1	SYS_OVLO threshold crossed interrupt mask **0 —** Mask removed. INTB pin is pulled low if corresponding interrupt status bit is set. **1 —** Mask enabled. INTB pin is not pulled low if corresponding interrupt status bit is set.
UNUSED	7 to 5	—	—	Unused

[1] Asynchronous Set, Read, and Write

Table 110. Register MISC_INT_SENSE0 - ADDR 0x2A

Name	Bit	R/W	Default	Description
PWRUP_S	0	R	0	Sense for interrupt to indicate completion on transition from STANDBY to RUN and from SLEEP to RUN **0 —** Transition not in progress **1 —** Transition in progress

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Table 110. Register MISC_INT_SENSE0 - ADDR 0x2A*...continued*

Name	Bit	R/W	Default	Description
PWRDN_S	1	R	0	Interrupt to indicate completion on transition from RUN to STANDBY and from RUN to SLEEP **0 —** Transition not in progress **1 —** Transition in progress
PWRON_S	2	R	0	Power on button event interrupt sense **0 —** PWRON low **1 —** PWRON high
LOW_SYS_WARN_S	3	R	0	LOW_SYS_WARN threshold crossed interrupt sense **0 —** SYS > LOW_SYS_WARN **1 —** SYS < LOW_SYS_WARN
SYS_OVLO_S	4	R	0	SYS_OVLO threshold crossed interrupt sense **0 —** SYS < SYS_OVLO **1 —** SYS > SYS_OVLO
UNUSED	7 to 5	—	—	Unused

Table 111. Register COINCELL_CONTROL - ADDR 0x30

Name	Bit	R/W	Default	Description
VCOIN	3 to 0	RW	0000	Coin cell charger charging voltage **0000 —** 1.8 V **0111 —** 3.3 V (goes up in 100 mV step per LSB)
COINCHEN	4	RW	0	Coin cell charger enable **0 —** Charger disabled **1 —** Charger enabled
UNUSED	7 to 5	—	—	Unused

Table 112. Register SW1_VOLT - ADDR 0x32

Name	Bit	R/W	Default	Description
SW1_VOLT	5 to 0	RW1S[1]	—	SW1 voltage setting register (Run mode) **000000 —** See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings **Reset condition —** POR
UNUSED	7 to 5	—	—	Unused

[1] Load from OTP fuse, Read, and Write

Table 113. Register SW1_STBY_VOLT - ADDR 0x33

Name	Bit	R/W	Default	Description
SW1_STBY_VOLT	5 to 0	RW1S[1]	—	SW1 output voltage setting register (Standby mode). The default value here should be identical to SW1_VOLT[5:0] register. **000000 —** See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings
UNUSED	7 to 6	—	—	Unused

[1] Load from OTP fuse, Read, and Write

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Table 114. Register SW1_SLP_VOLT - ADDR 0x34

Name	Bit	R/W	Default	Description
SW1_SLP_VOLT	5 to 0	RW1S[1]	—	SW1 output voltage setting register (Sleep mode). The default value here should be identical to SW1_VOLT[5:0] register. **000000 —** See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings
UNUSED	7 to 6	—	—	Unused

[1] Load from OTP fuse, Read, and Write

Table 115. Register SW1_CTRL - ADDR 0x35

Name	Bit	R/W	Default	Description
SW1_EN	0	RW1S[1]	0	Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Run mode **1 —** Regulator enabled in Run mode
SW1_STBY_EN	1	RW1S	0	Enables buck regulator in Standby mode. User can turn off regulator by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP). **0 —** Regulator disabled in Standby mode **1 —** Regulator enabled in Standby mode
SW1_OMODE	2	RW[2]	0	Enables buck regulator in Sleep mode. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Sleep mode **1 —** Regulator enabled in Sleep mode
SW1_LPWR	3	RW	0	Enables the buck to enter Low-power mode during Standby and Sleep **0 —** Regulator not in Low-power mode **1 —** Regulator in Low-power mode during Standby or Sleep modes
SW1_DVSSPEED	4	RW1S	0	Controls slew rate of DVS transitions. Loaded from OTP and changeable by user after boot up. Not used when OTP_SW1_DVS_SEL = 1. **0 —** DVS rate at 12.5 mV/2 µs **1 —** DVS rate at 12.5 mV/4 µs
SW1_FPWM_IN_DVS	5	RW	0	Enables CCM operation during DVS down **0 —** does not force FPWM during DVS **1 —** forces regulator to track the DVS reference while it is falling rather than relying on the load current to pull the voltage low
SW1_FPWM	6	RW	0	Forces buck to go into CCM mode **0 —** Not in FPWM mode **1 —** Forced in PWM mode irrespective of load current
SW1_RDIS_ENB	7	RW1S	0	Controls discharge resistor on output when regulator disabled **0 —** Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge. **1 —** Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor.

[1] Load from OTP fuse, Read, and Write
[2] Asynchronous Set, Read, and Write

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Table 116. Register SW1_SLP_VOLT - ADDR 0x36

Name	Bit	R/W	Default	Description
SW1_ILIM	1 to 0	RW1S[1]	00	Sets current limit of SW1 regulator **00 —** Typical current limit of 1.0 A **01 —** Typical current limit of 1.2 A **10 —** Typical current limit of 1.5 A **11 —** Typical current limit of 2.0 A
UNUSED	3 to 2	—	—	Unused
SW1_TMODE_SEL	4	RW	0	**0 —** TON control **1 —** TOFF control
UNUSED	7 to 5	—	—	Unused

[1] Load from OTP fuse, Read, and Write

Table 117. Register SW2_VOLT - ADDR 0x38

Name	Bit	R/W	Default	Description
SW2_VOLT	5 to 0	RW1S[1]	—	SW2 voltage setting register (Run mode) **000000 —**See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings
UNUSED	7 to 6	—	—	Unused

[1] Load from OTP fuse, Read, and Write

Table 118. Register SW2_STBY_VOLT - ADDR 0x39

Name	Bit	R/W	Default	Description
SW2_STBY_VOLT	5 to 0	RW1S[1]	—	SW2 output voltage setting register (Standby mode). The default value here should be identical to SW2_VOLT[5:0] register. **000000 —** See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings
UNUSED	7 to 6	—	—	Unused

[1] Load from OTP fuse, Read, and Write

Table 119. Register SW2_SLP_VOLT - ADDR 0x3A

Name	Bit	R/W	Default	Description
SW2_SLP_VOLT	5 to 0	RW1S[1]	—	SW2 output voltage setting register (Sleep mode). The default value here should be identical to SW2_VOLT[5:0] register. **000000 —** See Table 31 for voltage settings **111111 —** See Table 31 for voltage settings
UNUSED	7 to 6	—	—	Unused

[1] Load from OTP fuse, Read, and Write

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Table 120. Register SW2_CTRL - ADDR 0x3B

Name	Bit	R/W	Default	Description
SW2_EN	0	RW1S[1]	0	Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Run mode **1 —** Regulator enabled in Run mode
SW2_STBY_EN	1	RW1S	0	Enables buck regulator in Standby mode. User can turn off regulator by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP). **0 —** Regulator disabled in Standby mode **1 —** Regulator enabled in Standby mode
SW2_OMODE	2	RW	0	Enables buck regulator in Sleep mode. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Sleep mode **1 —** Regulator enabled in Sleep mode
SW2_LPWR	3	RW	0	Enables the buck to enter Low-power mode during Standby and Sleep modes **0 —** Regulator not in Low-power mode **1 —** Regulator in Low-power mode during Standby or Sleep
SW2_DVSSPEED	4	RW1S	0	Controls slew rate of DVS transitions. Loaded from OTP and changeable by user after boot up. Not used when OTP_SW2_DVS_SEL = 1. **0 —** DVS rate at 12.5 mV/2 µs **1 —** DVS rate at 12.5 mV/4 µs
SW2_FPWM_IN_DVS	5	RW	0	Enables CCM operation during DVS down **0 —** does not force FPWM during DVS **1 —** forces regulator to track the DVS reference while it is falling rather than relying on the load current to pull the voltage low
SW2_FPWM	6	RW	0	Forces buck to go into CCM mode **0 —** Not in FPWM mode **1 —** Forced in PWM mode irrespective of load current.
SW2_RDIS_ENB	7	RW1S	0	Controls discharge resistor on output when regulator disabled **0 —** Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge. **1 —** Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor.

[1] Load from OTP fuse, Read, and Write

Table 121. Register SW2_CTRL1 - ADDR 0x3C

Name	Bit	R/W	Default	Description
SW2_ILIM	1 to 0	RW1S	00	Sets current limit of SW2 regulator **00 —** Typical current limit of 1.0 A **01 —** Typical current limit of 1.2 A **10 —** Typical current limit of 1.5 A **11 —** Typical current limit of 2.0 A
UNUSED	3 to 2	—	—	Unused
SW2_TMODE_SEL	4	RW	0	**0 —** TON control **1 —** TOFF control
UNUSED	7 to 5	—	—	Unused

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Table 122. Register SW3_VOLT - ADDR 0x3E

Name	Bit	R/W	Default	Description
SW3_VOLT	3 to 0	RW1S	—	SW3 voltage setting register (Run mode). Loaded from fuses. Read only because DVS is not supported in this regulator. **0000 —** See Table 37 for voltage settings **1111 —** See Table 37 for voltage settings
UNUSED	7 to 4	—	—	Unused

Table 123. Register SW3_STBY_VOLT - ADDR 0x3F

Name	Bit	R/W	Default	Description
SW3_STBY_VOLT	3 to 0	RW1S	—	SW3 voltage setting register (Standby mode). Loaded from fuses. Read only because DVS is not supported in this regulator. **0000 —** See Table 37 for voltage settings **1111 —**See Table 37 for voltage settings
UNUSED	7 to 4	—	—	Unused

Table 124. Register SW3_SLP_VOLT - ADDR 0x40

Name	Bit	R/W	Default	Description
SW3_SLP_VOLT	3 to 0	RW1S	—	SW3 voltage setting register (Sleep mode). Loaded from fuses. Read only because DVS is not supported in this regulator. **0000 —** See Table 37 for voltage settings **1111 —** See Table 37 for voltage settings
UNUSED	7 to 4	—	—	Unused

Table 125. Register SW3_CTRL - ADDR 0x41

Name	Bit	R/W	Default	Description
SW3_EN	0	RW1S	0	Enables buck regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Run mode **1 —** Regulator enabled in Run mode
SW3_STBY_EN	1	RW1S	0	Enables buck regulator in Standby mode. User can turn off regulator by clearing this bit. The default value of this bit should be equal to the SW1_EN bit (based on OTP). **0 —** Regulator disabled in Standby mode **1 —** Regulator enabled in Standby mode
SW3_OMODE	2	RW	0	Enables buck regulator in Sleep mode. User can turn off regulator by clearing this bit. **0 —** Regulator disabled in Sleep mode **1 —** Regulator enabled in Sleep mode
SW3_LPWR	3	RW	0	Enables the buck to enter Low-power mode during Standby and Sleep modes **0 —** Regulator not in Low-power mode **1 —** Regulator in Low-power mode while in Standby or Sleep
UNUSED	4	—	—	Unused
UNUSED	5	—	—	Unused

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Table 125. Register SW3_CTRL - ADDR 0x41*...continued*

Name	Bit	R/W	Default	Description
SW3_FPWM	6	RW	0	Forces buck to go into CCM mode **0 —** Not in FPWM mode **1 —** Forced in PWM mode irrespective of load current
SW3_RDIS_ENB	7	RW1S	0	Controls discharge resistor on output when regulator disabled **0 —** Enables discharge resistor on output when regulator disabled. Resistor connected at FB pin when regulator disabled to force capacitor discharge. **1 —** Disables discharge resistor on output when regulator disabled. Resistor not connected at FB pin when regulator disabled. Relies on leakage/residue load to discharge output capacitor.

Table 126. Register SW3_CTRL1 - ADDR 0x42

Name	Bit	R/W	Default	Description
SW3_ILIM	1 to 0	RW1S	00	Sets current limit of SW3 regulator **00 —** Typical current limit of 1.0 A **01 —** Typical current limit of 1.2 A **10 —** Typical current limit of 1.5 A **11 —** Typical current limit of 2.0 A
UNUSED	3 to 2	—	—	Unused
SW3_TMODE_SEL	4	RW	0	**0 —** TON control **1 —** TOFF control
UNUSED	7 to 5	—	—	Unused

Table 127. Register VSNVS_CTRL - ADDR 0x48

Name	Bit	R/W	Default	Description
VSNVS_VOLT	2 to 0	RW1S	000	Not used in PF1550. Placeholder for future products.
CLKPULSE	3	RW	0	Optional bit used for evaluation (see IP block)
FORCEBOS	4	RW	0	Optional bit for evaluation **0 —** BOS circuit activated only when VSYS < UVDET **1 —** Forces best of supply circuit irrespective of UVDET
LIBGDIS	5	RW	0	Use to reduce quiescent current in coin cell mode **0 —** VSNVS local band gap enabled in coin cell mode **1 —** VSNVS local band gap disabled in coin cell mode to save quiescent current
UNUSED	7 to 6	—	—	Unused

Table 128. Register VREFDDR_CTRL - ADDR 0x4A

Name	Bit	R/W	Default	Description
VREFDDR_EN	0	RW1S	0	**0 —** Disables VREFDDR regulator **1 —** Enables VREFDDR regulator. This is set by the OTP sequence.

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Table 128. Register VREFDDR_CTRL - ADDR 0x4A*...continued*

Name	Bit	R/W	Default	Description
VREFDDR_STBY_EN	1	RW1S	0	The default value for this should be same as VREFDDREN **0 —** Disables VREFDDR regulator in Standby mode **1 —** Enables VREFDDR regulator in Standby mode if VREFDDREN = 1
VREFDDR_OMODE	2	RW	0	**0 —** Keeps VREFDDR off in Off mode **1 —** Enables VREFDDR in Sleep mode if VREFDDREN = 1
VREFDDR_LPWR	3	RW	0	**0 —** Disables VREFDDR Low-power mode **1 —** Enables VREFDDR Low-power mode
UNUSED	7 to 4	—	—	Unused

Table 129. Register LDO1_VOLT - ADDR 0x4C

Name	Bit	R/W	Default	Description
LDO1_VOLT	4 to 0	RW1S	—	LDO1 output voltage setting register. Loaded from OTP. **00000 —** See Table 41 for voltage settings **11111 —** See Table 41 for voltage settings
UNUSED	7 to 5	—	—	Unused

Table 130. Register LDO1_CTRL - ADDR 0x4D

Name	Bit	R/W	Default	Description
VLDO1_EN	0	RW1S	0	Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Disables regulator **1 —** Enables regulator
VLDO1_STBY_EN	1	RW1S	0	Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN. **0 —** Disables regulator **1 —** Enables regulator
VLDO1_OMODE	2	RW	0	Enables LDO in Sleep mode **0 —** Disables regulator **1 —** Enables regulator
VLDO1_LPWR	3	RW	0	Forces LDO to Low-power mode in Sleep and Standby modes **0 —** Not in Low-power mode during Standby and Sleep **1 —** Regulator in Low-power mode during Standby and Sleep
LDO1_LS_EN	4	RW1S	0	This is loaded from OTP_LDOy_LS_EN and changeable from 0 to 1 on power-up. Changing from 1 to 0 is not allowed. **0 —** Sets LDOy in LDO mode **1 —** Sets LDOy to a load switch (fully on) mode
UNUSED	7 to 5	—	—	Unused

Table 131. Register LDO2_VOLT - ADDR 0x4F

Name	Bit	R/W	Default	Description
LDO2_VOLT	3 to 0	RW1S	—	LDO2 output voltage setting register. Loaded from OTP. **0000 —** See Table 43 for voltage settings **1111 —** See Table 43 for voltage settings

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Table 131. Register LDO2_VOLT - ADDR 0x4F*...continued*

Name	Bit	R/W	Default	Description
UNUSED	7 to 4	—	—	Unused

Table 132. Register LDO2_CTRL - ADDR 0x50

Name	Bit	R/W	Default	Description
VLDO2_EN	0	RW1S	0	Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Disables regulator **1 —** Enables regulator
VLDO2_STBY_EN	1	RW1S	0	Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN. **0 —** Disables regulator **1 —** Enables regulator
VLDO2_OMODE	2	RW	0	Enables LDO in Sleep mode **0 —** Disables regulator **1 —** Enables regulator
VLDO2_LPWR	3	RW	0	Forces LDO to Low-power mode in Sleep and Standby modes **0 —** Not in Low-power mode during Standby and Sleep **1 —** Regulator in Low-power mode during Standby and Sleep
UNUSED	7 to 4	—	—	Unused

Table 133. Register LDO3_VOLT - ADDR 0x52

Name	Bit	R/W	Default	Description
LDO3_VOLT	4 to 0	RW1S	—	LDO3 output voltage setting register. Loaded from OTP. **00000 —** See Table 41 for voltage settings **11111 —** See Table 41 for voltage settings
UNUSED	7 to 5	—	—	Unused

Table 134. Register LDO3_CTRL - ADDR 0x53

Name	Bit	R/W	Default	Description
VLDO3_EN	0	RW1S	0	Enables LDO regulator. Loaded from OTP based on the sequence settings. User can turn off regulator by clearing this bit. **0 —** Disables regulator **1 —** Enables regulator
VLDO3_STBY_EN	1	RW1S	0	Enables LDO in Standby mode. Default value of this bit should be same as VLDO1_EN. **0 —** Disables regulator **1 —** Enables regulator
VLDO3_OMODE	2	RW	0	Enables LDO in Sleep mode **0 —** Disables regulator **1 —** Enables regulator
VLDO3_LPWR	3	RW	0	Forces LDO to Low-power mode in Sleep and Standby modes **0 —** Not in Low-power mode during Standby and Sleep **1 —** Regulator in Low-power mode during Standby and Sleep

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Table 134. Register LDO3_CTRL - ADDR 0x53*...continued*

Name	Bit	R/W	Default	Description
LDO3_LS_EN	4	RW1S	0	This is loaded from OTP_LDOy_LS_EN and changeable from 0 to 1 on power up. Changing from 1 to 0 is not allowed. **0 —** sets LDOy in LDO mode **1 —** sets LDOy to a load switch (fully on) mode
UNUSED	7 to 5	—	—	Unused

Table 135. Register PWRCTRL0 - ADDR 0x58

Name	Bit	R/W	Default	Description
STANDBYDLY	1 to 0	RW	01	Controls delay of Standby pin after synchronization **0 —** No additional delay **1 —** 32 kHz cycle additional delay **2 —** 32 kHz cycle additional delay **3 —** 32 kHz cycle additional delay
STANDBYINV	2	RW	0	Controls polarity of STANDBY pin **0 —** Standby pin input active high **1 —** Standby pin input active low
POR_DLY	5 to 3	RW1S	000	Controls delay of RESETBMCU pin after power up (loaded from OTP) **000 —** RESETBMCU goes high 2 ms after last regulator **010 —** RESETBMCU goes high 4 ms after last regulator **011 —** RESETBMCU goes high 8 ms after last regulator **100 —** RESETBMCU goes high 16 ms after last regulator **101 —** RESETBMCU goes high 128 ms after last regulator **110 —** RESETBMCU goes high 256 ms after last regulator **111 —** RESETBMCU goes high 1024 ms after last regulator
TGRESET	7 to 6	RW1S	00	Controls duration for which ONKEY has to be pushed low for a global reset (part goes to REGS_DISABLE) **00 —** 4 s **01 —** 8 s **10 —** 12 s **11 —** 16 s

Table 136. Register PWRCTRL1 - ADDR 0x59

Name	Bit	R/W	Default	Description
PWRONDBNC	1 to 0	RW	00	Controls debounce of PWRON when in push-button mode (PWRON_CFG = 1) **00 —** 31.25 ms falling edge; 31.25 ms rising edge **01 —** 31.25 ms falling edge; 31.25 ms rising edge **10 —** 125 ms falling edge; 31.25 ms rising edge **11 —** 750 ms falling edge; 31.25 ms rising edge
ONKEYDBNC	3 to 2	RW	00	Controls debounce of ONKEY push-button **00 —** 31.25 ms falling edge; 31.25 ms rising edge **01 —** 31.25 ms falling edge; 31.25 ms rising edge **10 —** 125 ms falling edge; 31.25 ms rising edge **11 —** 750 ms falling edge; 31.25 ms rising edge

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Table 136. Register PWRCTRL1 - ADDR 0x59*...continued*

Name	Bit	R/W	Default	Description
PWRONRSTEN	4	RW	0	Enables going to REGS_DISABLE or Sleep mode when PWRON_CFG = 1. See Section 10 "PF1550 state machine" for details. **0 —** Long press on PWRON button does not take state to REGS_DISABLE or Sleep **1 —** Long press on PWRON button takes state to REGS_DISABLE or Sleep
RESTARTEN	5	RW	0	Enables restart of system when PWRON push-button is held low for 5 s **0 —** No impact **1 —** When going to REGS_DISABLE via a long press of PWRON button, holding it low for 1 more second takes state back to RUN (Equally, a 5 second push restarts the system)
REGSCPEN	6	RW	0	Shuts down LDO if it enters a current limit fault. Controls LDO1, LDO2, and LDO3. **0 —** LDO does not shut down in the event of a current limit fault. Continues to current limit **1 —** LDO is turned off when it encounters a current limit fault
ONKEY_RST_EN	7	RW	1	Enables turning off of system via ONKEY. See Section 10 "PF1550 state machine" for details. **0 —** ONKEY cannot be used to turn off or restart system **1 —** ONKEY can be used to turn off or restart system

Table 137. Register PWRCTRL2 - ADDR 0x5A

Name	Bit	R/W	Default	Description
UVDET	1 to 0	RW1S	00	Sets UVDET threshold **00 —** Rising 2.65 V; Falling 2.55 V **01 —** Rising 2.8 V; Falling 2.7 V **10 —** Rising 3.0 V; Falling 2.9 V **11 —** Rising 3.1 V; Falling 3.0 V
LOW_SYS_WARN	3 to 2	RW	00	Sets LOW_SYS_WARN threshold **00 —** Rising 3.3 V; Falling 3.1 V **01 —** Rising 3.5 V; Falling 3.3 V **10 —** Rising 3.7 V; Falling 3.5 V **11 —** Rising 3.9 V; Falling 3.7 V
UNUSED	7 to 4	—	—	Unused

Table 138. Register PWRCTRL3 - ADDR 0x5B

Name	Bit	R/W	Default	Description
GOTO_SHIP	0	RW	0	Set this bit to go to SHIP mode from any state. See Section 10 "PF1550 state machine" for details. **0 —** No impact **1 —** PF1550 enters SHIP mode
GOTO_CORE_OFF	1	RW	0	Set this bit to go to CORE_OFF mode once in REGS_DISABLE state **0 —** No impact **1 —** PF1550 enters CORE_OFF mode when in REGS_DISABLE state
UNUSED	7 to 2	—	—	Unused

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Table 139. Register SW1_PWRDN_SEQ - ADDR 0x5F

Name	Bit	R/W	Default	Description
SW1_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

Table 140. Register SW2_PWRDN_SEQ - ADDR 0x60

Name	Bit	R/W	Default	Description
SW2_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

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Table 141. Register SW2_PWRDN_SEQ - ADDR 0x61

Name	Bit	R/W	Default	Description
SW3_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

Table 142. Register LDO1_PWRDN_SEQ - ADDR 0x62

Name	Bit	R/W	Default	Description
LDO1_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

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Table 143. Register LDO2_PWRDN_SEQ - ADDR 0x63

Name	Bit	R/W	Default	Description
LDO2_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the functional opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

Table 144. Register LDO3_PWRDN_SEQ - ADDR 0x64

Name	Bit	R/W	Default	Description
LDO3_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

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Table 145. Register VREFDDR_PWRDN_SEQ - ADDR 0x65

Name	Bit	R/W	Default	Description
VREFDDR_PWRDN_SEQ	2 to 0	RW1S	000	This contains same value as power-up sequence value by default. Power-up sequence is in mirror registers. xxx = The power-down sequencer performs the function opposite to the power-up sequencer. Each regulator has an associated register setting (SW1_PWRDN_SEQ[2:0], SW2_PWRDN_SEQ[2:0], SW3_PWRDN_SEQ[2:0], LDO1_PWRDN_SEQ[2:0], LDO2_PWRDN_SEQ[2:0], LDO3_PWRDN_SEQ[2:0]. VREFDDR_PWRDN_SEQ[2:0]) that sets its power-down sequence. The default setting of the above registers is equal to the corresponding power-up sequence setting. For example, SW1_PWRDN_SEQ[2:0] = OTP_SW1_PWRUP_SEQ[2:0]. When the power-down sequencer is activated, regulators are turned off one by one in the descending order of the XXX_PWRDN_SEQ[2:0] setting. This way, by default, power-down is a mirror of the power-up sequence. In one of the "System On" states, the processor can change the values of the XXX_PWRDN_SEQ[2:0] registers. The power-up sequence is fixed by OTP (or TBB). If all XXX_PWRDN_SEQ[2:0] = 0x00, the power-down sequencer is bypassed and all the regulators are turned off at once.
UNUSED	7 to 3	—	—	Unused

Table 146. Register STATE_INFO - ADDR 0x67

Name	Bit	R/W	Default	Description
STATE	5 to 0	R	000000	Indicates machine state **000000 —** Wait status **001100 —** RUN state **001101 —** STANDBY state **001110 —** SLEEP/LPSR state **101011 —** REGS_DISABLE state Other bits are reserved
UNUSED	7 to 6	—	—	Unused

Table 147. Register I2C_ADDR - ADDR 0x68

Name	Bit	R/W	Default	Description
I2C_SLAVE_ADDR_LSBS	2 to 0	R	000	Loaded from fuses. But read only in functional space. **000 —** Slave Address: 0x08 **001 —** Slave Address: 0x09 **010 —** Slave Address: 0x0A **011 —** Slave Address: 0x0B **100 —** Slave Address: 0x0C **101 —** Slave Address: 0x0D **110 —** Slave Address: 0x0E **111 —** Slave Address: 0x0F
USE_DEFAULT_ADD R	7	RW	0	DEFAULT ADDR

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Table 148. Register RC_16MHZ - ADDR 0x6B

Name	Bit	R/W	Default	Description
REQ_16MHZ	0	RW	0	Enables 16 MHz clock **0 —** 16 MHz clock enable controlled by state machine **1 —** 16 MHz clock always enabled
REQ_ACORE_ON	1	RW	0	Controls Analog core enable **0 —** Analog core enable controlled by state machine **1 —** Analog core always on
REQ_ACORE_HIPWR	2	RW	0	Controls Low-power mode of the analog core **0 —** Analog core Low-power mode controlled by state machine **1 —** Analog core never in Low-power mode
UNUSED	7 to 3	—	—	Unused

Table 149. Register KEY1 - ADDR 0x6B

Name	Bit	R/W	Default	Description
KEY1	7 to 0	RW	0x00	Unused

12.2 Specific Charger Registers (Offset is 0x80)

Table 150. Register CHG_INT - ADDR 0x00

Name	Bit	R/W	Default	Description
SUP_I	0	RW1S[1]	0	Supplement mode interrupt **0 —** The SUP_OK bit interrupt has not occurred or been cleared **1 —** The SUP_OK bit interrupt has occurred **Reset condition —** VCOREDIG_RSTB
BAT2SOC_I	1	RW1S	0	VBATT to VSYS overcurrent interrupt **0 —** The BAT2SOC_OK interrupt has not occurred or been cleared **1—** The BAT2SOC _OK bit interrupt has occurred **Reset condition —** VCOREDIG_RSTB
BAT_I	2	RW1S	0	Battery interrupt **0 —** The BAT_OK interrupt has not occurred or been cleared **1 —** The BAT_OK interrupt has occurred **Reset condition —** VCOREDIG_RSTB
CHG_I	3	RW1S	0	Charger interrupt **0 —** The CHG_OK interrupt has not occurred or been cleared **1 —** The CHG_OK interrupt has occurred **Reset condition —** VCOREDIG_RSTB
RSVD4	4	RW1S	0	Unused
VBUS_I	5	RW1S	0	VBUS interrupt **0 —** The VBUS_OK interrupt has not occurred or been cleared **1 —** The VBUS_OK interrupt has occurred **Reset condition —** VCOREDIG_RSTB
VBUS_DPM_I	6	RW1S	0	VBUS_DPM interrupt **0 —** The VBUS_DPM _OK interrupt has not occurred or been cleared **1 —** The VBUS_DPM _OK interrupt has occurred **Reset condition —** VCOREDIG_RSTB

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Table 150. Register CHG_INT - ADDR 0x00*...continued*

Name	Bit	R/W	Default	Description
THM_I	7	RW1S	0	THM interrupt. Occurs when Warm/Cool thresholds are crossed or when thermal foldback is active. After the interrupt has occurred, THM_OK bit can be read to know the source of the interrupt. If THM_OK = 0, warm/cool thresholds are crossed If THM_OK = 1, thermal foldback is active **0 —** THM interrupt has not occurred or has been cleared **1 —** THM interrupt has occurred **Reset condition —** VCOREDIG_RSTB

[1] Load from OTP fuse, Read, and Write

Table 151. Register CHG_INT_MASK - ADDR 0x02

Name	Bit	R/W	Default	Description
SUP_M	0	RW	1	Supplement mode interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
BAT2SOC_M	1	RW	1	VBATT to VSYS overcurrent interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
BAT_M	2	RW	1	Battery interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
CHG_M	3	RW	1	Charger interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
RSVD4	4	RW	1	Unused
VBUS_M	5	RW	1	VBUS interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
VBUS_DPM_M	6	RW	1	VBUS_DPM interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB
THM_M	7	RW	1	THM interrupt mask **0 —** Unmasked **1 —** Masked **Reset condition —** VCOREDIG_RSTB

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Table 152. Register CHG_INT_OK - ADDR 0x04

Name	Bit	R/W	Default	Description
SUP_OK	0	R	0	Supplement mode indicator **0 —** Supplement mode not detected **1 —** Supplement mode detected **Reset condition —** VCOREDIG_RSTB
BAT2SOC_OK	1	R	0	Single-bit battery overcurrent indicator **0 —** Battery to VSYS has not hit overcurrent limit **1 —** Battery to VSYS has hit overcurrent limit (BATTOC_SNS bit = 1) **Reset condition —** VCOREDIG_RSTB
BAT_OK	2	R	1	Single-bit battery status indicator. See BATT_SNS for more information. **0 —** The battery has an issue or the charger has been suspended, for example, BATT_SNS = 0x02 or 0x05 or 0x06 **1 —** The battery is okay, for example, BATT_SNS ≠ 0x02 or 0x05 or 0x06 **Reset condition —** VCOREDIG_RSTB
CHG_OK	3	R	0	Single-bit charger status indicator. See CHG_SNS for more information. **Reset condition —** VCOREDIG_RSTB **0 —** The charger is not charging, has suspended charging or Thermal Reg = 1, for example, CHG_SNS ≠ 0x00 or 0x01 or 0x02 or 0x03 **1 —** The charger is okay, for example, CHG_SNS = 0x00 or 0x01 or 0x02 or 0x03 **Reset condition —** VCOREDIG_RSTB
RSVD4	4	R	0	Unused
VBUS_OK	5	R	0	Single-bit VBUS_LIN input status indicator. See VBUS_LIN_SNS for more information. **0 —** The VBUS_LIN input is invalid. For example, VBUS_VALID = 0. **1 —** The VBUS_LIN input is valid. For example, VBUS_VALID = 1. **Reset condition —** VCOREDIG_RSTB
VBUS_DPM_OK	6	R	0	VBUS_DPM status indicator. This register provides status of input Dynamic Power Management threshold. **0 —** Not in VBUS_DPM mode **1 —** VBUS_DPM mode **Reset condition —** VCOREDIG_RSTB
THM_OK	7	R	1	Thermistor status indicator. This register provides information on whether battery temperature is within or outside the thermistor cool/warm thresholds. **0 —** Thermistor outside cool and warm thresholds **1 —** Thermistor between cool and warm thresholds **Reset condition —** VCOREDIG_RSTB

Table 153. Register VBUS_SNS - ADDR 0x06

Name	Bit	R/W	Default	Description
RSVD0	1 to 0	R	00	Unused
VBUS_UVLO_SNS	2	R	1	**0 —** VBUS_ LIN > VBUS_LIN_UVLO **1 —** VBUS_ LIN < VBUS_LIN_UVLO or when VBUS is detached

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Table 153. Register VBUS_SNS - ADDR 0x06*...continued*

Name	Bit	R/W	Default	Description
VBUS_IN2SYS_SNS	3	R	1	**0 —** VBUS_ LIN > VBATT + VIN2SYS **1 —** VBUS_ LIN < VBATT + VIN2SYS
VBUS_OVLO_SNS	4	R	0	**0 —** VBUS_ LIN < VBUS_LIN_OVLO **1 —** VBUS_ LIN > VBUS_LIN_OVLO
VBUS_VALID	5	R	0	**0 —** VBUS is not valid **1 —** VBUS is valid, VBUS_LIN > VBUS_LIN_UVLO, VBUS_LIN > VBATT + VIN2SYS, VBUS_LIN < VBUS_LIN_OVLO **Reset condition —** VCOREDIG_RSTB
RSVD6	6	R	0	Unused
VBUS_DPM_SNS	7	R	0	VBUS_LIN DPM sense details **0 —** VBUS _LIN DPM threshold has not been triggered **1 —** VBUS_LIN DPM threshold has been triggered

Table 154. Register CHG_SNS - ADDR 0x07

Name	Bit	R/W	Default	Description
CHG_SNS	3 to 0	R	1000	Charger sense **0 —** Charger is in precharge mode, CHG_OK = 1, VBATT < $V_{PRECHG.LB}$, T_J < T_{SHDN} **1 —** Charger is in fast-charge constant current mode, CHG_OK = 1, VBATT < VBATREG, T_J < T_{SHDN} **2 —** Charger is in fast-charge constant voltage mode, CHG_OK = 1, VBATT = VBATREG, T_J < T_{SHDN} **3 —** Charger is in end-of-charge mode, CHG_OK = 1, VBATT ≥ VBATREG, I_{BAT} = I_{EOC}, T_J < T_{SHDN} **4 —** Charger is in done mode, CHG_OK = 0, VBATT > VBATREG-VRESTART, T_J < T_{SHDN} **5 —** Reserved **6 —** Charger is in timer fault mode, CHG_OK = 0, VBATT < V_{BATOV}, if BATT_SNS = 0b001 then VBATT < VBATPC, T_J < T_{SHDN} **7 —** Charger is in thermistor suspend mode, CHG_OK = 0, VBATT < V_{BATOV}, if BATT_SNS = 0b001 then VBATT < $V_{PRECHG.LB}$, T_J < T_{SHDN} **8 —** Charger is off, input invalid and/or charger is disabled, CHG_OK = 0 **9 —** Battery overvoltage condition **10 —** Charger is off and T_J > T_{SHDN}, CHG_OK = 0 **11 —** Reserved **12 —** Charger block is in Linear only mode, not charging, CHG_OK = 0 **13 —** Reserved **14 —** Reserved **15 —** Reserved **Reset condition —** VCOREDIG_RSTB
RSVD4	4	R	0	Unused
WDT_SNS	5	R	0	Watchdog sense bit **0 —** Watchdog timer has not expired **1 —** Charger is off because the watchdog timer expired, CHG_OK = 0 **Reset condition —** VCOREDIG_RSTB

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Table 154. Register CHG_SNS - ADDR 0x07*...continued*

Name	Bit	R/W	Default	Description
THM_SNS	6	R	0	Cool/Warm sense bit **0 —** Thermistor temperature is between cool and warm thresholds **1 —** Thermistor temperature is < Cool, or > Warm threshold **Reset condition —** VCOREDIG_RSTB
TREG_SNS	7	R	0	Temperature regulation sense **0 —** The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available **1 —** The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation **Reset condition —** VCOREDIG_RSTB

Table 155. Register BATT_SNS - ADDR 0x08

Name	Bit	R/W	Default	Description
BATT_SNS	2 to 0	R	000	**0 —** 0x00 = No valid VBUS input **1 —** 0x01 = VBATT < $V_{PRECHG.LB}$ **2 —** 0x02 = the battery cannot charge beyond the precharge threshold and charging has suspended and is in timer fault mode. This condition is also reported in the CHG_SNS as 0x06. **3 —** Reserved **4 —** 0x04 = $V_{PRECHG.LB}$ < VBATT **5 —** 0x05 = the battery voltage is greater than the battery overvoltage flag threshold (V_{BATOV}). Tthis flag is generated only when there is a valid input. **6 —** 0x06 = battery not detected with a valid input and after system wake-up **7 —** Reserved **Reset condition —** VCOREDIG_RSTB
RSVD3	4 to 3	RW	00	Unused
BATTOC_SNS	5	R	0	VBATT to VSYS overcurrent fault **0 —** No fault **1 —** VBATT to VSYS in high current fault **Reset condition —** VCOREDIG_RSTB
RSVD6	7 to 6	RW	00	Unused

Table 156. Register CHG_OPER- ADDR 0x09

Name	Bit	R/W	Default	Description
CHG_OPER	1 to 0	RW1S[1]	01	Charger operation configuration **0 —** charger = off, linear = off. The BATFET switch is on to allow the battery to support the system. **1 —** charger = off, linear = on. When there is a valid VBUS input and no battery, the linear regulator regulates the VSYS voltage to VSYSMIN[1:0]. **2 —** charger = on, linear = on. When there is a valid input, the battery is charging. VSYS is the larger of $VSYS_{MIN}$ and VBATT + I_{BAT} * R_{BATFET}. **3 —** Reserved **Reset condition —** VCOREDIG_RSTB
UNUSED	2	RW	0	Unused

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Table 156. Register CHG_OPER- ADDR 0x09*...continued*

Name	Bit	R/W	Default	Description
WDTEN	3	RW	0	Enable watchdog timer bit. While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01. **0 —** Watchdog timer disabled **1 —** Watchdog timer enabled **Reset condition —** VCOREDIG_RSTB
DISBATFET	4	RW	0	VBATT to VSYS FET disable control **0 —** VBATT to VSYS FET is controlled by internal state machine **1 —** VBATT to VSYS FET is forced off **Reset condition —** VCOREDIG_RSTB
UNUSED	7 to 5	RW	000	Unused

[1] Load from OTP fuse, Read, and Write

Table 157. Register CHG_TMR - ADDR 0x0A

Name	Bit	R/W	Default	Description
FCHGTIME	2 to 0	RW1S	010	Fast-charge timer duration (t_{FC}) **0 —** Disable **1 —** 2 hrs **2 —** 4 hrs **3 —** 6 hrs **4 —** 8 hrs **5 —** 10 hrs **6 —** 12 hrs **7 —** 14 hrs **Reset condition —** VCOREDIG_RSTB
EOCTIME	5 to 3	RW1S	001	End-of-charge timer setting **0 —** 0 min (16 secs debounce) **1 —** 10 min **2 —** 20 min **3 —** 30 min **4 —** 40 min **5 —** 50 min **6 —** 60 min **7 —** 70 min **Reset condition —** VCOREDIG_RSTB
RSVD6	6	R	0	Unused
TPRECHG	7	RW1S	0	Precharge timer value. Used for low battery. **0 —** Precharge timer value = 30 min **1 —** Precharge timer value = 45 min **Reset condition —** VCOREDIG_RSTB

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Table 158. Register CHG_EOC_CNFG - ADDR 0x0D

Name	Bit	R/W	Default	Description
CHG_RESTART	1 to 0	RW1S	01	Charger restart threshold **00 —** 0x00 = 100 mV below the value programmed by CHG_CV_PRM **01 —** 0x01 = 150 mV below the value programmed by CHG_CV_PRM **02 —** 0x02 = 200 mV below the value programmed by CHG_CV_PRM **03 —** 0x03 = disabled **Reset condition —** VCOREDIG_RSTB
FORCE_BATT_ISO	2	RW1S	0	Unused
EOC_EXIT	3	RW1S	0	Unused
IEOC	6 to 4	RW	100	End-of-charge current threshold. End-of-charge occurs during fast-charge constant voltage mode and end-of-charge current measured as battery decays to the value programmed in this register. This transition starts the end-of-charge timer (t_{EOC}). **0 —** 5 mA **1 —** 10 mA **2 —** 20 mA **3 —** 30 mA **4 —** 50 mA **5 —** Reserved **6 —** Reserved **7 —** Reserved **Reset condition —** VCOREDIG_RSTB
EOC_MODE	7	RW1S	0	Unused

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Table 159. Register CHG_CURR_CNFG - ADDR 0x0E

Name	Bit	R/W	Default	Description
CHG_CC	4 to 0	RW1S	00000	Fast charge current selection. When the charger is enabled, the charge current limit is set by these bits. These bits range from 100 mA to 1.0 A. **0 —** 100 mA **1 —** 150 mA **2 —** 200 mA **3 —** 250 mA **4 —** 300 mA **5 —** 350 mA **6 —** 400 mA **7 —** 450 mA **8 —** 500 mA **9 —** 550 mA **10 —** 600 mA **11 —** 650 mA **12 —** 700 mA **13 —** 750 mA **14 —** 800 mA **15 —** 850 mA **16 —** 900 mA **17 —** 950 mA **18 —** 1000 mA **19 —** 1050 mA (Reserved) **20 —** 1100 mA (Reserved) **21 —** 1150 mA (Reserved) **22 —** 1200 mA (Reserved) **23 —** 1250 mA (Reserved) **24 —** 1300 mA (Reserved) **25 —** 1350 mA (Reserved) **26 —** 1400 mA (Reserved) **27 —** 1450 mA (Reserved) **28 —** 1500 mA (Reserved) **29 —** 1550 mA (Reserved) **30 —** 1600 mA (Reserved) **31 —** 1650 mA (Reserved) **Reset condition —** VCOREDIG_RSTB
PRECHGLB_THRS	6 to 5	RW1S	00	Precharge (low battery) charging voltage threshold setting **0 —** 2.8 V **1 —** 2.7 V (Reserved) **2 —** 2.9 V (Reserved) **3 —** 3.0 V (Reserved) **Reset condition —** VCOREDIG_RSTB
RSVD7	7	RW	0	Reserved

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Table 160. Register BATT_REG - ADDR 0x0F

Name	Bit	R/W	Default	Description
CHGCV	5 to 0	RW1S	101011	Battery termination voltage setting **0 —** 3.50 V **1 —** 3.50 V **2 —** 3.50 V **3 —** 3.50 V **4 —** 3.50 V **5 —** 3.50 V **6 —** 3.50 V **7 —** 3.50 V **8 —** 3.50 V **9 —** 3.52 V **10 —** 3.54 V **11 —** 3.56 V **12 —** 3.58 V **13 —** 3.60 V **14 —** 3.62 V **15 —** 3.64 V **16 —** 3.66 V **17 —** 3.68 V **18 —** 3.70 V **19 —** 3.72 V **20 —** 3.74 V **21 —** 3.76 V **22 —** 3.78 V **23 —** 3.80 V **24 —** 3.82 V **25 —** 3.84 V **26 —** 3.86 V **27 —** 3.88 V **28 —** 3.90 V **29 —** 3.92 V **30 —** 3.94 V **31 —** 3.96 V **32 —** 3.98 V **33 —** 4.00 V **34 —** 4.02 V **35 —** 4.04 V **36 —** 4.06 V **37 —** 4.08 V **38 —** 4.10 V **39 —** 4.12 V **40 —** 4.14 V **41 —** 4.16 V **42 —** 4.18 V **43 —** 4.20 V **44 —** 4.22 V **45 —** 4.24 V **46 —** 4.26 V

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Table 160. Register BATT_REG - ADDR 0x0F*...continued*

Name	Bit	R/W	Default	Description
				47 — 4.28 V **48 —** 4.30 V **49 —** 4.32 V **50 —** 4.34 V **51 —** 4.36 V **52 —** 4.38 V **53 —** 4.40 V **54 —** 4.42 V **55 —** 4.44 V **56 —** 4.44 V **57 —** 4.44 V **58 —** 4.44 V **59 —** 4.44 V **60 —** 4.44 V **61 —** 4.44 V **62 —** 4.44 V **63 —** 4.44 V **Reset condition —** VCOREDIG_RSTB
VSYSMIN	7 to 6	RW1S	00	Minimum system regulation voltage ($VSYS_{MIN}$) **0 —** 3.5 V **1 —** 3.7 V **2 —** 4.3 V **3 —** Reserved **Reset condition —** VCOREDIG_RSTB

Table 161. Register BATFET_CNFG - ADDR 0x11

Name	Bit	R/W	Default	Description
WDTCLR	1 to 0	RW	00	Watchdog timer clear bits. Writing "01" to these bits clears the watchdog timer when the watchdog timer is enabled. **0 —** The watchdog timer is not cleared **1 —** The watchdog timer is cleared **2 —** The watchdog timer is not cleared **3 —** The watchdog timer is not cleared **Reset condition —** VCOREDIG_RSTB
WD_BATFET_OFF	2	RW	0	Watchdog timer BATFET control **0 —** Not used in PF1550. See WDFLT_BFET_EN bit in Fault_BATFET_CNFG register. **1 —** Not used in PF1550. See WDFLT_BFET_EN bit in Fault_BATFET_CNFG register. **Reset condition —** VCOREDIG_RSTB
BOVRC_DISBATFET	3	RW1S	0	Disable BATFET in case of battery overcurrent limit **0 —** Charger controls BATFET switch; BATFET is turned off in case of battery overcurrent occurs for 16 ms (default) **1 —** BATFET is not turned off when battery overcurrent occurs. Charger operation remains undisturbed by overcurrent event. **Reset condition —** VCOREDIG_RSTB

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Table 161. Register BATFET_CNFG - ADDR 0x11*...continued*

Name	Bit	R/W	Default	Description
BATFET_OC	5 to 4	RW1S	11	VBATT to VSYS FET overcurrent threshold, 2 bits adjustment **0 —** Disabled **1 —** 2.2 A typ **2 —** 2.8 A typ **3 —** 3.2 A typ **Reset condition —** VCOREDIG_RSTB
WD_TIME	6	RW	0	Sets watchdog timer value **0 —** 80 s **0 —** 32 s **Reset condition —** VCOREDIG_RSTB
BOVRC_NOVBUS	7	RW	0	Enables/disables battery overcurrent protection when no VBUS is present **0 —** Disables battery overcurrent protection when no VBUS is present **1 —** Enables battery overcurrent protection when no VBUS is present **Reset condition —** VCOREDIG_RSTB

Table 162. Register THM_REG_CNFG - ADDR 0x12

Name	Bit	R/W	Default	Description
THM_CNFG	1 to 0	RW1S	01	Thermistor configuration. 2 bits adjustment. **0 —** Thermistor not in control of charger. T_{COOL} and T_{WARM} interrupts are still generated. Thermistor Suspend mode is not entered in this setting. CC and CV values are not altered when T_{COOL}/cold, T_{WARM}/hot thresholds are crossed. **1 —** Thermistor control in charger. Charging stops when battery temperature > T_{HOT} or < T_{COLD}. **2 —** JEITA 1 settings - Thermistor control in charger. Charging current and battery regulation voltage is reduced at battery temperature > T_{WARM} and < T_{COOL}. **3 —** JEITA 2 settings - Thermistor control in charger. Charging current is reduced at battery temperature > T_{WARM} and < T_{COOL}. Charger voltage is not changed. **Reset condition —** VCOREDIG_RSTB
REGTEMP	3 to 2	RW1S	01	Junction temperature thermal regulation loop set point. 2-bit adjustments. The charger's target current limit starts to fold back and the TREG_SNS bit is set if the junction temperature is greater than the REGTEMP set point. **0 —** 80 °C **1 —** 95 °C **2 —** 110 °C **3 —** 125 °C (Reserved) **Reset condition —** VCOREDIG_RSTB
THM_COLD	4	RW1S	0	Thermistor cold temperature selection **0 —** 0 °C **1 —** –10 °C **Reset condition —** VCOREDIG_RSTB
THM_HOT	5	RW1S	0	Thermistor hot temperature selection **0 —** 60 °C **1 —** 55 °C **Reset condition —** VCOREDIG_RSTB
RSVD6	6	RW	0	Unused

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Table 162. Register THM_REG_CNFG - ADDR 0x12*...continued*

Name	Bit	R/W	Default	Description
TEMP_FB_EN	7	RW1S	0	Enable/disable thermal foldback current function **0 —** Thermal foldback disabled **1 —** Thermal foldback enabled **Reset condition —** VCOREDIG_RSTB

Table 163. Register VBUS_INLIM_CNFG - ADDR 0x14

Name	Bit	R/W	Default	Description
RSVD0	2 to 0	RW	000	Unused
VBUS_LIN_ILIM	7 to 3	RW1S	01101	Maximum input current limit selection. 5-bit adjustment from 10 mA to 1500 mA. **0 —** 10 mA **1 —** 15 mA **2 —** 20 mA **3 —** 25 mA **4 —** 30 mA **5 —** 35 mA **6 —** 40 mA **7 —** 45 mA **8 —** 50 mA **9 —** 100 mA **10 —** 150 mA **11 —** 200 mA **12 —** 300 mA **13 —** 400 mA **14 —** 500 mA **15 —** 600 mA **16 —** 700 mA **17 —** 800 mA **18 —** 900 mA **19 —** 1000 mA **20 —** 1500 mA **21 —** Reserved **22 —** Reserved **23 —** Reserved **24 —** Reserved **25 —** Reserved **26 —** Reserved **27 —** Reserved **28 —** Reserved **29 —** Reserved **30 —** Reserved **31 —** Reserved **Reset condition —** CHGPOK_RSTB

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Table 164. Register VBUS_LIN_DPM - ADDR 0x15

Name	Bit	R/W	Default	Description
VBUS_DPM_REG	2 to 0	RW1S	000	VBUS regulation voltage (DPM mode) **0 —** 3.90 V **1 —** 4.00 V **2 —** 4.10 V **3 —** 4.20 V **4 —** 4.30 V **5 —** 4.40 V **6 —** 4.50 V **7 —** 4.60 V **Reset condition —** VCOREDIG_RSTB
PRECHGDBATT_THRSH	4 to 3	RW1S	00	Precharge threshold **0 —** Reserved **1 —** Reserved **2 —** Reserved **3 —** Reserved
VIN_DPM_STOP	5	RW1S	0	Dynamic input power management panic stop threshold **0 —** 200 mV **1 —** 250 mV **Reset condition —** VCOREDIG_RSTB
RSVD6	6	R	0	Unused
FET_SCALE	7	RW1S	0	Enables/disables BATFET scaling **0 —** Reserved **1 —** Reserved **Reset condition —** VCOREDIG_RSTB

Table 165. Register USB_PHY_LDO_CNFG - ADDR 0x16

Name	Bit	R/W	Default	Description
ACTDISPHY	0	RW1S	1	Active discharger enable bit for USBPHY **0 —** No active discharge **1 —** Active discharge when regulator disabled **Reset condition —** VCOREDIG_RSTB
USBPHY	1	RW1S	0	USBPHY voltage setting register **0 —** 3.3 V **1 —** 4.9 V **Reset condition —** VCOREDIG_RSTB
USBPHYLDO	2	RW1S	0	USBPHY LDO enable **0 —** Disabled **1 —** Enabled **Reset condition —** VCOREDIG_RSTB
RSVD3	3	RW	0	Unused
RSVD4	5 to 4	RW	00	Unused
RSVD6	7 to 6	RW	00	Unused

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Table 166. Register DBNC_DELAY_TIME - ADDR 0x18

Name	Bit	R/W	Default	Description
VBUS_OV_TDB	1 to 0	RW1S	00	VBUS overvoltage debounce delay **0 —** 10 µs (Reserved) **1 —** 100 µs **2 —** 1 ms **3 —** 10 ms **Reset condition —** VCOREDIG_RSTB
USB_PHY_TDB	3 to 2	RW1S	00	USBPHY debounce timer - not used in PF1550 **0 —** 0 ms **1 —** 16 ms **2 —** 32 ms **3 —** Not used **Reset condition —** VCOREDIG_RSTB
SYS_WKUP_DLY	5 to 4	RW1S	00	System wake-up time **0 —** 8.0 ms **1 —** 16 ms **2 —** 32 ms **3 —** 100 ms **Reset condition —** VCOREDIG_RSTB
RSVD6	7 to 6	RW	00	Unused

Table 167. Register CHG_INT_CNFG - ADDR 0x19

Name	Bit	R/W	Default	Description
CHG_INT_GEN	0	RW1S	0	Determines if an interrupt is generated at every mode transition in charger **0 —** Interrupt is not generated at every mode transition except transition from Fast Charge to CV **1 —** Interrupt is generated at every mode transition (Fast Charge, CV, EOC, DONE, No Charger) **Reset condition —** VCOREDIG_RSTB
EOC_INT	1	RW1S	0	Interrupt bit generated at end-of-charge **0 —** No interrupt bit is generated when end-of- charge current is triggered **1 —** Interrupt bit is generated when end-of-charge current is triggered **Reset condition —** VCOREDIG_RSTB
RSVD2	7 to 2	RW	000000	Unused

Table 168. Register THM_ADJ_SETTING - ADDR 0x1A

Name	Bit	R/W	Default	Description
THM_WARM	0	RW1S	0	Thermistor warm threshold setting **0 —** 45 °C **1 —** 50 °C **Reset condition —** VCOREDIG_RSTB
THM_COOL	1	RW1S	0	Thermistor cool threshold setting **0 —** 15 °C **1 —** 10 °C **Reset condition —** VCOREDIG_RSTB

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Table 168. Register THM_ADJ_SETTING - ADDR 0x1A*...continued*

Name	Bit	R/W	Default	Description
CV_ADJ	3 to 2	RW1S	00	JEITA Thermistor battery termination voltage subtraction setting **0 —** 60 mV **1 —** 100 mV **2 —** 160 mV **3 —** 200 mv **Reset condition —** VCOREDIG_RSTB
CC_ADJ	5 to 4	RW1S	00	JEITA Thermistor battery charging current setting (percentage of I_{FC}) **0 —** 25 % **1 —** 50 % **2 —** 75 % **3 —** 100 % **Reset condition —** VCOREDIG_RSTB
RSVD6	7 to 6	RW	00	Unused

Table 169. Register VBUS2SYS_CNFG - ADDR 0x1B

Name	Bit	R/W	Default	Description
VBUS2SYS_TDB	1 to 0	RW1S	00	VBUS to VSYS comparator debounce time **0 —** Reserved **1 —** 100 µs **2 —** 1 ms **3 —** 10 ms **Reset condition —** VCOREDIG_RSTB
VBUS2SYS_THRSH	2	RW1S	0	VBUS to VSYS comparator threshold setting **0 —** 50 mV **1 —** 175 mV **Reset condition —** VCOREDIG_RSTB
RSVD3	7 to 3	RW	00000	Unused

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Table 170. Register LED_PWM - ADDR 0x1C

Name	Bit	R/W	Default	Description
LED_PWM	5 to 0	RW	000000	LED PWM duty cycle setting **0 —** 0/32 (Off) **1 —** 1/32 **2 —** 2/32 **3 —** 3/32 **4 —** 4/32 **5 —** 5/32 **6 —** 6/32 **7 —** 7/32 **8 —** 8/32 **9 —** 9/32 **10 —** 10/32 **11 —** 11/32 **12 —** 12/32 **13 —** 13/32 **14 —** 14/32 **15 —** 15/32 **16 —** 16/32 **17 —** 17/32 **18 —** 18/32 **19 —** 19/32 **20 —** 20/32 **21 —** 21/32 **22 —** 22/32 **23 —** 23/32 **24 —** 24/32 **25 —** 25/32 **26 —** 26/32 **27 —** 27/32 **28 —** 28/32 **29 —** 29/32 **30 —** 30/32 **31 —** 31/32 **32 and higher —** 32/32 **Reset condition —** VCOREDIG_RSTB
LED_RAMP	6	RW	0	Enable PWM ramp enable **0 —** Ramp disable **1 —** Ramp enable **Reset condition —** VCOREDIG_RSTB
LED_EN	7	RW	0	LED driver enable **0 —** Disabled **1 —** Enabled **Reset condition —** VCOREDIG_RSTB

Table 171. Register FAULT_BATFET_CNFG - ADDR 0x1D

Name	Bit	R/W	Default	Description
OVFLT_BFET_EN	0	RW1S	0	BATFET control during battery overvoltage **0 —** BATFET is opened during battery overvoltage **1 —** BATFET remains closed **Reset condition —** VCOREDIG_RSTB

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Table 171. Register FAULT_BATFET_CNFG - ADDR 0x1D*...continued*

Name	Bit	R/W	Default	Description
WDFLT_BFET_EN	1	RW1S	0	BATFET control during watchdog fault **0 —** BATFET is opened during watchdog fault **1 —** BATFET remains closed **Reset condition —** VCOREDIG_RSTB
THMSUS_BFET_EN	2	RW1S	0	BATFET control during thermistor fault (< Cold or > Hot) **0 —** BATFET is opened during battery thermistor fault **1 —** BATFET remains closed **Reset condition —** VCOREDIG_RSTB
TSHDN_BFET_EN	3	RW1S	0	BATFET control during thermal shutdown **0 —** BATFET is opened during thermal shutdown **1 —** BATFET remains closed **Reset condition —** VCOREDIG_RSTB
TMRFLT_BFET_EN	4	RW1S	0	BATFET control during charger timer fault **0 —** BATFET is opened during charger timer fault **1 —** BATFET remains closed **Reset condition —** POR
RSVD5	5	RW1S	0	Unused
CTRL_CHGR_BET A_ SEL	7 to 6	RW1S	00	Reserved

Table 172. Register LED_CNFG - ADDR 0x1E

Name	Bit	R/W	Default	Description
LED_FREQ	1 to 0	RW	00	LED driver PWM frequency setting **0 —** 1.0 Hz **1 —** 0.5 Hz **2 —** 256 Hz **3 —** 8.0 Hz **Reset condition —** VCOREDIG_RSTB
LED_CURRENT	3 to 2	RW1S	00	LED driver current amplitude setting **0 —** Reserved **1 —** 6.0 mA **2 —** Reserved **3 —** Reserved **Reset condition —** VCOREDIG_RSTB
LED_CFG	4	RW1S	0	Controls LED on/blinking mode **0 —** LED on during charging; flashing during charger fault; off in DONE state **1 —** LED flashing during charging; on during charger fault; off in DONE state **Reset condition —** VCOREDIG_RSTB
LEDOVRD	5	RW	0	Enable software control of LED **0 —** LED controlled by state machine **1 —** LED controlled via software **Reset condition —** VCOREDIG_RSTB
RSVD4	7 to 6	RW	00	Unused

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Table 173. Register LED_CNFG - ADDR 0x1F

Name	Bit	R/W	Default	Description
CHGR_KEY2	7 to 0	RW	0x00	Reserved

12.3 Register PMIC bitmap

VCOREDIG_PORB [1]

PS_END_RSTB [2]

REGS_DISABLE_TOG_RSTB [3]

[1] Bits reset by invalid VCOREDIG
[2] Bits reset by PORB or RESETBMCU
[3] Bits reset by pulse to REGS_DISABLE mode

Table 174. Register PMIC bitmap

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
0x00	DEVICE_ID	Name	FAMILY[3:7]					DEVICE_ID[2:0]		
		Reset	0	1	1	1	1	1	0	0
		Type	R	R	R	R	R	R	R	R
0x01	OTP_FLAVOR	Name	—	—	OTP_FLAVOR[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	R	R	R	R	R	R
0x02	SILICON_REV	Name	FAB_FIN[7:6]		FULL_LAYER_REV[5:3]			METAL_LAYER_REV[2:0]		
		Reset	0	0	0	0	1	0	0	0
		Type	R	R	R	R	R	R	R	R
0x06	INT_CATEGORY	Name	MISC_INT	TEMP_INT	ONKEY_INT	LDO_INT	SW3_INT	SW2_INT	SW1_INT	CHG_INT
		Reset	0	0	0	0	0	0	0	0
		Type	R	R	R	R	R	R	R	R
0x08	SW_INT_STAT0	Name	—	—	—	—	—	SW3_LS_I	SW2_LS_I	SW1_LS_I
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1C	RW1C	RW1C
0x09	SW_INT_MASK0	Name	—	—	—	—	—	SW3_LS_M	SW2_LS_M	SW1_LS_M
		Reset	0	0	0	0	0	1	1	1
		Type	—	—	—	—	—	RW	RW	RW
0x0A	SW_INT_SENSE0	Name	—	—	—	—	—	SW3_LS_S	SW2_LS_S	SW1_LS_S
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	R	R	R
0x0B	SW_INT_STAT1	Name	—	—	—	—	—	SW3_HS_I	SW2_HS_I	SW1_HS_I
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1C	RW1C	RW1C
0x0C	SW_INT_MASK1	Name	—	—	—	—	—	SW3_HS_M	SW2_HS_M	SW1_HS_M
		Reset	0	0	0	0	0	1	1	1
		Type	—	—	—	—	—	RW	RW	RW
0x0D	SW_INT_SENSE1	Name	—	—	—	—	—	SW3_HS_S	SW2_HS_S	SW1_HS_S
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	R	R	R
0x0E	SW_INT_STAT2	Name	—	—	—	—	—	—	SW2_DVS_DONE_I	SW1_DVS_DONE_I
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	—	RW1C	RW1C
0x0F	SW_INT_MASK2	Name	—	—	—	—	—	—	SW2_DVS_DONE_M	SW1_DVS_DONE_M
		Reset	0	0	0	0	0	0	1	1
		Type	—	—	—	—	—	—	RW	RW

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Table 174. Register PMIC bitmap*...continued*

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
0x10	SW_INT_SENSE2	Name	—	—	—	—	—	—	SW2_DVS_S	SW1_DVS_S
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	—	R	R
0x18	LDO_INT_STAT0	Name	—	—	—	—	—	LDO3_FAULTI	LDO2_FAULTI	LDO1_FAULTI
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1C	RW1C	RW1C
0x19	LDO_INT_MASK0	Name	—	—	—	—	—	LDO3_FAULTM	LDO2_FAULTM	LDO1_FAULTM
		Reset	0	0	0	0	0	1	1	1
		Type	—	—	—	—	—	RW	RW	RW
0x1A	LDO_INT_SENSE0	Name	—	—	—	—	—	LDO3_FAULTS	LDO2_FAULTS	LDO1_FAULTS
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	R	R	R
0x20	TEMP_INT_STAT0	Name	—	—	—	—	—	THERM125I	—	THERM110I
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1C	—	RW1C
0x21	TEMP_INT_MASK0	Name	—	—	—	—	—	THERM125M	—	THERM110M
		Reset	0	0	0	0	1	1	1	1
		Type	—	—	—	—	—	RW	—	RW
0x22	TEMP_INT_SENSE0	Name	—	—	—	—	—	THERM125S	—	THERM110S
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	R	—	R
0x24	ONKEY_INT_STAT0	Name	—	—	ONKEY_8SI	ONKEY_4SI	ONKEY_3SI	ONKEY_2SI	ONKEY_1SI	ONKEY_PUSHI
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x25	ONKEY_INT_MASK0	Name	—	—	ONKEY_8SM	ONKEY_4SM	ONKEY_3SM	ONKEY_2SM	ONKEY_1SM	ONKEY_PUSHM
		Reset	0	0	1	1	1	1	1	1
		Type	—	—	RW	RW	RW	RW	RW	RW
0x26	ONKEY_INT_SENSE0	Name	—	—	ONKEY_8SS	ONKEY_4SS	ONKEY_3SS	ONKEY_2SS	ONKEY_1SS	ONKEY_PUSHS
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	R	R	R	R	R	R
0x28	MISC_INT_STAT0	Name	—	—	—	SYS_OVLO_I	LOW_SYS_WARN_I	PWRON_I	PWRDN_I	PWRUP_I
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW1C	RW1C	RW1C	RW1C	RW1C
0x29	MISC_INT_MASK0	Name	—	—	—	SYS_OVLO_M	LOW_SYS_WARN_M	PWRON_M	PWRDN_M	PWRUP_M
		Reset	0	0	0	1	1	1	1	1
		Type	—	—	—	RW	RW	RW	RW	RW
0x2A	MISC_INT_SENSE0	Name	—	—	—	SYS_OVLO_S	LOW_SYS_WARN_S	PWRON_S	PWRDN_S	PWRUP_S
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	R	R	R	R	R
0x30	COINCELL_CONTROL	Name				COINCHEN	VCOIN[3:0]			
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW	RW	RW	RW	RW
0x32	SW1_VOLT	Name	—	—	SW1_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x33	SW1_STBY_VOLT	Name	—	—	SW1_STBY_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x34	SW1_SLP_VOLT	Name	—	—	SW1_SLP_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x35	SW1_CTRL	Name	SW1_RDIS_ENB	SW1_FPWM	SW1_FPWM_IN_DVS	SW1_DVSSPEED	SW1_LPWR	SW1_OMODE	SW1_STBY_EN	SW1_EN
		Reset	0	0	0	0	0	0	0	0
		Type	RW1S	RW	RW	RW1S	RW	RW	RW1S	RW1S

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Table 174. Register PMIC bitmap*...continued*

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
0x36	SW1_CTRL1	Name	—	—	—	SW1_TMODE_SEL	—	—	SW1_ILIM[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW	—	—	RW1S	RW1S
0x38	SW2_VOLT	Name	—	—	SW2_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x39	SW2_STBY_VOLT	Name	—	—	SW2_STBY_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x3A	SW2_SLP_VOLT	Name	—	—	SW2_SLP_VOLT[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x3B	SW2_CTRL	Name	SW2_RDIS_ENB	SW2_FPWM	SW2_FPWM_IN_DVS	SW2_DVSSPEED	SW2_LPWR	SW2_OMODE	SW2_STBY_EN	SW2_EN
		Reset	0	0	0	0	0	0	0	0
		Type	RW1S	RW	RW	RW1S	RW	RW	RW1S	RW1S
0x3C	SW2_CTRL1	Name	—	—	—	SW2_TMODE_SEL	—	—	SW2_ILIM[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW	—	—	RW1S	RW1S
0x3E	SW3_VOLT	Name	—	—	—	—	SW3_VOLT[3:0]			
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW1S	RW1S	RW1S	RW1S
0x3F	SW3_STBY_VOLT	Name	—	—	—	—	SW3_STBY_VOLT[3:0]			
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW1S	RW1S	RW1S	RW1S
0x40	SW3_SLP_VOLT	Name	—	—	—	—	SW3_SLP_VOLT[3:0]			
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW1S	RW1S	RW1S	RW1S
0x41	SW3_CTRL	Name	SW3_RDIS_ENB	SW3_FPWM	—	SW3_DVSSPEED	SW3_LPWR	SW3_OMODE	SW3_STBY_EN	SW3_EN
		Reset	0	0	0	0	0	0	0	0
		Type	RW1S	RW	—	RW1S	RW	RW	RW1S	RW1S
0x42	SW3_CTRL1	Name	—	—	—	SW3_TMODE_SEL	—	—	SW3_ILIM[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW	—	—	RW1S	RW1S
0x48	VSNVS_CTRL	Name	—	—	LIBGDIS	FORCEBOS	CLKPULSE	VSNVS_VOLT[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	RW	RW	RW	RW1S	RW1S	RW1S
0x4A	VREFDDR_CTRL	Name	—	—	—	—	VREFDDR_LPWR	VREFDDR_OMODE	VREFDDR_STBY_EN	VREFDDR_EN
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW	RW	RW1S	RW1S
0x4C	LDO1_VOLT	Name	—	—	—	LDO1_VOLT[4:0]				
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW1S	RW1S	RW1S	RW1S	RW1S
0x4D	LDO1_CTRL	Name	—	—	—	LDO1_LS_EN	LDO1_LPWR	LDO1_OMODE	LDO1_STB Y_EN	VLDO1_EN
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW1S	RW	RW	RW1S	RW1S
0x4F	LDO2_VOLT	Name	—	—	—	—	LDO2_VOLT[3:0]			
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW1S	RW1S	RW1S	RW1S
0x50	LDO2_CTRL	Name	—	—	—	—	LDO2_LPWR	LDO2_OMODE	LDO2_STB Y_EN	VLDO2_EN
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW	RW	RW1S	RW1S
0x52	LDO3_VOLT	Name	—	—	—	LDO3_VOLT[4:0]				
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	RW1S	RW1S	RW1S	RW1S	RW1S
0x53	LDO3_CTRL	Name	—	—	—	LDO3_LS_EN	LDO3_LPWR	LDO3_OMODE	LDO3_STB Y_EN	VLDO3_EN
		Reset	0	0	0	0	0	0	0	0

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Table 174. Register PMIC bitmap*...continued*

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
		Type	—	—	—	RW1S	RW	RW	RW1S	RW1S
0x58	PWRCTRL0	Name	TGRESET[7:6]		POR_DLY[5:3]			STANDBYINV	STANDBYDLY[1:0]	
		Reset	0	0	0	0	0	0	0	1
		Type	RW1S	RW1S	RW1S	RW1S	RW1S	RW	RW	RW
0x59	PWRCTRL1	Name	ONKEY_RST_EN	REGSCPEN	RESTARTEN	PWRONRSTEN	ONKEYDBNC[3:2]		PWRONDBNC[1:0]	
		Reset	1	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW
015A	PWRCTRL2	Name	—	—	—	—	LOW_SYS_WARN[3:2]		UVDET[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	RW	RW	RW1S	RW1S
0x5B	PWRCTRL3	Name	—						GOTO_CORE_OFF	GOTO_SHIP
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW
0x5F	SW1_PWRDN_SEQ	Name	—	—	—	—	—	SW1_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x60	SW2_PWRDN_SEQ	Name	—	—	—	—	—	SW2_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x61	SW3_PWRDN_SEQ	Name	—	—	—	—	—	SW3_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x62	LDO1_PWRDN_SEQ	Name	—	—	—	—	—	LDO1_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x63	LDO2_PWRDN_SEQ	Name	—	—	—	—	—	LDO2_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x64	LDO3_PWRDN_SEQ	Name	—	—	—	—	—	LDO3_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x65	VREFDDR_PWRDN_SEQ	Name	—	—	—	—	—	VREFDDR_PWRDN_SEQ[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW1S	RW1S	RW1S
0x67	STATE_INFO	Name	—	—	STATE[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	R	R	R	R	R	R
0x68	I2C_ADDR	Name	USE_DEFAULT_ADDR	—	—	—	—	I2C_SLAVE_ADDR_LSBS[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	RW	—	—	—	—	R	R	R
0x69	IO_DRV0	Name	—	—	—	—	—	—	—	—
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW
0x6A	IO_DRV1	Name	—	—	—	—	—	—	—	—
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	—	RW	RW
0x6B	RC_16MHZ	Name	—	—	—	—	—	REQ_ACORE_HIPWR	REQ_ACORE_ON	REQ_16MHZ
		Reset	0	0	0	0	0	0	0	0
		Type	—	—	—	—	—	RW	RW	RW
0x6F	KEY1	Name	KEY1[7:0]							
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW

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12.4 Register charger bitmap

CHGPOK_RSTB [1]

VCOREDIG_RSTB [2]

[1] Bits reset by invalid VBUSIN
[2] Bits reset by invalid VCOREDIG

Table 175. Register charger bitmap

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
0x00	CHG_INT	Name	THM_I	VBUS_DPM_I	VBUS_I	RSVD4	CHG_I	BAT_I	BAT2SOC_I	SUP_I
		Reset	0	0	0	0	0	0	0	0
		Type	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
0x02	CHG_INT_MASK	Name	THM_M	VBUS_DPM_M	VBUS_M	RSVD4	CHG_M	BAT_M	BAT2SOC_M	SUP_M
		Reset	1	1	1	1	1	1	1	1
		Type	RW	RW	RW	RW	RW	RW	RW	RW
0x04	CHG_INT_OK	Name	THM_OK	VBUS_DPM_OK	VBUS_OK	RSVD4	CHG_OK	BAT_OK	BAT2SOC_OK	SUP_OK
		Reset	1	0	0	0	0	1	0	0
		Type	R	R	R	R	R	R	R	R
0x06	VBUS_SNS	Name	VBUS_DPM_SNS	RSVD6	VBUS_VALID_SNS	VBUS_OVLO_SNS	VBUS_IN2SYS_SNS	VBUS_UVLO_SNS	RSVD0[1:0]	
		Reset	0	0	0	0	1	1	0	0
		Type	R	R	R	R	R	R	R	R
0x07	CHG_SNS	Name	TREG_SNS	THM_SNS	WDT_SNS	RSVD4	CHG_SNS[3:0]			
		Reset	0	0	0	0	1	0	0	0
		Type	R	R	R	R	R	R	R	R
0x08	BATT_SNS	Name	RSVD6[7:6]		BATTOC_SNS	RSVD3[4:3]		BATT_SNS[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	R	RW	RW	R	R	R
0x09	CHG_OPER	Name	RSVD5[7:5]			DISBATFET	WDTEN	RSVD2	CHG_OPER[1:0]	
		Reset	0	0	0	0	0	0	0	1
		Type	RW	RW	RW	RW	RW	RW	RW1S	RW1S
0x0A	CHG_TMR	Name	TPRECHG	RSVD6	EOCTIME[5:3]FCHGTIME[2:0]					
		Reset	0	0	0	0	1	0	1	0
		Type	RW1S	R	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x0D	CHG_EOC_CNFG	Name	EOC_MODE	IEOC[6:4]			EOC_EXIT	FORCE_BATT_ISO	CHG_RESTART[1:0]	
		Reset	0	1	0	0	0	0	0	1
		Type	RW1S	RW	RW	RW	RW1S	RW1S	RW1S	RW1S
0x0E	CHG_CURR_CNFG	Name	RSVD7	PRECHGLB_THRSH[6:5]		CHG_CC[4:0]				
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x0F	BATT_REG	Name	MINVSYS[7:6]		CHGCV[5:0]					
		Reset	0	0	1	0	1	0	1	1
		Type	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x11	BATFET_CNFG	Name	BOVRC_NOVBUS	WD_TIME	BATFET_OC[5:4]		BOVRC_DISBATFET	WD_BATFET_OFF	WDTCLR[1:0]	
		Reset	0	0	1	1	0	0	0	0
		Type	RW	RW	RW1S	RW1S	RW1S	RW	RW	RW
0x12	THM_REG_CNFG	Name	TEMP_FB_EN	RSVD6	THM_HOT	THM_COLD	REGTEMP[3:2]		THM_CNFG[1:0]	
		Reset	0	0	0	0	0	1	0	1
		Type	RW1S	RW	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x14	VBUS_INLIM_CNFG	Name	VBUS_LIN_ILIM[7:3]					RSVD0[2:0]		
		Reset	0	1	1	0	1	0	0	0
		Type	RW1S	RW1S	RW1S	RW1S	RW1S	RW	RW	RW
0x15	VBUS_LIN_DPM	Name	FET_SCALE	RSVD6	VIN_DPM_STOP	PRECHGDBATT_THRSH[4:3]		VBUS_DPM_REG[2:0]		
		Reset	0	0	0	0	0	0	0	0
		Type	RW1S	R	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S

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Table 175. Register charger bitmap*...continued*

Address	Register name		BITS[7:0]							
			7	6	5	4	3	2	1	0
0x16	USB_PHY_LDO_CNFG	Name	RSVD6[7:6]		RSVD4[5:4]		RSVD3	USBPHYLDO	USBPHY	ACTDISPHY
		Reset	0	0	0	0	0	0	0	1
		Type	RW	RW	RW	RW	RW	RW1S	RW1S	RW1S
0x18	DBNC_DELAY_TIME	Name	RSVD6[7:6]		SYS_WKUP_DLY[5:4]		USB_PHY_TDB[3:2]		VBUS_OV_TDB[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x19	CHG_INT_CNFG	Name	RSVD2[7:2]						EOC_INT	CHG_INT_GEN
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW1S	RW1S
0x1A	THM_ADJ_SETTING	Name	RSVD6[7:6]		CC_ADJ[5:4]		CV_ADJ[3:2]		THM_COOL	THM_WARM
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x1B	VBUS2SYS_CNFG	Name	RSVD3[7:3]					VBUS2SYS_ THRSH	VBUS2SYS_TDB[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW1S	RW1S	RW1S
0x1C	LED_PWM	Name	LED_EN	LED_RAMP	LED_PWM[5:0]					
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW
0x1D	FAULT_BATFET_CNFG	Name	CTRL_CHGR_BETA_SEL[7:6]		RSVD5	TMRFLT_BFET_ EN	TSHDN_BFET_ EN	THMSUS_ BFET_EN	WDFLT_ BFEET_EN	OVFLT_BFEET_ EN
		Reset	0	0	0	0	0	0	0	0
		Type	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
0x1E	LED_CNFG	Name	RSVD4[7:6]		LEDOVRD	LED_CFG	LED_CURRENT[3:2]		LED_FREQ[1:0]	
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW1S	RW1S	RW1S	RW	RW
0x1F	CHGR_KEY2	Name	CHGR_KEY2[7:0]							
		Reset	0	0	0	0	0	0	0	0
		Type	RW	RW	RW	RW	RW	RW	RW	RW

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12.5 Register OTP bitmap

Table 176. Register OTP bitmap

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
0x1C	**OTP_PMIC_ CFG0**			UNUSED	UNUSED	UNUSED	OTP_PWRGD_ EN	OTP_SEQ_ CLK_SPEED	OTP_PWRON_ CFG	
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x04	0	0	0	0	0	1	0	0
	A3	0x04	0	0	0	0	0	1	0	0
	A4	0x04	0	0	0	0	0	1	0	0
	A5	0x04	0	0	0	0	0	1	0	0
	A6	0x04	0	0	0	0	0	1	0	0
	A7	0x04	0	0	0	0	0	1	0	0
	A8	0x04	0	0	0	0	0	1	1	0
	A9	0x04	0	0	0	0	0	1	0	0
0x1D	**OTP_SW1**		OTP_SW1_ DVSSPEED	OTP_SW1_RDIS_ ENB	OTP_SW1_VOLT[5:0]					
	A1 (Default)	0x80	1	0	0	0	0	0	0	0
	A2	0xA0	1	0	1	0	0	0	0	0
	A3	0XBF	1	0	1	1	1	1	1	1
	A4	0XA8	1	0	1	0	1	0	0	0
	A5	0XBF	1	0	1	1	1	1	1	1
	A6	0XB6	1	0	1	1	0	1	1	0
	A7	0XBF	1	0	1	1	1	1	1	1
	A8	0XBF	1	0	1	1	1	1	1	1
	A9	0XBF	1	0	1	1	1	1	1	1
0x1E	**OTP_SW1_SW2**		OTP_SW2_VOLT[5:0]						OTP_SW1_ DVS_SEL	OTP_SW1_ EN_AND_ STBY_EN
	A1 (Default)	0XA3	1	0	1	0	0	0	1	1
	A2	0x05	0	0	0	0	0	1	0	1
	A3	0x09	0	0	0	0	1	0	0	1
	A4	0xC1	1	1	0	0	0	0	0	1
	A5	0x0D	0	0	0	0	1	1	0	1
	A6	0x09	0	0	0	0	1	0	0	1
	A7	0x05	0	0	0	0	0	1	0	1
	A8	0x09	0	0	0	0	1	0	0	1
	A9	0xFF	1	1	1	1	1	1	1	1
0x1F	**OTP_SW2_SW3**		OTP_SW3_VOLT[3:0]				OTP_SW2_ DVS_SEL	OTP_SW2_ EN_AND_ STBY_EN	OTP_SW2_ DVSSPEED	OTP_SW2_ RDIS_ENB
	A1 (Default)	0x04	0	0	0	0	0	1	0	0
	A2	0x0E	0	0	0	0	1	1	1	0
	A3	0xFE	1	1	1	1	1	1	1	0
	A4	0x06	0	0	0	0	0	1	1	0
	A5	0xFE	1	1	1	1	1	1	1	0
	A6	0xFE	1	1	1	1	1	1	1	0
	A7	0x0E	0	0	0	0	1	1	1	0
	A8	0xFE	1	1	1	1	1	1	1	0
	A9	0xCE	1	1	0	0	1	1	1	0
0x20	**OTP_SW3__ SWxILIM**		OTP_SW3_ILIM[1:0]		OTP_SW2_ILIM[1:0]		OTP_SW1_ILIM[1:0]		OTP_SW3_ EN_AND_ STBY_EN	OTP_SW3_ RDIS_ENB
	A1 (Default)	0XFE	1	1	1	1	1	1	1	0
	A2	0xFE	1	1	1	1	1	1	1	0
	A3	0xFE	1	1	1	1	1	1	1	0
	A4	0xFE	1	1	1	1	1	1	1	0
	A5	0xFE	1	1	1	1	1	1	1	0
	A6	0xFE	1	1	1	1	1	1	1	0
	A7	0xFE	1	1	1	1	1	1	1	0
	A8	0xFE	1	1	1	1	1	1	1	0
	A9	0xFE	1	1	1	1	1	1	1	0

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Table 176. Register OTP bitmap*...continued*

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
0x21	**OTP_VREF_LDO1**		OTP_LDO1_LS_EN	OTP_LDO1_VOLT[4:0]					OTP_VREFDDREN_AND_STBY_EN	UNUSED
	A1 (Default)	0x16	0	0	0	1	0	1	1	0
	A2	0x42	0	1	0	0	0	0	1	0
	A3	0x42	0	1	0	0	0	0	1	0
	A4	0x7E	0	1	1	1	1	1	1	0
	A5	0x42	0	1	0	0	0	0	1	0
	A6	0x42	0	1	0	0	0	0	1	0
	A7	0x7E	0	1	1	1	1	1	1	0
	A8	0x42	0	1	0	0	0	0	1	0
	A9	0x6A	0	1	1	0	1	0	1	0
0x22	**OTP_LDO1_LDO2**		UNUSED	OTP_LDO2_EN_AND_STBY_EN	UNUSED	OTP_LDO2_VOLT[3:0]				OTP_LDO1_EN_AND_STBY_EN
	A1 (Default)	0x4F	0	1	0	0	1	1	1	1
	A2	0x5F	0	1	0	1	1	1	1	1
	A3	0x5F	0	1	0	1	1	1	1	1
	A4	0x5F	0	1	0	1	1	1	1	1
	A5	0x5F	0	1	0	1	1	1	1	1
	A6	0x5F	0	1	0	1	1	1	1	1
	A7	0x5F	0	1	0	1	1	1	1	1
	A8	0x5F	0	1	0	1	1	1	1	1
	A9	0x5F	0	1	0	1	1	1	1	1
0x23	**OTP_LDO3**		UNUSED	OTP_LDO3_EN_AND_STBY_EN	OTP_LDO3_LS_EN	OTP_LDO3_VOLT[4:0]				
	A1 (Default)	0x65	0	1	1	0	0	1	0	1
	A2	0x50	0	1	0	1	0	0	0	0
	A3	0x5F	0	1	0	1	1	1	1	1
	A4	0x50	0	1	0	1	0	0	0	0
	A5	0x5F	0	1	0	1	1	1	1	1
	A6	0x5F	0	1	0	1	1	1	1	1
	A7	0x5F	0	1	0	1	1	1	1	1
	A8	0x5F	0	1	0	1	1	1	1	1
	A9	0x50	0	1	0	1	0	0	0	0
0x24	**OTP_PMIC_CFG1**		UNUSED	OTP_UVDET[1:0]		OTP_POR_DLY[2:0]			OTP_TGRESET[1:0]	
	A1 (Default)	0x40	0	1	0	0	0	0	0	0
	A2	0x40	0	1	0	0	0	0	0	0
	A3	0x40	0	1	0	0	0	0	0	0
	A4	0x40	0	1	0	0	0	0	0	0
	A5	0x40	0	1	0	0	0	0	0	0
	A6	0x40	0	1	0	0	0	0	0	0
	A7	0x40	0	1	0	0	0	0	0	0
	A8	0x40	0	1	0	0	0	0	0	0
	A9	0x40	0	1	0	0	0	0	0	0
0x25	**OTP_SW1_SW2_SEQ**		UNUSED	UNUSED	OTP_SW2_PWRUP_SEQ[2:0]			OTP_SW1_PWRUP_SEQ[2:0]		
	A1 (Default)	0x11	0	0	0	1	0	0	0	1
	A2	0x2D	0	0	1	0	1	1	0	1
	A3	0x1B	0	0	0	1	1	0	1	1
	A4	0x1C	0	0	0	1	1	1	0	0
	A5	0x1B	0	0	0	1	1	0	1	1
	A6	0x1B	0	0	0	1	1	0	1	1
	A7	0x1B	0	0	0	1	1	0	1	1
	A8	0x1B	0	0	0	1	1	0	1	1
	A9	0x1B	0	0	0	1	1	0	1	1
0x26	**OTP_SW3_LDO1_SEQ**		UNUSED	UNUSED	OTP_LDO1_PWRUP_SEQ[2:0]			OTP_SW3_PWRUP_SEQ[2:0]		
	A1 (Default)	0x23	0	0	1	0	0	0	1	1

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Table 176. Register OTP bitmap*...continued*

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
	A2	0x09	0	0	0	0	1	0	0	1
	A3	0x1B	0	0	0	1	1	0	1	1
	A4	0x0A	0	0	0	0	1	0	1	0
	A5	0x1B	0	0	0	1	1	0	1	1
	A6	0x1B	0	0	0	1	1	0	1	1
	A7	0x1B	0	0	0	1	1	0	1	1
	A8	0x1B	0	0	0	1	1	0	1	1
	A9	0x1B	0	0	0	1	1	0	1	1
0x27	**OTP_LDO2_ LDO3_SEQ**		UNUSED	UNUSED	OTP_LDO3_PWRUP_SEQ[2:0]			OTP_LDO2_PWRUP_SEQ[2:0]		
	A1 (Default)	0x2C	0	0	1	0	1	1	0	0
	A2	0x09	0	0	0	0	1	0	0	1
	A3	0x1A	0	0	0	1	1	0	1	0
	A4	0x0A	0	0	0	0	1	0	1	0
	A5	0x1A	0	0	0	1	1	0	1	0
	A6	0x1A	0	0	0	1	1	0	1	0
	A7	0x1A	0	0	0	1	1	0	1	0
	A8	0x1A	0	0	0	1	1	0	1	0
	A9	0x1B	0	0	0	1	1	0	1	1
0x28	**OTP_PMIC_ CFG2**		OTP_SHIP_ COREOFF_CYA	OTP_I2C_SLV_ADDR[2:0]			OTP_I2C_ DEGLITCH_EN[0]	OTP_VREFDDR_PWRUP_SEQ[2:0]		
	A1 (Default)	0x05	0	0	0	0	0	1	0	1
	A2	0x05	0	0	0	0	0	1	0	1
	A3	0x03	0	0	0	0	0	0	1	1
	A4	0x03	0	0	0	0	0	0	1	1
	A5	0x03	0	0	0	0	0	0	1	1
	A6	0x03	0	0	0	0	0	0	1	1
	A7	0x03	0	0	0	0	0	0	1	1
	A8	0x03	0	0	0	0	0	0	1	1
	A9	0x03	0	0	0	0	0	0	1	1
0x29	**RSVD**		UNUSED	UNUSED	UNUSED	UNUSED	Reserved (OTP_VSNVS_VOLT[2:0])			Reserved (OTP_FORCE_ LICELL)
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x2A	**RSVD**		OTP_PMIC_SPARE0[7:0]							
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x2B	**OTP_CHG_CFG0**		Reserved (OTP_ CHGR_ THM_WARM)	Reserved (OTP_ CHGR_ THM_COOL)	OTP_CHGR_EOCTIME[2:0]			OTP_CHGR_ TPRECHG	OTP_CHGR_OPER[1:0]	
	A1 (Default)	0x02	0	0	0	0	0	0	1	0
	A2	0x01	0	0	0	0	0	0	0	1
	A3	0x02	0	0	0	0	0	0	1	0
	A4	0x02	0	0	0	0	0	0	1	0
	A5	0x02	0	0	0	0	0	0	1	0
	A6	0x01	0	0	0	0	0	0	0	1

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Table 176. Register OTP bitmap*...continued*

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
	A7	0x02	0	0	0	0	0	0	1	0
	A8	0x02	0	0	0	0	0	0	1	0
	A9	0x01	0	0	0	0	0	0	0	1
0x2C	**OTP_CHG_CFG1**		OTP_CHGR_CHG_RESTART[1:0]		Reserved (OTP_CHGR_FORCE_BATT_ISO)	Reserved (OTP_CHGR_EOC_EXIT)	Reserved (OTP_CHGR_EOC_MODE)	OTP_CHGR_FCHGTIME[2:0]		
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x2D	**OTP_CHG_CFG2**		OTP_CHGR_VSYSMIN[1:0]		OTP_CHGR_CHG_CC[4:0]					OTP_CHGR_TEMPFB_EN
	A1 (Default)	0x80	1	0	0	0	0	0	0	0
	A2	0x80	1	0	0	0	0	0	0	0
	A3	0x80	1	0	0	0	0	0	0	0
	A4	0x90	1	0	0	1	0	0	0	0
	A5	0x80	1	0	0	0	0	0	0	0
	A6	0x40	0	1	0	0	0	0	0	0
	A7	0x80	1	0	0	0	0	0	0	0
	A8	0x80	1	0	0	0	0	0	0	0
	A9	0x40	0	1	0	0	0	0	0	0
0x2E	**OTP_CHG_CFG3**		OTP_CHGR_BATFET_OC[1:0]		OTP_CHGR_CHGCV[5:0]					
	A1 (Default)	0x2B	0	0	1	0	1	0	1	1
	A2	0x2B	0	0	1	0	1	0	1	1
	A3	0x2B	0	0	1	0	1	0	1	1
	A4	0x2B	0	0	1	0	1	0	1	1
	A5	0x2B	0	0	1	0	1	0	1	1
	A6	0x2B	0	0	1	0	1	0	1	1
	A7	0x2B	0	0	1	0	1	0	1	1
	A8	0x2B	0	0	1	0	1	0	1	1
	A9	0x2B	0	0	1	0	1	0	1	1
0x2F	**OTP_CHG_CFG4**		UNUSED	OTP_CHGR_THM_CNFG[1:0]		OTP_CHGR_REGTEMP[1:0]		OTP_CHGR_THM_COLD	OTP_CHGR_THM_HOT	OTP_CHGR_BOVRC_DISBATFET
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x30	**OTP_CHG_CFG5**		UNUSED	UNUSED	OTP_CHGR_VIN_DPM_STOP	OTP_CHGR_VBUS_LIN_ILIM[4:0]				
	A1 (Default)	0x0E	0	0	0	0	1	1	1	0
	A2	0x14	0	0	0	1	0	1	0	0
	A3	0x14	0	0	0	1	0	1	0	0
	A4	0x14	0	0	0	1	0	1	0	0
	A5	0x14	0	0	0	1	0	1	0	0
	A6	0x14	0	0	0	1	0	1	0	0
	A7	0x14	0	0	0	1	0	1	0	0
	A8	0x14	0	0	0	1	0	1	0	0
	A9	0x14	0	0	0	1	0	1	0	0

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Table 176. Register OTP bitmap*...continued*

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
0x31	**OTP_CHG_CFG6**		OTP_CHGR_SYS_WKUP_DLY[1:0]		OTP_CHGR_ACTDISPHY	OTP_CHGR_USBPHY	OTP_CHGR_USBPHYLDO	OTP_CHGR_VBUS_DPM_REG[2:0]		
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x28	0	0	1	0	1	0	0	0
	A3	0x28	0	0	1	0	1	0	0	0
	A4	0x2E	0	0	1	0	1	1	1	0
	A5	0x28	0	0	1	0	1	0	0	0
	A6	0x28	0	0	1	0	1	0	0	0
	A7	0x28	0	0	1	0	1	0	0	0
	A8	0x28	0	0	1	0	1	0	0	0
	A9	0x28	0	0	1	0	1	0	0	0
0x32	**OTP_CHG_CFG7**		OTP_CHGR_CC_ADJ[1:0]		OTP_CHGR_CHG_INT_EN	OTP_CHGR_EOC_INT	OTP_CHGR_VBUS_OV_TDB[1:0]		Reserved (OTP_CHGR_USB_PHY_TDB[1:0])	
	A1 (Default)	0x04	0	0	0	0	0	1	0	0
	A2	0x04	0	0	0	0	0	1	0	0
	A3	0x04	0	0	0	0	0	1	0	0
	A4	0x14	0	0	0	1	0	1	0	0
	A5	0x04	0	0	0	0	0	1	0	0
	A6	0x04	0	0	0	0	0	1	0	0
	A7	0x04	0	0	0	0	0	1	0	0
	A8	0x04	0	0	0	0	0	1	0	0
	A9	0x04	0	0	0	0	0	1	0	0
0x33	**OTP_CHG_CFG8**		UNUSED	OTP_CHGR_LED_CURRENT[1:0]		OTP_CHGR_VBUS2SYS_TDB[1:0]		OTP_CHGR_VBUS2SYS_THRSH	OTP_CHGR_CV_ADJ[1:0]	
	A1 (Default)	0x28	0	0	1	0	1	0	0	0
	A2	0x28	0	0	1	0	1	0	0	0
	A3	0x28	0	0	1	0	1	0	0	0
	A4	0x28	0	0	1	0	1	0	0	0
	A5	0x28	0	0	1	0	1	0	0	0
	A6	0x28	0	0	1	0	1	0	0	0
	A7	0x28	0	0	1	0	1	0	0	0
	A8	0x28	0	0	1	0	1	0	0	0
	A9	0x28	0	0	1	0	1	0	0	0
0x34	**OTP_CHG_CFG9**		OTP_CHGR_LED_CNFG	OTP_CHGR_OVFLT_BFET_EN	OTP_CHGR_WDFLT_BFET_EN	OTP_CHGR_THMSUS_BFET_EN	OTP_CHGR_TSHDN_BFET_EN	OTP_CHGR_TMRFLT_BFET_EN	Reserved (OTP_CHGR_BETA_SEL[1:0])	
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x35	**OTP_CHG_CFG10**		UNUSED	UNUSED	UNUSED	Reserved (OTP_CHGR_FET_SCALE)	Reserved (OTP_CHGR_PRECHG_LOWBATT_THRSH[1:0])		OTP_CHGR_PRECHG_LOWBATT_THRSH[1:0]	
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x36	**RSVD**		OTP_CHGR_SPARE0[7:0]							
	A1 (Default)	0x00	0	0	0	0	0	0	0	0
	A2	0x00	0	0	0	0	0	0	0	0

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Table 176. Register OTP bitmap*...continued*

Address	Register name	Value	BIT[7:0]							
			7	6	5	4	3	2	1	0
	A3	0x00	0	0	0	0	0	0	0	0
	A4	0x00	0	0	0	0	0	0	0	0
	A5	0x00	0	0	0	0	0	0	0	0
	A6	0x00	0	0	0	0	0	0	0	0
	A7	0x00	0	0	0	0	0	0	0	0
	A8	0x00	0	0	0	0	0	0	0	0
	A9	0x00	0	0	0	0	0	0	0	0
0x37	**OTP_CRC_LSB**		CRC[1]LSB	—	—	—	—	—	—	—
	A1 (Default)	0xB5	1	0	1	1	0	1	0	1
	A2	0xB5	1	0	1	1	0	1	0	1
	A3	0xB5	1	0	1	1	0	1	0	1
	A4	0xB5	1	0	1	1	0	1	0	1
	A5	0xB5	1	0	1	1	0	1	0	1
	A6	0xB5	1	0	1	1	0	1	0	1
	A7	0xB5	1	0	1	1	0	1	0	1
	A8	0xB5	1	0	1	1	0	1	0	1
	A9	0xB5	1	0	1	1	0	1	0	1

13 Application details

13.1 Example schematic

Figure 28 shows a typical schematic of the PF1550 with key external components.

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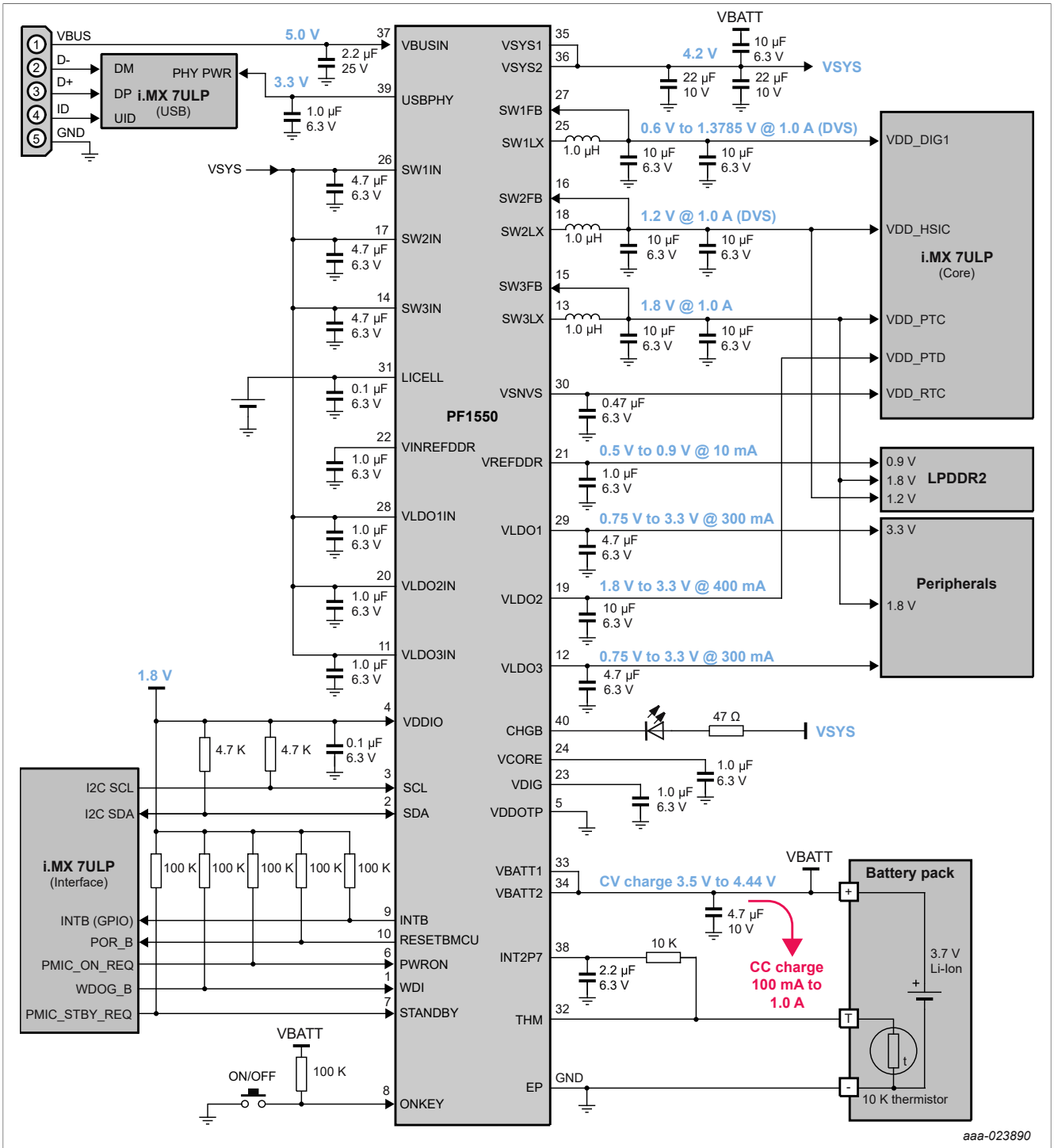

Figure 28. Typical schematic

13.2 Bill of materials

The following table shows an example bill of materials to be used with the PF1550.

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Table 177. Bill of materials

Block	Function	Description	Qty
VCORE	Analog IC supply	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
VDIG	Digital IC supply	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
INT2P7	Charger analog supply	CAP CER 2.2 µF 6.3 V 20% X5R 0201	1
USBPHY	USB PHY output capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
VBUSIN	VBUSIN bypass capacitor	CAP CER 2.2 µF 25 V 20 % X5R 0402	1
VSYS	VSYS capacitor	22 µF, 10 V, MLCC, X5R	2
VBATT	Bypass capacitor between VBATT and VSYS [1]	10 µF, 6.3 V, MLCC, X5R	1
VDDIO	VDDIO bypass capacitor	CAP CER 0.1 uF 6.3 V 20 % X5R 0201	1
THM	Thermistor bias resistor	10 kOhm, 0201	1
Buck 1	BUCK1 inductor	1.0 µH, +/−20 %, 120 mOhm typ, 1700 mA	1
	BUCK1 input capacitor	4.7 µF, 6.3 V, MLCC, X5R	1
	BUCK1 output capacitor	10 µF, 6.3 V, MLCC, X5R	2
Buck 2	BUCK2 inductor	1.0 µH, +/−20 %, 120 mOhm typ, 1700 mA	1
	BUCK2 input capacitor	4.7 µF, 6.3 V, MLCC, X5R	1
	BUCK2 output capacitor	10 µF, 6.3V, MLCC, X5R	2
Buck 3	BUCK3 inductor	1.0 µH, +/-20 %, 120 mOhm typ, 1700 mA	1
	BUCK3 input capacitor	4.7 µF, 6.3 V, MLCC, X5R	1
	BUCK3 output capacitor	10 µF, 6.3 V, MLCC, X5R	2
LDO1	LDO1 input capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
	LDO1 output capacitor	4.7 µF, 6.3 V, MLCC, X5R	1
LDO2	LDO2 input capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
	LDO2 output capacitor	10 µF, 6.3 V, MLCC, X5R	1
LDO3	LDO3 input capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
	LDO3 output capacitor	4.7 µF, 6.3 V, MLCC, X5R	1
VREFDDR	VREFDDR input capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
	VREFDDR output capacitor	CAP CER 1.0 µF 6.3 V 20 % X5R 0201	1
VSNVS	VSNVS output capacitor	CAP CER 0.47 µF 6.3 V 20 % X5R 0201	1
LICELL	LICELL bypass capacitor	CAP CER 0.1 µF 6.3 V 20 % X5R 0201	1

[1] ONLY for < 20mA EOC current threshold settings and to allow a smooth transition from CV to EOC state

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13.3 PF1550 layout guidelines

13.3.1 General board recommendations

- It is recommended to use an eight layer board stack-up arranged as follows:
  - High current signal
  - GND
  - Signal
  - Power
  - Power
  - Signal
  - GND
- Allocate TOP and BOTTOM PCB layers for POWER ROUTING (high current signals), copper-pour the unused area.
- Use internal layers sandwiched between two GND planes for the SIGNAL routing.

13.3.2 Component placement

It is desirable to keep all component related to the power stage as close to the PMIC as possible, specially decoupling input and output capacitors.

13.3.3 General routing requirements

- Some recommended things to keep in mind for manufacturability:
  - Via in pads require a 4.5 mil minimum annular ring. Pad must be 9.0 mils larger than the hole
  - Maximum copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
  - Minimum allowed spacing between line and hole pad is 3.5 mils
  - Minimum allowed spacing between line and line is 3.0 mils
- Care must be taken with SWxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high-power signals, like the ones on the SWxIN, SWxLX. They could be also shielded.
- Shield feedback traces of the regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
- Avoid coupling traces between important signal/low noise supplies (like VCORE, VDIG) from any switching node (for example, SW1LX, SW2LX, SW3LX).
- Make sure that all components related to a specific block are referenced to the corresponding ground.

13.3.4 Parallel routing requirements

- I^2C signal routing
  - CLK is the fastest signal of the system, so it must be given special care.
  - To avoid contamination of these delicate signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on

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adjacent layers. Make sure that the ground plane is uniform throughout the whole signal trace length.

– These signals can be placed on an outer layer of the board to reduce their capacitance with respect to the ground plane.
– Care must be taken with these signals not to contaminate analog signals, as they are high frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

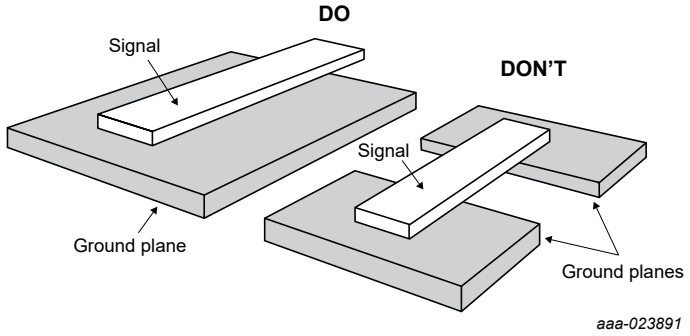

Figure 29. Recommended shielding for critical signals

13.3.5 Switching regulator layout recommendations

- Per design, the switching regulators in PF1550 are designed to operate with only one input bulk capacitor. However, it is recommended to add a high frequency filter input capacitor (CIN_hf), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
- Make high-current ripple traces low-inductance (short, high W/L ratio).
- Make high-current traces wide or copper islands.

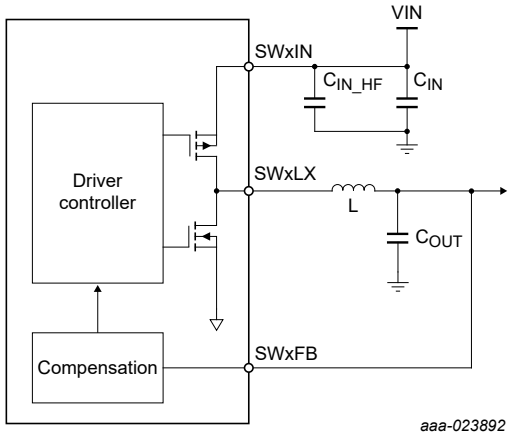

Figure 30. Generic buck regulator architecture

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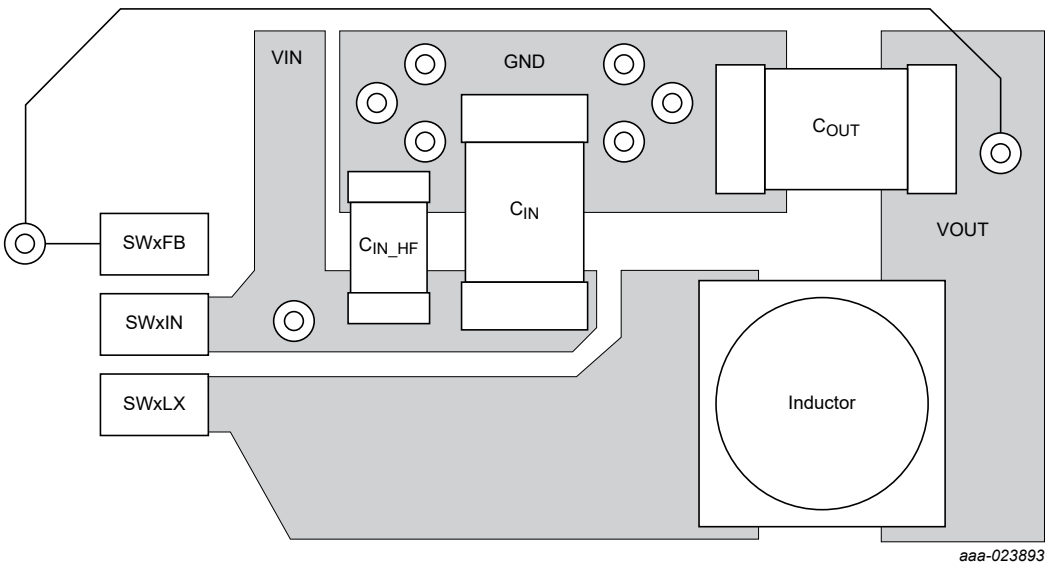

Figure 31. Layout example for buck regulators

13.4 Thermal information

13.4.1 Rating data

The thermal rating data of the packages has been simulated with the results listed in Table 3 .

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) is used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, continues to be commonly used.

The JEDEC standards can be consulted at http://www.jedec.org/.

13.4.2 Estimation of junction temperature

An estimation of the chip junction temperature T_J can be obtained from the equation: $T_J = T_A + (R_{\theta JA} \times P_D)$ with:

T_A = Ambient temperature for the package in °C

$R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W

P_D= Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

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At a known board temperature, the junction temperature T_J is estimated using the following equation $T_J = T_B + (R_{\theta JB} \times P_D)$ with

T_B = Board temperature at the package perimeter in °C

$R_{\theta JB}$ = Junction to board thermal resistance in °C/W

P_D = Power dissipation in the package in W

14 Package outline

The PF1550 uses a 40-pin QFN 5.0 mm x 5.0 mm with exposed pad, case number 98ASA00913D.

This drawing is available for download at http://www.nxp.com.

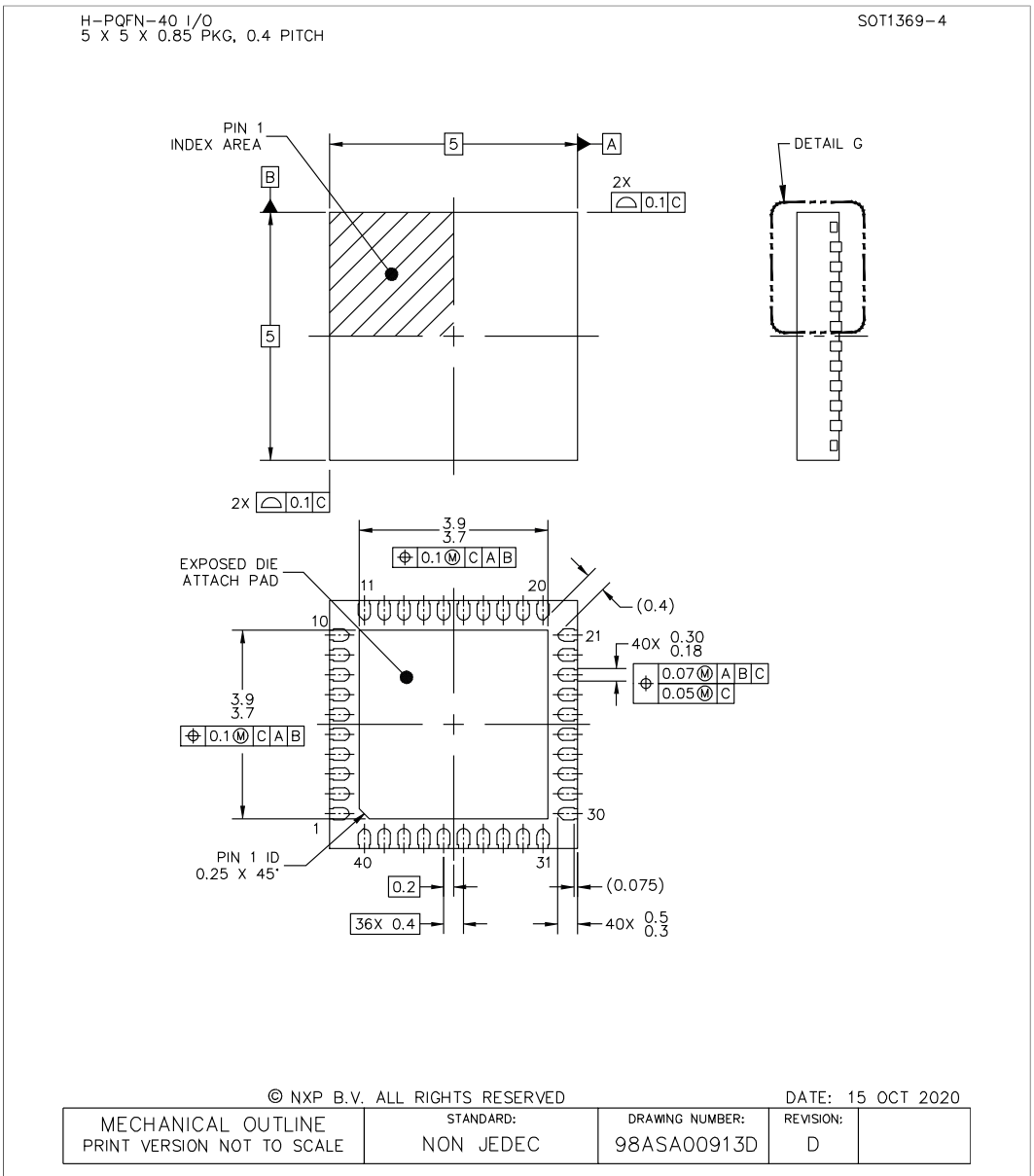

Figure 32. Package outline for HVQFN40 (SOT1369-4)

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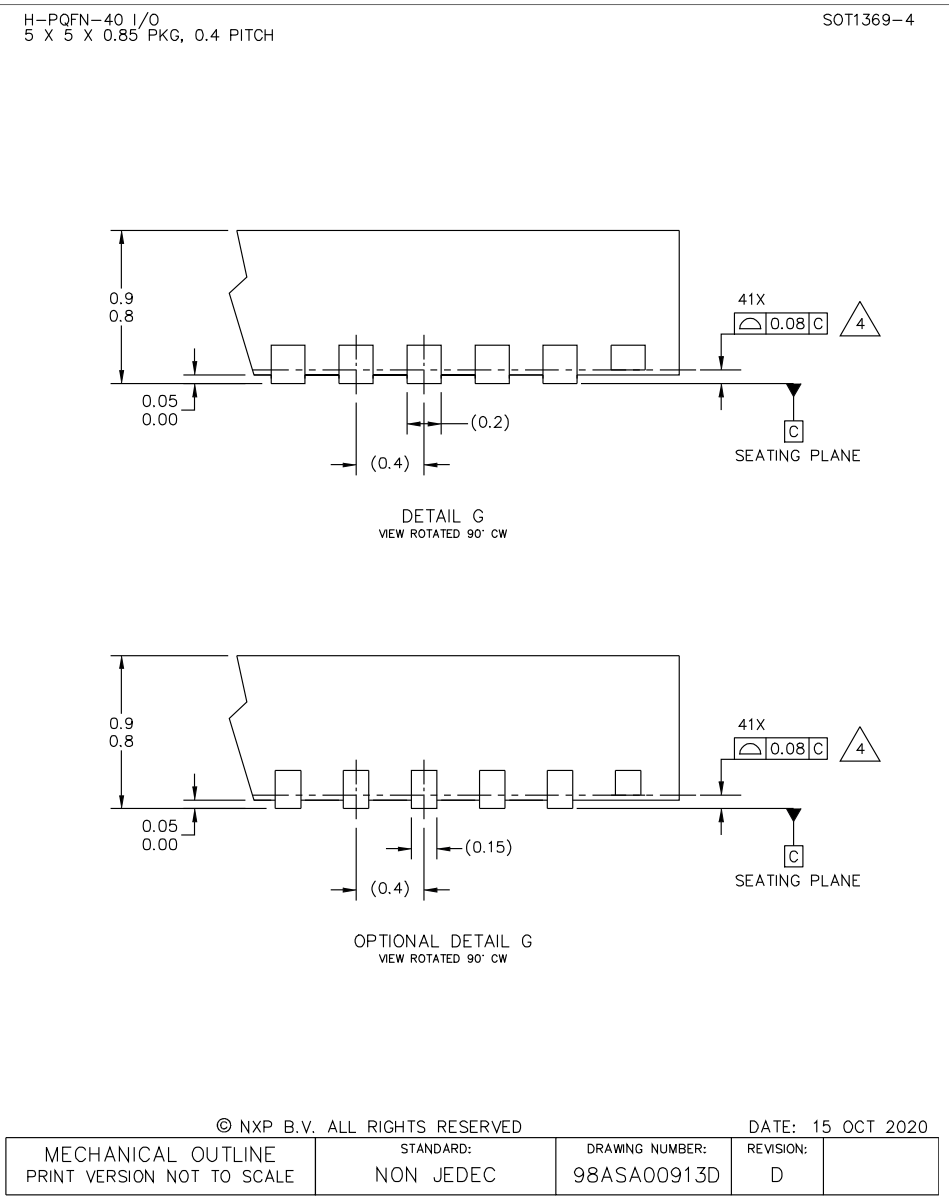

Figure 33. Package outline detail for HVQFN40 (SOT1369-4)

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H-PQFN-40 I/O
5 X 5 X 0.85 PKG, 0.4 PITCH

SOT1369-4

NOTES:

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2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
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Figure 34. Package outline notes for HVQFN40 (SOT1369-4)

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15 Revision history

Table 178. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PF1550 v.7.0	20210929	Product data sheet	CIN 202109033I	PF1550 v.6.0
Modifications	• Global: replaced “BAT_SNS” by “BATT_SNS” • Figure 16: replaced “BAT_SNS=0x09” by “BATT_SNS=0X05” • Section 8.9.4: replaced “BAT_SNS=0x09” by “BATT_SNS=0X05” • Table 152: updated the description for BAT_OK (“BAT_SNS = 0x06 or 0x07 or 0x09” replaced by “BATT_SNS = 0x02 or 0x05 or 0x06” and “BAT_SNS ≠ 0x06 or 0x07 or 0x09” replaced by “BATT_SNS ≠0x02 or 0x05 or 0x06”) • Table 152: updated the description for BAT2SOC_OK (replaced “BATT_SNS Bit 5 = 0b1” by “BATTOC_SNS bit = 1”)			
PF1550 v.6.0	20210305	Product data sheet	PCN 202012012F01	PF1550 v.5.0
Modifications	• Section 14: added "Optional Detail G with 0.15 mm lead edge package option" to package outline drawings			
PF1550 v.5.0	20190610	Product data sheet	—	PF1550 v.4.0
Modifications	Updated as per CIN 201904033I • Table 1: added MC32PF1550A9EP and MC34PF1550A9EP parts • Table 77: replaced "0.2 * VSNVS" by "0.4" and "0.8 * VSNVS" by "1.4" • Section 9.3: added Table 78 • Section 9.4: added Table 79 • Table 81: replaced "0.2 * VBATT" by "0.4", "0.8 * VBATT" by "1.4" and 3.6 by 4.8 • Section 11.1: updated Figure 27 • Table 85: added OTP configuration for A9 • Section 8.8.4: updated Figure 23 • Table 165: updated description for USBPHYLDO (replaced 0 by 1) • Figure 12, Figure 28: replaced "INT_2P7" by "INT2P7" and 1.0 µF by 2.2 µF • Section 12.5: added A9 OTP • Global: changed document status from Advance information to Product			
PF1550 v.4.0	20180928	Advance information	—	PF1550 v.3.0
Modifications	• Added MC32PF1550A0EP, MC32PF1550A8EP, MC34PF1550A0EP, and MC34PF1550A8EP parts to Table 1 • Added OTP configuration for A8 to Table 85			
PF1550 v.3.0	20180502	Advance information	—	PF1550 v.2.0
Modifications	• Changed PC parts to MC in Table 1 • Updated programming option for MC32PF1550A7EP and MC34PF1550A7EP (replaced LPDDR3 by LPDDR2) in Table 1 • Updated SDA and SCL pin description in Table 2 • Updated A7 OTP configuration for OTP_SW3_VOLT[5:0] and OTP_LDO1_VOLT[4:0] registers (replaced 3.3 V by 1.8 V and 1.8 V by 3.3 V) in Table 85 and modified Table 176 to reflect A7 OTP option updates • Updated min. and max. input current values in Table 6			
PF1550 v.2.0	20180202	Advance information	—	PF1550 v.1.0

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Table 178. Revision history...*continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications	• Updated Figure 10 • Updated Figure 28 • Updated description in Section 7.3.6 "LDO2 current limit protection" • Changed capacitor value from 4.7 µF to 10 µF in Section 7.3.3 "LDO2 external components" • Updated Figure 15, Figure 17, Figure 28 • Changed the value of LDO2 output capacitor from 4.7 µF to 10 µF in Table 177 • Updated Figure 3 (changed VUSB to VBUSIN • Updated Figure 4 (changed VDO3IN to VLDO3IN) • Corrected typos in Table 5, Table 6, Table 7, Table 8, Table 9, Table 10, Table 11, Table 13, Table 14, Table 17, and Table 18 • Updated quiescent current I_{LDO1Q} from 4.0 to 4.5 in Table 21 and added new parameter • Updated and added new parameters to Table 19 and Table 20 • Updated values for $I_{LDO2LIM}$ in Table 22 • Updated quiescent current I_{LDO3Q} from 4.0 to 4.5 in Table 23 • Updated typical and maximum value for REGS_DISABLE and SHIP MODE in Table 26 • Updated Section 6.3.3 "Output voltage setting in SW3" • Updated Figure 12, Figure 13, and Figure 14 • Changed OTP_SW2_DVS_SEL to DVS mode for A4 configuration in Table 85 • Changed OTP configuration for SW1 to 1.3875 V in Table 85 • Updated Table 176 and Table 177 • Updated $I_{Q_CHARGER_LQM}$ max. value from 2.5 to 3.0 in Table 6 • Updated values for V_{SWx} in Table 19 • Updated I_{LDO1Q} and I_{LDO3Q} values from 22 to 25 in Table 21 and Table 23 • Added part numbers to Table 1 • Updated typical value for t_{FC} in Table 13 • Updated $I_{SWxLIMH}$ values in Table 19 and Table 20 • Updated Figure 16 and Figure 17 • Added Section 9.7 • Added OTP configuration for A5 to Table 85 • Updated Table 1 • Added A6 and A7 OTP configurations to Table 85 • Updated Figure 3, Figure 16, and Figure 28 • Added Figure 27 • Updated values for $I_{SWxLIMH}$ and $I_{SW3LIMH}$ in Table 19 and Table 20 • Added ripple parameter to Table 20 • Updated values for frequency in Table 72 • Updated Table 116, Table 121, Table 126, Table 167, and Table 174 • Updated Section 12.5 • Replaced MINVSYS by VSYSMIN • Changed document status from Product preview to Advance information			
PF1550 v.1.0	20161012	Product preview	—	—

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