PF8100_PF8200

12-channel power management integrated circuit for high performance applications

Rev. 12 — 18 October 2024 **Product data sheet**



1 Overview

The PF8100/PF8200 is a power management integrated circuit (PMIC) designed for high performance i.MX 8 and S32x based applications. It features seven high-efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals.

Built-in one-time programmable (OTP) memory stores key startup configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

2 Features and benefits

- Up to seven high-efficiency buck converters
- Four linear regulators with load switch options
- RTC supply and coin cell charger
- Watchdog timer/monitor
- Monitoring circuit to fit automotive safety integrity level (ASIL) B
- One-time programmable (OTP) device configuration
- 3.4 MHz I^2C communication interface
- 56-pin 8 x 8 mm QFN package

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

3 Simplified application diagram

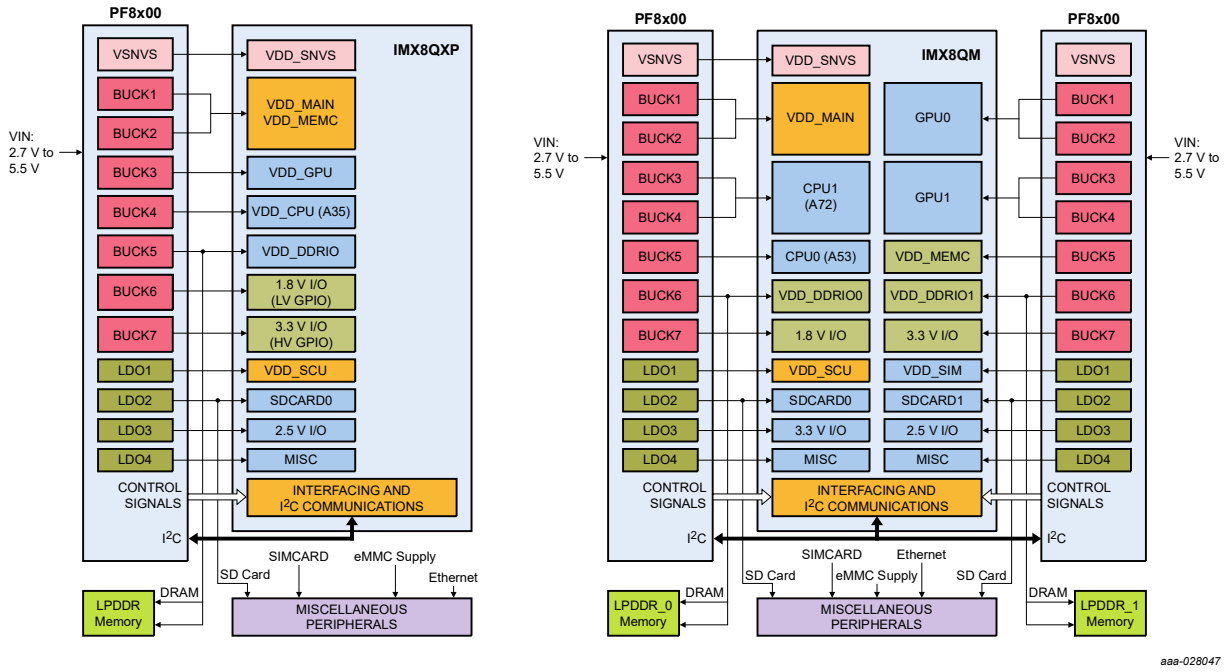


Figure 1. Simplified application diagram

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

4 Ordering information

Table 1. Device options

Type	Package		
	Name	Description	Version
PF8100 (automotive)	HVQFN56	HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, wettable flanks; 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-21 (DD/SC)
PF8200 (automotive)			
PF8100 (industrial)		HVQFN56, plastic, thermally enhanced very thin quad; flat non-leaded package, 56 terminals; 0.5 mm pitch; 8 mm x 8 mm x 0.85 mm body	SOT684-21
PF8100 (automotive/industrial)		HVQFN56, thermal enhanced very thin quad flat package, no leads, 56 terminals, 0.1 mm dimple wettable flank, 0.5 mm pitch, 8 mm x 8 mm x 0.9 mm body	SOT684-29(D)
PF8200 (automotive)		HVQFN56, thermal enhanced very thin quad flat package, no leads, 56 terminals, 0.1 mm dimple wettable flank, 0.5 mm pitch, 8 mm x 8 mm x 0.9 mm body	SOT684-29(D)

Table 2. Ordering information

Part number [1] [2] [3]	Target market	NXP processor	System comments	Safety grade	OTP [4]
MC33PF8100A0ES	Automotive	n/a	Not programmed	QM	n/a
MC33PF8100A0TS					
MC33PF8100CCES[5]	Automotive	i.MX8QXP	LPDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100CC.zip
MC33PF8100CCTS[5]					
MC33PF8100CFES	Automotive	i.MX8QXP	DDR3L memory	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100CF.zip
MC33PF8100CFTS					
MC33PF8100CHES	Automotive	i.MX8QM	DDR4 memory PMIC2	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100CH.zip
MC33PF8100CHTS					
MC33PF8100EAES	Automotive	LS1046A	DDR4 Memory (VDDQ + VTT)	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100EA.zip
MC33PF8100EATS					
MC33PF8100EPES	Automotive	i.MX8QM	LPDDR4 memory PMIC1	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100EP.zip
MC33PF8100EPTS					
MC33PF8100EQES	Automotive	i.MX8QM	LPDDR4 memory PMIC2	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100EQ.zip
MC33PF8100EQTS					
MC33PF8100ERES	Automotive	i.MX8QM	DDR4 memory PMIC1	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100ER.zip
MC33PF8100ERTS					
MC33PF8100FJES	Automotive	i.MX8QXP	LPDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100FJ.zip
MC33PF8100FJTS					
MC33PF8100F3ES	Automotive	LA1575	LDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC33PF8100F3.zip
MC33PF8100F3TS					
MC34PF8100A0EP	Industrial	n/a	Not programmed	QM	n/a
MC34PF8100A0TS					
MC34PF8100CCEP[5]	Industrial	i.MX8QXP	LPDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100CC.zip
MC34PF8100CCTS[5]					
MC34PF8100CFEP	Industrial	i.MX8QXP	DDR3L memory	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100CF.zip
MC34PF8100CFTS					
MC34PF8100CHEP	Industrial	i.MX8QM	DDR4 memory PMIC2	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100CH.zip
MC34PF8100CHTS					
MC34PF8100EPEP	Industrial	i.MX8QM	LPDDR4 memory PMIC1	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100EP.zip
MC34PF8100EPTS					
MC34PF8100EQEP	Industrial	i.MX8QM	LPDDR4 memory PMIC2	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100EQ.zip
MC34PF8100EQTS					
MC34PF8100EREP	Industrial	i.MX8QM	DDR4 memory PMIC1	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100ER.zip
MC34PF8100ERTS					

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 2. Ordering information...*continued*

Part number [1] [2] [3]	Target market	NXP processor	System comments	Safety grade	OTP [4]
MC34PF8100FJEP	Industrial	i.MX8QXP	LPDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100FJ.zip
MC34PF8100FJTS					
MC34PF8100F3EP	Industrial	LA1575	LDDR4 memory	QM	https://www.nxp.com/docs/en/supporting-information/MC34PF8100F3.zip
MC34PF8100F3TS					
MC33PF8200A0ES	Automotive	n/a	Not programmed	ASIL B	n/a
MC33PF8200A0TS					
MC33PF8200CXES	Automotive	LS1043A	LPDDR4 memory	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200CX.zip
MC33PF8200CXTS					
MC33PF8200D2ES	Automotive	S32V234	DDR3L memory 10 A core	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200D2.zip
MC33PF8200D2TS					
MC33PF8200DBES	Automotive	i.MX8QM	LPDDR4 memory PMIC2	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200DB.zip
MC33PF8200DBTS					
MC33PF8200DEES	Automotive	i.MX8QXP	LPDDR4 memory	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200DE.zip
MC33PF8200DETS					
MC33PF8200DFES	Automotive	i.MX8QXP	DDR3L memory	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200DF.zip
MC33PF8200DFTS					
MC33PF8200DHES	Automotive	i.MX8QM	DDR4 memory PMIC2	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200DH.zip
MC33PF8200DHTS					
MC33PF8200EMES	Automotive	LS1043	Triple phase (VDD)	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200EM.zip
MC33PF8200EMTS					
MC33PF8200ESES	Automotive	i.MX8QM	LPDDR4 memory PMIC1	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200ES.zip
MC33PF8200ESTS					
MC33PF8200ETES	Automotive	i.MX8QM	DDR4 memory PMIC1	ASIL B	https://www.nxp.com/docs/en/supporting-information/MC33PF8200ET.zip
MC33PF8200ETTS					

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Step-cut wettable flank for part numbers ending in ES, non-wettable flank for part numbers ending in EP, dimple wettable flank for part numbers ending in TS.
[3] The part numbers with the TS suffix are recommended for new designs.
[4] Part numbers that are the same except for ending in ES/EP or TS share the same OTP report.
[5] Not recommended for new designs. MC33PF8100FJTS or MC34PF8100FJTS are recommended instead.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

5 Applications

- Automotive Infotainment
- High-end consumer and industrial

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

6 Internal block diagram

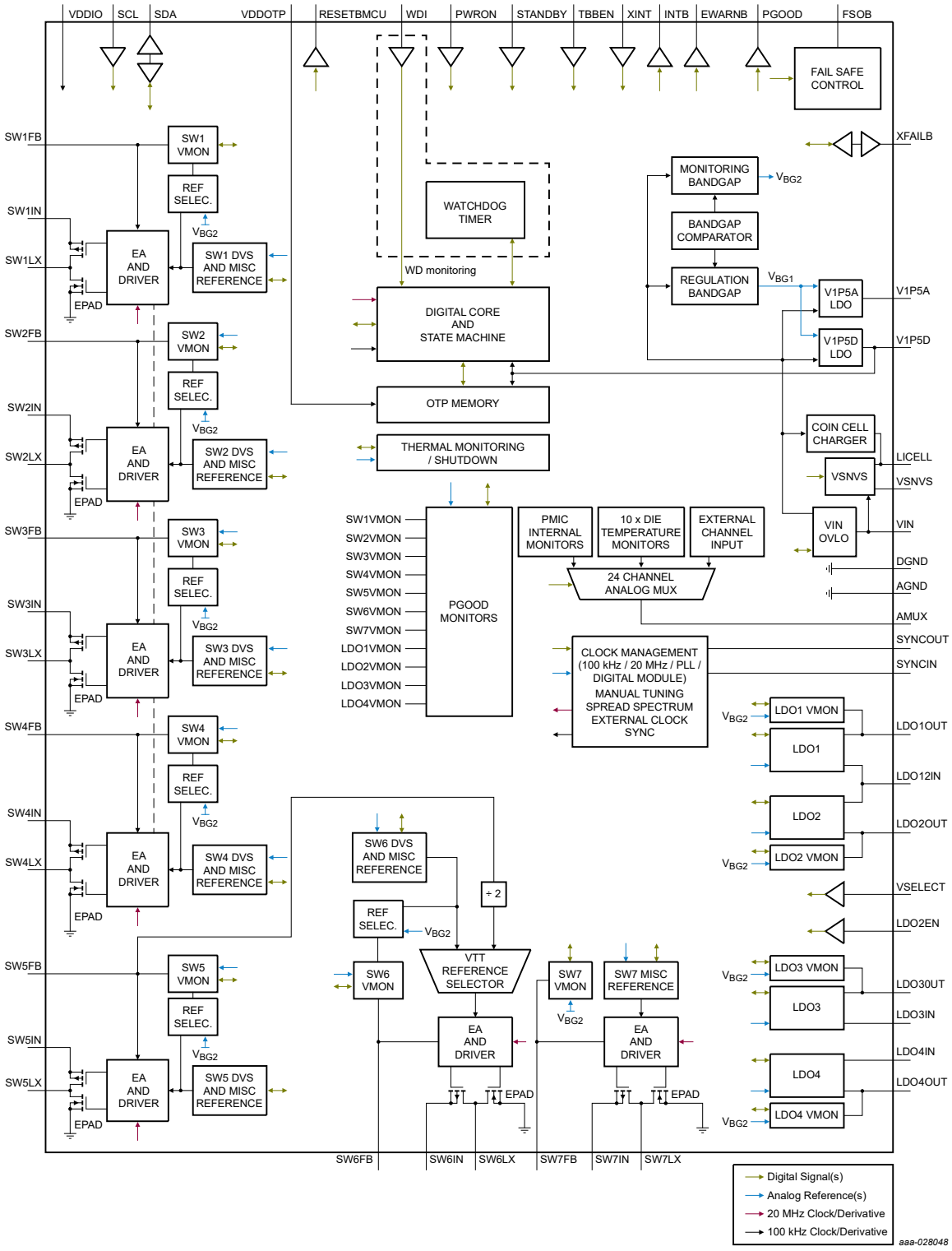


Figure 2. Internal block diagram

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

7 Pinning information

7.1 Pinning

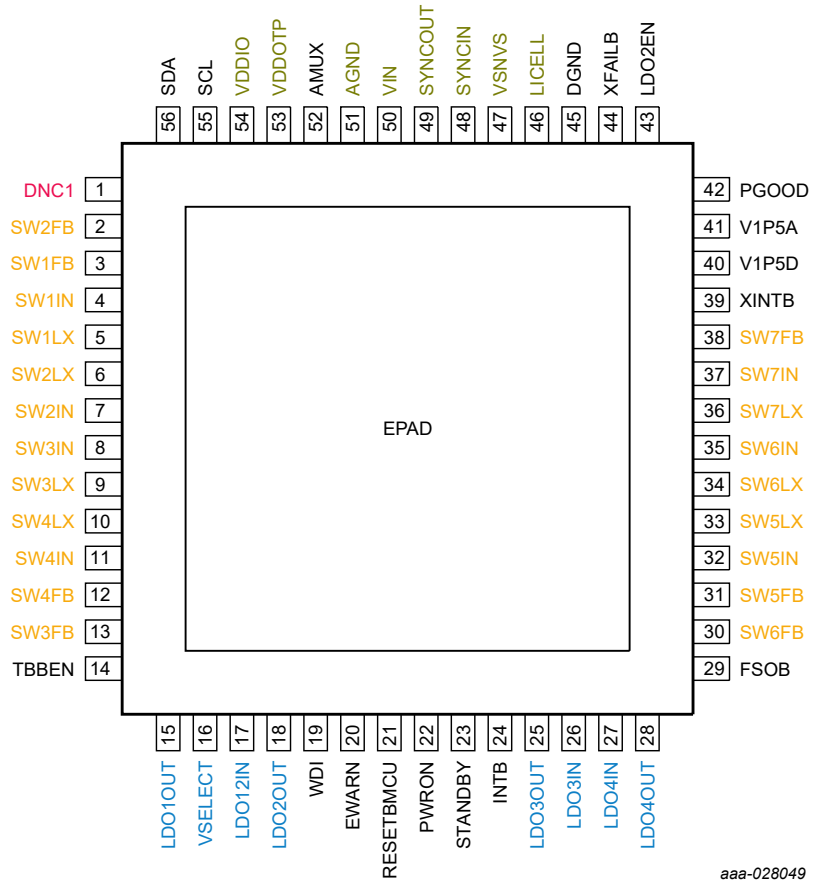


Figure 3. Pin configuration for HVQFN56

7.2 Pin description

Table 3. HVQFN56 pin description

Pin number	Symbol	Application description	Pin type	Min	Max	Units
1	DNC1	Do not connect	—	—	—	V
2	SW2FB	Buck 2 output voltage feedback	I	−0.3	6.0	V
3	SW1FB	Buck 1 output voltage feedback	I	−0.3	6.0	V
4	SW1IN	Buck 1 input supply	I	−0.3	6.0	V
5	SW1LX [1]	Buck 1 switching node	O	−0.3	6.0	V
6	SW2LX [1]	Buck 2 switching node	O	−0.3	6.0	V
7	SW2IN	Buck 2 input supply	I	−0.3	6.0	V
8	SW3IN	Buck 3 input supply	I	−0.3	6.0	V
9	SW3LX [1]	Buck 3 switching node	O	−0.3	6.0	V
10	SW4LX [1]	Buck 4 switching node	O	−0.3	6.0	V
11	SW4IN	Buck 4 input supply	I	−0.3	6.0	V

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 3. HVQFN56 pin description*...continued*

Pin number	Symbol	Application description	Pin type	Min	Max	Units
12	SW4FB	Buck 4 output voltage feedback	I	−0.3	6.0	V
13	SW3FB	Buck 3 output voltage feedback	I	−0.3	6.0	V
14	TBBEN	Try Before Buy enable pin	I	−0.3	6.0	V
15	LDO1OUT	LDO1 output	O	−0.3	6.0	V
16	VSELECT	LDO2 voltage select input	I	−0.3	6.0	V
17	LDO12IN	LDO1 and LDO2 input supply	I	−0.3	6.0	V
18	LDO2OUT	LDO2 output	O	−0.3	6.0	V
19	WDI	Watchdog Input from MCU	I	−0.3	6.0	V
20	EWARN	Early warning to MCU	O	−0.3	6.0	V
21	RESETBMCU	RESETBMCU open-drain output	O	−0.3	6.0	V
22	PWRON	PWRON input	I	−0.3	6.0	V
23	STANDBY	STANDBY input	I	−0.3	6.0	V
24	INTB	INTB open-drain output	O	−0.3	6.0	V
25	LDO3OUT	LDO3 output	O	−0.3	6.0	V
26	LDO3IN	LDO3 input supply	I	−0.3	6.0	V
27	LDO4IN	LDO4 input supply	I	−0.3	6.0	V
28	LDO4OUT	LDO4 output	O	−0.3	6.0	V
29	FSOB	Safety output pin	O	−0.3	6.0	V
30	SW6FB	Buck 6 output voltage feedback	I	−0.3	6.0	V
31	SW5FB	Buck 5 output voltage feedback	I	−0.3	6.0	V
32	SW5IN	Buck 5 input supply	I	−0.3	6.0	V
33	SW5LX [1]	Buck 5 switching node	O	−0.3	6.0	V
34	SW6LX [1]	Buck 6 switching node	O	−0.3	6.0	V
35	SW6IN	Buck 6 input supply	I	-0.3	6.0	V
36	SW7LX [1]	Buck 7 switching node	O	−0.3	6.0	V
37	SW7IN	Buck 7 input supply	I	−0.3	6.0	V
38	SW7FB	Buck 7 output voltage feedback	I	−0.3	6.0	V
39	XINTB	External interrupt input	I	−0.3	6.0	V
40	V1P5D	1.6 V digital core supply	O	−0.3	2.0	V
41	V1P5A	1.6 V analog core supply	O	−0.3	2.0	V
42	PGOOD	PGOOD open-drain output	O	−0.3	6.0	V
43	LDO2EN	LDO2 enable pin	I	−0.3	6.0	V
44	XFAILB	External Synchronization pin	I/O	-0.3	6.0	V
45	DGND	Digital ground	GND	−0.3	0.3	V
46	LICELL	Coin cell input	I	−0.3	5.5	V
47	VSNVS	VSNVS regulator output	O	−0.3	6.0	V
48	SYNCIN	External clock input pin for synchronization	I	−0.3	6.0	V
49	SYNCOUT	Clock out pin for external part synchronization	O	−0.3	6.0	V
50	VIN	Main input voltage to PMIC	I	−0.3	6.0	V

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 3. HVQFN56 pin description*...continued*

Pin number	Symbol	Application description	Pin type	Min	Max	Units
51	AGND	Analog ground	GND	−0.3	0.3	V
52	AMUX	Analog multiplexer output	O	−0.3	6.0	V
53	VDDOTP	OTP selection input	I	−0.3	10	V
54	VDDIO	I/O supply voltage. Connect to voltage rail between 1.6 V and 3.3 V	I	−0.3	6.0	V
55	SCL	I^2C clock signal	I	−0.3	6.0	V
56	SDA	I^2C data signal	I/O	−0.3	6.0	V
57	EPAD	Exposed pad Connect to ground	GND	−0.3	0.3	V

[1] Minimum voltage specification is given for DC voltage condition. While the regulator is switching, the LX pin may experience transient voltage spikes as low as −3.0 V during the dead band time(<5 ns). The LX pins are tolerant to such transient spikes, however, it is responsibility of the hardware designer to follow proper layout design guidelines to minimize the impact of parasitic inductance in the power path of the switching regulator, thus keeping the magnitude of the negative voltage spike at the LX pin below 3.0 V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

8 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
VIN	Main input supply voltage [1]	−0.3	—	6.0	V
SWxVIN, LDOxVIN	Regulator input supply voltage [1]	−0.3	—	6.0	V
VDDOTP	OTP programming input supply voltage	−0.3	—	10	V
VLICELL	Coin cell voltage	−0.3	—	5.5	V

[1] Pin reliability may be affected if system voltages are above the maximum operating range of 5.5 V for extended periods of time. To minimize system reliability impact, system must not operate above 5.5 V for more than 1800 sec over the lifetime of the device.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

9 ESD ratings

Table 5. ESD ratings

All ESD specifications are compliant with AEC-Q100 specification.

Symbol	Parameter	Min	Typ	Max	Unit
V_{ESD}	Human Body Model [1]	—	—	2000	V
V_{ESD}	Charge Device Model [1] QFN package - all pins	—	—	500	V
$I_{LATCHUP}$	Latch-up current	—	—	100	mA

[1] ESD testing is performed in accordance with the human body model (HBM) (CZAP = 100 pF, RZAP = 1500 Ω), and the charge device model (CDM), robotic (CZAP = 4.0 pF)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

10 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient operating temperature [1]	−40	—	105	°C
T_J	Junction temperature	−40	—	150	°C
T_{ST}	Storage temperature range	−55	—	150	°C
T_{PPRT}	Peak package reflow temperature	—	—	260	°C

[1] All parameters are specified up to a junction temperature of 150 °C. All parameters are tested at T_A from −40°C to 105 °C to allow headroom for self heating during operation. If higher T_A operation is required, proper thermal and loading consideration must be made to ensure device operation below the maximum T_J = 150 °C.

Table 7. QFN56 thermal resistance and package dissipation ratings

Symbol	Parameter	Min	Max	Unit
$R_{\theta JA}$	Junction to Ambient Natural Convection Single Layer Board (1s) [1] [2]	—	81	°C/W
$R_{\theta JA}$	Junction to Ambient Natural Convection Four Layer Board (2s2p) [1] [2]	—	27	°C/W
$R_{\theta JA}$	Junction to Ambient Natural Convection Eight Layer Board (2s6p)	—	22	°C/W
$R_{\theta JMA}$	Junction to Ambient (@200ft/min) Single Layer Board (1s) [1] [3]	—	66	°C/W
$R_{\theta JMA}$	Junction to Ambient (@200ft/min) Four Layer Board (2s2p) [1] [3]	—	22	°C/W
$R_{\theta JB}$	Junction to Board [4]	—	11	°C/W
$R_{\theta JC}$	Junction to Case (bottom) [5]	—	0.6	°C/W
ΨJT	Junction to package (top) [6]	—	1	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
[3] Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
[6] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

11 Operating conditions

Table 8. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Main input supply voltage	UVDET	—	5.5	V
V_{LICELL}	LICELL input voltage range	—	—	4.2	V

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

12 General description

12.1 Features

The PF8100/PF8200 is a power management integrated circuit (PMIC) designed to be the primary power management building block for NXP high-end multimedia application processors from the i.MX 8 and S32x series. It is also capable of providing power solution to the high end i.MX 6 series as well as several non-NXP processors.

- Buck regulators
  - SW1, SW2, SW3, SW4, SW5, SW6: 0.4 V to 1.8 V; 2500 mA; up to 1.5 % accuracy
  - SW7; 1.0 V to 4.1 V; 2500 mA; 2 % accuracy
  - Dynamic voltage scaling on SW1, SW2, SW3, SW4, SW5, and SW6
  - SW1, SW2 configurable as a dual phase regulator
  - SW3, SW4 configurable as a dual phase regulator
  - SW5, SW6 configurable as a dual phase regulator
  - SW1, SW2 and SW3 configurable as a triple phase regulator with up to 7.5 A current capability
  - SW1, SW2, SW3 and SW4 configurable as a quad phase regulator with up to 10 A current capability
  - VTT termination mode on SW6
  - Programmable current limit
  - Spread-spectrum and manual tuning of switching frequency
- LDO regulators
  - LDO1, 1.5 V to 5.0 V, 400 mA: 3 % accuracy with optional load switch mode
  - LDO2, 1.5 V to 5.0 V, 400 mA; 3 % accuracy with optional load switch mode and selectable hardware/ software control
  - LDO3, 1.5 V to 5.0 V, 400 mA; 3 % accuracy with optional load switch mode
  - LDO4, 1.5 V to 5.0 V, 400 mA; 3 % accuracy with optional load switch mode
- RTC LDO/Switch supply from system supply or coin cell
  - RTC supply VSNVS 1.8 V/3.0 V/3.3 V, 10 mA
  - Battery backed memory including coin cell charger with programmable charge current and voltage
- System features
  - Fast PMIC startup
  - Advanced state machine for seamless processor interface
  - High speed I^2C interface support (up to 3.4 MHz)
  - PGOOD monitor
  - User programmable standby and off modes
  - Programmable soft start sequence and power down sequence
  - Programmable regulator configuration
  - 24 channel analog multiplexer for smart system monitoring/diagnostic
- OTP (One time programmable) memory for device configuration
- Monitoring circuit to fit ASIL B Safety level
  - Independent voltage monitoring with programmable fault protection
  - Advance thermal monitoring and protection
  - External watchdog monitoring and programmable internal watchdog counter
  - I^2C CRC and write protection mechanism
  - Analog built-in self-test (ABIST)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

12.2 Functional block diagram

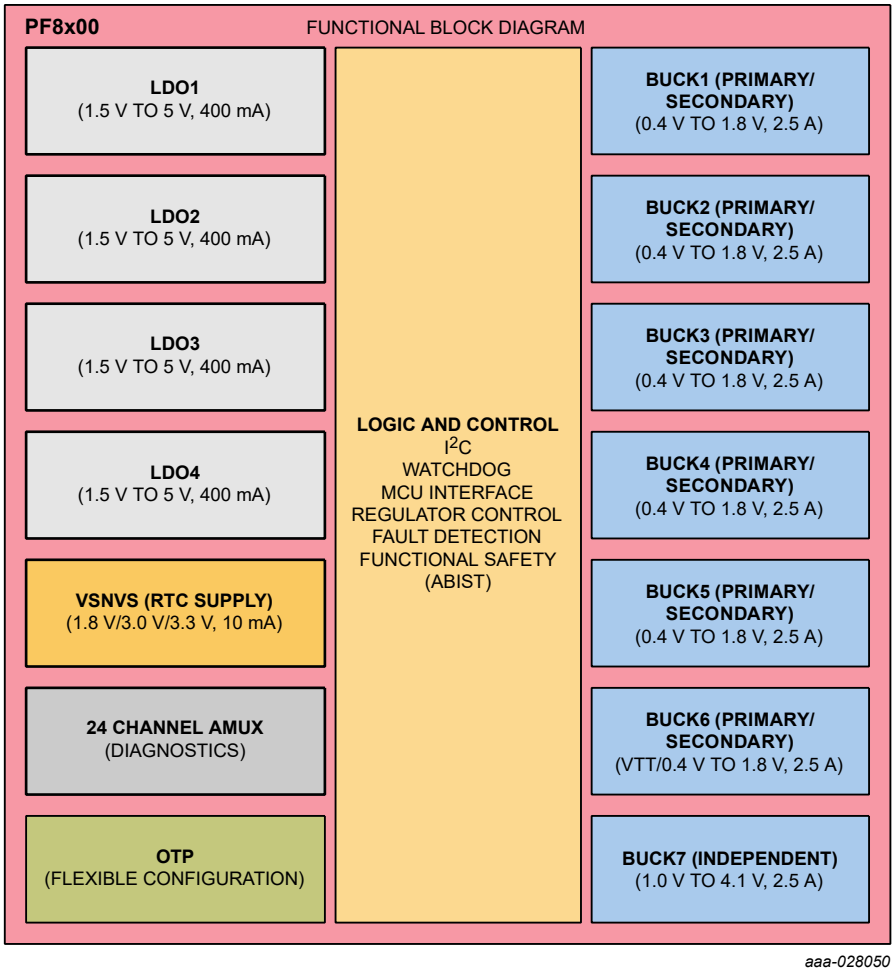


Figure 4. Functional block diagram

12.3 Power tree summary

The following table shows a summary of the voltage regulators in the PF8100/PF8200.

Table 9. Voltage supply summary

Regulator	Type	Input supply	Regulated output range (V)	VOUT programmable step (mV)	IRATED (mA)
SW1	Buck	SW1IN [1]	0.4 V to 1.8 V	6.25	2500
SW2	Buck	SW2IN [1]	0.4 V to 1.8 V	6.25	2500
SW3	Buck	SW3IN [1]	0.4 V to 1.8 V	6.25	2500
SW4	Buck	SW4IN [1]	0.4 V to 1.8 V	6.25	2500
SW5	Buck	SW5IN [1]	0.4 V to 1.8 V	6.25	2500
SW6	Buck	SW6IN [1]	VTT/0.4 V to 1.8 V	6.25	2500
SW7	Buck	SW7IN [1]	1.0 V to 4.1 V	—	2500
LDO1	Linear (P-type)	LDO12IN	1.5 V to 5.0 V	—	400

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 9. Voltage supply summary*...continued*

Regulator	Type	Input supply	Regulated output range (V)	VOUT programmable step (mV)	IRATED (mA)
LDO2	Linear (P-type)	LDO12IN	1.5 V to 5.0 V	—	400
LDO3	Linear (P-type)	LDO3IN	1.5 V to 5.0 V	—	400
LDO4	Linear (P-type)	LDO4IN	1.5 V to 5.0 V	—	400
VSNVS	LDO/Switch	VIN/LICELL	1.8 V/3.0 V/3.3 V	—	10

[1] Input supply for switching regulators must be capable to sink current to avoid overvoltage condition during the power down sequence of the device.

12.4 Device differences

Table 10. Device differences

Description	PF8200	PF8100	Bits not available on PF8100
During the self-test, the device checks: • The high speed oscillator circuit is operating within a maximum of 15 % tolerance • A CRC is performed on the mirror registers during the self-test routine to ensure the integrity of the registers before powering up • ABIST test on all voltage monitors and toggling signals	Available	Not available	AB_SWx_OV AB_SWx_UV AB_LDOx_OVAB_LDOx_UV STEST_NOK
Fail-safe state: to lock down the system in case of critical failures cycling the PMIC on/off	Available	Not available	FS_CNT[3:0] OTP_FS_BYPASS OTP_FS_MAX_CNT[3:0] OTP_FS_OK_TIMER[2:0]
ABIST on demand	Available	Not available	AB_RUN
Active safe state: allow the FSOB to remain asserted as long as any of the non-safe conditions are present. Allow the system to be set in safe state via the FSOB pin.	Available	Not available	FSOB_ASS_NOK OTP_FSOB_ASS_EN (always 0)
Secure I^2C write: I^2C write procedure to modify registers dedicated to safety features (I^2C CRC is still available)	Available	Not available	I2C_SECURE_EN OTP_I2C_SECURE _EN (always 0) RANDOM_GEN[7:0] RANDOM_CHK[7:0]

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

13 State machine

The PF8100/PF8200 features a state of the art state machine for seamless processor interface. The state machine handles the IC start up, provides fault monitoring and reporting, and protects the IC and the system during fault conditions.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

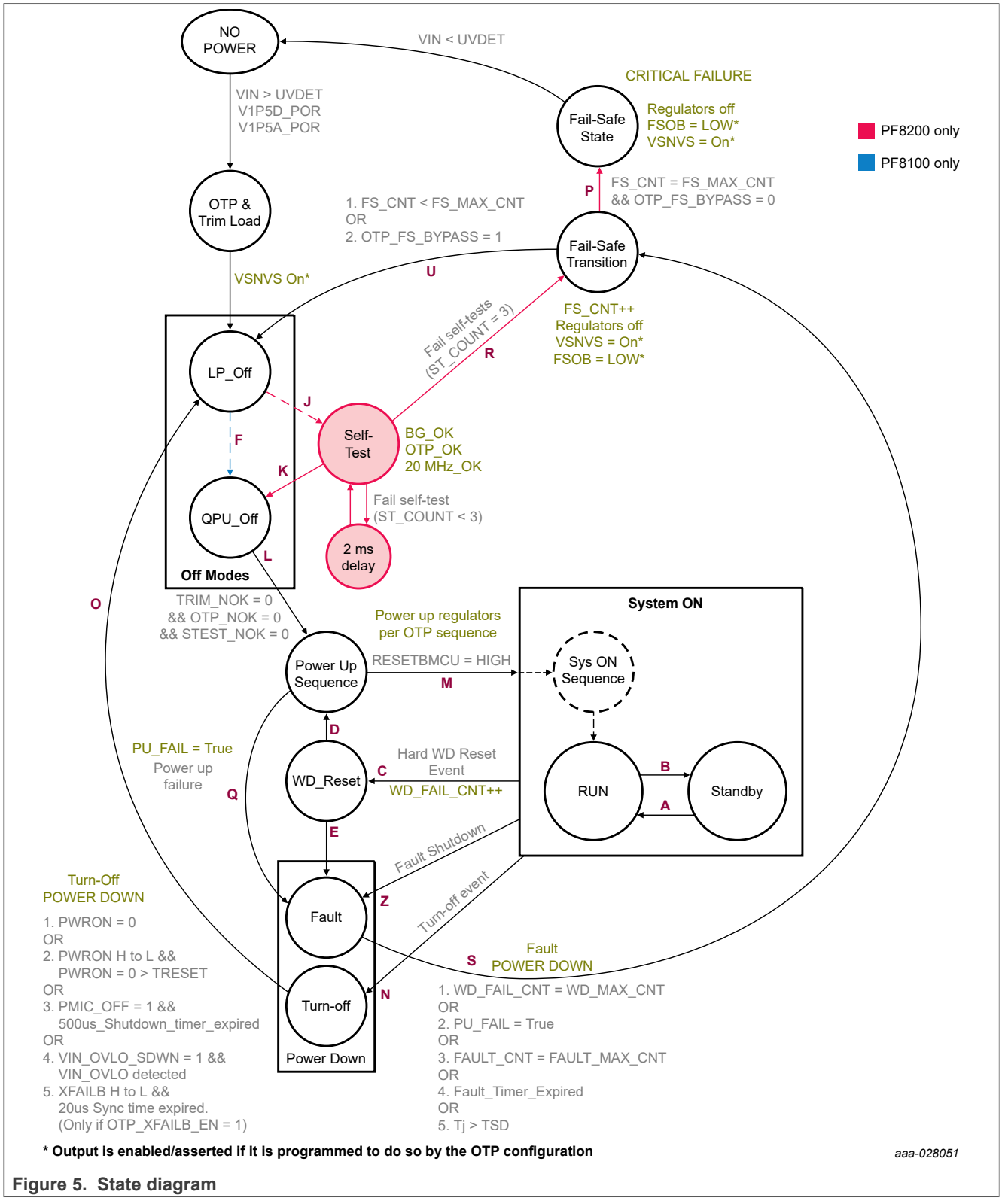


Figure 5. State diagram

Table 11 lists the conditions for the different state machine transitions.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 11. State machine transition definition

Symbol	Description	Conditions
Transition A	Standby to run	1. STANDBY = 0 && STANDBYINV bit = 0
		2. STANDBY = 1 && STANDBYINV bit = 1
Transition B	Run to standby	1. (STANDBY = 1 && STANDBYINV bit = 0
		2. STANDBY = 0 && STANDBYINV bit = 1
Transition C	System on to WD reset	1. Hard WD Reset event
Transition D	WD reset to system on	1. 30 µs delay passed && WD_EVENT_CNT < WD_MAX_CNT
Transition E	WD reset to power down (fault)	1. WD_EVENT_CNT = WD_MAX_CNT
Transition J	LP_Off to self-test **(PF8200 only)**	Transitory off state: device pass through LP_Off to Self-Test to QPU_Off (no power up event present) 1. LPM_OFF = 1 && TBBEN = Low
		Power up event from LP_Off state 2. LPM_OFF = 0 && TBBEN = Low && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET< VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0
		Power up event from LP_Off state 3. LPM_OFF = 0 && TBBEN = Low && (PWRON H to L && OTP_PWRON_MODE = 1 && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0
		Conditions: Transitory Off state to go into TBB Mode. Device pass through LP_Off to Self-Test to QPU_Off (no power up event present) 4. TBBEN = high (V1P5D)
Transition K	Self-test to QPU_Off **(PF8200 only)**	1. Pass Self-Tests
		2. TBBEN = high (V1P5D)
Transition F	LP_Off to QPU_Off **(PF8100 only)**	Transitory Off state: device pass through LP_Off to QPU_Off (no power up event present) 1. LPM_OFF = 1 && TBBEN = Low
		Power up event from LP_Off state 2. LPM_OFF = 0 && TBBEN = Low && (PWRON = 1 && OTP_PWRON_MODE = 0) && UVDET< VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0
		Power up event from LP_Off state 3. LPM_OFF =0 && TBBEN = Low && (PWRON H to L && OTP_PWRON_MODE = 1) && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && $T_J < T_{SD}$ && TRIM_NOK = 0 && OTP_NOK = 0
		Transitory Off state: device pass through LP_Off to QPU_Off (no power up event present) 4. TBBEN = High (V1P5D)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 11. State machine transition definition*...continued*

Symbol	Description	Conditions
Transition L	QPU_Off to power up	Transitory QPU_Off state, power on event occurs from LP_Off state, after self-test is passed, QPU_Off is just a transitory state until power up sequence starts. 1. LPM_OFF = 0 && TBBEN = Low && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 2. LPM_OFF = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state 3. LPM_OFF = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK=0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state during TBB mode 4. TBBEN = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Power up event from QPU_Off state during TBB mode 5. TBBEN = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 0
		Transitory QPU_Off state, Power on event occurs from LP_Off state, after self-test is passed, QPU_Off is just a transitory state until power up sequence starts 6. LPM_OFF = 0 && TBBEN = Low && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = HIGH
		Power up event from QPU_Off state 7. LPM_OFF = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = HIGH
		Power up event from QPU_Off state 8. LPM_OFF = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = HIGH

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 11. State machine transition definition*...continued*

Symbol	Description	Conditions
		Power up event from QPU_Off state during TBB mode 9. TBBEN = 1 && (PWRON = 1 && OTP_PWRON_MODE = 0) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = HIGH
		Power up event from QPU_Off state during TBB mode 10. TBBEN = 1 && (PWRON H to L && OTP_PWRON_MODE = 1) && $T_J < T_{SD}$ && UVDET < VIN < VIN_OVLO (or VIN_OVLO disabled) && TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0 && OTP_XFAILB_EN = 1 && XFAILB = HIGH
Transition M	Power up sequence to system on	1. RESETBMCU is released as part of the power up sequence
Transition N	System on to power down (turn off)	Requested turn off event 1. OTP_PWRON_MODE = 0 && PWRON = 0
		Requested turn off event 2. OTP_PWRON_MODE = 1 && (PWRON H to L && PWRON = low for t > TRESET)
		Requested turn off event 3. PMIC_OFF = 1 && 500 µs_Shutdown_Timer_Expired
		Protective turn off event (no PMIC fault) 4. VIN_OVLO_SDWN=1 && VIN_OVLO detected for longer than VIN_OVLO_DBNC time
		External turn off event (no PMIC fault) 5. OTP_XFAILB_EN = 1 && XFAILB → Low && 20 µs synchronization time is expired
Transition Z	System on to power down (fault)	Turn off event due to PMIC fault 1. Fault Timer expired
		Turn off event due to PMIC fault 2. FAULT_CNT = FAULT_MAX_CNT
		Turn off event due to PMIC fault 3. Thermal shutdown $T_J > T_{SD}$
Transition O	Power down (turn off) to LP_Off	Requested turn off event moves directly to LP_Off 1. Power down sequences finished
Transition Q	Power up to power down (fault)	Power up failure 1. Failure during power up sequence
Transition R	Self-test to fail-safe transition	1. Self-tests fail 3 times && TBBEN = low
Transition S	Power down (fault) to fail-safe transition	Turn off event due to a fault condition moves to fail-safe transition 1. Power down sequence is finished
Transition U	Fail-safe transition to LP_Off	1. FS_CNT < FS_MAX_CNT
		2. OTP_FS_BYPASS = 1
Transition P	Fail-safe transition to fail-safe state **(PF8200 only)**	1. FS_CNT = FS_MAX_CNT && OTP_FS_BYPASS = 0

13.1 State descriptions

13.1.1 OTP/TRIM load

Upon VIN application V1P5D and V1P5A regulators are turned on automatically. Once the V1P5D and V1P5A cross their respective POR thresholds, the fuses (for trim and OTP) are loaded into the mirror registers and into the functional I^2C registers if configured by the voltage on the VDDOTP pin.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The fuse circuits have a CRC error check routine which reports and protects against register loading errors on the mirror registers. If a register loading error is detected, the corresponding TRIM_NOK or OTP_NOK flag is asserted. See Section 17 "OTP/TBB and default configurations" for details on handling fuse load errors.

If no fuse load errors are present, VSNVS is configured as indicated in the OTP configuration bits, and the state machine moves to the LP_OFF state.

13.1.2 LP_Off state

The LP_Off state is a low power off mode selectable by the LPM_OFF bit during the system on modes. By default, the LPM_OFF = 0 when VIN crosses the UVDET threshold, therefore the state machine stops at the LP_Off state until a valid power up event is present. When LPM_OFF= 1, the state machine transitions automatically to the QPU_Off state if no power up event has been present and waits in the QPU_Off until a valid power up event is present.

The selection of the LPM_OFF bit is based on whether prioritizing low quiescent current (stay in LP_Off) or quick power up (move to QPU_Off state).

If a power up event is started in LP_Off state with LPM_OFF = 0 and a fuse loading error is detected, the PF8100/PF8200 ignores the power up event and remains in the LP_Off state to avoid any potential damage to the system.

To be in LP_Off state, it is necessary to have VIN present. If a valid LICELL is present, but VIN is below the UVDET, the PF8100/PF8200 enters the coin cell state.

13.1.3 Self-test routine (PF8200 only)

When device transitions from the LP_Off state, it turns on all necessary internal circuits as it moves into the self-test routine and performs a self-check routine to verify the integrity of the internal circuits.

During the self-test routine the following blocks are verified:

- The high speed clock circuit is operating within a maximum of 15 % tolerance
- The output of the voltage generation bandgap and the monitoring bandgap are not more than 4 % to 12 % apart from each other
- A CRC is performed on the mirror registers during the self-test routine, to ensure the integrity of the registers before powering up
- ABIST test on all voltage monitors.

To allow for varying settling times for the internal bandgap and clocks, the self-test block is executed up to 3 times (with 2.0 ms between each test) if a failure is encountered, the state machine proceeds to the fail-safe transition.

A failure in the ABIST test is not interpreted as a self-test failure and it only sets the corresponding ABIST flag for system information. The MCU is responsible for reading the information and deciding whether it can continue with a safe operation. See Section 18.1 "System safety strategy" for more information about the functional safety strategy of PF8200.

Upon a successful self-test, the state machine proceeds to the QPU_Off state.

13.1.4 QPU_Off state

The QPU_Off state is a higher power consumption off mode, in which all internal circuitry required for a power on is biased and ready to start a power up sequence.

If LPM_OFF = 1 and no turn on event is present, the device stops at the QPU_Off state, and waits until a valid turn on event is present.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

In this state, if VDDIO supply is provided externally, the device is able to communicate through I^2C to access and modify the mirror registers in order to operate the device in TBB mode or to program the OTP registers as described in Section 17 "OTP/TBB and default configurations".

By default, the coin cell charger is disabled during the QPU_Off state when VIN crosses the UVDET threshold, but it may be turned on or off in this state once it is programmed by COINCHG_OFF during the system-on states.

If a power up event is started and any of the TRIM_NOK, OTP_NOK or STEST_NOK flags are asserted, the device ignores the power up event and remains in the QPU_Off state. See Section 17 "OTP/TBB and default configurations" for more details on debugging a fuse loading failure.

Upon a power up event, the default configuration from OTP or hardwire is loaded into their corresponding I^2C functional register in the transition from QPU_Off to power up state.

13.1.5 Power up sequence

During the power up sequence, the external regulators are turned on in a predefined order as programmed by the default (OTP or hardwire) sequence.

If PGOOD is used as a GPO, it can also be set high as part of the power up sequence in order to allow sequencing of any external supply/device controlled by the PGOOD pin.

The RESETBMCU is also programmed as part of the power up sequence, and it is used as the condition to enter system-on states. The RESETBMCU may be released in the middle of the power up sequence, in this case, the remaining supplies in the power up continues to power up as the device is in the run state. See Section 14.5.2 "Power up sequencing" for details.

13.1.6 System-on states

During the system-on states, the MCU is powered and out of reset and the system is fully operational.

The system on is a virtual state composed by two modes of operations:

- Run state
- Standby state

Register to control the regulators output voltage, regulator enable, interrupt masks, and other miscellaneous functions can be written to or read from the functional I^2C register map during the system-on states.

13.1.6.1 Run state

If the power up state is successfully completed, the state machine transitions to the run state. In this state, RESETBMCU is released high, and the MCU is expected to boot up and set up specific registers on the PMIC as required during the system boot up process.

The run mode is intended to be used as the normal mode of operation for the system.

Each regulator has specific registers to control its output voltage, operation mode and/or enable/disable state during the run state.

By default, the VSWx_RUN[7:0] / VLDOx_RUN[3:0] registers are loaded with the data stored in the OTP_VSWx[7:0] or OTP_VLDOx[3:0] bits respectively.

SW7 uses only one global register to configure the output voltage during run or standby mode. Upon power up the VSW7[4:0] bits are loaded with the values of the OTP_VSW7[4:0].

Upon power up, if the switching regulator is part of the power up sequence, the SWx_RUN_MODE[1:0] bits will be loaded as needed by the system:

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

- When OTP_SYNCIN_EN = 1, default SWx_RUN_MODE at power up is always set to PWM (0b01)
- When OTP_SYNCOUT_EN = 1, default SWx_RUN_MODE at power up is always set to PWM (0b01)
- When OTP_FSS_EN = 1, default SWx_RUN_MODE at power up shall always set to PWM (0b01)
- If none of the above conditions are met, the default value of the SWx_RUN_MODE bits at power up will be set by the OTP_SW_MODE bits.

When OTP_SW_MODE = 0, the default value of the SWx_RUN_MODE bits are set to 0b11 (autoskip).

When OTP_SW_MODE = 1, the default value of the SWx_RUN_MODE bits are set to 0b01 (PWM).

If the switching regulator is not part of the power up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b00 (OFF mode).

Likewise, if the LDO is part of the power up sequence, the LDOx_RUN_EN bit is set to 1 (enabled) by default. If the LDO is not selected as part of the power up sequence, the LDOx_RUN_EN bit is set to 0 (disabled) by default.

In a typical system, each time the processor boots up (PMIC transitions from off mode to run state), all output voltage configurations are reset to the default OTP configuration, and the MCU should configure the PMIC to its desired usage in the application.

13.1.6.2 Standby state

The standby state is intended to be used as a low power (state retention) mode of operation. In this state, the voltage regulators can be preset to a specific low power configuration in order to reduce the power consumption during system's sleep or state retention modes of operations.

The standby state is entered when the STANDBY pin is pulled high or low as defined by the STANBYINV bit. The STANDBY pin is pulled high/low by the MCU to enter/exit system low power mode. See Section 14.9.2 "STANDBY" for detailed configuration of the STANDBY pin.

Each regulator has specific registers to control its output voltage, operation mode and/or enable/disable state during the standby state.

By default, the VSWx_STBY[7:0] / VLDOx_STBY[3:0] registers are loaded with the data stored in the OTP_VSWx[7:0] or OTP_VLDOx[3:0] bits respectively.

Upon power up, if the switching regulator is part of the power up sequence, the SWx_STBY_MODE[1:0] bits will be loaded as needed by the system:

- When OTP_SYNCIN_EN = 1, default SWx_STBY_MODE at power up is always set to PWM (0b01)
- When OTP_SYNCOUT_EN = 1, default SWx_STBY_MODE at power up is always set to PWM (0b01)
- When OTP_FSS_EN = 1, default SWx_STBY_MODE at power up shall always set to PWM (0b01)
- If none of the conditions above are met, the default value of the SWx_STBY_MODE bits at power up will be set by the OTP_SW_MODE bits.

When OTP_SW_MODE = 0, the default value of the SWx_STBY_MODE bits are set to 0b11 (autoskip).

When OTP_SW_MODE = 1, the default value of the SWx_STBY_MODE bits are set to 0b01 (PWM).

If the switching regulator is not part of the power up sequence, the SWx_STBY_MODE[1:0] bits are loaded with 0b00 (OFF mode).

Likewise, if the LDO is part of the power up sequence, the LDOx_RUN_EN bit is set to 1 (enabled) by default. If the LDO is not selected as part of the power up sequence, the LDOx_RUN_EN bit is set to 0 (disabled) by default.

Upon power up, the standby registers are loaded with the same default OTP values as the run mode. The MCU is expected to program the desired standby values during boot up.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

If any of the external regulators are disabled in the standby state, the power down sequencer is engaged as described in Section 14.6.2 "Power down sequencing".

13.1.7 WD_Reset

When a hard watchdog reset is present, the state machine increments the WD_EVENT_CNT[3:0] register and compares against the WD_MAX_CNT[3:0] register. If WD_EVENT_CNT[3:0] = WD_MAX_CNT[3:0], the state machine detects a cyclic watchdog failure, it powers down the external regulators and proceeds to the fail-safe transition.

If WD_EVENT_CNT[3:0] < WD_MAX_CNT[3:0], the state machine performs a hard WD reset.

A hard WD reset can be generated from either a transition in the WDI pin or a WD event initiated by the internal watchdog counter as described in Section 15.11.2 "Watchdog reset behaviors".

13.1.8 Power down state

During power down state, all regulators except VSNVS are disabled as configured in the power down sequence. The power down sequence is programmable as defined in Section 14.6.2 "Power down sequencing".

Two types of events may lead to the power down sequence:

- Non faulty turn off events: move directly into LP_Off state as soon as power down sequence is finalized
- Turn off events due to a PMIC fault: move to the fail-safe transition as soon as the power down sequence is finalized

13.1.9 Fail-safe transition

The fail-safe transition is entered if the PF8100/PF8200 initiates a turn off event due to a PMIC fault.

If the fail-safe transition is entered, the PF8100/PF8200 provides four FAIL bits to indicate the source of the failure:

- The PU_FAIL is set to 1 when the device shuts down due to a power up failure
- The WD_FAIL is set to 1 when the device shuts down due to a watchdog event counter max out
- The REG_FAIL is set to 1 when the device shuts down due to a regulator failure (fault counter maxed out or fault timer expired)
- The TSD_FAIL is set to 1 when the device shuts down due to a thermal shutdown

The value of the FAIL bits is retained as long as VIN > UVDET.

The MCU can read the FAIL bits during the system-on states in order to obtain information about the previous failure and can clear them by writing a 1 to them, provided the state machine is able to power up successfully after such failure.

In PF8200, when the state machine enters the fail-safe transition, a fail-safe counter is compared and increased, if the FS_CNT[3:0] reaches the maximum count, the device can be programmed to move directly to the fail-safe state to prevent a cyclic failure from happening.

13.1.10 Fail-safe state (PF8200 only)

The fail-safe state works as a safety lock-down upon a critical device/system failure. It is reached when the FS_CNT [3:0] = FS_MAX_CNT [3:0].

A bit is provided to enable or disable the device to enter the fail-safe state upon a cyclic failure. When the OTP_FS_BYPASS = 1, the fail-safe bypass operation is enabled and the device always move to the LP_Off state, regardless of the value of the FS_CNT[3:0]. If the OTP_FS_BYPASS = 0, the fail-safe bypass is disabled, and the device moves to the fail-safe state when the proper condition is met.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The maximum number of times the device can pass through the fail-safe transition continuously prior to moving to a fail state is programmed by the OTP_FS_MAX_CNT[3:0] bits. If the FS_MAX_CNT[3:0] = 0x00, the device moves into the fail-safe state as soon as it fails for the very first time.

If the FSOB pin is programmed to assert upon a specific fault, the FSOB pin remains asserted low during the fail-safe state if the corresponding fault is present when PF8200 reaches the fail-safe state.

The device can exit the fail-safe state only after a power cycle (VIN crossing UVDET) event is present.

To avoid reaching the fail-safe state due to isolated fail-safe transition events, the FS_CNT [3:0] is gradually decreased based on a fail-safe OK timer. The OTP_FS_OK_TIME[2:0] bits select the default time configuration for the fail-safe OK timer between 1 to 60 min.

Table 12. Fail-safe OK timer configuration

OTP_FS_OK_TIME[2:0]	FS_CNT decrease period (min)
000	1
001	5
010	10
011	15
100	20
101	30
110	45
111	60

When the fail-safe OK timer reaches the configured time during the system-on states, the state machine decreases the FS_CNT[3:0] bits by one and starts a new count until the FS_CNT[3:0] is 0x00. The FS_CNT[3:0] may be manually cleared during the system on state if the system wants to control this counter manually.

13.1.11 Coin cell state

When VIN is not present and LICELL pin has a valid voltage, the device is placed into a coin cell state. In such state, only VSNVS remains on (if programmed to do so by the OTP_VSNVSVOTL[1:0] bits) and is expected to provide power to the SNVS domain on the MCU as long as the LICELL pin has a valid input suitable to supply the configured VSNVS output voltage.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

14 General device operation

14.1 UVDET

UVDET works as the main operation threshold for the PF8100/PF8200. Crossing UVDET on the rising edge is a mandatory condition for OTP fuses to be loaded into the mirror registers and allows the main PF8100/PF8200 operation.

If VIN is below the UVDET threshold, the device remains in an unpowered state if no valid LICELL is present, or in the LICELL mode if a valid LICELL voltage is present. A 200 mV hysteresis is implemented on the UVDET comparator to set the falling threshold.

Table 13. UVDET threshold

Symbol	Parameter	Min	Typ	Max	Unit
UVDET	Rising UVDET	2.7	2.8	2.9	V
UVDET	Falling UVDET	2.5	2.6	2.7	V

14.2 VIN OVLO condition

The VIN_OVLO circuit monitors the main input supply of the PF8100/PF8200. When this block is enabled, the PF8100/PF8200 monitors its input voltage and can be programmed to react to an overvoltage in two ways:

- When the VIN_OVLO_SDWN = 0, the VIN_OVLO event triggers an OVLO interrupt but does not turn off the device
- When the VIN_OVLO_SDWN = 1, the VIN_OVLO event initiates a power down sequence

When the VIN_OVLO_EN = 0, the OVLO monitor is disabled and when the VIN_OVLO_EN = 1, the OVLO monitor is enabled. The default configuration of the VIN_OVLO_EN bit is set by the OTP_VIN_OVLO_EN bit in OTP. Likewise, the default value of the VIN_OVLO_SDWN bit is set by the OTP_VIN_OVLO_SDWN upon power up.

During a power up transition, if the OTP_VIN_OVLO_SDWN = 0 the device allows the external regulators to come up and the PF8100/PF8200 announces the VIN_OVLO condition through an interrupt. If the OTP_VIN_OVLO_SDWN = 1, the device stops the power up sequence and returns to the corresponding off mode.

Debounce on the VIN_OVLO comparator is programmable to 10 µs, 100 µs or 1.0 ms, by the VIN_OVLO_DBNC[1:0] bits. The default value for the VIN_OVLO debounce is set by the OTP_VIN_OVLO_DBNC[1:0] bits upon power up.

Table 14. VIN_OVLO debounce configuration

VIN_OVLO_DBNC[1:0]	VIN OVLO debounce value (µs)
00	10
01	100
10	1000
11	Reserved

Table 15. VIN_OVLO specifications

Symbol	Parameter	Min	Typ	Max	Unit
VIN_OVLO	VIN overvoltage lockout rising [1]	5.55	5.8	6.0	V
VIN_OVLO_HYS	VIN overvoltage lockout hysteresis [1]	—	—	200	mV

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

[1] Operating the device above the maximum VIN = 5.5 V for extended periods of time may degrade and cause permanent damage to the device.

14.3 IC startup timing with PWRON pulled up

The PF8100/PF8200 features a fast internal core power up sequence to fulfill system power up timings of 5.0 ms or less, from power application until MCU is out of reset. Such requirement needs a maximum ramp up time of 1.5 ms for VIN to cross the UVDET threshold in the rising edge.

A maximum core biasing time of 1.5 ms from VIN crossing to UVDET until the beginning of the power up sequence is ensured to allow up to 1.5 ms time frame for the voltage regulators power up sequence.

Timing for the external regulators to start up is programmed by default in the OTP fuses.

The 5.0 ms power up timing requirement is only applicable when the PWRON pin operates in level sensitive mode OTP_PWRON_MODE = 0, however turn on timing is expected to be the same for both level or edge sensitive modes after the power on event is present.

In applications using the VSNVS regulator, if VSNVS is required to reach regulation before system regulators come up, the system should use the SEQ[7:0] bits to delay the system regulators to allow enough time for VSNVS to reach regulation before the power up sequence is started.

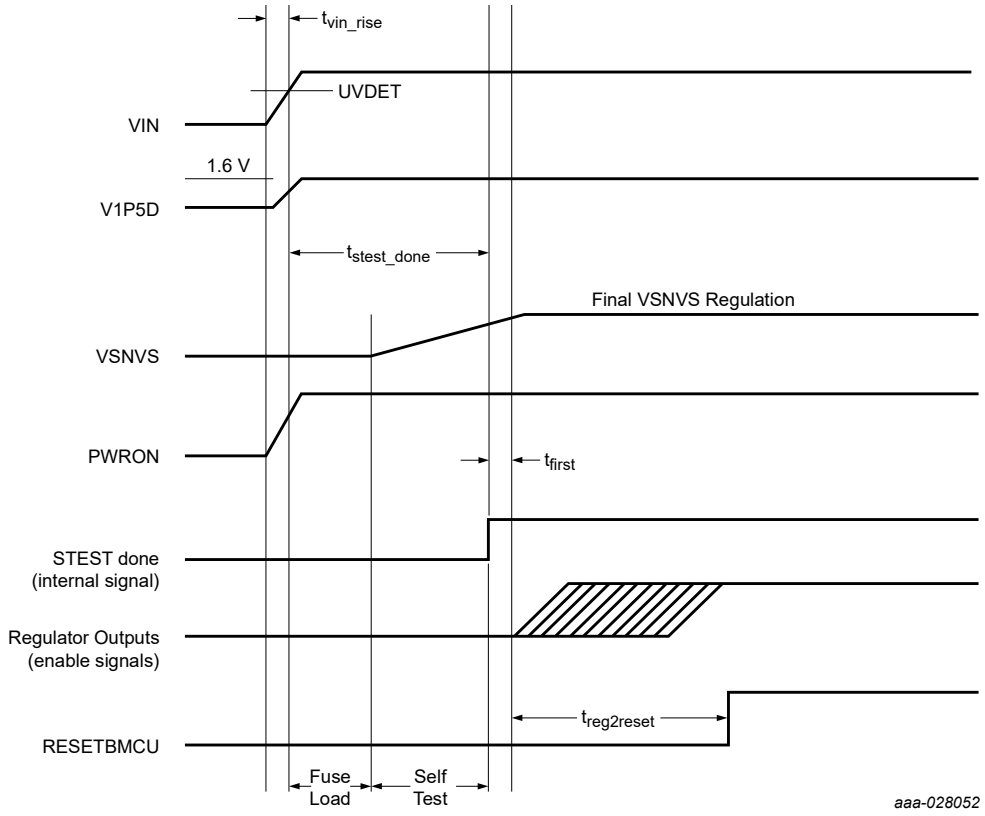


Figure 6. Startup with PWRON pulled up

Table 16. Startup timing requirements (PWRON pulled up)

Symbol	Parameter	Min	Typ	Max	Unit
t_{vin_rise}	Rise time of VIN from VPWR application to UVDET (system dependent)	10	—	1500	µs
t_{stest_done}	Time from VIN crossing UVDET to STEST_done going high (self-test performed and passed)	—	—	1.4	ms

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 16. Startup timing requirements (PWRON pulled up) *...continued*

Symbol	Parameter	Min	Typ	Max	Unit
t_{first}	Time from STEST_done to first slot of power up sequence	—	—	100	µs
$t_{reg2reset}$	Time from first regulator enabled to RES ETBMCU asserted to guarantee 5.0 ms PMIC boot up [1]	—	—	1.5	ms

[1] External regulators power up sequence time ($t_{reg2reset}$) is programmed by OTP and may be longer than 1.5 ms. However, 1.5 ms is the maximum allowed time to ensure power up within 5.0 ms.

14.4 IC startup timing with PWRON pulled low during VIN application

It is possible that PWRON is held low when VIN is applied. By default, LPM_OFF bit is reset to 0 upon crossing UVDET, therefore the PF8100/PF8200 remains in the LP_Off state as described in Section 13.1.2 "LP_Off state". In this scenario, quiescent current in the LP_Off state is kept to a minimum. When PWRON goes high with LPM_OFF = 0, the PMIC startup is expected to take longer, since it has to enable most of the internal circuits and perform the self-test before starting a power up sequence.

Figure 7 shows startup timing with LPM_OFF = 0.

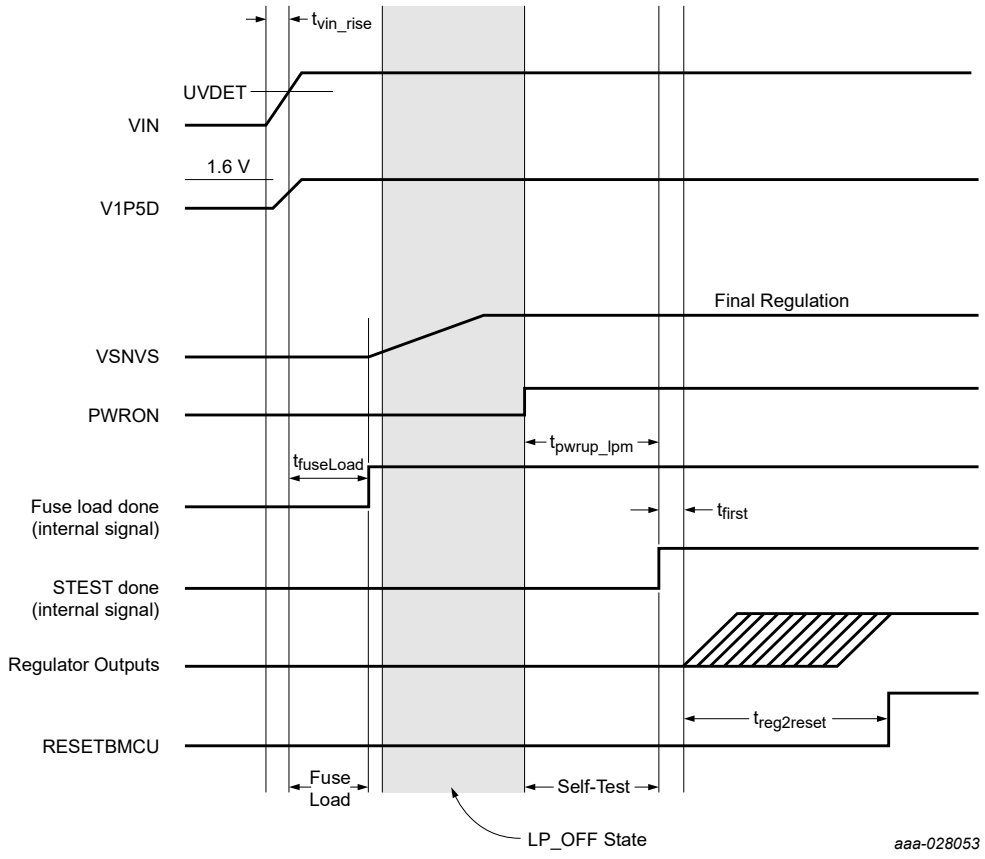


Figure 7. Startup with PWRON driven high externally and bit LPM_OFF = 0

Table 17. Startup with PWRON driven high externally and LPM_OFF = 0

Symbol	Parameter	Min	Typ	Max	Unit
t_{vin_rise}	Rise time of VIN from VPWR application to UVDET (system dependent)	10	—	1500	µs

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 17. Startup with PWRON driven high externally and LPM_OFF = 0*...continued*

Symbol	Parameter	Min	Typ	Max	Unit
$t_{fuseload}$	Time from VIN crossing UVDET to Fuse_Load_ done (fuse loaded correctly)	—	—	600	µs
t_{pwrup_lpm}	Time from PWRON going high to the STEST_ done (self-test performed and passed)	—	—	700	µs
t_{first}	Time from STEST_done to first slot of power up sequence	—	—	100	µs
$t_{reg2reset}$	Time from first regulator enabled to RES ETBMCU asserted to guarantee 5.0 ms PMIC boot up [1]	—	—	1.5	ms

[1] External regulators power up sequence time ($t_{reg2reset}$) is programmed by OTP and may be longer than 1.5 ms.

14.5 Power up

14.5.1 Power up events

Upon a power cycle (VIN > UVDET), the LPM_OFF bit is reset to 0, therefore the device moves to the LP_Off state by default. The actual value of the LPM_OFF bit can be changed during the run mode and is maintained until VIN crosses the UVDET threshold.

In either one of the off modes, the PF8100/PF8200 can be enabled by the following power up events:

1. When OTP_PWRON_MODE = 0, PWRON pin is pulled high.
2. When OTP_PWRON_MODE = 1, PWRON pin experiences a high to low transition and remains low for as long as the PWRON_DBNC timer.

A power up event is valid only if:

- VIN > UVDET
- VIN < VIN_OVLO (unless the OVLO is disabled or OTP_VIN_OVLO_SDWN = 0)
- Tj < thermal shutdown threshold
- TRIM_NOK = 0 && OTP_NOK = 0 && STEST_NOK = 0

14.5.2 Power up sequencing

The power up sequencer controls the time and order in which the voltage regulators and other controlling I/O are enabled when going from the off mode into the run state.

The OTP_SEQ_TBASE[1:0] bits set the default time base for the power up and power down sequencer.

The SEQ_TBASE[1:0] bits can be modified during the system-on states in order to change the sequencer timing during run/standby transitions as well as the power down sequence.

Table 18. Power up time base register

OTP bits OTP_SEQ_TBASE[1:0]	Functional bits SEQ_TBASE[1:0]	Sequencer time base (µs)
00	00	30
01	01	120
10	10	250
11	11	500

The power up sequence may include any of the following:

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

- Switching regulators
- LDO Regulators
- PGOOD pin if programmed as a GPO
- RESETBMCU

The default sequence slot for each one of these signals is programmed via the OTP configuration registers. And they can be modified in the functional I^2C register map to change the order in which the sequencer behaves during the run/standby transitions as well as the power down sequence.

The _SEQ[7:0] bits set the regulator/pin sequence from 0 to 254. Sequence code 0x00 indicates that the particular output is not part of the startup sequence and remains in off (in case of a regulator) or remains low/disabled (in case of PGOOD pin used as a GPO).

Table 19. Power up sequence registers

OTP bits OTP_SWx_SEQ[7:0]/ OTP_LDOx_SEQ[7:0]/ OTP_PGOOD_SEQ[7:0]/ OTP_RESETBMCU_SEQ[7:0]	Functional bits SWx_SEQ[7:0]/ LDOx_SEQ[7:0]/ PGOOD_SEQ[7:0]/ RESETBMCU_SEQ[7:0]	Sequence slot	Startup time (µs)
00000000	00000000	Off	Off
00000001	00000001	0	SLOT0 (right after PWRON event is valid)
00000010	00000010	1	SEQ_TBASE x SLOT1
. . .	. . .	. . .	. . .
11111111	11111111	254	SEQ_TBASE x SLOT254

If RESETBMCU is not programmed in the OTP sequence, it will be enabled by default after the last regulator programmed in the power up sequence.

When the _SEQ[7:0] bits of all regulators and PGOOD used as a GPIO are set to 0x00 (off) and a power on event is present, the device moves to the run state in secondary mode. In this mode, the device is enabled without any voltage regulator or GPO enabled. If the RESETBMCU is not programed in a power up sequence slot, it is released when the device enters the run state.

The secondary mode is a special case of the power up sequence to address the scenario where the PF8100/PF8200 is working as a secondary PMIC, and supplies are meant to be enabled by the MCU during the system operation. In this scenario, if RESETBMCU is used, it is connected to the primary RESETBMCU pin.

The PWRUP_I interrupt bit is asserted at the end of the power up sequence when the time slot of the last regulator in the sequence has ended.

Figure 8 provides an example of the power up/down sequence coming from the off modes.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

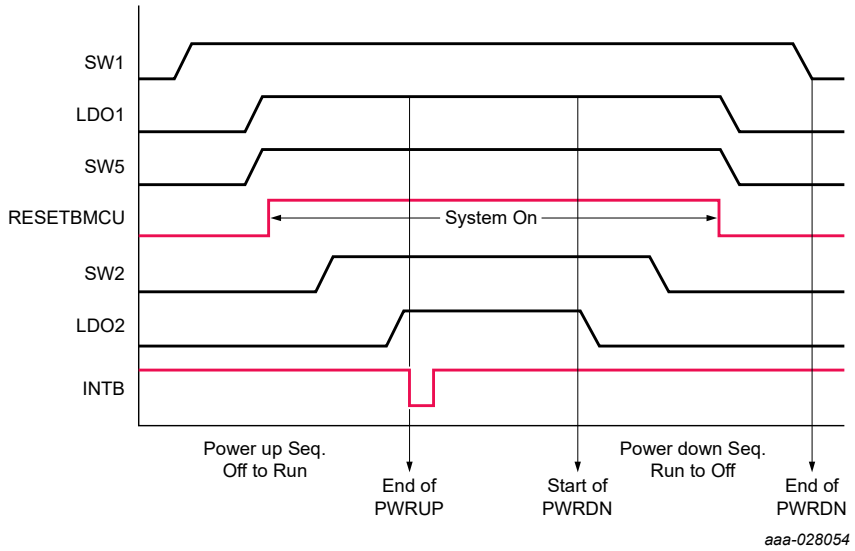


Figure 8. Power up/down sequence between off and system-on states

When transitioning from standby mode to run mode, the power up sequencer is activated only if any of the external regulators is re-enabled during this transition. If none of the regulators toggle from off to on and only voltage changes are being performed when entering or exiting standby mode, the changes for the voltage regulators are made simultaneously rather than going through the power up sequencer.

Figure 9 shows an example of the power up/down sequence when transitioning between run and standby modes.

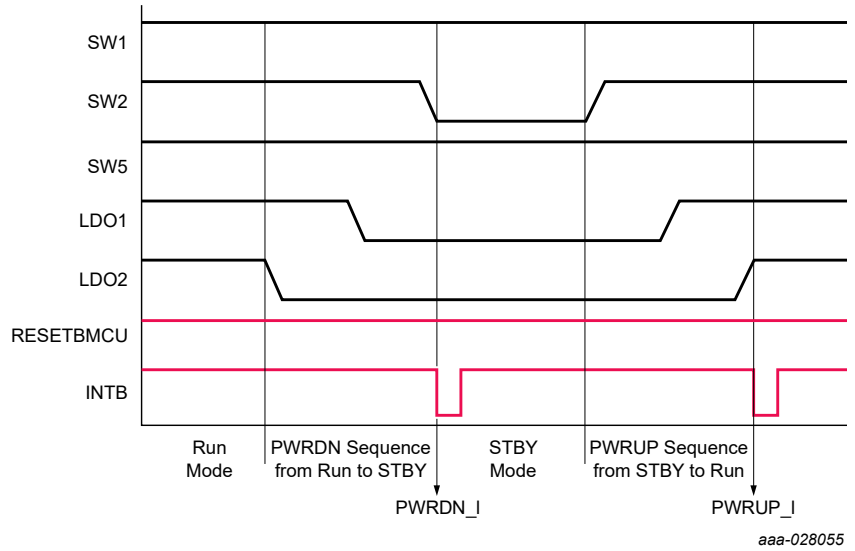


Figure 9. Power up/down sequence between run and standby

The PWRUP_I interrupt is set while transitioning from standby to run, even if the sequencer is not used. This is used to indicate that the transition is complete and device is ready to perform proper operation.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

14.6 Power down

14.6.1 Turn off events

Turn off events may be requested by the MCU (non-PMIC fault related) or due to a critical failure of the PMIC (hard fault condition).

The following are considered non-PMIC failure turn off events:

1. When OTP_PWRON_MODE = 0, the device starts a power down sequence when the PWRON pin is pulled low.
2. When OTP_PWRON_MODE = 1, the device starts a power down sequence when the PWRON pin sees a transition from high to low and remains low for longer than TRESET.
3. When bit PMIC_OFF is set to 1, the device starts a 500 µs shutdown timer. When the shutdown timer is started, the PF8100/PF8200 sets the SDWN_I interrupt and asserts the INTB pin provided it is not masked. At this point, the MCU can read the interrupt and decide whether to continue with the turn off event or stop it in case it was sent by mistake.
   If the SDWN_I bit is cleared before the 500 µs shutdown timer is expired, the shutdown request is cancelled and the shutdown timer is reset; otherwise, if the shutdown timer is expired, the PF8100/PF8200 starts a power down sequence.
   The PMIC_OFF bit self-clears after SDWN_I flag is cleared.
4. When VIN_OVLO_EN = 1 and VIN_OVLO_SDWN = 1, and a VIN_OVLO event is present.

Turn off events due to a hard fault condition:

1. If an OV, UV or ILIM condition is present long enough for the fault timer to expire.
2. In the event that an OV, UV or ILIM condition appears and clears cyclically, and the FAULT_CNT[3:0] = FAULT_MAX_CNT[3:0].
3. If the watchdog fail counter is overflown, that is WD_EVENT_CNT = WD_MAX_CNT.
4. When Tj crosses the thermal shutdown threshold as the temperature rises.

When the PF8100/PF8200 experience a turn off event due to a hard fault condition, the devices pass through the fail-safe transition after regulators have been powered down.

14.6.2 Power down sequencing

During a power down sequence, output voltage regulators can be turned off in two different modes as defined by the PWRDWN_MODE bit.

1. When PWRDWN_MODE = 0, the regulators power down in sequential mode.
2. When PWRDWN_MODE = 1, the regulators power down by groups.

During transition from run to standby, the power down sequencer is activated in the corresponding mode. If any of the external regulators are turned off in the standby configuration. If external regulators are not turned off during this transition, the power down sequencer is bypassed and the transition happens at once (any associated DVS transitions could still take time).

The PWRDN_I interrupt is set at the end of the transition from run to standby when the last regulator has reached its final state, even if external regulators are not turned off during this transition.

14.6.2.1 Sequential power down

When the device is set to the sequential power down, it uses the same _SEQ[7:0] registers as the power up sequence to power down in reverse order.

All regulators with the _SEQ[7:0] bits set to 0x00, power down immediately and the remaining regulators power down one OTP_SEQ_TBASE[1:0] delay after, in reverse order as defined in the _SEQ[7:0] bits.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

If PGOOD pin is used as a GPO, it is de-asserted as part of the power down sequence as indicated by the PGOOD_SEQ[7:0] bits.

If the MCU requires a different power down sequence, it can change the values of the SEQ_TBASE[1:0] and the _SEQ[7:0] bits during the system-on states.

When the state machine pass through any of the off modes, the contents of the SEQ_TBASE[1:0] and _SEQ[7:0] bits are reloaded with the corresponding mirror register (OTP) values before it starts the next power up sequence.

14.6.2.2 Group power down

When the device is configured to power down in groups, the regulators are assigned to a specific power down group. All regulators assigned to the same group are disabled at the same time when the corresponding group is due to be disabled.

Power down groups shut down in decreasing order starting from the lowest hierarchy group with a regulator shutting down (for instance, Group 4 being the lowest hierarchy and Group 1 the highest hierarchy group). If no regulators are set to the lowest hierarchy group, the power down sequence timer starts off the next available group that contains a regulator to power down.

Each regulator has its own _PDGRP[1:0] bits to set the power down group it belongs to as shown in Table 20.

Table 20. Power down regulator group bits

OTP_SWx_PDGRP[1:0] OTP_LDOx_PDGRP[1:0] OTP_PGOOD_PDGRP[1:0] OTP_RESETBMCU_PDGRP[1:0]	SWx_PDGRP[1:0] LDOx_PDGRP[1:0] PGOOD_PDGRP[1:0] RESETBMCU_PDGRP[1:0]	Description
00	00	Regulator belongs to Group 4
01	01	Regulator belongs to Group 3
10	10	Regulator belongs to Group 2
11	11	Regulator belongs to Group 1

If PGOOD pin is used as a GPO, the PGOOD_PDGRP[1:0] is used to turn off the PGOOD pin in a specific group during the power down sequence. If PGOOD pin is used in power good mode, it is recommended that the OTP_PGOOD_PDGRP bits are set to 11 to ensure the group power down sequencer does not detect these bits as part of Group 4.

Each one of power down groups have programmable time delay registers to set the time delay after the regulators in this group have been turned off, and the next group can start to power down.

Table 21. Power down counter delay

OTP bits OTP_GRPx_DLY[1:0]	Functional bits GRPx_DLY[1:0]	Power down delay (µs)
00	00	120
01	01	250
10	10	500
11	11	1000

If RESETBMCU is required to be asserted first before any of the external regulators from the corresponding group, the RESETBMCU_DLY provides a selectable delay to disable the regulators after RESETBMCU is asserted.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 22. Programmable delay after RESETBMCU is asserted

OTP bits OTP_RESETBMCU_DLY[1:0]	Functional bits RESETBMCU_DLY[1:0]	RESETBMCU delay (µs)
00	00	No delay
01	01	10
10	10	100
11	11	500

If RESETBMCU_DLY is set to 0x00, all regulators in the same power down group as RESETBMCU is disabled at the same time RESETBMCU is asserted.

Figure 10 shows an example of the power down sequence when PWRDWN_MODE = 1.

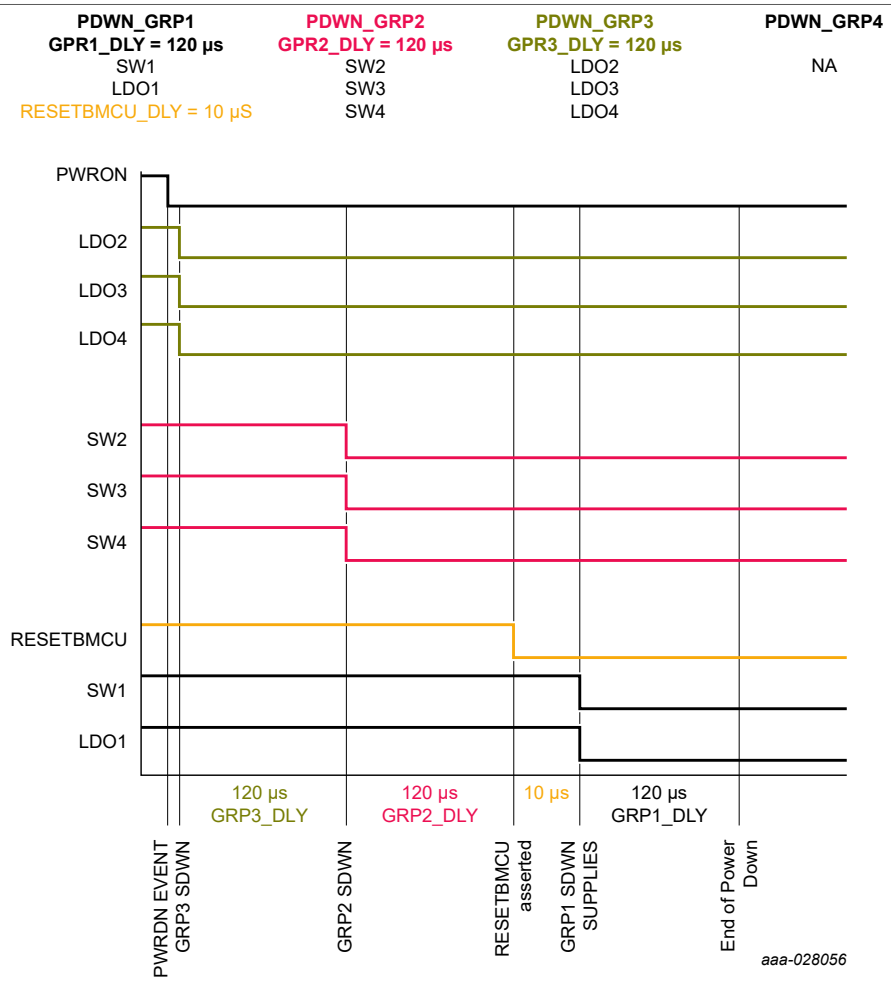


Figure 10. Group power down sequence example

14.6.2.3 Power down delay

After a power down sequence is started, the PWRON pin shall be masked until the sequence is finished and the programmable power down delay is reached, then the device can power up again if a power-up event is present. The power down delay time can be programed on OTP via the OTP_PD_SEQ_DLY[1:0] bits.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 23. Power down delay selection

OTP_PD_SEQ_DLY[1:0]	Delay after power down sequence
00	No delay
01	1.5 ms
10	5.0 ms
11	10 ms

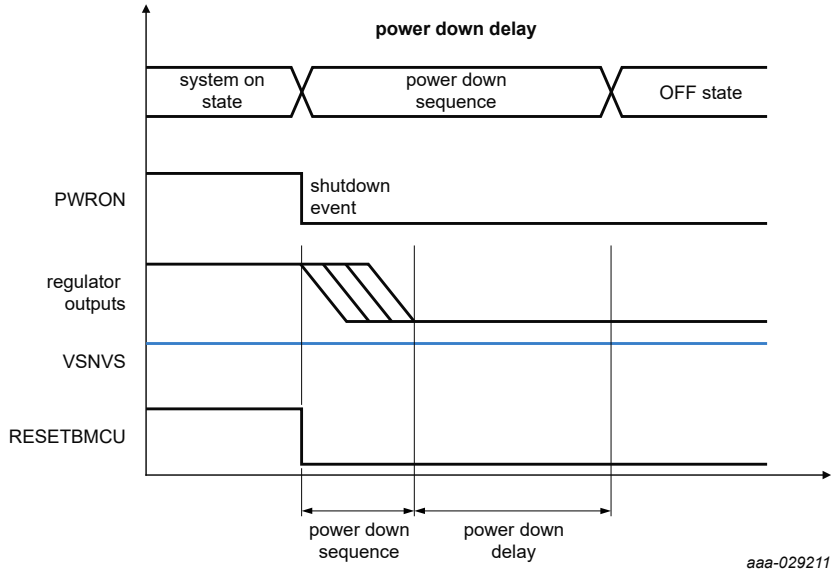


Figure 11. Power down delay

The default value of the OTP_PD_SEQ_DLY[1:0] bits on an unprogrammed OTP device shall be 00.

14.7 Fault detection

Three types of faults are monitored per regulator: UV, OV and ILIM. Faults are monitored during power up sequence, run, standby and WD reset states. A fault event is notified to the MCU through the INTB pin if the corresponding fault is not masked.

The fault configuration registers are reset to their default value after the power up sequences, and system must configure them as required during the boot-up process via I^2C commands.

For each type of fault, there is an I^2C bit that is used to select whether the regulator is kept enabled or disabled when the corresponding regulator experience a fault event.

SWx_ILIM_STATE / LDOx_ILIM_STATE

- 0 = regulator disable upon an ILIM fault event
- 1 = regulator remains on upon an ILIM fault event

SWx_OV_STATE / LDOx_OV_STATE

- 0 = regulator disable upon an OV fault event
- 1 = regulator remains on upon an OV fault event

SWx_UV_STATE / LDOx_UV_STATE

- 0 = regulator disable upon an UV fault event
- 1 = regulator remains on upon an UV fault event

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The following table lists the functional bits associated with enabling/disabling the external regulators when they experience a fault.

Table 24. Regulator control during fault event bits

Regulator	Bit to disable the regulator during current limit	Bit to disable the regulator during undervoltage	Bit to disable the regulator during overvoltage
SW1	SW1_ILIM_STATE	SW1_UV_STATE	SW1_OV_STATE
SW2	SW2_ILIM_STATE	SW2_UV_STATE	SW2_OV_STATE
SW3	SW3_ILIM_STATE	SW3_UV_STATE	SW3_OV_STATE
SW4	SW4_ILIM_STATE	SW4_UV_STATE	SW4_OV_STATE
SW5	SW5_ILIM_STATE	SW5_UV_STATE	SW5_OV_STATE
SW6	SW6_ILIM_STATE	SW6_UV_STATE	SW6_OV_STATE
SW7	SW7_ILIM_STATE	SW7_UV_STATE	SW7_OV_STATE
LDO1	LDO1_ILIM_STATE	LDO1_UV_STATE	LDO1_OV_STATE
LDO2	LDO2_ILIM_STATE	LDO2_UV_STATE	LDO2_OV_STATE
LDO3	LDO3_ILIM_STATE	LDO3_UV_STATE	LDO3_OV_STATE
LDO4	LDO4_ILIM_STATE	LDO4_UV_STATE	LDO4_OV_STATE

ILIM faults are debounced for 1.0 ms before they can be detected as a fault condition. If the regulator is programed to disable upon an ILIM condition, the regulator turns off as soon as the ILIM condition is detected.

OV/UV faults are debounced as programmed by the OV_DB and UV_DB registers, before they are detected as a fault condition. If the regulator is programmed to disable upon an OV or UV, the regulator will turn off if the fault persist for longer than 300 µs after the OV/UV fault has been detected.

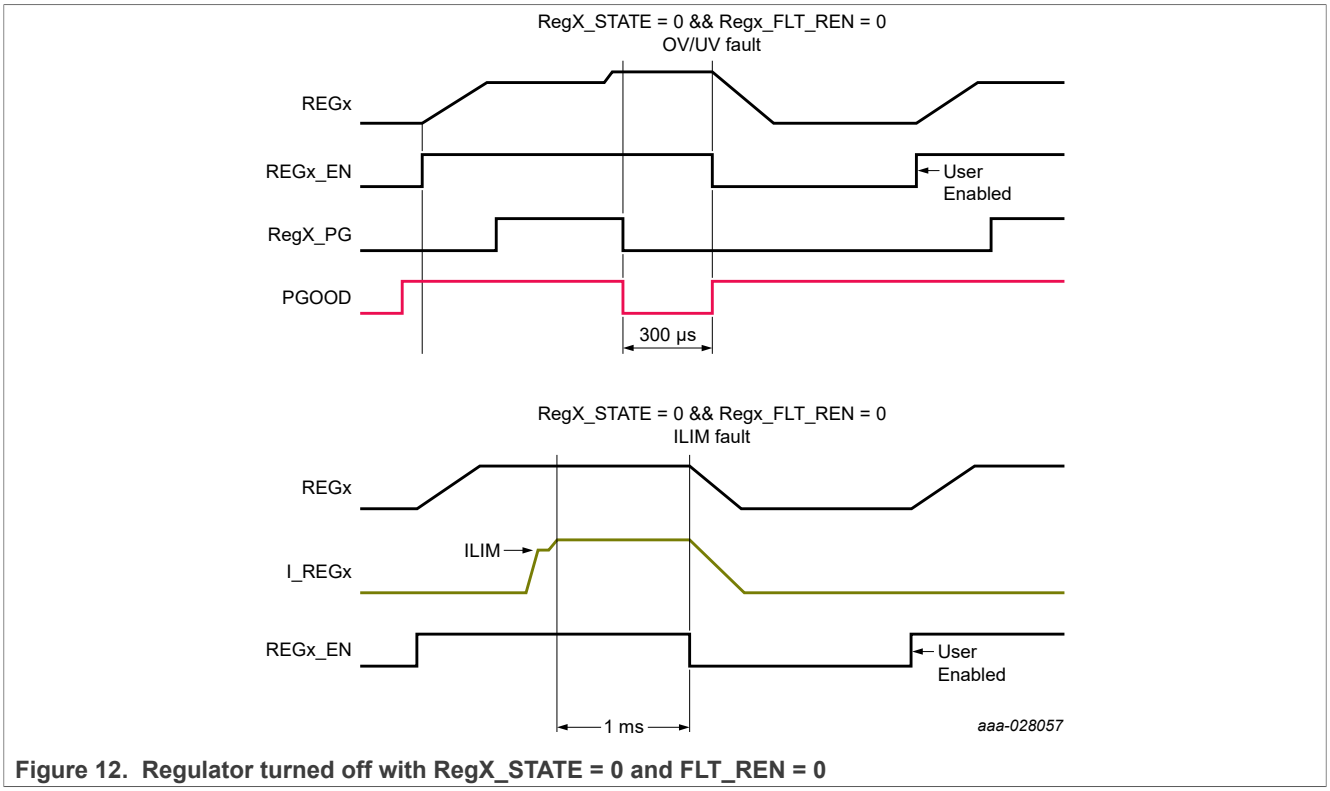


Figure 12. Regulator turned off with RegX_STATE = 0 and FLT_REN = 0

When a regulator is programmed to disable upon an OV, UV, or ILIM fault, a bit is provided to decide whether a regulator can return to its previous configuration or remain disabled when the fault condition is cleared.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

SWx_FLT_REN / LDOx_FLT_REN

- 0 = regulator remains disabled after the fault condition is cleared or no longer present
- 1 = regulator returns to its previous state if fault condition is cleared

If a regulator is programmed to remain disabled after clearing the fault condition, the MCU can turn it back on during the system on states by toggling off and on the corresponding mode/enable bits.

When the bit SWx_FLT_REN = 1, if a regulator is programmed to turn off upon an OV, UV or ILIM condition, the regulator returns to its previous state 500 µs after the fault condition is cleared. If the regulator is programmed to turn off upon an ILIM condition, the device may take up to 1.0 ms to debounce the ILIM condition removal, in addition to the 500 µs wait period to re-enable the regulator.

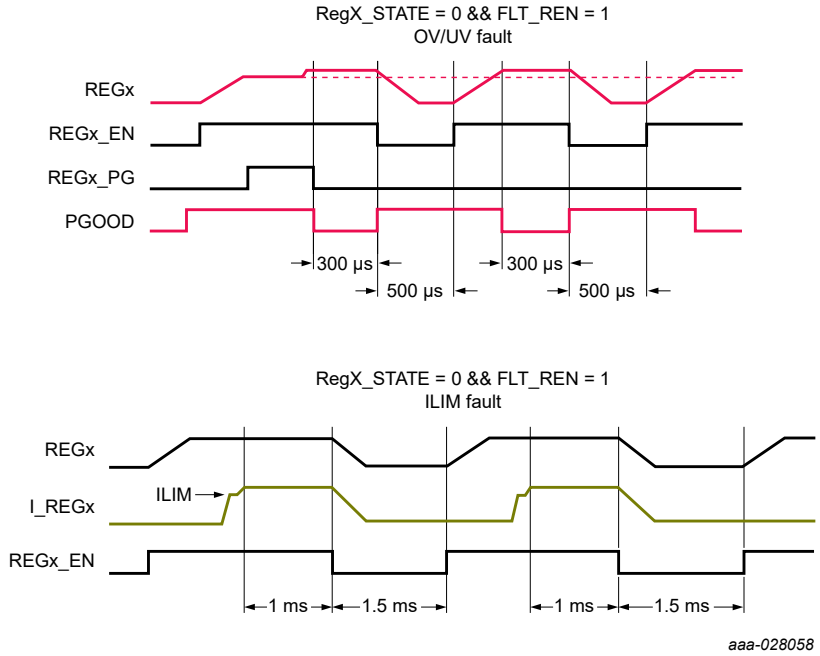


Figure 13. Regulator turned off with RegX_STATE = 0 and FLT_REN = 1

When the LDO2 is controlled by hardware using the LDO2EN pin and programmed to turn off upon an OV, UV or ILIM fault, the LDO2_FLT_REN bit still controls whether the regulator returns to its previous state or not regardless the state of the LDO2EN pin.

If LDO2 controlled by LDO2EN pin is instructed to remain disabled by the LDO2_FLT_REN bit, it recovers hardware control by modifying the LDO2_EN bits in the I^2C register maps. See Section 14.9.10 "LDO2EN" for details on hardware control of LDO2 regulator.

To avoid fault cycling, a global fault counter is provided. Each time any of the external regulators encounter a fault event, the PF8100/PF8200 compares the value of the FAULT_CNT[3:0] against the FAULT_MAX_CNT, and if it not equal, it increments the FAULT_CNT[3:0] and proceeds with the fault protection mechanism.

The processor is expected to read the counter value and reset it when the faults have been cleared and the device returns to a normal operation. If the processor does not reset the fault counter and it equals the FAULT_MAX_CNT[3:0] value, the state machine initiates a power down sequence.

The default value of the FAULT_MAX_CNT[3:0] is loaded from the OTP_FAULT_MAX_CNT[3:0] bits during the power up sequence.

When the FAULT_MAX_CNT[3:0] is set to 0x00, the system disables the turn-off events due to a Fault Counter maxing out.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

When a regulator experiences a fault event, a fault timer is started. While this timer is in progress, the expectation is that the processor takes actions to clear the fault. For example, it could reduce its load in the event of a current limit fault, or turn off the regulator in the event of an overvoltage fault.

If the fault clears before the timer expires, the state machine resumes the normal operation, and the fault timer gets reset. If the fault does not clear before the timer expires, a power down sequence is initiated to turn off the voltage regulators.

The default value of the fault timer is set by the OTP_TIMER_FAULT[3:0], however the duration of the fault timer can be changed during the system on states by modifying the TIMER_FAULT[3:0] bits in the I^2C registers.

Table 25. Fault timer register configuration

OTP bits OTP_TIMER_FAULT [3:0]	Functional bits TIMER_FAULT [3:0]	Timer value (ms)
0000	0000	1
0001	0001	2
0010	0010	4
0011	0011	8
0100	0100	16
0101	0101	32
0110	0110	64
0111	0111	128
1000	1000	256
1001	1001	512
1010	1010	1024
1011	1011	2056
1100	1100	Reserved
1101	1101	Reserved
1110	1110	Reserved
1111	1111	Disabled

Each voltage regulator has a dedicated I^2C bit that is used to bypass the fault detection mechanism for each specific fault.

SWx_ILIM_BYPASS / LDOx_ILIM_BYPASS

- 0 = ILIM protection enabled
- 1 = ILIM fault bypassed

SWx_OV_BYPASS / LDOx_OV_BYPASS

- 0 = OV protection enabled
- 1 = OV fault bypassed

SWx_UV_BYPASS / LDOx_UV_BYPASS

- 0 = UV protection enabled
- 1 = UV fault bypassed

Table 26. Fault bypass bits

Regulator	Bit to bypass a current limit	Bit to bypass an undervoltage	Bit to bypass an overvoltage
SW1	SW1_ILIM_BYPASS	SW1_UV_BYPASS	SW1_OV_BYPASS

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 26. Fault bypass bits...*continued*

Regulator	Bit to bypass a current limit	Bit to bypass an undervoltage	Bit to bypass an overvoltage
SW2	SW2_ILIM_BYPASS	SW2_UV_BYPASS	SW2_OV_BYPASS
SW3	SW3_ILIM_BYPASS	SW3_UV_BYPASS	SW3_OV_BYPASS
SW4	SW4_ILIM_BYPASS	SW4_UV_BYPASS	SW4_OV_BYPASS
SW5	SW5_ILIM_BYPASS	SW5_UV_BYPASS	SW5_OV_BYPASS
SW6	SW6_ILIM_BYPASS	SW6_UV_BYPASS	SW6_OV_BYPASS
SW7	SW7_ILIM_BYPASS	SW7_UV_BYPASS	SW7_OV_BYPASS
LDO1	LDO1_ILIM_BYPASS	LDO1_UV_BYPASS	LDO1_OV_BYPASS
LDO2	LDO2_ILIM_BYPASS	LDO2_UV_BYPASS	LDO2_OV_BYPASS
LDO3	LDO3_ILIM_BYPASS	LDO3_UV_BYPASS	LDO3_OV_BYPASS
LDO4	LDO4_ILIM_BYPASS	LDO4_UV_BYPASS	LDO4_OV_BYPASS

The default value of the OV_BYPASS, UV_BYPASS and ILIM_BYPASS bits upon power up can be configured by their corresponding OTP bits.

Bypassing the fault detection prevents the specific fault from starting any of the protective mechanism:

- Increment the counter
- Start the Fault timer
- Disable the regulator if the corresponding _STATE bit is 0
- OV / UV condition asserting the PGOOD pin low

When a fault is bypassed, the corresponding interrupt bit is still set and the INTB pin is asserted, provided the interrupt has not been masked.

14.7.1 Fault monitoring during power up state

An OTP bit is provided to select whether the output of the switching regulators is verified during the power up sequence and used as a gating condition to release the RESETBMCU or not.

- When OTP_PG_CHECK = 0, the output voltage of the regulators is not checked during the power up sequence and power good indication is not required to de-assert the RESETBMCU. In this scenario, the OV/UV monitors are masked until RESETBMCU is released; after this event, all regulators may start checking for faults after their corresponding blanking period.
- When OTP_PG_CHECK = 1, the output voltage of the regulators is verified during the power up sequence and a power good condition is required to release the RESETBMCU.

When OTP_PG_CHECK = 1, OV and UV faults during the power up sequence are reported based on the internal PG (Power Good) signals of the corresponding external regulator. The PGOOD pin can be used as an external indicator of an OV/UV failure when the RESETBMCU is ready to be de-asserted and it has been configured in the PGOOD mode. See Section 14.9.8 "PGOOD" for details on PGOOD pin operation and configuration.

Regardless of the PGOOD pin configured as a power good indicator or not, the PF8100/PF8200 masks the detection of an OV/UV failure until RESETBMCU is ready to be released, at this point the device checks for any OV/UV condition for the regulators turned on so far. If all regulators powered up before or in the same sequence slot than RESETBMCU are in regulation, RESETBMCU is de-asserted and the power up sequence can continue as shown in Figure 14.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

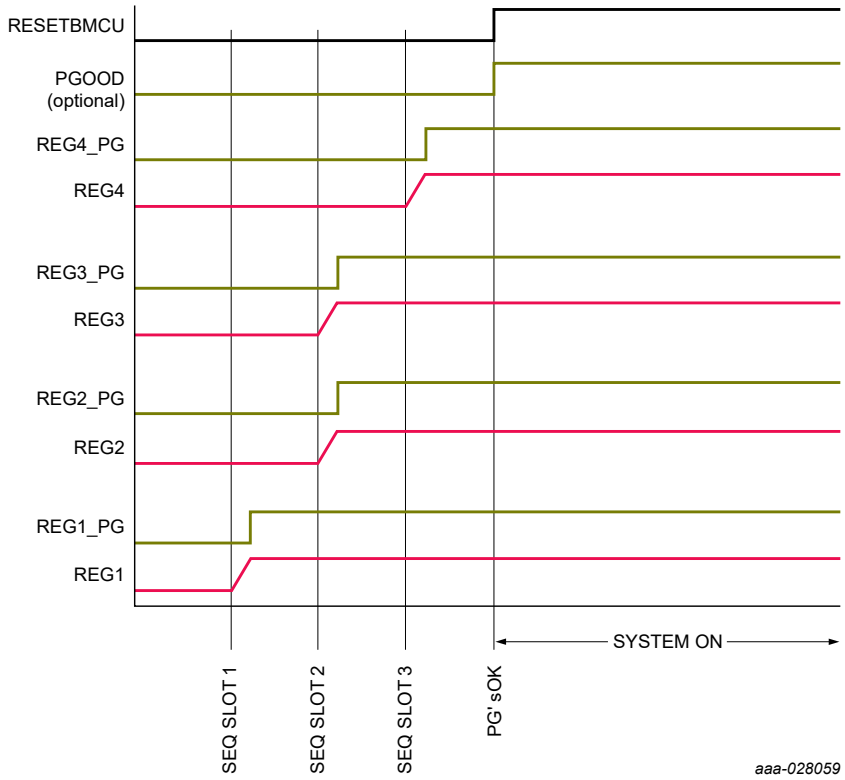


Figure 14. Correct power up (no fault during power up)

If any of the regulators are powered up before RESETBMCU is out of regulator, RESETBMCU is not de-asserted and the power up sequence is stopped for up to 2.0 ms. If the fault is cleared and all internal PG signals are asserted within the 2.0 ms timer, RESETBMCU is de-asserted and the power up sequence continues where it stopped as shown in Figure 15.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

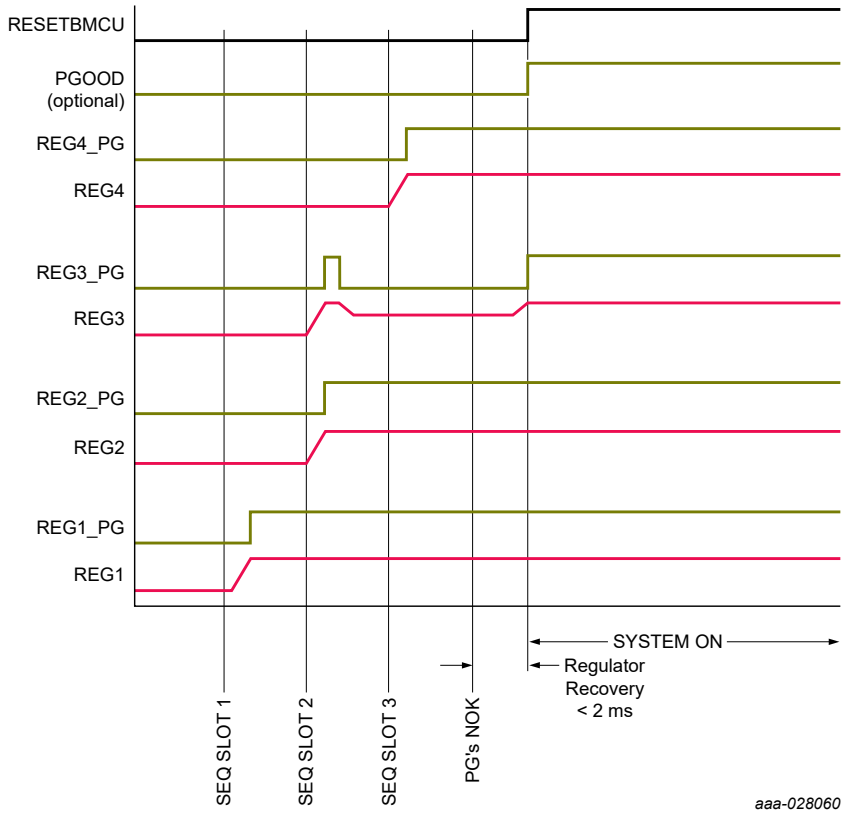


Figure 15. Power up sequencer with a temporary failure

If the faulty condition is not cleared within the 2.0 ms timer, the power up sequence is aborted and the PF8100/ PF8200 turn off all voltage regulators enabled so far as shown in Figure 16.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

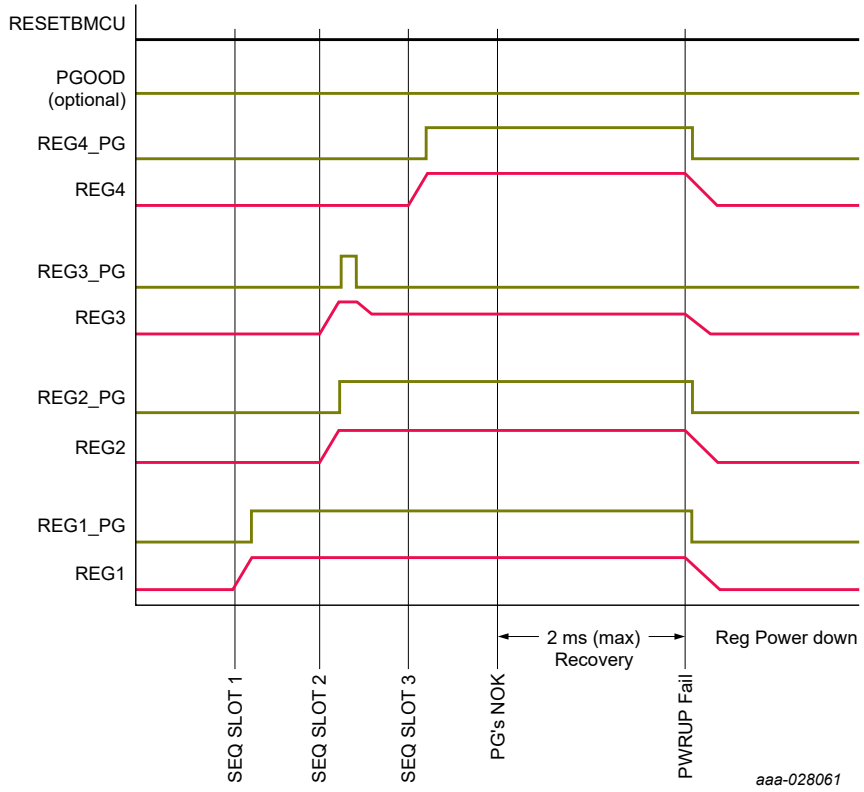


Figure 16. Power up sequencer aborted as fault persists for longer than 2.0 ms

Supplies enabled after RESETBMCU are checked for OV, UV and ILIM faults after each of them is enabled. If an OV, UV or ILIM condition is present, the PF8100/PF8200 starts a fault detection and protection mechanism as described in Section 14.7 "Fault detection". At this point, the MCU should be able to read the interrupt and react upon a fault event as defined by the system.

When OTP_PG_CHECK=1, if PGOOD is used as a GPIO, it may be released at any time in the power up sequence as long as the RESETBMCU is released after one or more of the SW or LDO regulators.

If a regulator fault occurs after RESETBMCU is de-asserted but before the power up sequence is finalized, the power up sequence continues to turn on the remaining regulators as configured, even if a fault detection mechanism is active on an earlier regulator.

14.8 Interrupt management

The MCU is notified of any interrupt through the INTB pin and various interrupt registers.

The interrupt registers are composed by three types of bits to help manage all the interrupt requests in the PF8100/PF8200:

- The interrupt latch XXXX_I: this bit is set when the corresponding interrupt event occurs. It can be read at any time, and is cleared by writing a 1 to the bit.
- The mask bit XXXX_M: this bit controls whether a given interrupt latch pulls the INTB pin low or not.
- When the mask bit is 1, the interrupt latch does not control the INTB pin.
- When the mask bit is 0, INTB pin is pulled low as long as the corresponding latch bit is set.
- The sense bit XXXX_S: if available, the sense bit provides the actual status of the signal triggering the interrupt.

The INTB pin is a reflection of an “OR” logic of all the interrupt status bits which control the pin.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Interrupts are stored in two levels on the interrupts registers. At first level, the SYS_INT register provides information about the Interrupt register that originated the interrupt event.

The corresponding SYS_INT bits will be set as long as the INTB pin is programmed to assert with any of the interrupt bits of the respective interrupt registers.

- STATUS1_I: this bit is set when the interrupt is generated within the INT STATUS1 register
- STATUS2_I: this bit is set when the interrupt is generated within the INT STATUS2 register
- MODE_I: this bit is set when the interrupt is generated within the SW MODE INT register
- ILIM_I: this bit is set when the interrupt is generated within any of the SW ILIM INT or LDO ILIM INT registers
- UV_I: this bit is set when the interrupt is generated within any of the SW UV INT or LDO UV INT registers
- OV_I: this bit is set when the interrupt is generated within any of the SW OV INT or LDO OV INT registers
- PWRON_I: this bit is set when the interrupt is generated within the PWRON INT register
- EWARN_I: is set when an early warning event occurs to indicate an imminent shutdown

The SYS_INT bits are set when the INTB pin is asserted by any of the second level interrupt bits that have not been masked in their corresponding mask registers. When the second level interrupt bit is cleared, the corresponding first level interrupt bit on the SYS_INT register will be cleared automatically.

The INTB pin will remain asserted if any of the first level interrupt bit is set, and it will be de-asserted only when all the unmasked second level interrupts are cleared and thus all the first level interrupts are cleared as well.

At second level, the remaining registers provide the exact source for the interrupt event.

Table 27 shows a summary of the interrupt latch, mask and sense pins available on the PF8100/PF8200.

Table 27. Interrupt registers

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
INT STATUS1	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	XINTB_I	FSOB_I	VIN_OVLO_I
INT MASK1	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	XINTB_M	FSOB_M	VIN_OVLO_M
INT SENSE1	—	—	—	—	—	XINTB_S	FSOB_S	VIN_OVLO_S
THERM INT	WDI_I	FSYNC_FLT_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I	THERM_95_I	THERM_80_I
THERM MASK	WDI_M	FSYNC_FLT_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M	THERM_95_M	THERM_80_M
THERM SENSE	WDI_S	FSYNC_FLT_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S	THERM_95_S	THERM_80_S
SW MODE INT	—	SW7_MODE_I	SW6_MODE_I	SW5_MODE_I	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
SW MODE MASK	—	SW7_MODE_M	SW6_MODE_M	SW5_MODE_M	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
SW ILIM INT	—	SW7_ILIM_I	SW6_ILIM_I	SW5_ILIM_I	SW4_ILIM_I	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
SW ILIM MASK	—	SW7_ILIM_M	SW6_ILIM_M	SW5_ILIM_M	SW4_ILIM_M	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
SW ILIM SENSE	—	SW7_ILIM_S	SW6_ILIM_S	SW5_ILIM_S	SW4_ILIM_S	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
LDO ILIM INT	—	—	—	—	LDO4_ILIM_I	LDO3_ILIM_I	LDO2_ILIM_I	LDO1_ILIM_I
LDO ILIM MASK	—	—	—	—	LDO4_ILIM_M	LDO3_ILIM_M	LDO2_ILIM_M	LDO1_ILIM_M
LDO ILIM SENSE	—	—	—	—	LDO4_ILIM_S	LDO3_ILIM_S	LDO2_ILIM_S	LDO1_ILIM_S
SW UV INT	—	SW7_UV_I	SW6_UV_I	SW5_UV_I	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
SW UV MASK	—	SW7_UV_M	SW6_UV_M	SW5_UV_M	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
SW UV SENSE	—	SW7_UV_S	SW6_UV_S	SW5_UV_S	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
SW OV INT	—	SW7_OV_I	SW6_OV_I	SW5_OV_I	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
SW OV MASK	—	SW7_OV_M	SW6_OV_M	SW5_OV_M	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
SW OV SENSE	—	SW7_OV_S	SW6_OV_S	SW5_OV_S	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
LDO UV INT	—	—	—	—	LDO4_UV_I	LDO3_UV_I	LDO2_UV_I	LDO1_UV_I
LDO UV MASK	—	—	—	—	LDO4_UV_M	LDO3_UV_M	LDO2_UV_M	LDO1_UV_M
LDO UV SENSE	—	—	—	—	LDO4_UV_S	LDO3_UV_S	LDO2_UV_S	LDO1_UV_S
LDO OV INT	—	—	—	—	LDO4_OV_I	LDO3_OV_I	LDO2_OV_I	LDO1_OV_I
LDO OV MASK	—	—	—	—	LDO4_OV_M	LDO3_OV_M	LDO2_OV_M	LDO1_OV_M
LDO OV SENSE	—	—	—	—	LDO4_OV_S	LDO3_OV_S	LDO2_OV_S	LDO1_OV_S
PWRON INT	BGMON_I	PWRON_8S_I	PWRON_4S_I	PRON_3S_I	PWRON_2S_I	PWRON_1S_I	PWRON_REL_I	PWRON_PUSH_I

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 27. Interrupt registers...*continued*

Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PWRON MASK	BGMON_M	PWRON_8S_M	PWRON_4S_M	PRON_3S_M	PWRON_2S_M	PWRON_1S_M	PWRON_REL_M	PWRON_PUSH_M
PWRON SENSE	BGMON_S	—	—	—	—	—	—	PWRON_S
SYS INT	EWARN_I	PWRON_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I

14.9 I/O interface pins

The PF8100/PF8200 PMIC is fully programmable via the I^2C interface. Additional communication between MCU, PF8100/PF8200 and other companion PMIC is provided by direct logic interfacing including INTB, RESETBMCU, PGOOD, among other pins.

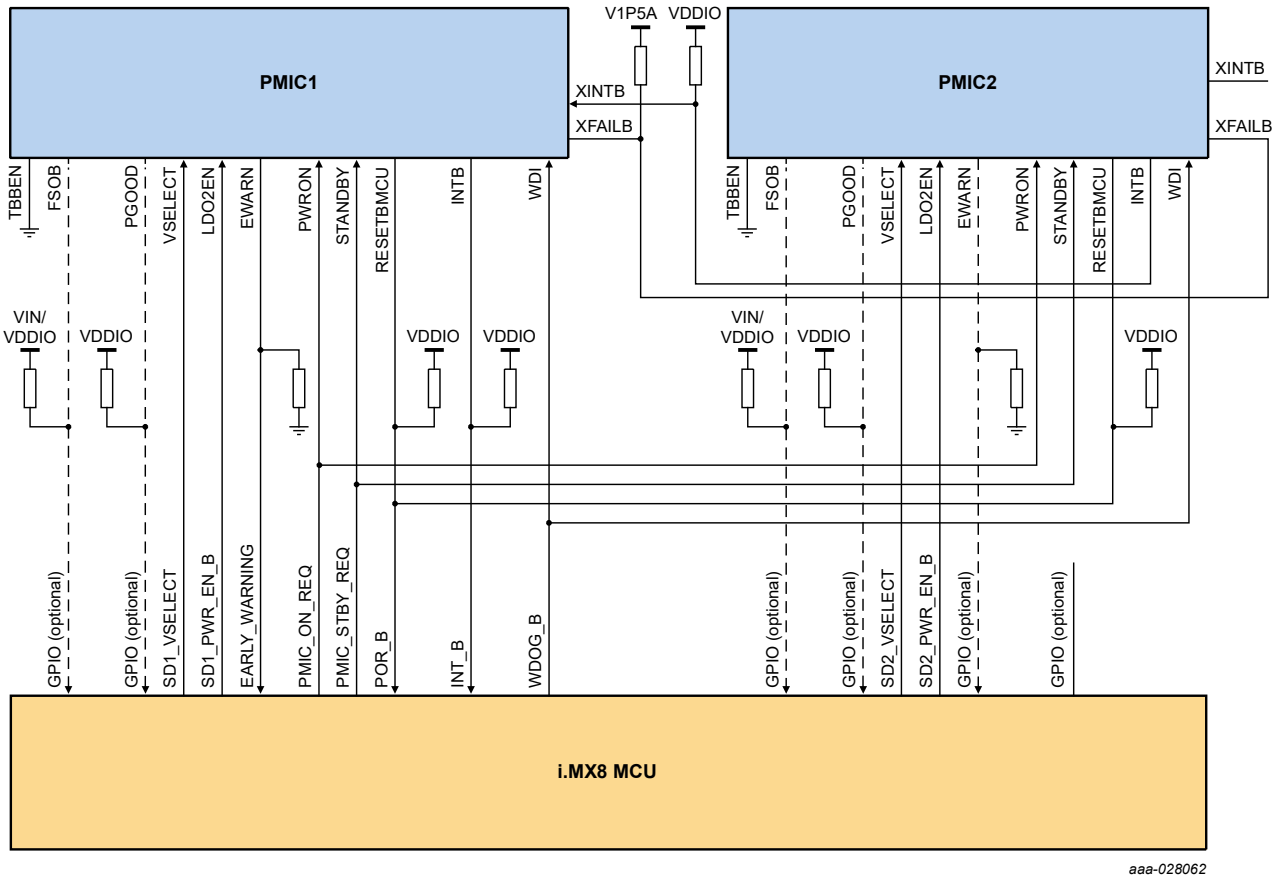


Figure 17. I/O interface diagram

Table 28. I/O electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
PWRON_ V_{IL}	PWRON low input voltage	—	—	0.4	V
PWRON_ V_{IH}	PWRON high input voltage	1.4	—	5.5	V
STANDBY_ V_{IL}	STANDBY low input voltage	—	—	0.4	V
STANDBY_ V_{IH}	STANDBY high input voltage	1.4	—	5.5	V
RESETBMCU_ V_{OL}	RESETBMCU low output voltage 10 mA load current	0	—	0.4	V
INTB_ V_{OL}	INTB low output voltage 10 mA load current	0	—	0.4	V

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 28. I/O electrical specifications...*continued*

Symbol	Parameter	Min	Typ	Max	Unit
XINTB_ V_{IL}	XINTB low input voltage	—	—	0.3*VDDIO	V
XINTB_ V_{IH}	XINTB high input voltage	0.7*VDDIO	—	5.5	V
R_{XINTB_PU}	XINTB internal pullup resistance	0.475	1.0	—	MΩ
WDI_ V_{IL}	WDI low input voltage	—	—	0.3*VDDIO	V
WDI_ V_{IH}	WDI high input voltage	0.7*VDDIO	—	5.5	V
R_{WDI_PD}	WDI internal pull down resistance	0.475	1.0	—	MΩ
EWARN_ V_{OH}	EWARN high output voltage 2.0 mA load current	VDDIO − 0.5	—	VDDIO	V
PGOOD_ V_{OL}	PGOOD low output voltage 10 mA load current	0	—	0.4	V
VSELECT_ V_{IL}	VSELECT low input voltage	—	—	0.3*VDDIO	V
VSELECT_ V_{IH}	VSELECT high input voltage	0.7*VDDIO	—	5.5	V
$R_{VSELECT_PD}$	VSELECT internal pull down resistance	0.475	1.0	—	MΩ
LDO2EN_ V_{IL}	LDO2EN low input voltage	—	—	0.3*VDDIO	V
LDO2EN_ V_{IH}	LDO2EN high input voltage	0.7*VDDIO	—	5.5	V
R_{LDO2EN_PD}	LDO2EN internal pull down resistance	0.475	1.0	—	MΩ
TBBEN_ V_{IL}	TBBEN low input voltage	—	—	0.4	V
TBBEN_ V_{IH}	TBBEN high input voltage	1.4	—	5.5	V
R_{TBBEN_PD}	TBBEN internal pull down resistance	0.475	1.0	—	MΩ
XFAILB_V_{IL}	XFAILB low input voltage	—	—	0.4	V
XFAILB_V_{IH}	XFAILB high input voltage	1.4	—	5.5	V
XFAILB_V_{OH}	XFAILB high output voltage Pulled-up to V1P5A	V1P5A − 0.5	—	—	V
XFAILB_V_{OL}	XFAILB low output voltage 10 mA load current	0	—	0.4	V
FSOB_ V_{OL}	FSOB low output voltage −10 mA	0	—	0.4	V
SCL_ V_{IL}	SCL low input voltage	—	—	0.3*VDDIO	V
SCL_ V_{IH}	SCL high input voltage	0.7*VDDIO	—	VDDIO	V
SDA_ V_{IL}	SDA low input voltage	—	—	0.3*VDDIO	V
SDA_ V_{IH}	SDA high input voltage	0.7*VDDIO	—	VDDIO	V
SDA_ V_{OL}	SDA low output voltage −20 mA load current	0	—	0.4	V

14.9.1 PWRON

PWRON is an input signal to the IC that acts as a power up event signal in the PF8100/PF8200.

The PWRON pin has two modes of operations as programed by the OTP_PWRON_MODE bit.

When OTP_PWRON_MODE = 0 the PWRON pin operates in level sensitive mode. In this mode, the device is in the corresponding off mode when the PWRON pin is pulled low. Pulling the PWRON pin high is a necessary condition to generate a power on event.

PWRON may be pulled up to VSNVS or VIN with an external 100 kΩ resistor if device is intended to come up automatically with VIN application. See Section 14.5 "Power up" for details on power up requirements.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

When OTP_PWRON_MODE = 1, the PWRON pin operates in edge sensitive mode. In this mode, PWRON is used as an input from a push button connected to the PMIC.

When the switch is not pressed, the PWRON pin is pulled up to VIN externally through a 100 kΩ resistor. When the switch is pressed, the PWRON pin should be shorted to ground. The PWRON_S bit is high whenever the PWRON pin is at logic 0 and is low whenever the PWRON pin is at logic 1.

The PWRON pin has a programmable debounce on the rising and falling edges as shown below.

Table 29. PWRON debounce configuration in edge detection mode

Bits	Value	Falling edge debounce (ms)	Rising edge debounce (ms)
PWRON_DBNC[1:0]	00	32	32
PWRON_DBNC[1:0]	01	32	32
PWRON_DBNC[1:0]	10	125	32
PWRON_DBNC[1:0]	11	750	32

The default value for the power on debounce is set by the OTP_PWRON_DBNC[1:0] bits.

Pressing the PWRON switch for longer than the debounce time starts a power on event as well as generate interrupts which the processor may use to initiate PMIC state transitions.

During the system-on states, when the PWRON button is pushed (logic 0) for longer than the debounce setting, the PWRON_PUSH_I interrupt is generated. When the PWRON button is released (logic 1) for longer than the debounce setting, the PWRON_REL_I interrupt is generated.

The PWRON_1S_I, PWRON_2S_I, PWRON_3S_I, PWRON_4S_I and PWRON_8S_I interrupts are generated when the PWRON pin is held low for longer than 1, 2, 3, 4 and 8 seconds respectively.

If PWRON_RST_EN = 1, pressing the PWRON for longer than the delay programmed by TRESET[1:0] forces a PMIC reset. A PMIC reset initiates a power down sequence, wait for 30 µs to allow all supplies to discharge and then it powers back up with the default OTP configuration.

If PWRON_RST_EN = 0, the device starts a turn off event after push button is pressed for longer than TRESET[1:0].

Table 30. TRESET configuration

TRESET[1:0]	Time to reset
00	2 s
01	4 s
10	8 s
11	16 s

The default value of the TRESET delay is programmable through the OTP_TRESET[1:0] bits.

14.9.2 STANDBY

STANDBY is an input signal to the IC, when this pin is asserted, the device enters the standby mode and when de-asserted, the part exits standby mode.

STANDBY can be configured as active high or active low using the STANDBYINV bit.

Table 31. Standby pin polarity control

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
0	0	Not in standby mode
0	1	In standby mode

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 31. Standby pin polarity control*...continued*

STANDBY (pin)	STANDBYINV (I^2C bit)	STANDBY control
1	0	In standby mode
1	1	Not in standby mode

14.9.3 RESETBMCU

RESETBMCU is an open-drain, active low output used to bring the processor (and peripherals) in and out of reset.

The time slot RESETBMCU is de-asserted during the power up sequence is programmed by the OTP_RESETBMCU_SEQ[7:0] bits, and it is a condition to enter the system-on states.

During the system-on states, the RESETBMCU is de-asserted (pulled high), and it is asserted (pulled low) as indicated in the power down sequence, when a system power down or reset is initiated.

In the application, RESETBMCU can be pulled up to VDDIO or VSNVS by a 100 kΩ external resistor.

14.9.4 INTB

INTB is an open-drain, active low output. This pin is asserted (pulled low) when any interrupt occurs, provided that the interrupt is not masked.

INTB is de-asserted after the corresponding interrupt latch is cleared by software, which requires writing a “1” to the interrupt bit.

An INTB_TEST bit is provided to allow a manual test of the INTB pin. When INTB_TEST is set to 1, the interrupt pin asserts for 100 µs and then de-asserts to its normal state. The INTB_TEST bit self-clears to 0 automatically after the test pulse is generated.

In the application, INTB can be pulled up to VDDIO with an external 100 kΩ resistor.

14.9.5 XINTB

XINTB is an input pin used to receive an external interrupt and trigger an interrupt event on the PF8100/PF8200. It is meant to interact with the INTB pin of a companion PMIC, in order to simplify MCU interaction to identify the source of the interrupt.

A high to low transition on the XINTB pin sets the XINTB_I interrupt bit and causes the INTB to be asserted, provided the interrupt is not masked.

The XINTB_S bit follows the actual status of the XINTB pin even when the XINTB_I has been cleared or the interrupt has been masked.

This pin is internally pulled up to VDDIO with a 1.0 MΩ resistors; therefore, it can be left unconnected when the XINTB is not used.

14.9.6 WDI

WDI is an input pin to the PF8100/PF8200 and is intended to operate as an external watchdog monitor.

When the WDI pin is connected to the watchdog output of the processor, this pin is used to detect a pulse to indicate a watchdog event is requested by the processor. When the WDI pin is asserted, the device starts a watchdog event to place the PMIC outputs in a default known state.

The WDI pin is monitored during the system on states. In the off modes and during the power up sequence, the WDI pin is masked until RESETBMCU is de-asserted.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The WDI can be configured to assert on the rising or the falling edge using the OTP_WDI_INV bit.

- When OTP_WDI_INV = 0, the device starts a WD event on the falling edge of the WDI.
- When OTP_WDI_INV = 1, the device starts a WD event on the rising edge of the WDI.

A 10 µs debounce filter is implemented on either rising or falling edge detection to prevent false WDI signals to start a watchdog event.

The OTP_WDI_MODE bit allows the WDI pin to react in two different ways:

- When OTP_WDI_MODE = 1, a WDI asserted performs a hard WD reset.
- When OTP_WDI_MODE = 0, a WDI asserted performs a soft WD reset.

The WDI_STBY_ACTIVE bit allows the WDI pin to generate a watchdog event during the standby state.

- When WDI_STBY_ACTIVE = 0, asserting the WDI will not generate a watchdog event during the standby state.
- When WDI_STBY_ACTIVE = 1, asserting the WDI will start a watchdog event during the standby state.

The OTP_WDI_STBY_ACTIVE is used to configure whether the WDI is active in the standby state or not by default upon power up.

See Section 15.11 "Watchdog event management" for details on watchdog event.

14.9.7 EWARN

EWARN is an active high output, used to notify that an imminent power failure is about to occur. It should be pulled down to GND by a 100 kΩ resistor.

When a power down is initiated due to a fault, the EWARN pin is asserted before the device starts powering down as defined by the EWARN_TIME[1:0] bits in order to allow the system to prepare for the imminent shutdown.

The following faults cause the EWARN pin to be asserted:

- Fault timer expired
- FAULT_CNT = FAULT_MAX_CNT
- Thermal Shutdown t_J > TSD
- VIN_OVLO event when VIN_OVLO_SDWN=1

Table 32. EWARN time configuration

OTP_EWARN_TIME[1:0]	EWARN delay time
00	100 µs
01	5.0 ms
10	20 ms
11	50 ms

When the EWARN pin is asserted, an interrupt will be generated and the EWARN_I bit will be set to announce to the system of an imminent shutdown event.

In the Off modes, EWARN remains de-asserted (pulled low).

In the event of a power loss (VIN removed), the EWARN pin is asserted upon crossing the V_{WARNTH} threshold to notify to the processor that VIN may be lost and allow some time to prepare for the power loss.

Table 33. Early warning threshold

Symbol	Parameter	Min	Typ	Max	Unit
V_{WARNTH}	Early warning threshold	2.7	2.8	2.9	V

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

14.9.8 PGOOD

PGOOD is an open drain output programmable as a Power Good indicator pin or GPO. In the application, PGOOD can be pulled up to VDDIO with a 100 kΩ resistor.

When OTP_PG_ACTIVE = 0, the PGOOD pin is used as a general purpose output.

As a GPO, during the run state, the state of the pin is controlled by the RUN_PG_GPO bit in the functional I^2C registers:

- When RUN_PG_GPO = 1, the PGOOD pin is high
- When RUN_PG_GPO = 0, the PGOOD pin is low

During the standby state, the state of the pin is controlled by the STBY_PG_GPO bit in the functional I^2C registers:

- When STBY_PG_GPO = 1, the PGOOD pin is high
- When STBY_PG_GPO = 0, the PGOOD pin is low

When used as a GPO, the PGOOD pin can be enabled high as part of the power up sequence as programmed by the OTP_SEQ_TBASE[1:0] and the OTP_PGOOD_SEQ[7:0] bits. If enabled as part of the power up sequence, both the RUN_PG_GPO and STBY_PG_GPO bits are loaded with 1, otherwise they are loaded with 0 upon power up.

When OTP_PG_ACTIVE = 1, the PGOOD pin is in Power good (PG) mode and it acts as a PGOOD indicator for the selected output voltages in the PF8100/PF8200.

There is an individual PG monitor for every regulator. Each monitor provide an internal PG signal that can be selected to control the status of the PGOOD pin upon an OV or UV condition when the corresponding SWxPG_EN / LDOxPG_EN bits are set. The status of the PGOOD pin is a logic AND function of the internal PG signals of the selected monitors.

- When the PG_EN = 1, the corresponding regulator becomes part of the AND function that controls the PGOOD pin.
- When the PG_EN = 0, the corresponding regulator does not control the status of the PGOOD pin.

The PGOOD pin is pulled low when any of the selected regulator outputs falls above or below the programmed OV/UV thresholds and a corresponding OV/UV interrupt is generated. If the faulty condition is removed, the corresponding OV_S/UV_S bit goes low to indicate the output is back in regulation, however, the interrupt remains latched until it is cleared.

The actual condition causing the interrupt (OV, UV) can be read in the fault interrupt registers. For more details on handling interrupts, see Section 14.8 "Interrupt management".

When a particular regulator is disabled (via OTP, or I^2C, or by change in state of PMIC such as going to standby mode), it no longer controls the PGOOD pin.

In the Off mode and during the power up sequence, the PGOOD pin is held low until RESETBMCU is ready to be released, at this point, the PG monitors are unmasked and the PGOOD pin is released high if all the internal PG monitors are in regulation. In the event that one or more outputs are not in regulation by the time RESETBMCU is ready to de-assert, the PGOOD pin is held low and the PF8100/PF8200 performs the corresponding fault protection mechanism as described in Section 14.7.1 "Fault monitoring during power up state".

14.9.9 VSELECT

VSELECT is an input pin used to select the output voltage of LDO2 when bit VSELECT_EN = 1.

- When VSELECT pin is low, the LDO2 output is programmed to 3.3 V.
- When VSELECT pin is high, the LDO2 output is programmed to 1.8 V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

When VSELECT_EN = 0, the output of LDO2 is given by the VLDO2_RUN[3:0] bits.

When the PF8100/PF8200 is in the standby mode, the output voltage of LDO2 follows the configuration as selected by the VLDO2_STBY[3:0] bits, regardless of the value of VSELECT_EN bit.

The default value of the VSELECT_EN bit is programmed by the OTP_VSELECT_EN bit in the OTP fuses.

A read only bit is provided to monitor the actual state of the VSELECT pin. When the VSELECT pin is low, the VSELECT_S bit is 0 and when the VSELECT pin is high, the VSELECT_S bit is set to 1.

14.9.10 LDO2EN

LDO2EN is an input pin used to enable or disable LDO2 when the bit LDO2HW_EN = 1.

When LDO2HW_EN = 1, the status of LDO2 output can also be controlled by the LDO2_RUN_EN bit in the run mode or the LDO2_STBY_EN bit in the standby mode.

Table 34. LDO control in run or standby mode

LDO2EN pin	LDO2HW_EN bit	LDO2_RUN_EN LDO2_STBY_EN	LDO2 output
Do not care	0	0	Disabled
Do not care	0	1	Enabled
Do not care	1	0	Disabled
Low	1	1	Disabled
High	1	1	Enabled

The default controlling mode for LDO2 is programed by the OTP_LDO2HW_EN bit in the OTP fuses.

A read only bit is provided to monitor the actual state of the LDO2EN pin. When the LDO2EN pin is low, the LDO2EN_S bit is 0 and when the LDO2EN pin is high, the LDO2EN_S bit is set to 1.

14.9.11 FSOB (safety output)

The FSOB pin is a configurable, active low, open drain output used as a safety output to keep the system in a safe state upon a power up and/or during a specific failure event.

The FSOB pin is externally pulled up to VIN or VDDIO with a 470 kΩ resistor and it is de-asserted high in normal operation.

The FSOB pin can be configured in active safe state mode or fault safe state mode as programmed by the OTP_FSOB_ASS_EN bit in the OTP fuses.

The PF8200 device allows configuration of the FSOB pin to operate in active safe state or fault safe state modes via the OTP_FSOB_ASS_EN bit in the OTP fuses. Additionally on the PF8200 device, if the secure I2C write mechanism is enabled, all FSOB flags require a secure write for them to be cleared (write 1 to clear + RANDOM_GEN read + RANDOM_CHK write).

In the PF8100 device, the OTP_FSOB_ASS_EN bit is not available, therefore it can only operate in fault safe state mode.

14.9.11.1 FSOB fault safe state

If the OTP_FSOB_ASS_EN = 0, the active safe state mode is disabled and the FSOB operate in the fault safe state mode. In this mode, the FSOB pin may still be asserted if programmed by other fault events.

In the fault safe state mode, the FSOB is de-asserted by default, and can be asserted as programmed by the FSOB fault selection bits.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

A bit is provided to enable the FSOB to be asserted when a regulator fault (OV, UV, ILIM) is present.

- If FSOB_SOFTFAULT = 0, the FSOB pin is not asserted by any OV, UV, or ILIM fault.
- If FSOB_SOFTFAULT = 1, an OV, UV, or ILIM fault on any of the regulators causes the FSOB pin to assert and remain asserted regardless of it being corrected or not, and also asserts the FSOB_SFAULT_NOK flag.

A bit is provided to enable the FSOB to be asserted when a WD reset occurs due to a WDI event.

- If FSOB_WDI = 0, the FSOB pin is not asserted by a WDI event.
- If FSOB_WDI = 1, a WDI event causes the FSOB pin to assert and the FSOB_WDI_NOK flag to be set.

A bit is provided to enable the FSOB to be asserted when a WD reset occurs due to an internal WD counter fault is present.

- If FSOB_WDC = 0, the FSOB pin is not asserted by a WD reset started by the internal WD counter.
- If FSOB_WDC = 1, a WD reset is started by the internal WD counter causing the FSOB pin to be asserted and the FSOB_WDC_NOK flag to be set.

A bit is provided to enable the FSOB to be asserted when a hard fault shutdown has occurred.

- If FSOB_HARDFAULT = 0, the FSOB pin is not asserted by a hard fault.
- If FSOB_HARDFAULT = 1, any of the hard fault shutdown events cause the FSOB pin to be asserted and the FSOB_HFAULT_NOK flag to be set.

Any of the following events are considered a hard fault shutdown:

- Fault timer expired
- FAULT_CNT = FAULT_MAX_CNT (regulator fault counter max out)
- WD_EVENT_CNT = WD_MAX_CNT (watchdog event counter max out)
- Power up failure
- Thermal shutdown

The FSOB pin is released when all the FSOB fault flags are cleared or VIN falls below the UVDET threshold.

14.9.11.2 FSOB active safe state (PF8200 only)

If the OTP_FSOB_ASS_EN = 1, the active safe state mode is enabled.

In the active safe state mode, the FSOB pin is programmed to be asserted low after OTP fuses are loaded and remain asserted as long as the PMIC is forced in safe state.

In this mode of operation, the PMIC is forced in the safe state under following conditions:

- Any of the ABIST flags are set during the self-test at power up.
- The FSOB_WDI_NOK is set when FSOB is programmed to assert via the FSOB_WDI bit
- The FSOB_SFAULT_NOK is set when FSOB is programmed to assert via the FSOB_SOFTFAULT bit
- Hard WD Reset (voltage regulators and RESETBMCU reset)
- Device is in any of the off mode and the RESETBMCU is asserted low
- The FSOB_ASS_NOK flag is asserted

Each time the PMIC is forced into the safe state, the FSOB pin will be asserted low and the FSOB_ASS_NOK flag will be set to 1 in order to keep the system in the safe state until the MCU verify that it is safe to return to normal operation.

During the active safe state mode, the PMIC can exit the safe state and release the FSOB pin if the following conditions are met:

- RESETBMCU is de-asserted (system on)
- All ABIST flags are all 0 (ABIST OK)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

- No regulator faults are present
- The FSOB_WDI_NOK and/or FSOB_SFAULT_NOK faults are cleared if programmed to be set by the FSOB_WDI and FSOB_SOFTFAULT bits respectively
- All other NOK flags in the FSOB_FLAGS register, including the FSOB_ASS_NOK flag, are cleared

A soft WD reset may also assert the FSOB pin only if programmed by the FSOB_WDI bit.

Likewise, the FSOB_SOFTFAULT bit can select whether the FSOB pin is asserted as soon as an OV, UV or ILIM fault is present even when this condition has not yet lead to a fault shutdown. In this scenario the system is placed in a safe state while the MCU tries to clear the fault and command the PF8200 to come out of the safe state when all faults have been cleared.

14.9.12 TBBEN

The TBBEN is an input pin provided to allow the user to program the mirror registers in order to operate the device with a custom configuration as well as programming the default values on the OTP fuses.

- When TBBEN pin is pulled low to ground, the device is operating in normal mode.
- When TBBEN pin is pulled high to V1P5D device enables the TBB configuration mode.

See Section 17 "OTP/TBB and default configurations" for details on TBB and OTP operation.

When TBBEN pin is pulled high to V1P5D the following conditions apply:

- The device uses a fixed I^2C device address (0x08)
- Disable the watchdog operation, including WDI monitoring and internal watchdog timer
- Disable the CRC and I^2C secure write mechanism while no power up event is present (TBB/OTP programming mode).

Disabling the watchdog operation may be required for in-line MCU programming where output voltages are required but watchdog operation should be completely disabled.

14.9.13 XFAILB

XFAILB is a bidirectional pin with an open drain output used to synchronize the power up and power down sequences of two or more PMIC's. It should be pulled up externally to V1P5A supply.

The OTP_XFAILB_EN bit is used to enable or disable the XFAILB mode of operation.

- When OTP_XFAILB_EN = 0, the XFAILB mode is disabled and any events on this pin are ignored
- When OTP_XFAILB_EN = 1, the XFAILB mode is enabled

When the XFAILB mode is enabled, and the PF8200 has a turn off event generated by an internal fault, the XFAILB pin is asserted low 20 µs before starting the power down sequence.

A power down event caused by the following conditions will assert the XFAILB pin:

- Fault timer expired
- FAULT_CNT = FAULT_MAX_CNT (regulator fault counter max out)
- WD_EVENT_CNT = WD_MAX_CNT (watchdog event counter max out)
- Power up failure
- Thermal shutdown
- Hard WD event

The XFAILB pin is forced low during the off mode.

During the system-on states, if the XFAILB pin is externally pulled low, it will detect an XFAIL event after a 20 µs debounce. When an XFAIL event is detected, the XFAILB pin is asserted low internally and the device starts a power down sequence.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

If a PWRON event is present, the device starts a turn on event and proceeds to release the XFAILB pin when its ready to start the power up sequence state. If the XFAILB pin is pulled down externally during the power up event, the PF8200 will stop the power up sequence until the pin is no longer pulled down externally. This will help both PMIC's to synchronize the power up sequence allowing it to continue only when both PMIC's are ready to initiate the power up sequence.

A hard WD event will set the XFAILB pin 20 µs before it starts its power down sequence. After all regulators outputs have been turned off, the device will release the XFAILB pin internally after a 30 µs delay, proceed to load the default OTP configuration and wait for the XFAILB pin to be released externally before it can restart the power up sequence.

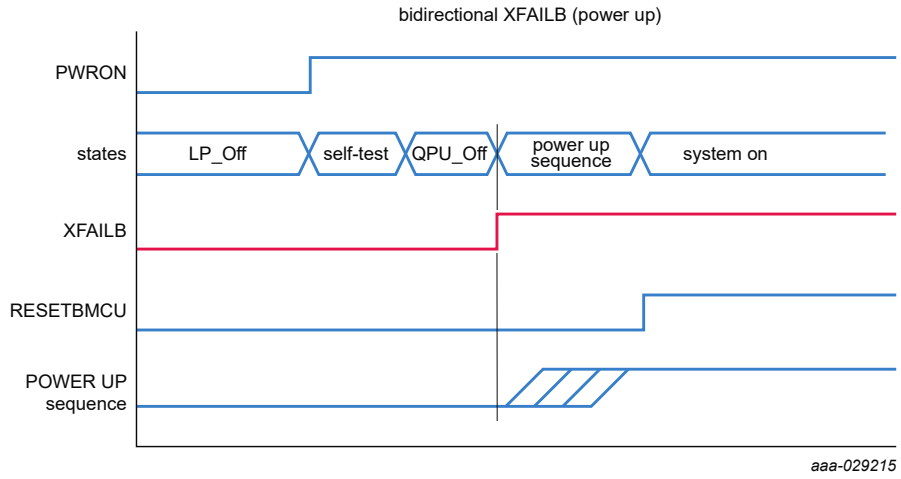


Figure 18. XFAILB behavior during a power up sequence

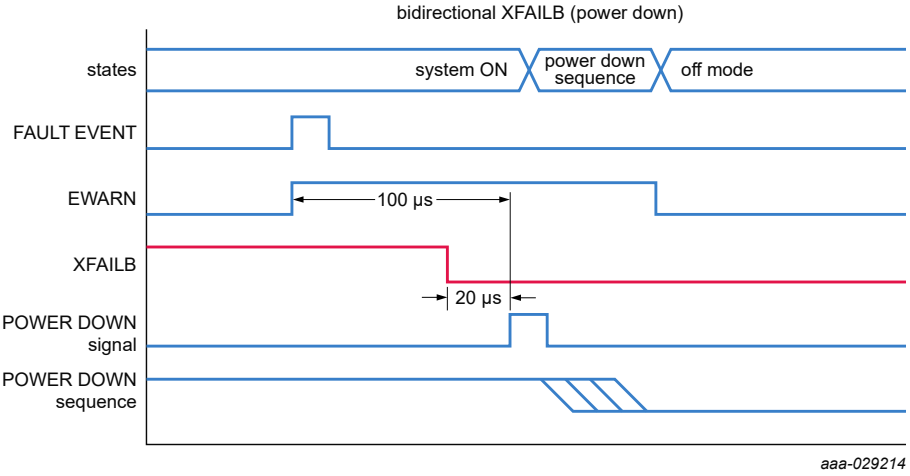


Figure 19. XFAILB behavior during a power down sequence

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

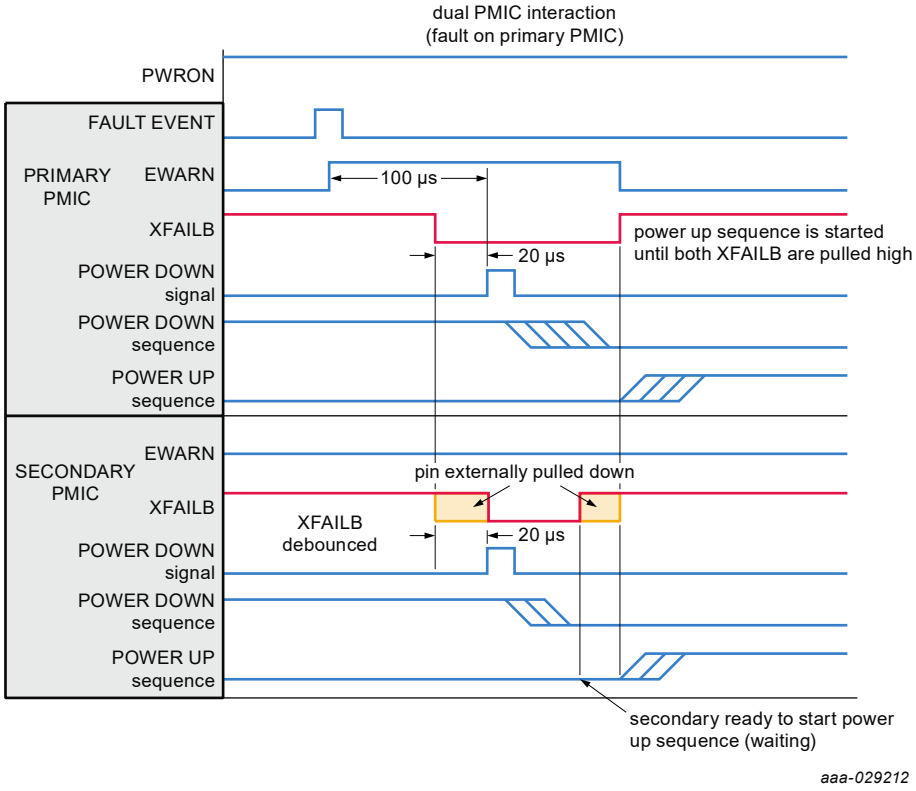


Figure 20. Behavior during an external XFAILB event

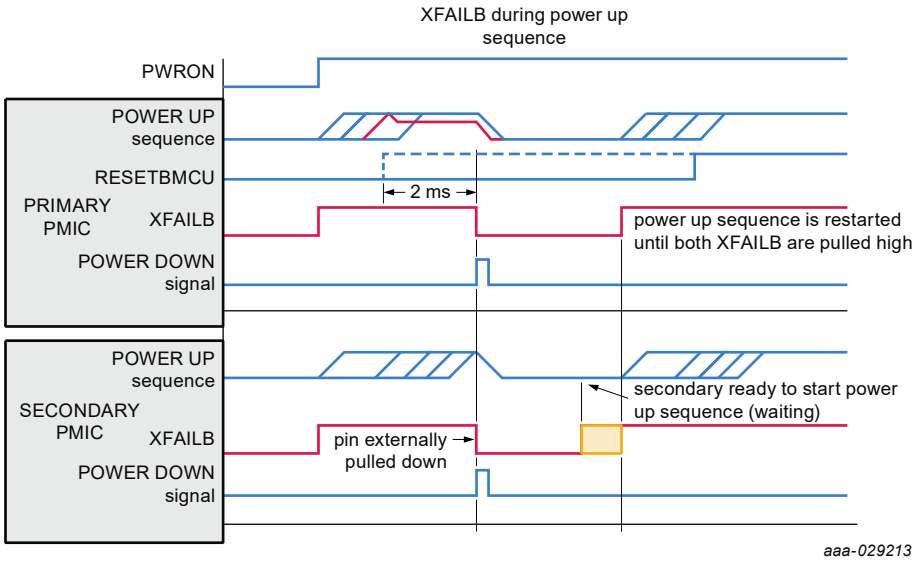


Figure 21. External XFAILB event during a power up sequence

14.9.14 SDA and SCL (I^2C bus)

Communication with the PF8100/PF8200 is done through I^2C and it supports high-speed operation mode with up to 3.4 MHz operation. SDA and SCL are pulled up to VDDIO with 2.2 kΩ resistors. It is recommended to use 1.5 kΩ if 3.4 MHz I^2C speed is required.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The PF8100/PF8200 is designed to operate as a secondary device during I²C communication. The default I²C device address is set by the OTP_I2C_ADD[2:0].

Table 35. I²C address configuration

OTP_I2C_ADD[2:0]	Device address
000	0x08
001	0x09
010	0x0A
011	0x0B
100	0x0C
101	0x0D
110	0x0E
111	0x0F

See http://www.nxp.com/documents/user_manual/UM10204.pdf for detailed information on the digital I²C communication protocol implementation.

During an I²C transaction, the communication will latch after the 8th bit is sent. If the data sent is not a multiple of 8 bit, any word with less than 8 bits will be ignored. If only 7 bits are sent, no data is written and the logic will not provide an ACK bit to the MCU.

From an IC level, a wrong I²C command can create a system level safety issue. For example, though the MCU may have intended to set a given regulator's output to 1.0 V, it may be erroneously registered as 1.1 V due to noise in the bus.

To prevent a wrong I²C configuration, various protective mechanisms are implemented.

14.9.14.1 I²C CRC verification

When this feature is enabled, a selectable CRC verification is performed on each I²C transaction.

- When OTP_I2C_CRC_EN = 0, the CRC verification mechanism is disabled.
- When OTP_I2C_CRC_EN = 1, the CRC verification mechanism is enabled.

After each I²C transaction, the device calculates the corresponding CRC byte to ensure the configuration command has not been corrupted.

When a CRC fault is detected, the PF8100/PF8200 ignores the erroneous configuration command and triggers a CRC_I interrupt asserting the INTB pin, provided the interrupt is not masked.

The PF8100/PF8200 implements a CRC-8-SAE, per the SAE J1850 specification.

- Polynomial = 0x1D
- Initial value = 0xFF

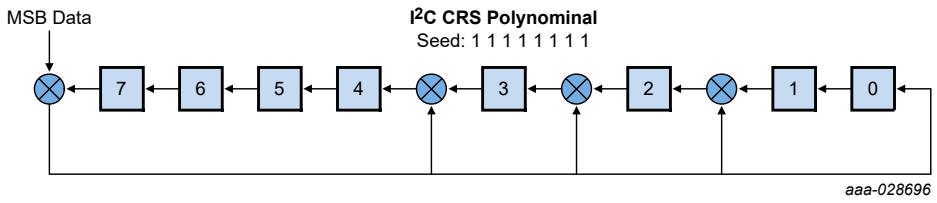


Figure 22. 8 bit SAE J1850 CRC polynomial

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

14.9.14.2 I²C secure write

A secure write mechanism is implemented for specific registers critical to the functional safety of the device.

- When OTP_I2C_ SECURE_EN = 0, the secure write is disabled.
- When OTP_I2C_ SECURE_EN = 1, the secure write is enabled.

When the secure write is enabled, a specific sequence must be followed in order to grant writing access on the corresponding secure register.

Secure write sequence is as follows:

- MCU sends command to modify the secure registers
- PMIC generates a random code in the RANDOM_GEN register
- MCU reads the random code from the RANDOM_GEN register and writes it back on the RANDOM_CHK register

The PMIC compares the RANDOM_CHK against the RANDOM_GEN register:

- If RANDOM_CHK [7:0] = RANDOM_GEN[7:0], the device applies the configuration on the corresponding secure register, and self-clears both the RANDOM_GEN and RANDOM_CHK registers.
- If RANDOM_CHK[7:0] different from RANDOM_GEN[7:0], the device ignores the configuration command and self-clears both the RANDOM_GEN and RANDOM_CHK registers.

In the event the MCU sends any other command instead of providing a value for the RANDOM_CHK register, the state machine cancels the ongoing secure write transaction and performs the new I²C command.

In the event the MCU does not provide a value for the RANDOM_CHK register, the I²C transaction will time out 10 ms after the RANDOM_GEN code is generated, and device is ready for a new transaction.

Table 36. Secure bits

Register	Bit	Description
ABIST OV1	AB_SW1_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW2_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW3_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW4_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW5_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW6_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV1	AB_SW7_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV2	AB_LDO1_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV2	AB_LDO2_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV2	AB_LDO3_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST OV2	AB_LDO4_OV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW1_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW2_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW3_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW4_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW5_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW6_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV1	AB_SW7_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV2	AB_LDO1_UV	Writing a 1 to this flag to clear the ABIST fault notification

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 36. Secure bits *...continued*

Register	Bit	Description
ABIST UV2	AB_LDO2_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV2	AB_LDO3_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST UV2	AB_LDO4_UV	Writing a 1 to this flag to clear the ABIST fault notification
ABIST RUN	AB_RUN	Writing a 1 starts an ABIST on demand
FSOB FLAGS	FSOB_ASS_NOK	Writing a 1 to this flag to clear the FSOB flag
FSOB FLAGS	FSOB_SFAULT_NOK	Writing a 1 to this flag to clear the FSOB flag
FSOB FLAGS	FSOB_WDI_NOK	Writing a 1 to this flag to clear the FSOB flag
FSOB FLAGS	FSOB_WDC_NOK	Writing a 1 to this flag to clear the FSOB flag
FSOB FLAGS	FSOB_HFAULT_NOK	Writing a 1 to this flag to clear the FSOB flag
CTRL1	TMP_MON_EN	Writing a 0 disables the thermal monitor, preventing the thermal interrupts and thermal shutdown event from being detected
CTRL1	VIN_OVLO_EN	Writing a 0 disables the VIN overvoltage lockout monitor completely
CTRL1	VIN_OVLO_SDWN	Writing a 0 disables a shutdown event upon a VIN overvoltage condition (only interrupts are provided)
CTRL1	WD_EN	Writing a 0 disables the watchdog counter block
CTRL1	WD_STBY_EN	Writing a 0 disables the watchdog counter during the standby mode
CTRL1	WDI_STBY_ACTIVE	Writing a 0 disables the monitoring of WDI input during standby mode
CTRL1	I2C_SECURE_EN	Writing a 0 disables de I^2C secure write mode
VMONEN1	SW1VMON_EN	Writing a 0 disables the OV/UV monitor for SW1
VMONEN1	SW2VMON_EN	Writing a 0 disables the OV/UV monitor for SW2
VMONEN1	SW3VMON_EN	Writing a 0 disables the OV/UV monitor for SW3
VMONEN1	SW4VMON_EN	Writing a 0 disables the OV/UV monitor for SW4
VMONEN1	SW5VMON_EN	Writing a 0 disables the OV/UV monitor for SW5
VMONEN1	SW6VMON_EN	Writing a 0 disables the OV/UV monitor for SW6
VMONEN1	SW7VMON_EN	Writing a 0 disables the OV/UV monitor for SW7
VMONEN2	LDO1VMON_EN	Writing a 0 disables the OV/UV monitor for LDO1
VMONEN2	LDO2VMON_EN	Writing a 0 disables the OV/UV monitor for LDO2
VMONEN2	LDO3VMON_EN	Writing a 0 disables the OV/UV monitor for LDO3
VMONEN2	LDO4VMON_EN	Writing a 0 disables the OV/UV monitor for LDO4

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15 Functional blocks

15.1 Analog core and internal voltage references

All regulators use the main bandgap as the reference for the output voltage generations, this bandgap is also used as reference for the internal analog core and digital core supplies. The performance of the regulators is directly dependent on the performance of the bandgap.

No external DC loading is allowed on V1P5A and V1P5D. V1P5D is kept powered as long as there is a valid supply and/or valid coin cell and it may be used as a reference voltage for the VDDOTP and TBBEN pins during system power on.

A second bandgap is provided as the reference for all the monitoring circuits. This architecture allows the PF8200 to provide a reliable way to detect not only single point, but also latent faults in order to meet the metrics required by an ASIL B level application.

Table 37. Internal supplies electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{1P5D}	V1P5D output voltage	1.50	1.60	1.65	V
C_{1P5D}	V1P5D output capacitor	—	1.0	—	µF
V_{1P5A}	V1P5A output voltage	1.50	1.60	1.65	V
C_{1P5A}	V1P5A output capacitor	—	1.0	—	µF

15.2 Coin cell charger

A coin cell or super capacitor may be connected to the LICELL pin, the PF8100/PF8200 features a simple constant current charger available at the LICELL pin.

The COINCHG_EN bit is used to enable or disable the coin cell charger during the system-on states (run and standby) via I^2C.

- When COINCHG_EN = 0 the coin cell charger is disabled in run or standby modes.
- When COINCHG_EN = 1 the coin cell charger is enabled in run or standby modes.

The COINCHG_EN bit is reset to 0, when VIN crosses the UVDET threshold.

During the run mode, the coin cell charger utilizes a 60 µA charging current. If enabled during standby mode, the coin cell charger utilizes only a 10 µA charging current to be able to maintain low power consumption while still being able to maintain the backup battery voltage charged at all time.

The COINCHG_OFF bit is used to enable or disable the coin cell charger during the QPU_Off state via I^2C. In this mode, the charger utilizes a 10 µA charging current.

- When COINCHG_OFF = 0 the coin cell charger is disabled in QPU_Off state.
- When COINCHG_OFF = 1 the coin cell charger is enabled in QPU_Off state.

If the system requires to allow charging of the coin cell during the QPU_Off, the system should enable the COINCHG_OFF bit during the run mode and the charger turns on during the QPU_Off state, if programmed to stay in this state after power down. The COINCHG_OFF bit is reset to 0, when VIN crosses the UVDET threshold.

The VCOIN[3:0] bits set the target charging voltage for the LICELL pin as shown in the table below. The OTP_VCOIN[3:0] bits are used to set the default voltage for the coin cell battery charger.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 38. Coin cell charger voltage level

VCOIN[3:0]	Target LICELL voltage (V)
0000	1.8
0001	2.0
0010	2.1
0011	2.2
0100	2.3
0101	2.4
0110	2.5
0111	2.6
1000	2.7
1001	2.8
1010	2.9
1011	3.0
1100	3.1
1101	3.2
1110	3.3
1111	3.6

Table 39. Coin cell electrical characteristics

All parameters specified for T_A = −40 °C to 105 °C, VIN = 5.0 V, All output voltage settings, typical external components, unless otherwise noted. Typical values are specified for T_A = 25 °C, VIN = 5.0 V, typical external components, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	2.5	—	5.5	V
$V_{COINACC}$	Voltage accuracy (2.6 V to 3.6 V)	−3.0	—	3.0	%
$V_{COINACC}$	Voltage accuracy (1.8 V to 2.5 V)	−4.0	—	4.0	%
$V_{COINHDR}$	Input voltage headroom Minimum VIN headroom to guarantee V_{COIN} regulation at I_{COINHI}	300	—	—	mV
$V_{COINHYS}$	Charging hysteresis	60	100	200	mV
$I_{COINACC}$	Current accuracy	−30	—	30	%
I_{COINHI}	Coin cell charger current in run mode	—	60	—	µA
I_{COINLO}	Coin cell charger current in standby and QPU_Off	—	10	—	µA
$I_{QCOINCH}$	Quiescent current when coin cell is charging	0	10	20	µA
$V_{COINRLHYS}$	Reverse leakage comparator hysteresis	50	100	170	mV
$V_{COINRLTR}$	Reverse leakage comparator trip voltage at rising edge (V_{IN} − V_{COIN}) at every VCOIN setting	100	200	300	mV
$V_{COINRLTF}$	Reverse leakage comparator trip voltage at falling edge (V_{IN} − V_{COIN}) at every VCOIN setting	0	100	250	mV

15.3 VSNVS LDO/switch

VSNVS is a 10 mA LDO/switch provided to power the RTC domain in the processor. In systems using the i.MX 8 processors, it powers the VDD_SNVS_IN domain of the MCU.

Three scenarios may be possible during VIN application:

1. Coin cell was applied for the first time before VIN power up.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

2. Coin cell is not present upon VIN power up.
3. Coin cell has been present after a previous power cycle.

If coin cell is first applied without VIN present, VSNVS remains disabled until VIN > UVDET and the VSNVS gets loaded with the OTP fuse configuration.

When VIN is applied and no coin cell is present, VSNVS is initially disabled and it is only enabled to its regulation point after OTP fuses are loaded.

If coin cell has been present after a previous power cycle, the VSNVS configuration is reloaded from the OTP registers when the VIN crosses the UVDET threshold. This way, if the VSNVS was modified via the I^2C configuration bit, it will always be reset to the default value after a VIN power cycle.

When VIN < V_{WARNTH}, a best of supply circuit decides whether VSNVS is powered by VIN or LICELL.

- When VIN is rising and VIN > UVDET, VSNVS is powered by VIN. When operating from VIN, it can regulate the output to 1.8 V, 3.0 V or 3.3 V. If the configured output voltage is higher than the input source, the VSNVS operates in dropout mode to track the input voltage.
- When operating from LICELL, it regulates the output when the output voltage is selected at 1.8 V. VSNVS operates as a switch from LICELL when the output voltage setting is selected to 3.0 V or 3.3 V.

The following table shows the expected operation of the VSNVS block for different voltage settings and different input voltage conditions.

Table 40. VSNVS operation description

OTP_VSNVSVOLT[1:0]	VSNVS output voltage (V)	VIN	Expected VSNVS output
00	Disabled	Do not care	VSNVS is disabled on OTP
01	1.8	< V_{WARNTH} falling	Regulate to 1.8 V from the highest of VIN or LICELL [1]
01	1.8	> UVDET rising	Regulate to 1.8 V from VIN
10	3.0	< V_{WARNTH} falling	Switch mode from the highest of VIN or LICELL
10	3.0	> UVDET rising	Regulate to 3.0 from VIN [1]
11	3.3	< V_{WARNTH} falling	Switch mode from the highest of VIN or LICELL
11	3.3	> UVDET rising	Regulate to 3.3 from VIN [1]

[1] Regulator is in drop off mode, if input is not enough to regulate to set point.

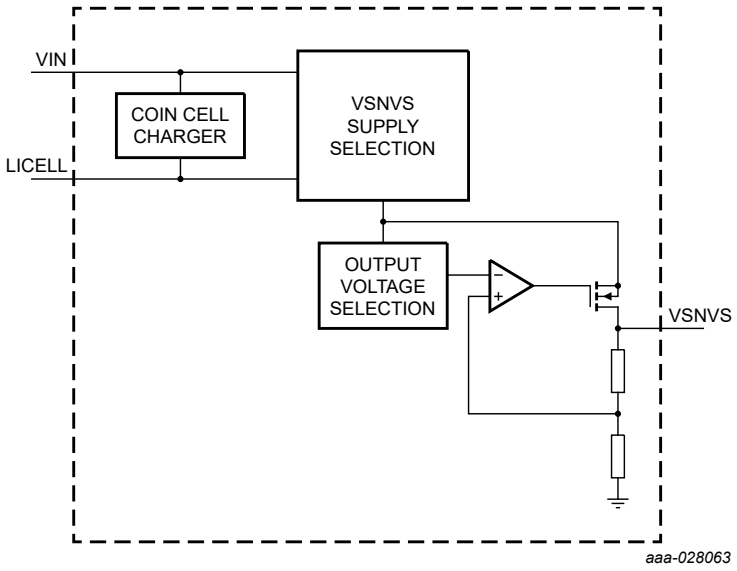


Figure 23. VSNVS block diagram

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The VSNVS output keeps regulation through all states, including the system-on, off modes, power down sequence, watchdog reset, fail-safe transition and fail-safe state as long as it has a valid input (VIN or LICELL), and the output has been configured by the OTP_VSNVSVOLT[1:0] registers.

Table 41. VSNVS output voltage configuration

OTP_VSNVSVOLT[1:0]	VSNVSVOLT[1:0]	VSNVS output voltage (V)
00	00	Off
01	01	1.8
10	10	3.0
11	11	3.3

For system debugging purposes, the VSNVS output may be changed during the system-on states by changing the VSNVSVOLT[1:0] bits in the functional I^2C registers.

Table 42. VSNVS electrical characteristics

All parameters are specified at T_A = −40 °C to 105 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN_SNVS}	Operating voltage range from VIN	2.5	—	5.5	V
V_{LICELL_SNVS}	Operating voltage range from LICELL	1.728	—	5.5	V
I_{SNVS}	VSNVS load current range	0	—	10	mA
V_{SNVS_ACC}	VSNVS output voltage accuracy in LDO mode	−5.0	—	5.0	%
V_{SNVS_RDSON}	VSNVS LDO on resistance VSNVSVOLT[1:0] = 10 or 11	—	—	20	Ω
VSNVS_IQ	VSNVS quiescent current in LDO mode	—	5.0	—	µA
V_{SNVS_HDR}	VSNVS LDO headroom voltage Minimum voltage above setting VSNVSVOLT[1:0] = 10 or 11 to guarantee regulation with 5 % tolerance	200	—	—	mV
V_{SNVS_HDR}	VSNVS LDO headroom voltage Minimum voltage above setting VSNVSVOLT[1:0] = 01 to guarantee regulation with 5 % tolerance	500	—	—	mV
V_{SNVS_OS}	VSNVS startup overshoot	—	—	200	mV
V_{SNVS_TRANS}	VSNVS load transient	−100	—	100	mV
$V_{SNVS_SW_R}$	VSNVS switch mode resistance VSNVSVOLT[1:0] = 10 or 11	—	—	20	Ω
$V_{SNVS_LICELL_IQ}$	VSNVS quiescent current in switch mode VSNVSVOLT[1:0] = 10 or 11	—	1.0	—	µA
V_{SNVS_ILIM}	VSNVS current limit	20	—	70	mA
V_{SNVS_TON}	VSNVS turn on time Block enabled to VSNVS at 90 % of final value	—	—	1.35	ms

15.4 Type 1 buck regulators (SW1 to SW6)

The PF8100/PF8200 features six low-voltage regulators with input supply range from 2.5 V to 5.5 V and output voltage range from 0.4 V to 1.8 V in 6.25 mV steps. Each voltage regulator is capable to supply 2.5 A and features a programmable soft-start and DVS ramp for system power optimization.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

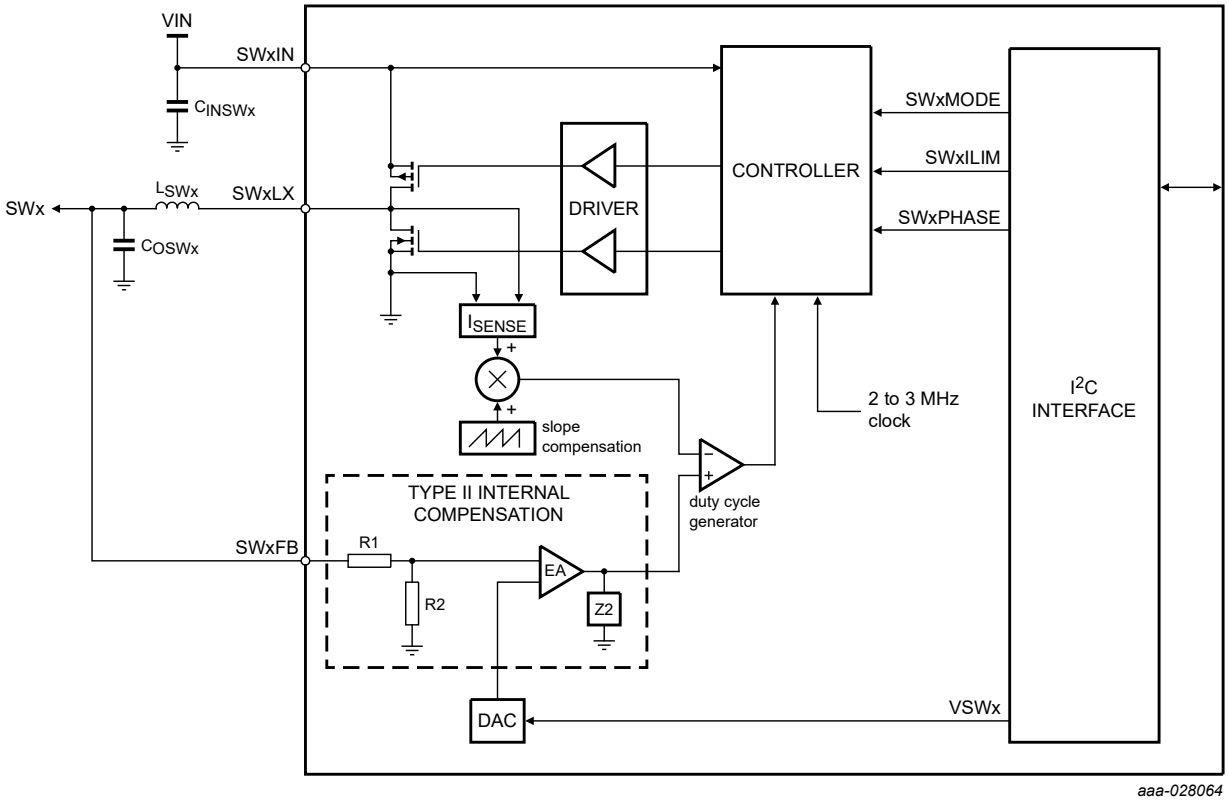


Figure 24. Buck regulator block diagram

The OTP_SWxDVS_RAMP bit sets the default step/time ratio for the power up ramp during the power up/down sequence as well as the DVS slope during the system on.

The power down ramp and DVS rate of the Type 1 buck regulators can be modified during the system-on states by changing the SWxDVS_RAMP bit on the I²C register map.

Table 43. DVS ramp speed configuration

SWxDVS_RAMP bit	DVS ramp speed
0	Slow DVS ramp
1	Fast DVS ramp

The DVS ramp rate is based on the internal clock configuration as shown in Table 44.

Table 44. Ramp rates

All ramp rates are typical values.
Clock frequency tolerance = ± 6 %.

CLK_FREQ[3:0]	Clock frequency (MHz)	Regulators frequency (MHz)	SWxDVS_RAMP = 0 DVS_Up (mV/µs)	SWxDVS_RAMP = 0 DVS_Down (mV/µs)	SWxDVS_RAMP = 1 DVS_Up (mV/µs)	SWxDVS_RAMP = 1 DVS_Down (mV/µs)
0000	20	2.5	7.813	5.208	15.625	10.417
0001	21	2.625	8.203	5.469	16.406	10.938
0010	22	2.75	8.594	5.729	17.188	11.458
0011	23	2.875	8.984	5.990	17.969	11.979
0100	24	3	9.375	6.250	18.750	12.500
1001	16	2	6.250	4.167	12.500	8.333
1010	17	2.125	6.641	4.427	13.281	8.854
1011	18	2.25	7.031	4.688	14.063	9.375

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 44. Ramp rates...*continued*

All ramp rates are typical values.
Clock frequency tolerance = ± 6 %.

CLK_FREQ[3:0]	Clock frequency (MHz)	Regulators frequency (MHz)	SWxDVS_RAMP = 0 DVS_Up (mV/µs)	SWxDVS_RAMP = 0 DVS_Down (mV/µs)	SWxDVS_RAMP = 1 DVS_Up (mV/µs)	SWxDVS_RAMP = 1 DVS_Down (mV/µs)
1100	19	2.375	7.422	4.948	14.844	9.896

Type 1 Buck regulators use 8 bits to set the output voltage.

- The VSWx_RUN[7:0] set the output voltage during the run mode.
- The VSWx_STBY[7:0] set the output voltage during the standby mode.

The default output voltage configuration for the run and the standby modes is loaded from the OTP_VSWx[7:0] registers upon power up.

Table 45. Output voltage configuration

Set point	VSWx_RUN[7:0] VSWx_STBY[7:0]	V_{SWxFB} (V)
0	00000000	0.40000
1	00000001	0.40625
2	00000010	0.41250
3	00000011	0.41875
. .	. .	. .
175	10101111	1.49375
176	10110000	1.50000
177	10110001	1.80000
178 to 255	10110010 to 11111111	Reserved

DVS operation is available for all voltage settings between 0.4 V to 1.5 V. However, the SWx regulator is not intended to perform DVS transitions to or from the 1.8 V configuration. In the event a voltage change is requested between any of the low voltage settings and 1.8 V, the switching regulator is automatically disabled first and then re-enabled at the selected voltage level to avoid an uncontrolled transition to the new voltage setting.

Each regulator is provided with two bits to set its mode of operation.

- The SWx_RUN_MODE[1:0] bits allow the user to change the mode of operation of the SWx regulators during the run state. If the regulator was programmed as part of the power up sequence, the SWx_RUN_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise, it is loaded with 0b00 (disabled).
- The SWx_STBY_MODE[1:0] bits allow the user to change the mode of operation of the SWx regulators during the standby state. If the regulator was programmed as part of the power up sequence, the SWx_STBY_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise, it is loaded with 0b00 (disabled).

Table 46. SW regulator mode configuration

SWx_MODE[1:0]	Mode of operation
00	OFF
01	PWM mode
10	PFM mode
11	Autoskip mode

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The SWx_MODE_I interrupt asserts the INTB pin when any of the Type 1 regulators have changed the mode of operation, provided the corresponding interrupt is not masked.

To avoid potential detection of an OV/UV fault during SWx ramp up, it is recommended to power up the regulator in PWM or autoskip mode.

The type 1 buck regulators use 2 bits SWxILIM[1:0], to program the current limit detection.

Table 47. SWx current limit selection

SWxILIM[1:0]	Typical current limit
00	2.1 A
01	2.6 A
10	3.0 A
11	4.5 A

The current limit specification is given with respect to the inductor peak current. To calculate the DC current at which the buck regulator enters into current limitation, it is necessary to calculate the inductor ripple current. An ideal approximation is enough to obtain the ripple current as follows:

$$\Delta iL = VOUT \times (1 - VOUT / VIN) / (L \times FSW)$$

where L is the inductance value and FSW is the selected switching frequency.

The DC current limit is then calculated by

$$DC\ ILIM = ILIM - (\Delta iL / 2)$$

in order to account for component tolerances, use the minimum inductor value per the inductor specification.

During single phase operation, all buck regulators use 3 bits (SWxPHASE[2:0]) to control the phase shift of the switching frequency. Upon power up, the switching phase of all regulators is defaulted to 0 degrees and can be modified during the system-on states.

Table 48. SWx phase configuration

SWx_PHASE[2:0]	Phase shift [degrees]
000	45
001	90
010	135
011	180
100	225
101	270
110	315
111	0 (default)

Each one of the buck regulator provide 2 OTP bits to configure the value of the inductor used in the corresponding block. The OTP_SWx_LSELECT[1:0] allow to choose the inductor as shown in Table 49.

Table 49. SWx inductor selection bits

OTP_SWx_LSELECT[1:0]	Inductor value
00	1.0 µH
01	0.47 µH

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 49. SWx inductor selection bits*...continued*

OTP_SWx_LSELECT[1:0]	Inductor value
10	1.5 µH
11	Reserved

15.4.1 SW6 VTT operation

SW6 features a selectable VTT mode to create VTT termination for DDR memories.

When SW6_VTTEN = 1, the VTT mode is enabled. In this mode, SW6 reference voltage is internally connected to SW5FB output through a divider by 2.

During the VTT mode the DVS operation on SW6 is disabled and SW6 output is given by V_{SW5FB} / 2. In this mode, the minimum output voltage configuration for SW5 should be 800 mV to ensure the SW6 is still within the regulation range at its output.

During the power up sequence, the SW6 (VTT) may be turned on in the same or at a later slot than SW5, as required by the system. When SW6 and SW5 are enabled in the same slot, SW6 will always track the VSW5/2. When SW6 is enabled after SW5, it will ramp up gradually to a predefined voltage and once this voltage is reached, it will start tracking VSW5/2. The user may adjust the value at which the SW6 should start tracking the voltage on the SW5 regulator by setting the OTP_VSW6 register accordingly.

During normal operation, if the SW5 is disabled via the I^2C command, SW6 will track the output of SW5 and both regulators will be discharged together and pulled down internally. When SW5 is enabled back via the I^2C commands, the SW5 output will ramp-up to the corresponding voltage while SW6 is always VSW5/2.

When only SW6 is disabled, the PMIC uses the OTP_VTT_PDOWN bit to program whether the SW6 regulator is disabled with the output in high impedance or discharged internally.

- When OTP_VTT_PDOWN = 0, the output is disabled in high impedance mode.
- When OTP_VTT_PDOWN = 1, the output is disabled with the internal pull down enabled.

When SW6 is requested to enable back again, the SW6 will ramp-up to the voltage set on the VSW6_RUN or VSW6_STBY registers. Once it reaches the final DVS value, it will change its reference to start tracking SW5 output again. Note that VSW6_RUN(STBY) must be set to VSW5_RUN(STBY)/2 or the closest code by the MCU to ensure proper operation.

When operating in VTT mode, the minimum output voltage configuration for SW5 should be 800 mV to ensure the SW6 is still within the regulation range at its output.

15.4.2 Multiphase operation

Regulators SW1, SW2, SW3 and SW4 can be configured in quad phase mode. In this mode, SW1 registers control the output voltage and other configurations. Likewise, SW1FB pin becomes the main feedback node for the resulting voltage rail, however all four FB pins should be connected together. In quad phase operation, each phase can be independently set via the corresponding SWxPHASE[1:0] bits.

Regulators SW1, SW2 and SW3 can be configured in triple phase mode. In this mode, SW1 registers control the output voltage and other configurations. Likewise, SW1FB pin becomes the main feedback node for the resulting voltage rail, however all three FB pins should be connected together. In triple phase operation, each phase can be independently set via the corresponding SWxPHASE[1:0] bits.

When SW1 to SW3 are configured in triple phase, the SW4 operates in single phase.

Regulators SW1 and SW2 can be configured in dual phase mode. In this mode, SW1 registers control the output voltage and other configurations. Likewise, SW1FB pin becomes the main feedback node for the resulting voltage rail, however the two FB pins should be connected together. In dual phase operation, each phase can be independently set via the corresponding SWxPHASE[1:0] bits.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

The OTP_SW1CONFIG[1:0] bits are used to select the dual phase configuration for SW1/SW2, as well as triple or quad phase configuration.

Table 50. OTP_SW1CONFIG register description

OTP_SW1CONFIG[1:0]	Description
00	SW1 and SW2 operate in single phase mode
01	SW1/SW2 operate in dual phase mode
10	SW1/SW2/SW3/SW4 operate in quad phase mode
11	SW1/SW2/SW3 operate in triple phase mode

Regulators SW3 and SW4 can be configured in dual phase mode. In this mode, SW4 registers control the output voltage and other configurations. Likewise, SW4FB pin becomes the main feedback node for the resulting voltage rail, however the two FB pins should be connected together.

In dual phase operation, each phase can be independently set via the corresponding SWxPHASE[1:0] bits.

The OTP_SW4CONFIG[1:0] bits are used to select the dual phase operation of SW3/SW4.

Table 51. OTP SW4CONFIG register description

OTP_SW4CONFIG[1:0]	Description
00	SW3 and SW4 operate in single phase mode
01	SW3/SW4 operate in dual phase mode
10	Reserved
11	Reserved

Configuring regulators SW1 through SW4 in quad phase or triple phase operation overrides the configuration of the OTP_SW4CONFIG[1:0] bits.

Regulators SW5 and SW6 can be configured in dual phase mode. In this mode, SW5 registers control the output voltage and other configurations. Likewise, SW5FB pin becomes the main feedback node for the resulting voltage rail, however the two FB pins should be connected together.

In dual phase operation, each phase can be independently set via the corresponding SWxPHASE[1:0] bits.

The OTP_SW5CONFIG[1:0] bits are used to select single or dual phase configuration for SW5/SW6.

Table 52. OTP_SW5CONFIG register description

OTP_SW5CONFIG[1:0]	Description
00	SW5 and SW6 operate in single phase mode
01	SW5/SW6 operate in dual phase mode
10	Reserved
11	Reserved

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

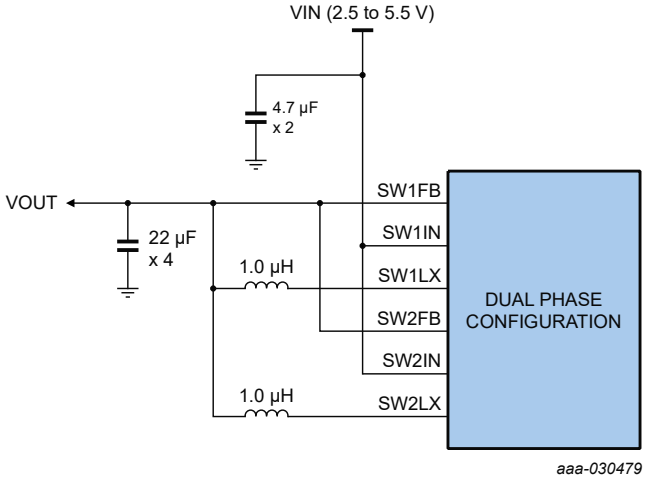


Figure 25. Dual phase configuration

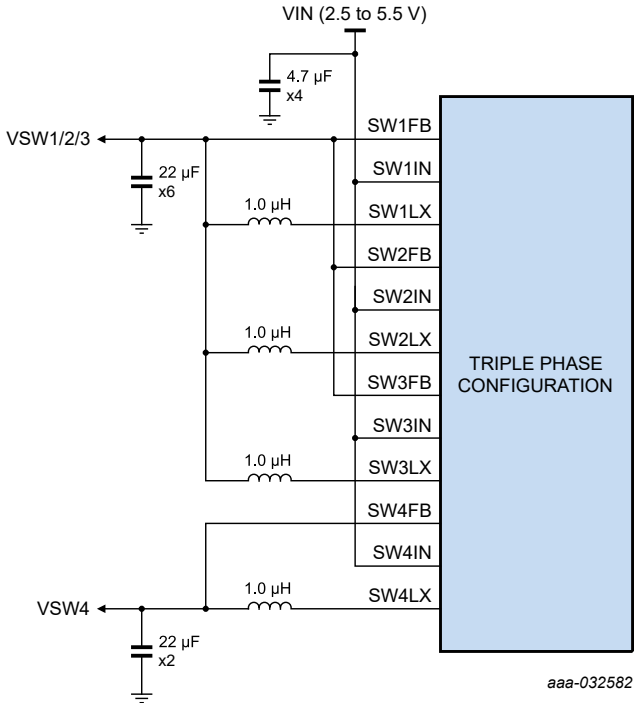


Figure 26. Triple phase configuration

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

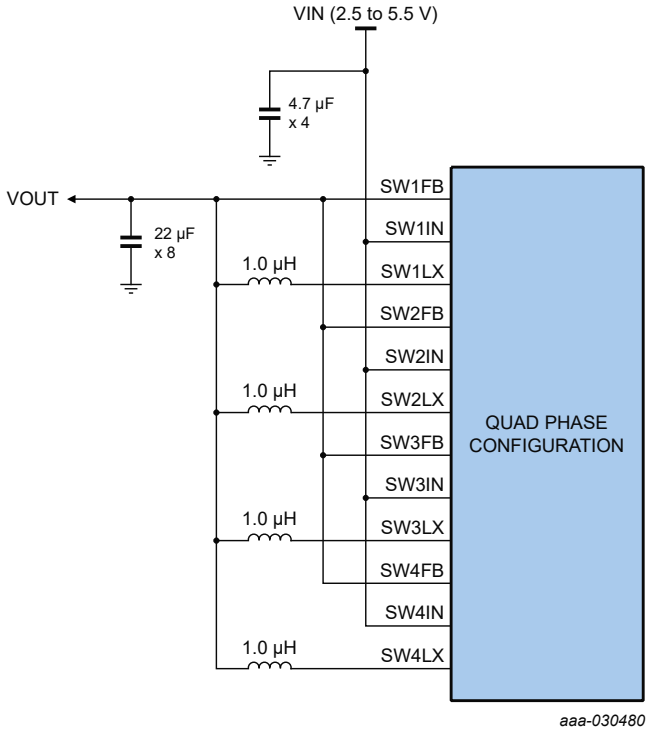


Figure 27. Quad phase configuration

15.4.3 Electrical characteristics

Table 53. Type 1 buck regulator electrical characteristics

All parameters are specified at T_A = −40 to 105 °C, VIN = V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at VIN = V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
V_{SWxIN} [3]	Operating functional input voltage	UVDET	—	5.5	V
V_{SWxACC}	Output voltage accuracy PWM mode 0.4 V ≤ V_{SWxFB} < 0.8 V 0 ≤ I_{SWx} ≤ 2.5 A	−10	—	10	mV
V_{SWxACC}	Output voltage accuracy PWM mode 0.8 V ≤ V_{SWxFB} ≤ 1.0 V 0 ≤ I_{SWx} ≤ 2.5 A	−1.5	—	1.5	%
V_{SWxACC}	Output voltage accuracy PWM mode 1.0 V < V_{SWxFB} ≤ 1.5 V 0 ≤ I_{SWx} ≤ 2.5 A	−1.5	—	1.5	%
V_{SWxACC}	Output voltage accuracy PWM mode V_{SWxFB} = 1.8 V 0 ≤ I_{SWx} ≤ 2.5 A	−1.5	—	1.5	%
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode 0.4 V ≤ V_{SWxFB} ≤ 1.5 V 0 ≤ I_{SWx} ≤ 100 mA	−36	—	36	mV
$V_{SWxACCPFM}$	Output voltage accuracy PFM mode V_{SWxFB} = 1.8 V 0 ≤ I_{SWx} ≤ 100 mA	−57	—	57	mV
$t_{PFMtoPWM}$	PFM to PWM transition time	30	—	—	µs
I_{SWx}	Max load current in single phase [4]	2500	—	—	mA

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 53. Type 1 buck regulator electrical characteristics...*continued*

All parameters are specified at T_A = −40 to 105 °C, VIN = V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at VIN = V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
I_{SWx_DP}	Max load current in dual phase [4]	5000	—	—	mA
I_{SWx_TP}	Max load current in triple phase	7500	—	—	mA
I_{SWx_QP}	Max load current in quad phase	10000	—	—	mA
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 00	1.6	2.1	2.5	A
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 01	2.0	2.6	3.1	A
I_{SWxLIM}	Current limiter - inductor peak current detection SWxILIM[1:0] = 10	2.4	3.0	3.7	A
I_{SWxLIM}	Current limiter - inductor peak current detection [5] SWxILIM[1:0] = 11	3.6	4.5	5.45	A
I_{SW5LIM}	Current limiter - inductor peak current detection [6] SW5ILIM[1:0] = 11	3.9	4.5	5.45	A
$I_{SWxNLIM}$	Negative current limit in single phase mode	0.6	1.0	1.4	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 00 (primary)	3.2	4.2	5.0	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 01 (primary)	4.0	5.2	6.2	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 10 (primary)	4.8	6.0	7.4	A
$I_{SWxxLIM_DP}$	Current limit in dual phase operation SWxILIM = 11 (primary)	7.2	9.0	10.9	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SW1ILIM[1:0] = 00	4.8	6.3	7.5	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SW1ILIM[1:0] = 01	6.0	7.8	9.3	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SW1ILIM[1:0] = 10	7.2	9.0	11.1	A
$I_{SWxxLIM_TP}$	Current limit in triple phase operation SW1ILIM[1:0] = 11	10.8	13.5	16.35	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SW1ILIM = 00	7.2	8.4	10	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SW1ILIM = 01	8.0	10.4	12.4	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SW1ILIM = 10	9.6	12.0	14.8	A
$I_{SWxxLIM_QP}$	Current limit in quad phase operation SW1ILIM = 11	14.4	18.0	21.8	A
V_{SWxOSH}	Startup overshoot SWxDVS RAMP = 6.25 mV/µs VSWxIN = 5.5 V, VSWxFB= 1.0 V	−25	25	50	mV
t_{ONSWx}	Turn on time From enable to 90 % of end value SWxDVS RAMP = 0 (6.25 mV/µs) VSWxIN = 5.5 V, VSWxFB= 1.0 V	—	160	—	µs
$t_{ONSWxMAX}$	Maximum turn on time From enable to 90 % of end value SWxDVS RAMP = 0 (6.25 mV/µs) VSWxIN = 5.5 V, VSWxFB= 1.5 V	—	—	310	µs
t_{ONSWx_MIN}	Minimum turn on time From enable to 90 % of end value SWxDVS RAMP = 1 (12.5 mV/µs) VSWxIN = 5.5 V, VSWxFB= 0.4 V	34.2	—	—	µs
η_{SWx}	Efficiency (PFM mode, 1.0 V, 1.0 mA)	—	80	—	%
η_{SWx}	Efficiency (PFM mode, 1.0 V, 50 mA)	—	81	—	%
η_{SWx}	Efficiency (PFM Mode, 1.0 V, 100 mA)	—	82	—	%
η_{SWx}	Efficiency (PWM mode, 1.0 V, 500 mA)	—	83	—	%

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 53. Type 1 buck regulator electrical characteristics...*continued*

All parameters are specified at T_A = −40 to 105 °C, VIN = V_{SWxIN} = UVDET to 5.5 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at VIN = V_{SWxIN} = 5.0 V, V_{SWxFB} = 1.0 V, I_{SWx} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
η_{SWx}	Efficiency (PWM mode, 1.0 V, 1000 mA)	—	82	—	%
η_{SWx}	Efficiency (PWM mode, 1.0 V, 2000 mA)	—	79	—	%
F_{SWx}	PWM switching frequency range Frequency set by CLK_FREQ[3:0]	 1.9	 2.5	 3.15	MHz
$T_{OFFminSWx}$	Minimum off time	—	27	—	ns
T_{DBSWx}	Deadband time	—	3.0	—	ns
T_{slew}	Slewing time (10 % to 90 %)	—	—	5.0	ns
D_{VSWx}	Output ripple in PWM mode	—	—	1.0	%
$V_{SWxLOTR}$	Transient load regulation (overshoot/undershoot) at 0.8 V < V_{SWxFB} ≤ 1.2 V ILoad = 200 mA to 1.0 A, di/dt = 2.0 A/µs (single phase) ILoad = 400 mA to 2.0 A, di/dt = 4.0 A/µs (dual phase) ILoad = 600 mA to 3.0 A, di/dt = 6.0 A/µs (triple phase) ILoad = 800 mA to 4.0 A, di/dt = 8.0 A/µs (quad phase) Output capacitance = 44 µF per phase	 −25	 —	 +25	mV
$V_{SWxLOTR}$	Transient load regulation (overshoot/undershoot) at 1.25 < V_{SWxFB} < 1.8 V ILoad = 200 mA to 1.0 A, di/dt = 2.0 A/µs (single phase) ILoad = 400 mA to 2.0 A, di/dt = 4.0 A/µs (dual phase) ILoad = 600 mA to 3.0 A, di/dt = 6.0 A/µs (triple phase) ILoad = 800 mA to 4.0 A, di/dt = 8.0 A/µs (quad phase) Output capacitance = 44 µF per phase	 −3.0	 —	 +3.0	%
I_{RCS}	DCM (skip mode) reverse current sense threshold Current flowing from PGND to SWxLX	 −200	 —	 200	mA
I_{SWxQ}	Quiescent current PFM mode	 —	 14	 —	µA
I_{SWxQ}	Quiescent current Auto skip mode	 —	 160	 250	µA
I_{SWxQ_DP}	Quiescent current in dual phase PWM mode	—	200	320	µA
I_{SWxQ_QP}	Quiescent current in quad phase PWM mode	—	240	480	µA
$R_{ONSWxHS}$	SWx high-side P-MOSFET $R_{DS(on)}$ [7]	—	—	135	mΩ
$R_{ONSWxLS}$	SWx low-side N-MOSFET $R_{DS(on)}$ [7]	—	—	80	mΩ
R_{SWxDIS}	Discharge resistance Regulator disabled and ramp down completed	 20	 70	 120	Ω

[1] For VSWx configurations greater than 1.35 V, full parametric operation is guaranteed for 2.7 V < SWxVIN < 5.5 V. Below 2.7 V, the SWx regulators are fully functional with degraded operation due to headroom limitation.
[2] For VSWx = 1.8 V, output capacitance should be kept at or below the maximum recommended value. Likewise, it is recommended to use the slow turn-on/off ramp rate to ensure the output is discharged completely when it is disabled.
[3] VSWxIN must be connected to VIN to ensure proper device operation.
[4] The Type 1 buck regulator in single or dual phase configuration is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken to prevent reaching PMIC thermal shutdown during high ambient temperature conditions.
[5] Current limit applicable to SW1, SW2, SW3, SW4, and SW6
[6] Current limit applicable to SW5 to ensure maximum power requirement for the MEMC rail in i.MX8QM systems.
[7] Max $R_{DS(on)}$ does not include bondwire resistance. Consider +50 % tolerance to account for bondwire and pin loss.

Table 54. Recommended external components

Symbol	Parameter	Min	Typ	Max	Unit
L	Output inductor Maximum inductor DC resistance 50 mΩ [1] Minimum saturation current at full load: 3.0 A	0.47	1.0	1.5	µH
C_{out}	Output capacitor Use 2 x 22 µF, 6.3 V X7T ceramic capacitor to reduce output capacitance ESR.	—	44	—	µF
C_{in}	Input capacitor 4.7 µF, 10 V X7R ceramic capacitor	—	4.7	—	µF

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

[1] Keep inductor DCR as low as possible to improve regulator efficiency.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15.5 Type 2 buck regulator (SW7)

The PF8100/PF8200 also features one single phase low-voltage buck regulator (SW7) with an input voltage range between 2.5 V and 5.5 V and an output voltage range from 1.0 V to 4.1 V.

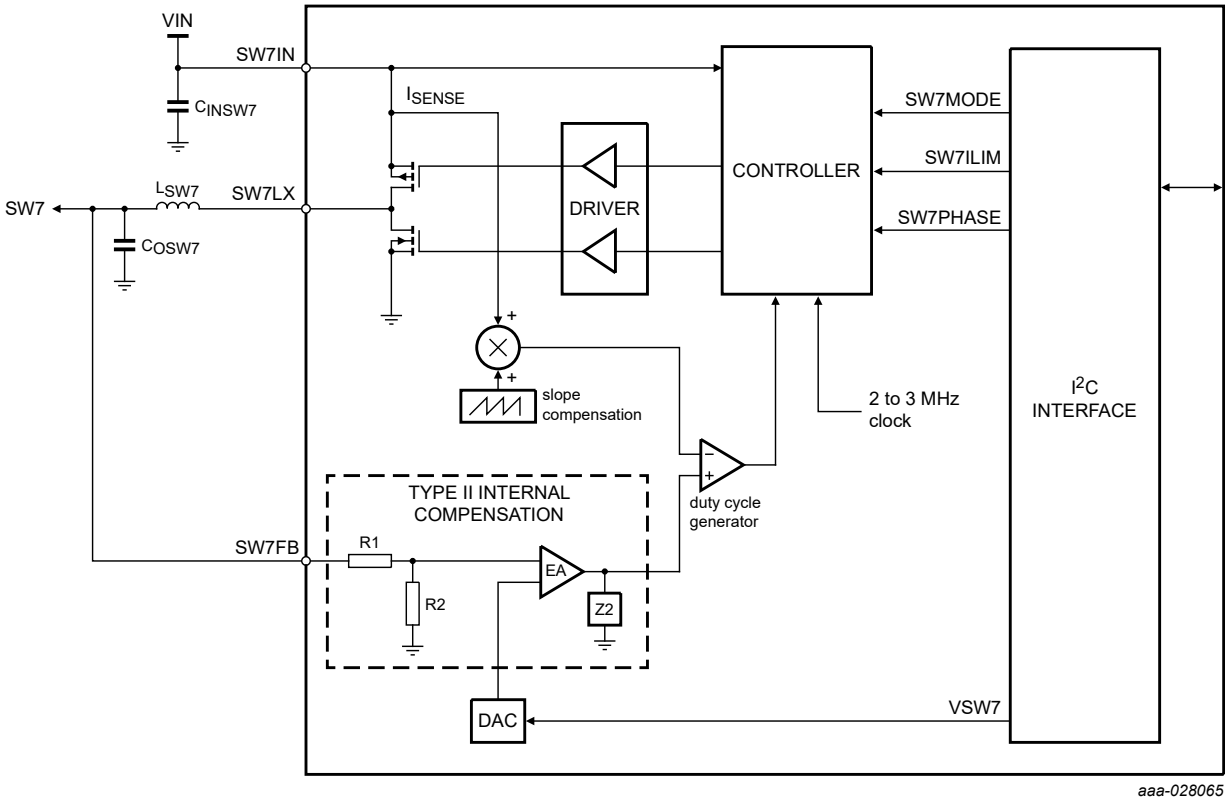


Figure 28. Type 2 buck regulator block diagram

Buck regulator SW7 uses 5 bits to set the output voltage. The VSW7[4:0] sets the output voltage during the run and the standby mode.

The SW7 is designed to have a fixed voltage for entire system operation. In the event a system requires this regulator to change its output voltage during the system-on states, when the SW7 is commanded to change its voltage via the I^2C command, the output will be discharged first and then enabled back to the new voltage level as stated in the VSW7[4:0] bits.

The default output voltage configuration for the run and the standby modes is loaded from the OTP_VSW7[4:0] registers upon power up.

Table 55. SW7 output voltage configuration

Set point	VSW7[4:0]	V_{SW7FB} (V)
0	0 0000	1.00
1	0 0001	1.10
2	0 0010	1.20
3	0 0011	1.25
4	0 0100	1.30
5	0 0101	1.35
6	0 0110	1.50
7	0 0111	1.60
8	0 1000	1.80

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 55. SW7 output voltage configuration*...continued*

Set point	VSW7[4:0]	V_{SW7FB} (V)
9	0 1001	1.85
10	0 1010	2.00
11	0 1011	2.10
12	0 1100	2.15
13	0 1101	2.25
14	0 1110	2.30
15	0 1111	2.40
16	1 0000	2.50
17	1 0001	2.80
18	1 0010	3.15
19	1 0011	3.20
20	1 0100	3.25
21	1 0101	3.30
22	1 0110	3.35
23	1 0111	3.40
24	1 1000	3.50
25	1 1001	3.80
26	1 1010	4.00
27	1 1011	4.10
28	1 1100	4.10
29	1 1101	4.10
30	1 1110	4.10
31	1 1111	4.10

Regulator SW7 is provided with two bits to set its mode of operation.

- The SW7_RUN_MODE[1:0] bits allow the user to change the mode of operation of the SW7 regulators during the run state. If the regulator was programmed as part of the power up sequence, the SW7_RUN_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise, it is loaded with 0b00 (disabled).
- The SW7_STBY_MODE[1:0] bits allow the user to change the mode of operation of the SW7 regulators during the standby state. If the regulator was programmed as part of the power up sequence, the SW7_STBY_MODE[1:0] bits are loaded with 0b11 (autoskip) by default. Otherwise it is loaded with 0b00 (disabled).

Table 56. SW7 regulator mode configuration

SW7_MODE[1:0]	Mode of operation
00	OFF
01	PWM mode
10	PFM mode
11	Autoskip mode

The SW7_MODE_I interrupt asserts the INTB pin when the SW7 regulator has changed the mode of operation, provided the corresponding interrupt is not masked.

When the device toggles from run to standby mode, the SW7 output voltage remains the same, unless the regulator is enabled/disabled by the corresponding SW7_RUN_MODE[1:0] or SW7_STBY_MODE[1:0] bits.

The SW7ILIM [1:0] bits are used to program the current limit detection level of SW7.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 57. SW7 current limit selection

SW7ILIM[1:0]	Typical current limit
00	2.1 A
01	2.6 A
10	3.0 A
11	4.5 A

The current limit specification is given with respect to the inductor peak current. To calculate the DC current at which the buck regulator enters into current limitation, it is necessary to calculate the inductor ripple current. An ideal approximation is enough to obtain the ripple current as follows:

$$\Delta iL = VOUT \times (1 - VOUT / VIN) / (L \times FSW)$$

where L is the inductance value and FSW is the selected switching frequency.

The DC current limit is then calculated by

$$DC\ ILIM = ILIM - (\Delta iL / 2)$$

in order to account for component tolerances, use the minimum inductor value per the inductor specification.

Regulator SW7 uses 3 bits (SWxPHASE[2:0]) to control the phase shift of the switching frequency. Upon power up, the switching phase is defaulted to 0 degrees and can be modified during the system-on states.

Table 58. SW7 phase configuration

SW7_PHASE[2:0]	Phase shift [degrees]
000	45
001	90
010	135
011	180
100	225
101	270
110	315
111	0

SW7 buck regulator provide 2 OTP bits to configure the value of the inductor used in the power stage. The OTP_SW7_LSELECT[1:0] allow to choose the inductor as shown in the following table.

Table 59. SW7 inductor selection bits

OTP_SW7_LSELECT[1:0]	Inductor value
00	1.0 µH
01	0.47 µH
10	1.5 µH
11	Reserved

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15.5.1 Electrical characteristics

Table 60. Type 2 buck regulator electrical characteristics

All parameters are specified at T_A = −40 to 105 °C, VIN = V_{SW7IN} = UVDET to 5.5 V, V_{SW7FB} = 1.8 V, I_{SW7} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at VIN = V_{SW7IN} = 5.0 V, V_{SW7FB} = 1.8 V, I_{SW7} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
V_{SW7IN}	Operating input voltage range [1] 1.2 V < V_{SW7FB} ≤ 1.85 V, DCR ≤ 40 mΩ	UVDET	—	5.5	V
V_{SW7IN}	Operating input voltage range [1] 1.85 V < V_{SW7FB} < 4.1 V, DCR ≤ 40 mΩ	V_{SW7FB} + 0.65	—	5.5	V
V_{SW7ACC}	Output voltage accuracy PWM mode 0 ≤ I_{SW7} ≤ 2.5 A	−2.0	—	2.0	%
V_{SW7ACC}	Output voltage accuracy PFM mode 0 ≤ I_{SW7} ≤ ΔI/2	−4.0	—	4.0	%
$t_{PFMtoPWM}$	PFM to PWM transition time	10	—	—	µs
I_{SW7}	Maximum output load [2]	2500	—	—	mA
I_{SW7LIM}	Current limiter - inductor peak current detection SW7ILIM = 00	1.6	2.1	2.5	A
I_{SW7LIM}	Current limiter - inductor peak current detection SW7ILIM = 01	2.0	2.6	3.1	A
I_{SW7LIM}	Current limiter - inductor peak current detection SW7ILIM = 10	2.4	3.0	3.7	A
I_{SW7LIM}	Current limiter - inductor peak current detection SW7ILIM = 11	3.6	4.5	5.45	A
$I_{SW7NILIM}$	Negative current limit - inductor valley current detection	0.7	1.0	1.3	A
$t_{SW7RAMP}$	Soft-start ramp time during power up and power down V_{SW7FB} = 1.8 V	90	—	200	µs
t_{ONSW7}	Turn on time From regulator enabled to 90 % of end value V_{SW7FB} = 1.8 V	100	180	300	µs
V_{SW7OSH}	Startup overshoot	−50	—	50	mV
η_{SW7}	Efficiency PFM mode, 3.3 V, 1.0 mA, T_J = 125 °C	—	85	—	%
η_{SW7}	Efficiency PFM mode, 3.3 V, 50 mA, T_J = 125 °C	—	88	—	%
η_{SW7}	Efficiency PFM mode, 3.3 V, 100 mA, T_J = 125 °C	—	90	—	%
η_{SW7}	Efficiency PWM mode, 3.3 V, 400 mA, T_J = 125 °C	—	91	—	%
η_{SW7}	Efficiency PWM mode, 3.3 V, 1000 mA, T_J = 125 °C	—	92	—	%
η_{SW7}	Efficiency PWM mode, 3.3 V, 2000 mA, T_J = 125 °C	—	90	—	%
F_{SWx}	PWM switching frequency range Frequency set by CLK_FREQ[3:0]	1.9	2.5	3.15	MHz
$T_{ONminSW7}$	Minimum on time	—	50	—	ns
T_{DBSW7}	Deadband time	—	3.0	—	ns
T_{slew}	Slewing time 10 % to 90 % V_{SW7IN} = 5.5 V	—	—	5.0	ns

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 60. Type 2 buck regulator electrical characteristics...*continued*

All parameters are specified at T_A = −40 to 105 °C, VIN = V_{SW7IN} = UVDET to 5.5 V, V_{SW7FB} = 1.8 V, I_{SW7} = 500 mA, typical external component values, f_{SW} = 2.25 MHz, unless otherwise noted. Typical values are characterized at VIN = V_{SW7IN} = 5.0 V, V_{SW7FB} = 1.8 V, I_{SW7} = 500 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
ΔV_{SW7}	Output ripple Output cap ESR ~ 10 mΩ, 2 × 22 µF	 −1.0	 —	 1.0	%
$V_{SW7LOTR}$	Transient load regulation (overshoot/undershoot) Transient load = 200 mA to 1.0 A step di/dt = 2.0 A/ms Cout = 20 µF effective V_{SW7FB} = 1.8 V	 −50	 —	 50	mV
I_{RCS}	DCM (skip mode) reverse current sense threshold	—	10	—	mA
I_{SW7Q}	Quiescent current PFM mode	 —	 18	 —	µA
I_{SW7Q}	Quiescent current Auto skip mode	 —	 150	 250	µA
$R_{ONSW7HS}$	SW7 high-side P-MOSFET $R_{DS(on)}$ [3]	—	—	135	mΩ
$R_{ONSW7LS}$	SW7 low-side N-MOSFET $R_{DS(on)}$ [3]	—	—	80	mΩ
R_{SW7DIS}	SW7 discharge resistance (normal operation)	—	100	200	Ω
R_{SW7TBB}	SW7 discharge resistance during TBB mode TBBEN = 1 and QPU_OFF state	 1.0	 2	 —	kΩ

[1] VSW7IN must be connected to VIN to ensure proper operation.
[2] The Type 2 buck regulator is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken to prevent reaching PMIC thermal shutdown during high ambient temperature conditions.
[3] Max $R_{DS(on)}$ does not include bondwire resistance. Consider +50 % tolerance to account for bondwire and pin losses.

Table 61. Recommended external components

Symbol	Parameter	Min	Typ	Max	Unit
L	Output inductor Maximum inductor DC resistance 50 mΩ [1] Minimum saturation current at full load: 3.0 A	0.47	1.0	1.5	µH
C_{out}	Output capacitor Use 2 x 22 µF, 6.3 V X7T ceramic capacitor to reduce output capacitance ESR	—	44	—	µF
C_{in}	Input capacitor 4.7 µF, 10 V X7R ceramic capacitor	—	4.7	—	µF

[1] Keep inductor DCR as low as possible to improve regulator efficiency.

15.6 Linear regulators

The PF8100/PF8200 has four low drop-out (LDO) regulators with the following features:

- 400 mA current capability
- Input voltage range from 2.5 V to 5.5 V
- Programmable output voltage between 1.5 V and 5.0 V
- Soft-start ramp control during power up (enable)
- Discharge mechanism during power down (disable)
- OTP programmable Load switch mode

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

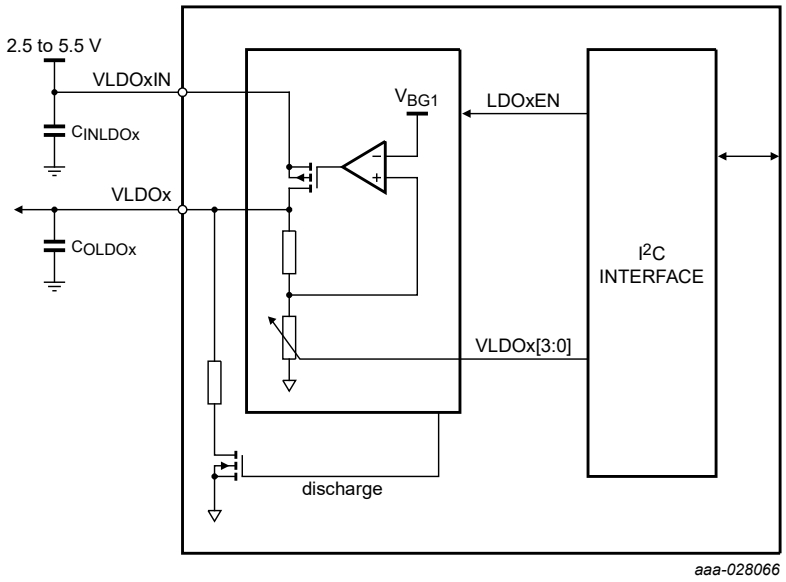


Figure 29. LDOx regulator block diagram

LDO1 and LDO2 share the same input supply; LDO12IN while LDO3 and LDO4 have their own dedicated input supply pin, LDO3IN and LDO4IN respectively.

The four LDOs are provided with one bit to enable or disable its output during the system-on states.

- When LDOx_RUN_EN = 0, the LDO is disabled during the run mode. If the regulator is part of the power up sequence, this bit is set during the power up sequence. Otherwise it is defaulted to 0.
- When LDOx_STBY_EN = 0, the LDO is disabled during the standby mode. If the regulator is part of the power up sequence, this bit is set during the power up sequence. Otherwise it is defaulted to 0.

The mode of operation of the LDOx is selected on OTP via the OTP_LDOxLS bit.

Table 62. LDO operation description

LDOx_RUN_EN / LDOx_STBY_EN	OTP_LDOxLS	LDO operation mode (Run or standby mode)
0	X	Disabled with output pull down active
1	0	Enabled in normal mode
1	1	Enabled in load switch configuration

The LDOs use four bits to set the output voltage.

- The VLDOx_RUN[3:0] sets the output voltage during the run mode.
- The VLDOx_STBY[3:0] sets the output voltage during standby mode.

The default output voltage configuration for the run and the standby mode is loaded from the OTP_VLDOx[3:0] registers on power up.

Table 63. LDO output voltage configuration

Set point	VLDOx_RUN[3:0] VLDOx_STBY[3 :0]	VLDOx output (V)
0	0000	1.5
1	0001	1.6
2	0010	1.8
3	0011	1.85
4	0100	2.15

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 63. LDO output voltage configuration*...continued*

Set point	VLDOx_RUN[3:0] VLDOx_STBY[3 :0]	VLDOx output (V)
5	0101	2.5
6	0110	2.8
7	0111	3.0
8	1000	3.1
9	1001	3.15
10	1010	3.2
11	1011	3.3
12	1100	3.35
13	1101	1.65
14	1110	1.7
15	1111	5.0

LDO2 can be controlled by hardware using the VSELECT and LDO2EN pins. When controlling the LDO2 by hardware, the output voltage can be selectable by the VSELECT pin as well as enable/disable by the LDO2EN pin.

15.6.1 LDO load switch operation

When the OTP_LDOxLS bit is set to 1, the corresponding LDO operates as a load switch, allowing a pass-through from the LDOxVIN to the corresponding LDOxVOUT output through a maximum 130 mΩ resistance. In this mode of operation, the input must be kept inside the LDO operating input voltage range (2.5 V to 5.5 V)

When the LDO regulator is set in Load switch mode, the LDOxEN bit is used to enable or disable the switch.

15.6.2 LDO regulator electrical characteristics

Table 64. LDO regulator electrical characteristics

All parameters are specified at T_A = −40 to 105 °C, V_{LDOxIN} = 2.5 V to 5.5 V, V_{LDOx} = 1.8 V, I_{LDOx} = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{LDOxIN} = 5.5 V, V_{LDOx} = 1.8 V, I_{LDOx} = 100 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units
V_{LDOxIN}	LDOx operating input voltage range 1.5 V ≤ V_{LDOx} < 2.25 V	2.5	—	5.5	V
V_{LDOxIN}	LDOx operating input voltage range 2.25 V < V_{LDOx} < 5.0 V	VLDOxNOM + 0.25	—	5.5	V
I_{LDOx}	Maximum load current	400	—	—	mA
$V_{LDOxTOL}$	Output voltage tolerance 1.5 V ≤ V_{LDOx} ≤ 5.0 V 0 mA < I_{LDOx} ≤ 400 mA	−3.0	—	3.0	%
$V_{LDOxLOR}$	Load regulation	—	0.1	0.20	mV/mA
$V_{LDOxLIR}$	Line regulation	—	—	20	mV/mA
$I_{LDOxLIM}$	Current limit I_{LDOx} when VLDOx is forced to $V_{LDOxNOM}$/2	450	850	1400	mA
I_{LDOxQ}	Quiescent current (measured at T_A = 25 °C)	—	7.0	10	µA
$R_{DS(on)}$	Drop-out/load switch on resistance V_{LDOINx} = 3.3 V (at T_J =125 °C)	—	—	150 [1]	mΩ
$PSRR_{VLDOx}$	DC PSRR I_{LDOx} = 150 mA VLDOx[3:0] = 0000 to 1111 V_{LDOINx} = $V_{LDOxINMIN}$	48	—	—	dB

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 64. LDO regulator electrical characteristics...*continued*

All parameters are specified at T_A = −40 to 105 °C, V_{LDOxIN} = 2.5 V to 5.5 V, V_{LDOx} = 1.8 V, I_{LDOx} = 100 mA, typical external component values, unless otherwise noted. Typical values are characterized at V_{LDOxIN} = 5.5 V, V_{LDOx} = 1.8 V, I_{LDOx} = 100 mA, and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units
TR_{VLDOx}	Turn on rise time (soft-start ramp) 10 % to 90 % of end value V_{LDOx} = 3.3 V I_{LDOx} = 0.0 mA	—	220	360	µs
t_{ONLDOx}	Turn on time Enable to 90 % of end value V_{LDOx} = 5.0 V I_{LDOx} = 0.0 mA	—	—	400	µs
$t_{OFFLDOx}$	Turn off time Disable to 10 % of initial value V_{LDOx} = 5.0 V I_{LDOx} = 0.0 mA	—	—	3500	µs
$V_{LDOxOSHT}$	Startup overshoot V_{LDOINx} = $V_{LDOINxMIN}$ V_{LDOx} = 5.0 V I_{LDOx} = 0.0 mA	—	1.0	2.0	%
$V_{LDOxLOTR}$	Transient load response I_{LDOx} = 10 mA to 200 mA in 2.0 µs Peak of overshoot or undershoot of LDOx with respect to final value	−6.0	—	6.0	%
$T_{onLDOxLS}$	Load switch mode turn on rise time	—	150	300	µs
$R_{dischLDOx}$	Output discharge resistance when LDO is disabled LDO and Switch mode	50	100	300	Ω
I_{LSxLIM}	Load switch mode current limit when enabled LSxILIM_EN = 1	450	850	1400	mA
$R_{LDOxTBB}$	LDOx pull down resistance during TBB mode TBBEN = 1 & in QPU_OFF state	1.0	2.0	—	kΩ

[1] Max $R_{DS(on)}$ does not include bondwire resistance. Consider 40 % tolerance to account for bondwire and pin loses.

15.7 Voltage monitoring

The PF8100/PF8200 provides OV and UV monitoring capability for the following voltage regulators:

- SW1 to SW7
- LDO1 to LDO4

A programmable UV threshold is selected via the OTP_SWxUV_TH[1:0] and OTP_LDOxUV_TH[1:0] bits. UV threshold selection represents a percentage of the nominal voltage programmed on each regulator.

Table 65. UV threshold configuration register

OTP_SWxUV_TH[1:0] OTP_LDOxUV_TH[1:0]	UV threshold level
00	95 %
01	93 %
10	91 %
11	89 %

A programmable OV threshold is selected via the OTP_SWxOV_TH[1:0] and OTP_LDOxOV_TH[1:0] bits. OV threshold selection represents a percentage of the nominal voltage programmed on each regulator.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 66. OV threshold configuration register

OTP_SWxOV_TH OTP_LDOxOV_TH	OV threshold level
00	105 %
01	107 %
10	109 %
11	111 %

Two functional bits are provided to program the UV debounce time for all the voltage regulators.

Table 67. UV debounce timer configuration

UV_DB[1:0]	UV debounce time
00	5 µs
01	15 µs
10	25 µs
11	40 µs

The default value of the UV_DB[1:0] upon a full register reset is 0b10

Two functional bits to program the OV debounce time for all the voltage regulators.

Table 68. OV debounce timer configuration

OV_DB[1:0]	OV debounce time
00	25 µs
01	50 µs
10	80 µs
11	125 µs

The default value of the OV_DB[1:0] upon a full register reset is 0b00

The VMON_EN bits enable or disable the OV/UV monitor for each one of the external regulators (SWxVMON_EN, LDOxVMON_EN).

- When the VMON_EN bit of a specific regulator is 1, the voltage monitor for that specific regulator is enabled.
- When the VMON_EN bit of a specific regulator is 0, the voltage monitor for that specific regulator is disabled.

By default, the VMON_EN bits are set to 1 on power up.

When the I2C_SECURE_EN = 1, a secure write must be performed to set or clear the VMON_EN bits to enable or disable the voltage monitoring for a specific regulator.

On enabling a regulator, the UV/OV monitor is masked until the corresponding regulator reaches the point of regulation. If a voltage monitor is disabled, the UV_S and OV_S indicators from that monitor are reset to 0.

Figure 30 shows the PF8100/PF8200 voltage monitoring architecture.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

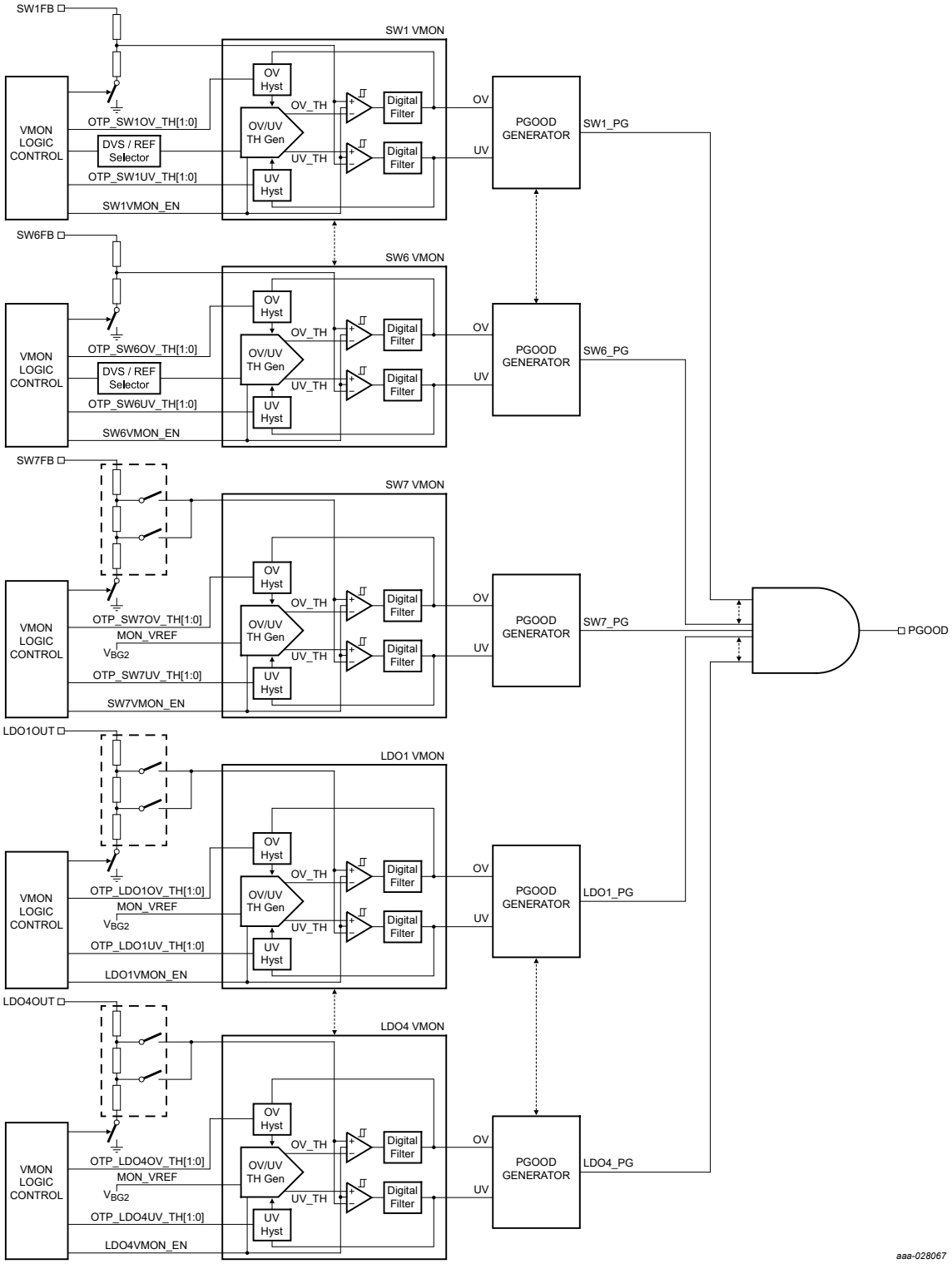


Figure 30. Voltage monitoring architecture

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15.7.1 Electrical characteristics

Table 69. VMON Electrical characteristics

All parameters are specified at T_A = –40 °C to 105 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V, V_{xFB} = 1.5 V (Type 1 Buck Regulator), 3.3 V (Type 2 Buck regulator, LDO Regulator), and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{QON}	Block quiescent current, when block is enabled One block per regulator	— 	10	13	µA
I_{OFF}	Block leakage current when disabled	—	—	500	nA
t_{ON_MON}	Voltage monitor settling time after enabled	—	—	30	µs
$V_{xFBUVHysteresis}$	Power good (UV) hysteresis Voltage difference between UV rising and falling thresholds	0.5	—	1.0	%
V_{UV_Tol}	Undervoltage falling threshold accuracy With respect to target feedback voltage tolerance For type 2 switching regulator and LDO regulator For type 1 switching regulator when V_{SWxFB} > 0.75 V	−2	—	2	%
V_{UV_Tol}	Under voltage falling threshold accuracy With respect to target feedback voltage For type 1 switching regulator when VSWxFB ≤ 0.75 V	−3	—	3	%
t_{UV_DB}	Power good (UV) debounce time UV_DV = 00	2.5	5.0	7.5	µs
	Power good (UV) debounce time UV_DV = 01	10	15	20	µs
	Power good (UV) debounce time UV_DV = 10	20	30	40	µs
	Power good (UV) debounce time UV_DV = 11	25	40	55	µs
V_{OV_Tol}	Overvoltage rising threshold accuracy With respect to target feedback voltage tolerance For type 2 switching regulator and LDO regulators For type 1 switching regulator when V_{SWxFB} > 0.75 V	−2	—	2	%
V_{OV_Tol}	Overvoltage rising threshold With respect to target feedback voltage tolerance For type 1 switching regulator when V_{SWxFB} ≤ 0.75 V	−3	—	3	%
$V_{xFBOVHysteresis}$	Overvoltage (OV) hysteresis Voltage difference between OV rising and falling thresholds	0.5	—	1.0	%
t_{OV_DB}	Power good (OV) debounce time OV_DV = 00	20	30	40	µs
	Power good (OV) debounce time OV_DV = 01	35	50	65	µs
	Power good (OV) debounce time OV_DV = 10	55	80	105	µs
	Power good (OV) debounce time OV_DV = 11	90	135	160	µs

15.8 Clock management

The clock management provides a top-level management control scheme of internal clock and external synchronization intended to be primarily used for the switching regulators. The clock management incorporates various sub-blocks:

- Low power 100 kHz clock
- Internal high frequency clock with programmable frequency
- Phase Locked Loop (PLL)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

A digital clock management interface is in charge of supporting interaction among these blocks.

The clock management provides clocking signals for the internal state machine, the switching frequencies for the seven buck converters as well as the multiples of those switching frequencies in order to enable phase shifting for multiple phase operation.

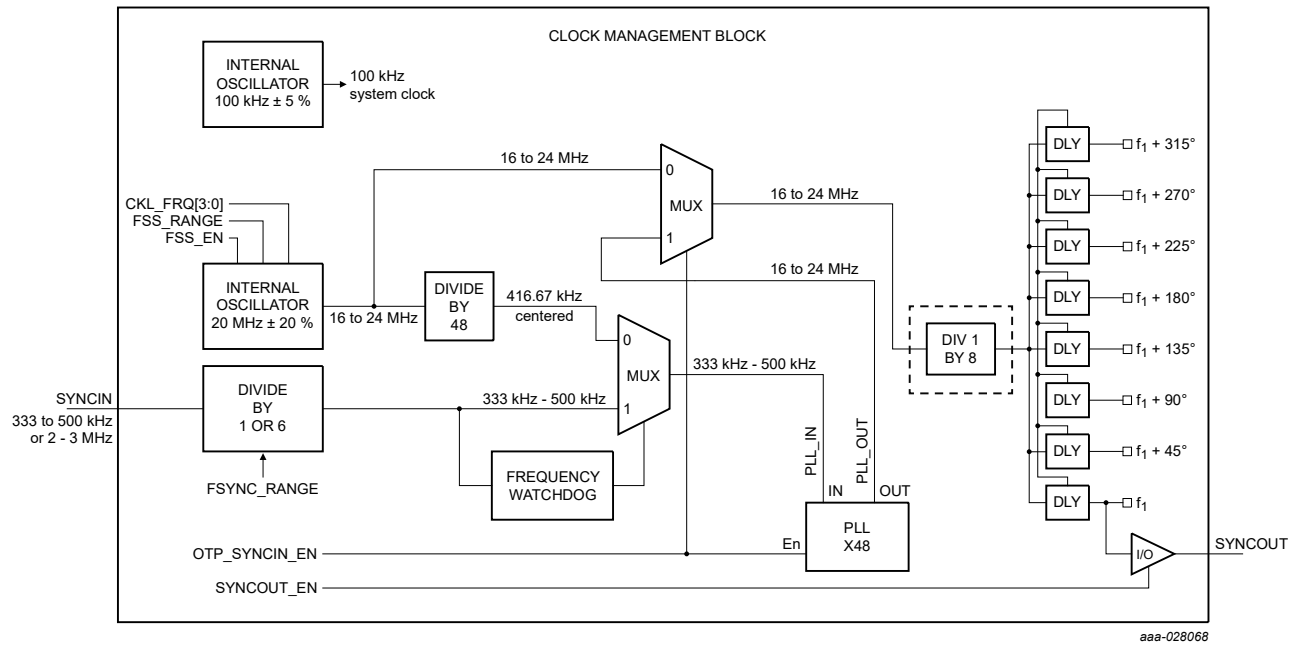


Figure 31. Clock management architecture

15.8.1 Low frequency clock

A low power 100 kHz clock is provided for overall logic and digital control. Internal logic and debounce timers are based on this 100 kHz clock.

15.8.2 High frequency clock

The PF8100/PF8200 features a high frequency clock with nominal frequency of 20 MHz. Clock frequency is programmable over a range of ±20 % via the CLK_FREQ[3:0] control bits.

15.8.3 Manual frequency tuning

The PF8100/PF8200 features a manual frequency tuning to set the switching frequency of the high frequency clock. The CLK_FREQ [3:0] bits allow a manual frequency tuning of the high frequency clock from 16 MHz to 24 MHz.

If a frequency change of two or more steps is requested by a single I^2C command, the device performs a gradual frequency change passing through all steps in between with a 5.2 µs time between each frequency step. When the frequency reaches the programmed value, the FREQ_RDY_I asserts the INTB pin, provided it is not masked.

When the internal clock is used as the main frequency for the power generation, an internal frequency divider by 8 is used to generate the switching frequency for all the buck regulators. Adjusting the frequency of the high frequency clock allows for manual tuning of the switching frequencies for the buck regulators from 2.0 MHz to 3.0 MHz.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 70. Manual frequency tuning configuration

CLK_FREQ[3:0]	High speed clock frequency (MHz)	Switching regulators frequency (MHz)
0000	20	2.500
0001	21	2.625
0010	22	2.750
0011	23	2.875
0100	24	3.000
0101	Not used	Not used
0110	Not used	Not used
0111	Not used	Not used
1000	Not used	Not used
1001	16	2.000
1010	17	2.125
1011	18	2.250
1100	19	2.375
1101	Not used	Not used
1110	Not used	Not used
1111	Not used	Not used

The default switching frequency is set by the OTP_CLK_FREQ[3:0] bits.

Manual tuning cannot be applied when frequency spread-spectrum or external clock synchronization is used. However, during external clock synchronization, it is recommended to program the CLK_FREQ[3:0] bits to match the external frequency as close as possible.

15.8.4 Spread-spectrum

The internal clock provides a programmable frequency spread spectrum with two ranges for narrow spread and wide spread to help manage EMC in the automotive applications.

- When the FSS_EN = 1, the frequency spread-spectrum is enabled.
- When the FSS_EN = 0, the frequency spread-spectrum is disabled.

The default state of the FSS_EN bit upon a power up can be configured via the OTP_FSS_EN bit.

The FSS_RANGE bit is provided to select the clock frequency range.

- When FSS_RANGE = 0, the maximum clock frequency range is ±5 %.
- When FSS_RANGE = 1, the maximum clock frequency range is ±10 %.

The default value of the FSS_RANGE bit upon a power up can be configured via the OTP_FSS_RANGE bit.

The frequency spread-spectrum is performed at a 24 kHz modulation frequency when the internal high frequency clock is used to generate the switching frequency for the switching regulators. When the external clock synchronization is enabled, the spread-spectrum is disabled.

Figure 32 shows implementation of spread-spectrum for the two settings.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

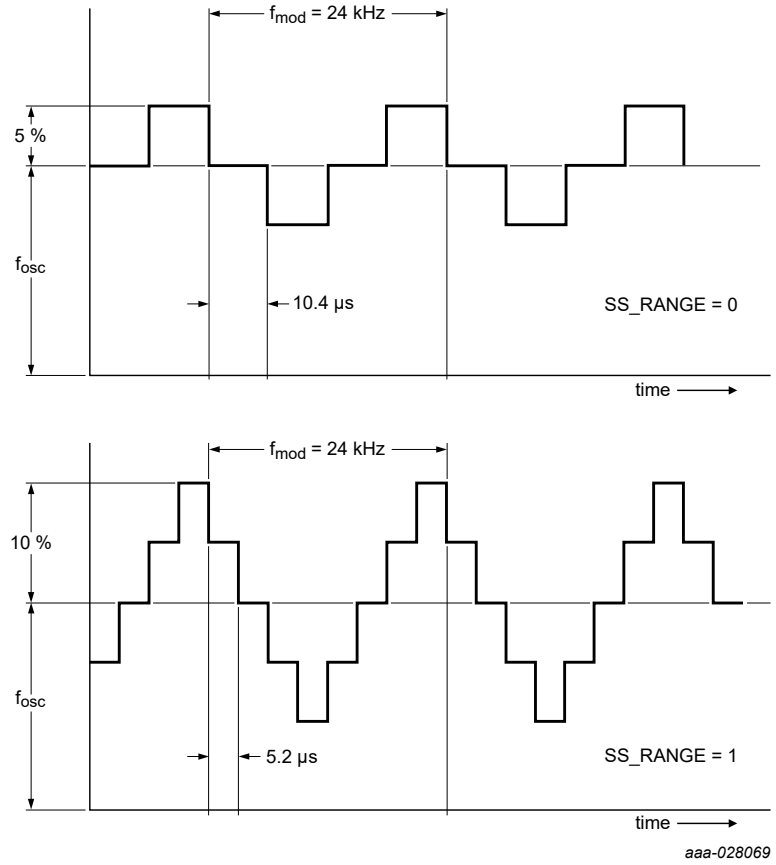


Figure 32. Spread-spectrum waveforms

If the frequency spread-spectrum is enabled, the switching regulators should be set in PWM mode to ensure clock synchronization at all time.

If the external clock synchronization is enabled, (SYNCIN_EN = 1), the spread spectrum is disabled regardless of the value of the FSS_EN bit.

15.8.5 Clock Synchronization

An external clock can be fed via the SYNCIN pin to synchronize the switching regulators to this external clock.

When the OTP_SYNCIN_EN = 0, the external clock synchronization is disabled. In this case, the PLL is disabled, and the device always uses the internal high frequency clock to generate the main frequency for the switching regulators.

When the OTP_SYNCIN_EN = 1, the external clock synchronization is enabled. In this case, the internal PLL is always enabled and it uses either the internal high frequency clock or the SYNCIN pin as it source to generate the main frequency for the switching regulators.

If the SYNCIN function is not used, the pin should be grounded. If the external clock is meant to start up after the PMIC has started, the SYNCIN pin must be maintained low until the external clock is applied.

The SYNCIN pin is prepared to detect clock signals with a 1.8 V or 3.3 V amplitude and within the frequency range set by the FSYNC_RANGE bit.

- When the FSYNC_RANGE = 0, the input frequency range at SYNCIN pin should be between 2000 kHz and 3000 kHz.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

- When the FSYNC_RANGE = 1, the input frequency range at SYNCIN pin should be between 333 kHz and 500 kHz.

The OTP_FSYNC_RANGE bit is used to select the default frequency range accepted in the SYNCIN pin.

The external clock duty cycle at the SYNCIN pin should be between 40 % and 60 %. An input frequency in the SYNCIN pin outside the range defined by the FSYNC_RANGE bit is detected as invalid. If the external clock is not present or invalid, the device automatically switches to the internal clock and sets the FSYNC_FLT_I interrupt, which in turn asserts the INTB pin provided it is not masked.

The FSYNC_FLT_S bit is set to 1 as long as the input frequency is not preset or invalid, and it is cleared to 0 when the SYNCIN has a valid input frequency.

The device switches back to the external switching frequency only when both, the FSYNC_FLT_I interrupt has been cleared and the SYNCIN pin sees a valid frequency.

When the external clock is selected, the switching regulators should be set in PWM mode to ensure clock synchronization at all time.

Upon an external clock failure, the MCU must proof the integrity of the external clock by implementing a three-step diagnostic strategy.

1. MCU acknowledges and finds the source of the interrupt event.
2. After deciding the interrupt is generated by the FSYNC_FLT_I event, the MCU reads the FSYNC_FLT_S bit to verify if the fault condition is persistent or not.
3. a. If FSYNC_FLT_S bit is 0, the fault condition can be considered a transient condition and the system is ready to switch over to the external clock by clearing the FSYNC_FLT_I flag.
   b. If the FSYNC_FLT_S bit is 1, the fault is considered a persistent fault and the MCU must take corrective action to send the system to safe operation.

The system designer is responsible to define the tolerance time to allow the external frequency to be lost before taking a corrective action such as stopping the system or placing the system in safe state in safety related applications.

The SYNCOUT pin is used to synchronize an external device to the PF8100/PF8200.

The SYNCOUT pin outputs the main frequency used for the switching regulators in the range of 2.0 MHz to 3.0 MHz. The SYNCOUT_EN bit can be used to enable or disable the SYNCOUT feature via I^2C during the system-on states.

- When SYNCOUT_EN = 0, the SYNCOUT feature is disabled and the pin is internally pulled to ground.
- When SYNCOUT_EN = 1, the SYNCOUT pin toggles at the base frequency used by the switching regulators.

The SYNCOUT function can be enabled or disabled by default by using the OTP_SYNCOUT_EN bit.

Table 71. Clock management specifications

All parameters are specified at T_A = −40 to 105 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Low frequency clock					
$I_{Q100KHz}$	100 kHz clock quiescent current	—	—	3.0	µA
$f_{100KHzACC}$	100 kHz clock accuracy	−5.0	—	5.0	%
High frequency clock					
f_{20MHz}	High frequency clock nominal frequency via CLK_FREQ[3:0] = 0000	—	20	—	MHz
$f_{20MzACC}$	High frequency clock accuracy	−6.0	—	6.0	%

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 71. Clock management specifications...*continued*

All parameters are specified at T_A = −40 to 105 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{20MHzStep}$	Clock step transition time Minimum time to transition from one frequency step to the next in manual tuning mode	—	5.2	—	µs
FSS_{RANGE}	Spread-spectrum range FSS_RANGE= 0 via CLK_FREQ[3:0] Spread-spectrum is done around center frequency of 20 MHz	—	±5.0	—	%
FSS_{RANGE}	Spread-spectrum range FSS_RANGE= 1 via CLK_FREQ[3:0] Spread-spectrum is done around center frequency of 20 MHz	—	±10	—	%
FSS_{mod}	Spread spectrum frequency modulation	—	24	—	kHz
Clock synchronization					
f_{SYNCIN}	SYNCIN input frequency range FSYNC_RANGE = 0	2000	—	3000	kHz
f_{SYNCIN}	SYNCIN input frequency range FSYNC_RANGE = 1	333	—	500	kHz
$f_{SYNCOUT}$	SYNCOUT output frequency range via CLK_FREQ[3:0]	2000	—	3000	kHz
$V_{SYNCINLO}$	Input frequency low voltage threshold	—	—	0.3*VDDIO	V
$V_{SYNCINHI}$	Input frequency high voltage threshold	0.7*VDDIO	—	—	V
R_{PD_SYNCIN}	SYNCIN internal pull down resistance	0.475	1.0	__	MΩ
$V_{SYNCOUTLO}$	Output frequency low voltage threshold	0	—	0.4	V
$V_{SYNCOUTHI}$	Output frequency high voltage threshold	VDDIO − 0.5	—	—	V

15.9 Thermal monitors

The PF8100/PF8200 features ten temperature sensors spread around the die. These sensors are located at the following locations:

1. Center of die	6. Vicinity of SW5
2. Vicinity of SW1	7. Vicinity of SW6
3. Vicinity of SW2	8. Vicinity of SW7
4. Vicinity of SW3	9. Vicinity of LDO1-2
5. Vicinity of SW4	10. Vicinity of LDO3-4

The temperature sensor at the center of the die is used to generate the thermal interrupts and thermal shutdown.

The output of all temperature sensors are internally connected to the Analog MUX, allowing the user to read the raw voltage equivalent to the temperature on each sensor. The processor can read outputs of the other temperature sensors and take appropriate action (such as reduce loading, or turning off regulator) if the temperature exceeds desired limits at any point in the die.

Figure 33 shows a high level block diagram of the thermal monitoring architecture in PF8100/PF8200.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

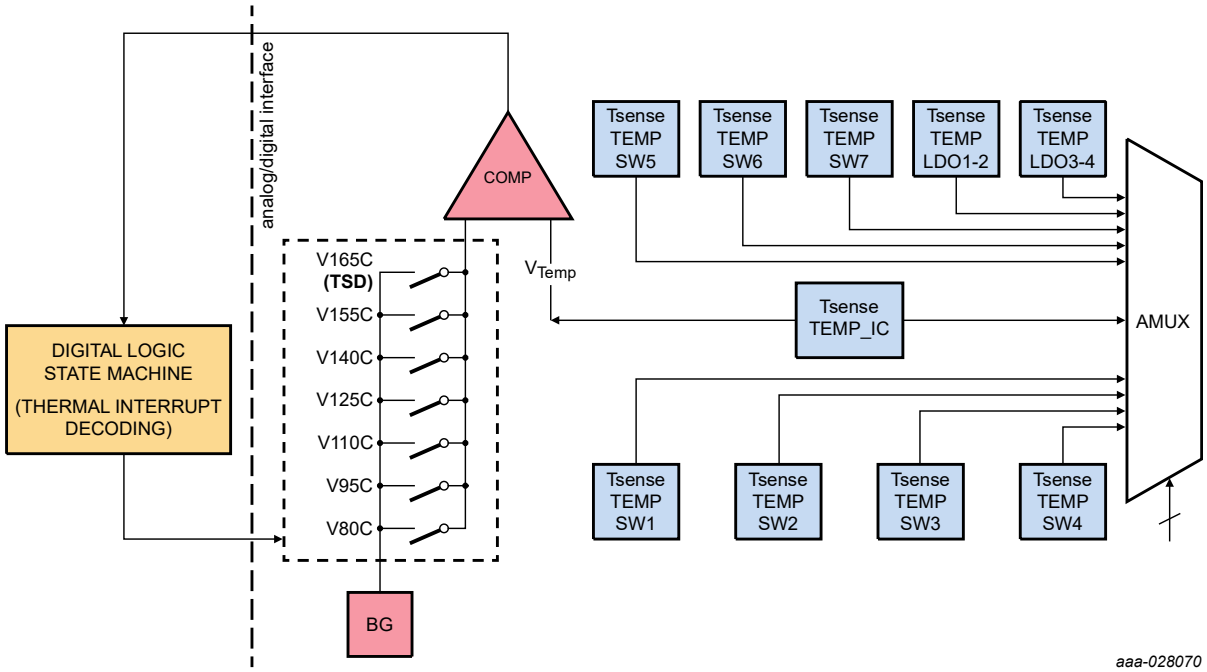


Figure 33. Thermal monitoring architecture

Table 72. Thermal monitor specifications

Symbol	Parameter [1]	Min	Typ	Max	Unit
V_{IN}	Operating voltage range of thermal circuit	UVDET	—	5.5	V
TCOF	Thermal sensor coefficient	—	–3.5	—	mV/ºC
V_{TSROOM}	Thermal sensor voltage 24 ºC	—	1.414	—	V
T_{SEN_RANGE}	Thermal sensor temperature range	–40	—	175	ºC
V_{TEMP_MAX}	Thermal sensor output voltage range	0	—	1.8	V
T_{80C}	80 ºC temperature threshold	70	80	90	ºC
T_{95C}	95 ºC temperature threshold	85	95	105	ºC
T_{110C}	110 ºC temperature threshold	100	110	120	ºC
T_{125C}	125 ºC temperature threshold	115	125	135	ºC
T_{140C}	140 ºC temperature threshold	130	140	150	ºC
$T1_{55C}$	155 ºC temperature threshold	145	155	165	ºC
T_{SD}	Thermal shutdown threshold	155	165	175	ºC
T_{WARN_HYS}	Thermal threshold hysteresis	—	5.0	—	ºC
T_{SD_HYS}	Thermal shutdown hysteresis	—	10	—	ºC
t_temp_db	Debounce timer for temperature thresholds (bidirectional)	—	10	—	µs
$t_{Sinterval}$	Sampling interval time When TMP_MON_AON = 1	—	3.0	—	ms
$t_{Swindow}$	Sampling window When TMP_MON_AON = 1	—	450	—	µs

[1] Sensor temperature is calculated with the following formula: T [°C] = (V_{TSENSE} – 1.498 V) / TCOF, where V_{TSENSE} is the thermal sensor voltage measured on the corresponding AMUX channel.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

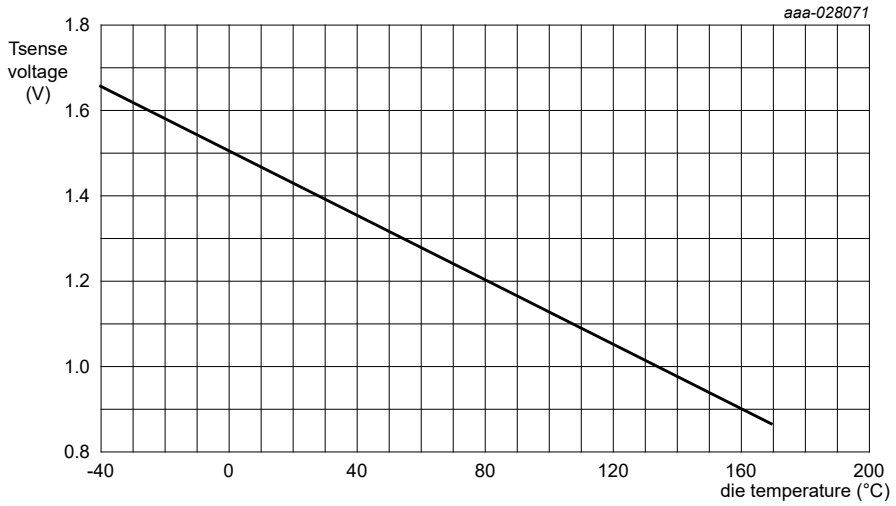


Figure 34. Thermal sensor voltage characteristics

As the temperature crosses the thermal thresholds, the corresponding interrupts are set to notify the system. The processor may take appropriate action to bring down the temperature (either by turning off external regulators, reducing load, or turning on a fan).

A 5 ºC hysteresis is implemented on a falling temperature in order to release the corresponding THERM_x_S signal. When the shutdown threshold is crossed, the PF8100/PF8200 initiates a thermal shutdown and it prevents from turning back on until the 15 ºC thermal shutdown hysteresis is crossed as the device cools down.

The temperature monitor can be enabled or disabled via I^2C with the TMP_MON_EN bit.

- When TMP_MON_EN = 0, the temperature monitor circuit is disabled.
- When TMP_MON_EN = 1, the temperature monitor circuit is enabled.

In the run state, the temperature sensor can operate in always on or sampling modes.

- When the TMP_MON_AON = 1, the device is always on during the run mode.
- When the TMP_MON_AON = 0, the device operates in sampling mode to reduce current consumption in the system. In sampling mode, the thermal monitor is turned on during 450 µs at a 3.0 ms sampling interval.

In the standby mode, the thermal monitor operates only in sampling mode as long as the TMP_MON_EN = 1

Table 73. Thermal monitor bit description

Bit(s)	Description
THERM_80_I, THERM_80_S, THERM_80_M	Interrupt, sense and mask bits for 80 ºC threshold
THERM_95_I, THERM_95_S, THERM_95_M	Interrupt, sense and mask bits for 95 ºC threshold
THERM_110_I, THERM_110_S, THERM_110_M	Interrupt, sense and mask bits for 110 ºC threshold
THERM_125_I, THERM_125_S, THERM_125_M	Interrupt, sense and mask bits for 125 ºC threshold
THERM_140_I, THERM_140_S, THERM_140_M	Interrupt, sense and mask bits for 140 ºC threshold
THERM_155_I, THERM_155_S, THERM_155_M	Interrupt, sense and mask bits for 155 ºC threshold
TMP_MON_EN	Disables temperature monitoring circuits when cleared
TMP_MON_AON	When set, the temperature monitoring circuit is always ON. When cleared, the temperature monitor operates in sampling mode.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15.10 Analog multiplexer

A 24 channel Analog Multiplexer (AMUX) is provided to allow access to various internal voltages within the PMIC. The selected voltage is buffered and made available on the AMUX output pin during the system-on states.

When the AMUX_EN bit is 0, the AMUX block is disabled and the output remains pulled down to ground.

When the AMUX_EN bit is 1, the AMUX block is enabled and the system may select the channel to be read by using the AMUX_SEL[4:0] bits.

Table 74. AMUX channel selection

AMUX_EN	AMUX_SEL[4:0]	AMUX selection	Internal signal dividing ratio
0	X XXXX	AMUX disabled and pin pulled-down to ground	N/A
1	0 0000	AMUX disabled in high impedance mode	N/A
1	0 0001	VIN	4
1	0 0010	VSNVS	3.5
1	0 0011	LICELL	3
1	0 0100	SW1_FB	1.25 (1.8 V setting) 1 (all other settings)
1	0 0101	SW2_FB	1.25 (1.8 V setting) 1 (All other settings)
1	0 0110	SW3_FB	1.25 (1.8 V setting) 1 (all other settings)
1	0 0111	SW4_FB	1.25 (1.8 V setting) 1 (all other settings)
1	0 1000	SW5_FB	1.25 (1.8 V setting) 1 (all other settings)
1	0 1001	SW6_FB	1.25 (1.8 V setting) 1 (all other settings)
1	0 1010	SW7_FB	10/3.5 = 2.86
1	0 1011	LDO1	10/3 = 3.33
1	0 1100	LDO2	10/3 = 3.33
1	0 1101	LDO3	10/3 = 3.33
1	0 1110	LDO4	10/3 = 3.33
1	0 1111	TEMP_IC	1
1	1 0000	TEMP_SW1	1
1	1 0001	TEMP_SW2	1
1	1 0010	TEMP_SW3	1
1	1 0011	TEMP_SW4	1
1	1 0100	TEMP_SW5	1
1	1 0101	TEMP_SW6	1
1	1 0110	TEMP_SW7	1
1	1 0111	TEMP_LDO1_2	1
1	1 1000	TEMP_LDO3_4	1
1	1 1001 to 1 1111	Reserved	N/A

All selectable input signals are conditioned internally to fall within an operating output range from 0.3 V to 1.65 V, However, the AMUX pin is clamped to a maximum 2.5 V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 75. AMUX specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Operational voltage	UVDET	—	5.5	V
I_{REF}	Current reference range	0.95	1.0	1.05	µA
V_{OFFSET}	AMUX output voltage offset (input to output)	–6.25	—	6.25	mV
I_{QAMUX}	AMUX quiescent current	—	110	—	µA
t_{AMUX_ON}	AMUX settling time (off to channel transition) Max step size of 1.8 V; output cap 150 pF	—	—	50	µs
t_{AMUX_CHG}	AMUX settling time (channel to channel transition) Max step size of 1.8 V; output cap 150 pF	—	—	50	µs
V_{CLAMP}	AMUX clamping voltage	1.8	2.5	3.1	V
RA_{DIV_CH1}	Channel 1 Internal divider ratio Input source = VIN	3.97	4.0	4.05	—
RA_{DIV_CH2}	Channel 2 internal divider ratio Input source = VSNVS	3.48	3.5	3.54	—
RA_{DIV_CH3}	Channel 3 internal divider ratio Input source = LICELL	2.98	3.0	3.04	—
$RA_{DIV_CH4_9}$	Channel 4 to 9 internal divider ratio Input source = Type 1 regulators at 1.8 V configuration	1.241	1.25	1.267	—
RA_{DIV_CH10}	Channel 10 internal divider ratio Input source = Type 2 regulator	2.85	2.86	2.91	—
$RA_{DIV_CH10_14}$	Channel 11 to 14 internal divider ratio Input source = LDO regulators	3.32	3.35	3.39	—

15.11 Watchdog event management

A watchdog event may be started in two ways:

- The WDI pin toggles low due to a watchdog failure on the MCU
- The internal watchdog expiration counter reach the maximum value the WD timer is allowed to expire

A watchdog event initiated by the WDI pin may perform a hard WD reset or a soft WD reset as defined by the WDI_MODE bit. A watchdog event initiated by the internal watchdog always performs a hard WD reset.

15.11.1 Internal watchdog timer

The internal WD timer counts up and it expires when it reaches the value in the WD_DURATION[3:0] register. When the WD timer starts counting, the WD_CLEAR flag is set to 1. Clearing the WD_CLEAR flag within the valid window is interpreted as a successful watchdog refresh and the WD timer gets reset. The MCU must write a 1 to clear the WD_CLEAR flag.

The WD timer is reset when device goes into any of the off modes and does not start counting until RESETBMCU is deasserted in the next power up sequence.

The OTP_WD_DURATION[3:0] selects the initial configuration for the watchdog window duration between 1.0 ms and 32768 ms (typical values).

The watchdog window duration can change during the system-on states by modifying the WD_DURATION[3:0] bits on the functional register map. If the WD_DURATION[3:0] bits get changed during the system-on states, the WD timer is reset.

Table 76. Watchdog duration register

WD_DURATION[3:0]	Watchdog timer duration (ms)
0000	1
0001	2

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 76. Watchdog duration register*...continued*

WD_DURATION[3:0]	Watchdog timer duration (ms)
0010	4
0011	8
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

The WD_EXPIRE_CNT[2:0] counter is used to ensure no cyclic watchdog condition occurs. When the WD_CLEAR flag is cleared successfully before the WD timer expires, the WD_EXPIRE_CNT[2:0] is decreased by 1. Every time the WD timer is not successfully refreshed, it gets reset and starts a new count and the WD_EXPIRE_CNT[2:0] is increased by 2.

If WD_EXPIRE_CNT[2:0] = WD_MAX_EXPIRE[2:0], a WD event is initiated. The default maximum amount of time the watchdog can expire before starting a WD Reset, is set by the OTP_WD_MAX_EXPIRE[2:0]. Writing a value less than or equal to 0x02 on the OTP_WD_MAX_EXPIRE causes the watchdog event to be initiated, as soon as the WD Timer expires for the first time.

The OTP_WDWINDOW bit selects whether the watchdog is singled ended or window mode.

- When OTP_WDWINDOW = 0, the WD_CLEAR flag can be cleared within 100 % of the watchdog timer.
- When OTP_WDWINDOW = 1, the WD_CLEAR flag can only be cleared within the second half of the programmed watchdog timer. Clearing the WD_CLEAR flag within the first half of the watchdog window is interpreted as a failure to refresh the watchdog.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

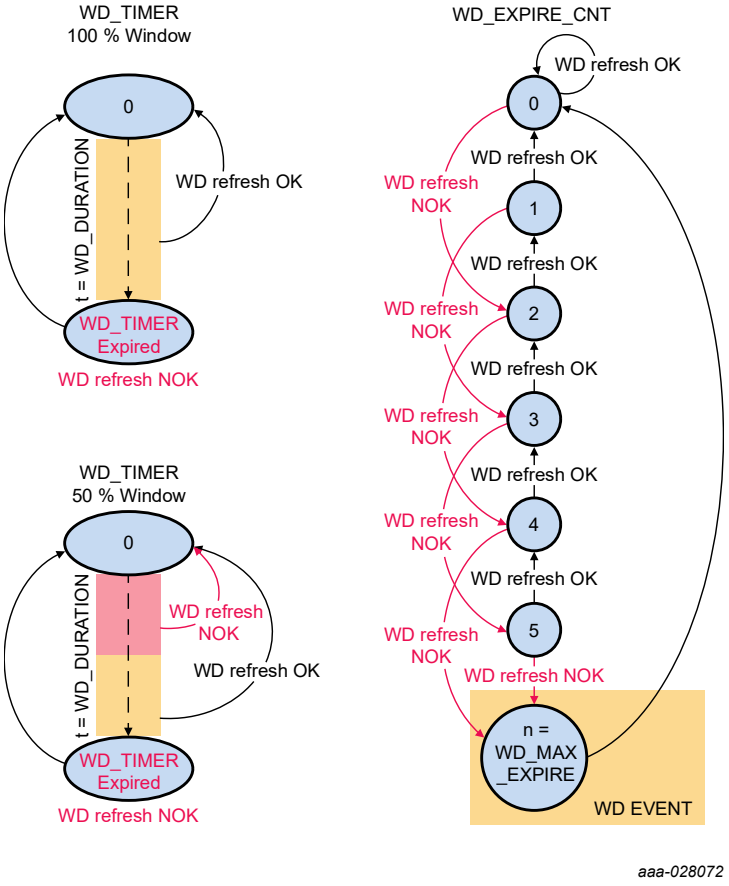


Figure 35. Watchdog timer operation

The watchdog function can be enabled or disabled by writing the WD_EN bit on the I^2C register map. When the I2C_SECURE_EN = 1, a secure write must be performed to change the WD_EN bit.

- When WD_EN = 0 the internal watchdog timer operation is disabled.
- When WD_EN = 1 the internal watchdog timer operation is enabled.

The OTP_WD_EN bit is used to select the default status of the watchdog counter upon power up.

The watchdog function can be programmed to be enabled or disabled during the standby state by writing the WD_STBY_EN bit on the I^2C register map. When the I2C_SECURE_EN = 1, a secure write must be performed to modify the WD_STBY_EN bit.

- When WD_STBY_EN = 0 the internal watchdog timer operation during standby is disabled.
- When WD_STBY_EN = 1 the internal watchdog timer operation during standby is enabled.

The OTP_WD_STBY_EN bit selects whether the watchdog is active in standby mode by default or not.

15.11.2 Watchdog reset behaviors

When a watchdog event is started, a watchdog (WD) reset is performed. There are two types of watchdog reset:

- Soft WD reset
- Hard WD reset

A soft WD reset is used as a safe way for the MCU to force the PMIC to return to a known default configuration without forcing a POR Reset on the MCU. During a soft WH reset, the RESETBMCU remains deasserted all the time.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Upon a soft WD reset, a partial OTP register re-load is performed on the registers as shown in Table 77.

Table 77. Soft WD register reset

Bit name	Register	Bits
Configuration registers		
STANDBYINV	CTRL2	2
RUN_PG_GPO	CTRL2	1
STBY_PG_GPO	CRTL2	0
RESETBMCU_SEQ[7:0]	RESETBMCU PWRUP	7:0
PGOOD_SEQ[7:0]	PGOOD PWRUP	7:0
WD_EN	CTRL1	3
WD_DURATION[3:0]	WD CONFIG	3:0
WD_STBY_EN	CTRL1	2
WDI_STBY_ACTIVE	CTRL1	1
SW registers		
SWx_WDBYPASS	SWx CONFIG1	1
SWx_PG_EN	SWx CONFIG1	0
SWxDVS_RAMP	SWx CONFIG2	5
SWxILIM[1:0]	SWx CONFIG2	4:3
SWxPHASE[2:0]	SWx CONFIG2	2:0
SWx_SEQ[7:0]	SWx PWRUP	7:0
SWx_PDGRP[1:0]	SWx MODE	5:4
SWx_STBY_MODE [1:0]	SWx MODE	3:2
SWx RUN_MODE [1:0]	SWx MODE	1:0
VSWx_RUN [7:0]	SWx RUN VOLT	7:0
VSWx_STBY [7:0]	SWx STBY VOLT	7:0
VSW7 [4:0]	SW7 VOLT	4:0
SW6_VTTEN	SW6_CONFIG2	6
LDO registers		
LDOx_WDBYPASS	LDOx CONFIG1	1
LDOx_PG_EN	LDOx CONFIG1	0
LDOx_PDGRP[1:0]	LDOx CONFIG2	6:5
LDO2HW_EN	LDO2 CONFIG2	4
VSELECT_EN	LDO2 CONFIG2	3
LDOxLS	LDOx CONFIG2	2
LDOx_RUN_EN	LDOx CONFIG2	1
LDOx_STBY_EN	LDOx CONFIG2	0
LDOx_SEQ [7:0]	LDOx PWRUP	7:0
VLDOx_RUN[3:0]	LDOx RUN VOLT	3:0
VLDOx_STBY[3:0]	LDOx STBY VOLT	3:0

A soft WD reset may require all or some regulators to be reset to their default OTP configuration. In the event a regulator is required to keep its current configuration during a soft WD reset, a watchdog bypass bit is provided for each regulator (SWx_WDBYPASS / LDOx_WDBYPASS).

- When the WDBYPASS = 0, the watchdog bypass is disabled and the output of the corresponding regulator is returned to its default OTP value during the soft WD reset.
- When the WDBYPASS = 1, the watchdog bypass is enabled and the output of the corresponding regulator is not affected by the soft WD reset, keeping its current configuration.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

During a soft WD reset, only regulators that are activated in the power up sequence go back to their default voltage configuration if their corresponding WDBYPASS = 0.

Switching regulators returning to their default voltages configuration, will gradually reach the new output voltage using its DVS configuration. LDO regulators returning to their default configuration, will change to the default output voltage configuration instantaneously. Regulators with WDBYPASS = 0 and which are not activated during the power up sequence will turn off immediately.

After all output voltages, have transitioned to their corresponding default values, the device waits for at least 30 µs before returning to the run state and announces it has finalized the soft WD reset by asserting the INTB pin, provided the WDI_I interrupt is not masked.

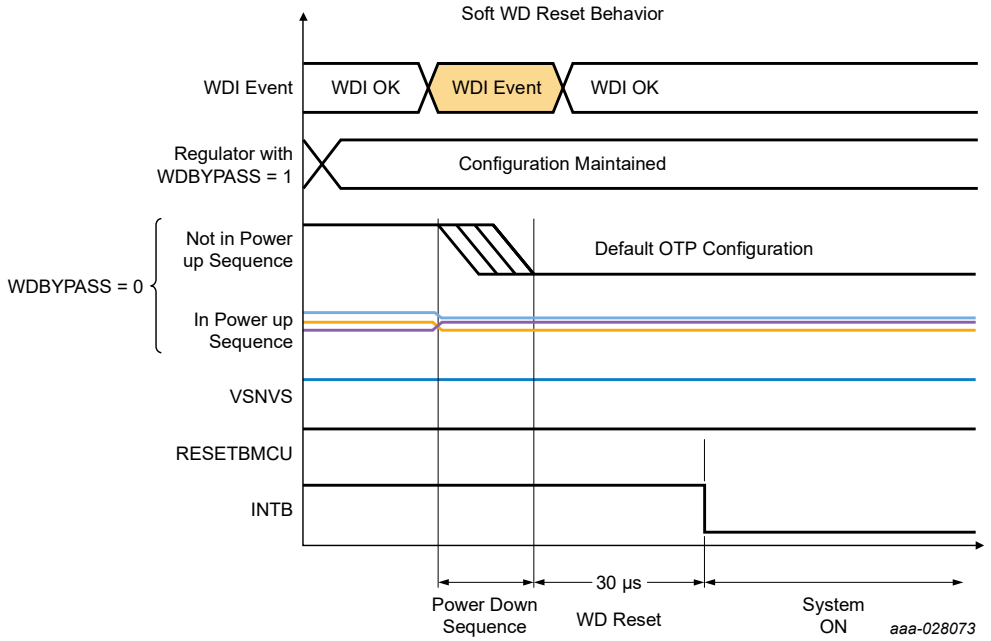


Figure 36. Soft WD reset behavior

A hard WD reset is used to force a system power-on reset when the MCU has becomes unresponsive. In this scenario, a full OTP register reset is performed.

During a hard WD reset, the device turn off all regulators and deassert RESETBMCU as indicated by the power down sequence. If PGOOD is programmed as a GPO and configured as part of the power up sequence, it will also be disabled accordingly.

After all regulator's outputs have gone through the power down sequence and the power down delay is finished, the device waits for 30 µs before reloading the default OTP configuration and gets ready to start a power up sequence if the XFAILB pin is not held low externally.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

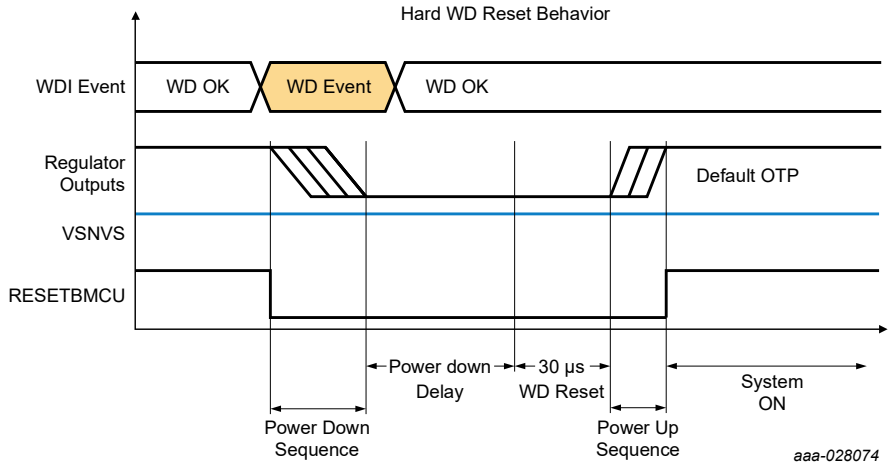


Figure 37. Hard WD reset behavior

After a WD reset, the PMIC may enter the standby state depending on the status of STANDBY pin.

Every time a WD event occurs, the WD_EVENT_CNT[3:0] nibble is incremented. To prevent continuous failures, if the WD_EVENT_CNT[3:0] = WD_MAX_CNT[3:0] the state machine proceeds to the fail-safe transition. The MCU is expected to clear the WD_EVENT_CNT[3:0] when it is able to do so in order to keep proper operation. Upon power up, the WD_MAX_CNT[3:0] is loaded with the values on the OTP_WD_MAX_CNT[3:0] bits.

Every time the device passes through the off states, the WD_EVENT_CNT[3:0] is reset to 0x00, to ensure the counter has a fresh start after a device power down.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

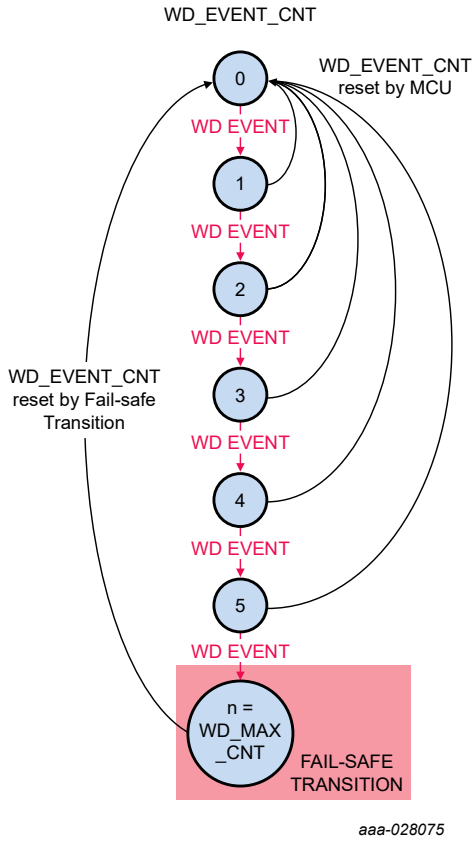


Figure 38. Watchdog event counter

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

16 I²C register map

The PF8100/PF8200 provide a complete set of registers for control and diagnostics of the PMIC operation. The configuration of the device is done at two different levels.

At first level, the OTP Mirror registers provide the default hardware and software configuration for the PMIC upon power up. These are one time programmable and should be defined during the system development phase, and are not meant to be modified during the application. See Section 17 "OTP/TBB and default configurations" for more details on the OTP configuration feature.

At a second level, the PF8100/PF8200 provides a set of functional registers intended for system configuration and diagnostics during the system operation. These registers are accessible during the system-on states and can be modified at any time by the System Control Unit.

The device ID register provides general information about the PMIC.

- DEVICE_FAM[3:0]: indicates the PF8x00 family of devices
  0100 (fixed)
- DEVICE_ID[3:0]: provides the device type identifier
  0000 = PF8100
  1000 = PF8200

Registers 0x02 and 0x03 provide a customizable program ID registers to identify the specific OTP configuration programmed in the part.

- EMREV (Address 0x02): contains the MSB bits PROG_ID[8:11]
- PROG_ID (Address 0x03): contains the LSB bit PROG_ID[7:0]

16.1 PF8200 functional register map

RESET SIGNALS	
UVDET	Reset when VIN crosses UVDET threshold
OFF_OTP	Bits are loaded with OTP values (mirror register)
OFF_TOGGLE	Reset when device goes to OFF mode
SC	Self-clear after write
NO_VSNVS	Reset when BOS has no valid input VIN < UVDET and coin cell < 1.8 V (VSNVS not present)

R/W types	
R	Read only
R/W	Read and Write
RW1C	Read, Write a 1 to clear
R/SW	Read/Secure Write
R/TW	Read/Write on TBB only

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	DEVICE ID	R	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
01	REV ID	R	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
02	EMREV	R	PROG_ID[11:8]				—	EMREV[2:0]		
03	PROG ID	R	PROG_ID[7:0]							
04	INT STATUS1	RW1C	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	XINTB_I	FSOB_I	VIN_OVLO_I
05	INT MASK1	R/W	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	XINTB_M	FSOB_M	VIN_OVLO_M
06	INT SENSE1	R	—	—	—	—	—	XINTB_S	FSOB_S	VIN_OVLO_S
07	THERM INT	RW1C	WDI_I	FSYNC_FLT_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I	THERM_95_I	THERM_80_I
08	THERM MASK	R/W	WDI_M	FSYNC_FLT_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M	THERM_95_M	THERM_80_M
09	THERM SENSE	R	WDI_S	FSYNC_FLT_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S	THERM_95_S	THERM_80_S
0A	SW MODE INT	RW1C	—	SW7_MODE_I	SW6_MODE_I	SW5_MODE_I	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
0B	SW MODE MASK	R/W	—	SW7_MODE_M	SW6_MODE_M	SW5_MODE_M	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
12	SW ILIM INT	RW1C	—	SW7_ILIM_I	SW6_ILIM_I	SW5_ILIM_I	SW4_ILIM_I	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
13	SW ILIM MASK	R/W	—	SW7_ILIM_M	SW6_ILIM_M	SW5_ILIM_M	SW4_ILIM_M	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
14	SW ILIM SENSE	R	—	SW7_ILIM_S	SW6_ILIM_S	SW5_ILIM_S	SW4_ILIM_S	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
15	LDO ILIM INT	RW1C	—	—	—	—	LDO4_ILIM_I	LDO3_ILIM_I	LDO2_ILIM_I	LDO1_ILIM_I
16	LDO ILIM MASK	R/W	—	—	—	—	LDO4_ILIM_M	LDO3_ILIM_M	LDO2_ILIM_M	LDO1_ILIM_M
17	LDO ILIM SENSE	R	—	—	—	—	LDO4_ILIM_S	LDO3_ILIM_S	LDO2_ILIM_S	LDO1_ILIM_S
18	SW UV INT	RW1C	—	SW7_UV_I	SW6_UV_I	SW5_UV_I	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
19	SW UV MASK	R/W	—	SW7_UV_M	SW6_UV_M	SW5_UV_M	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
1A	SW UV SENSE	R	—	SW7_UV_S	SW6_UV_S	SW5_UV_S	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
1B	SW OV INT	RW1C	—	SW7_OV_I	SW6_OV_I	SW5_OV_I	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
1C	SW OV MASK	R/W	—	SW7_OV_M	SW6_OV_M	SW5_OV_M	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
1D	SW OV SENSE	R	—	SW7_OV_S	SW6_OV_S	SW5_OV_S	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
1E	LDO UV INT	RW1C	—	—	—	—	LDO4_UV_I	LDO3_UV_I	LDO2_UV_I	LDO1_UV_I
1F	LDO UV MASK	R/W	—	—	—	—	LDO4_UV_M	LDO3_UV_M	LDO2_UV_M	LDO1_UV_M
20	LDO UV SENSE	R	—	—	—	—	LDO4_UV_S	LDO3_UV_S	LDO2_UV_S	LDO1_UV_S
21	LDO OV INT	RW1C	—	—	—	—	LDO4_OV_I	LDO3_OV_I	LDO2_OV_I	LDO1_OV_I
22	LDO OV MASK	R/W	—	—	—	—	LDO4_OV_M	LDO3_OV_M	LDO2_OV_M	LDO1_OV_M
23	LDO OV SENSE	R	—	—	—	—	LDO4_OV_S	LDO3_OV_S	LDO2_OV_S	LDO1_OV_S
24	PWRON INT	RW1C	BGMON_I	PWRON_8S_I	PWRON_4S_I	PRON_3S_I	PWRON_2S_I	PWRON_1S_I	PWRON_REL_I	PWRON_PUSH_I
25	PWRON MASK	R/W	BGMON_M	PWRON_8S_M	PWRON_4S_M	PRON_3S_M	PWRON_2S_M	PWRON_1S_M	PWRON_REL_M	PWRON_PUSH_M
26	PWRON SENSE	R	BGMON_S	—	—	—	—	—	—	PWRON_S
27	SYS INT	R	EWARN_I	PWRON_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
29	HARD FAULT FLAGS	RW1C	—	—	—	—	PU_FAIL	WD_FAIL	REG_FAIL	TSD_FAIL
2A	FSOB FLAGS	R/SW	—	—	—	FSOB_ASS_NOK	FSOB_SFAULT _NOK	FSOB_WDI_NOK	FSOB_WDC_NOK	FSOB_HFAULT_ NOK
2B	FSOB SELECT	R/W	—	—	—	—	FSOB_SOFTFAULT	FSOB_WDI	FSOB_WDC	FSOB_HARDFAULT
2C	ABIST OV1	R/SW	—	AB_SW7_OV	AB_SW6_OV	AB_SW5_OV	AB_SW4_OV	AB_SW3_OV	AB_SW2_OV	AB_SW1_OV
2D	ABIST OV2	R/SW	—	—	—	—	AB_LDO4_OV	AB_LDO3_OV	AB_LDO2_OV	AB_LDO1_OV
2E	ABIST UV1	R/SW	—	AB_SW7_UV	AB_SW6_UV	AB_SW5_UV	AB_SW4_UV	AB_SW3_UV	AB_SW2_UV	AB_SW1_UV
2F	ABIST UV2	R/SW	—	—	—	—	AB_LDO4_UV	AB_LDO3_UV	AB_LDO2_UV	AB_LDO1_UV
30	TEST FLAGS	R/TW	—	—	—	LDO2EN_S	VSELECT_S	STEST_NOK	TRIM_NOK	OTP_NOK
31	ABIST RUN	R/SW	—	—	—	—	—	—	—	AB_RUN
33	RANDOM GEN	R	RANDOM_GEN[7:0]							
34	RANDOM CHK	R/W	RANDOM_CHK[7:0]							
35	VMONEN1	R/SW	—	SW7VMON_EN	SW6VMON_EN	SW5VMON_EN	SW4VMON_EN	SW3VMON_EN	SW2VMON_EN	SW1VMON_EN
36	VMONEN2	R/SW	—	—	—	—	LDO4VMON_EN	LDO3VMON_EN	LDO2VMON_EN	LDO1VMON_EN
37	CTRL1	R/SW	VIN_OVLO_EN	VIN_OVLO_SDWN	WDI_MODE	TMP_MON_EN	WD_EN	WD_STBY_EN	WDI_STBY_ACTIVE	I2C_SECURE_EN
38	CTRL2	R/W	VIN_OVLO_DBNC[1:0]		—	TMP_MON_AON	LPM_OFF	STANDBYINV	RUN_PG_GPO	STBY_PG_GPO
39	CTRL3	R/W	OV_DB[1:0]		UV_DB[1:0]		—	—	PMIC_OFF	INTB_TEST
3A	PWRUP CTRL	R/W	—	PWRDWN_MODE	PGOOD_PDGRP[1:0]		RESETBMCU_PDGRP[1:0]		SEQ_TBASE[1:0]	
3C	RESETBMCU PWRUP	R/W	RESETBMCU_SEQ[7:0]							
3D	PGOOD PWRUP	R/W	PGOOD_SEQ[7:0]							
3E	PWRDN DLY1	R/W	GRP4_DLY[1:0]		GRP3_DLY[1:0]		GRP2_DLY[1:0]		GRP1_DLY[1:0]	
3F	PWRDN DLY2	R/W	—	—	—	—	—	—	RESETBMCU_DLY[1:0]	
40	FREQ CTRL	R/W	SYNCOUT_EN	FSYNC_RANGE	FSS_EN	FSS_RANGE	CLK_FREQ[3:0]			
41	COINCELL CTRL	R/W	—	—	COINCHG_EN	COINCHG_OFF	VCOIN[3:0]			
42	PWRON	R/W	—	—	—	PWRON_DBNC [1:0]		PWRON_RST_EN	TRESET[1:0]	
43	WD CONFIG	R/W	—	—	—	—	WD_DURATION[3:0]			
44	WD CLEAR	R/W1C	—	—	—	—	—	—	—	WD_CLEAR
45	WD EXPIRE	R/W	—	WD_MAX_EXPIRE[2:0]			—	WD_EXPIRE_CNT[2:0]		
46	WD COUNTER	R/W	WD_MAX_CNT [3:0]				WD_EVENT_CNT [3:0]			
47	FAULT COUNTER	R/W	FAULT_MAX_CNT[3:0]				FAULT_CNT [3:0]			
48	FSAFE COUNTER	R/W	—	—	—	—	FS_CNT [3:0]			
49	FAULT TIMERS	R/W	—	—	—	—	TIMER_FAULT[3:0]			
4A	AMUX	R/W	—	—	AMUX_EN	AMUX_SEL [4:0]				

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
4D	SW1 CONFIG1	R/W	SW1_UV_BYPASS	SW1_OV_BYPASS	SW1_ILIM_BYPASS	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_STATE	SW1_WDBYPASS	SW1_PG_EN
4E	SW1 CONFIG2	R/W	SW1_FLT_REN	—	SW1DVS_RAMP	SW1ILIM[1:0]		SW1PHASE[2:0]		
4F	SW1 PWRUP	R/W	SW1_SEQ[7:0]							
50	SW1 MODE	R/W	—	—	SW1_PDGRP[1:0]		SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]	
51	SW1 RUN VOLT	R/W	VSW1_RUN[7:0]							
52	SW1 STBY VOLT	R/W	VSW1_STBY[7:0]							
55	SW2 CONFIG1	R/W	SW2_UV_BYPASS	SW2_OV_BYPASS	SW2_ILIM_BYPASS	SW2_UV_STATE	SW2_OV_STATE	SW2_ILIM_STATE	SW2_WDBYPASS	SW2_PG_EN
56	SW2 CONFIG2	R/W	SW2_FLT_REN	—	SW2DVS_RAMP	SW2ILIM[1:0]		SW2PHASE[2:0]		
57	SW2 PWRUP	R/W	SW2_SEQ[7:0]							
58	SW2 MODE1	R/W	—	—	SW2_PDGRP[1:0]		SW2_STBY_MODE[1:0]		SW2_RUN_MODE[1:0]	
59	SW2 RUN VOLT	R/W	VSW2_RUN[7:0]							
5A	SW2 STBY VOLT	R/W	VSW2_STBY[7:0]							
5D	SW3 CONFIG1	R/W	SW3_UV_BYPASS	SW3_OV_BYPASS	SW3_ILIM_BYPASS	SW3_UV_STATE	SW3_OV_STATE	SW3_ILIM_STATE	SW3_WDBYPASS	SW3_PG_EN
5E	SW3 CONFIG2	R/W	SW3_FLT_REN	—	SW3DVS_RAMP	SW3ILIM[1:0]		SW3PHASE[2:0]		
5F	SW3 PWRUP	R/W	SW3_SEQ[7:0]							
60	SW3 MODE1	R/W	—	—	SW3_PDGRP[1:0]		SW3_STBY_MODE[1:0]		SW3_RUN_MODE[1:0]	
61	SW3 RUN VOLT	R/W	VSW3_RUN[7:0]							
62	SW3 STBY VOLT	R/W	VSW3_STBY[7:0]							
65	SW4 CONFIG1	R/W	SW4_UV_BYPASS	SW4_OV_BYPASS	SW4_ILIM_BYPASS	SW4_UV_STATE	SW4_OV_STATE	SW4_ILIM_STATE	SW4_WDBYPASS	SW4_PG_EN
66	SW4 CONFIG2	R/W	SW4_FLT_REN	—	SW4DVS_RAMP	SW4ILIM[1:0]		SW4PHASE[2:0]		
67	SW4 PWRUP	R/W	SW4_SEQ[7:0]							
68	SW4 MODE1	R/W	—	—	SW4_PDGRP[1:0]		SW4_STBY_MODE[1:0]		SW4_RUN_MODE[1:0]	
69	SW4 RUN VOLT	R/W	VSW4_RUN[7:0]							
6A	SW4 STBY VOLT	R/W	VSW4_STBY[7:0]							
6D	SW5 CONFIG1	R/W	SW5_UV_BYPASS	SW5_OV_BYPASS	SW5_ILIM_BYPASS	SW5_UV_STATE	SW5_OV_STATE	SW5_ILIM_STATE	SW5_WDBYPASS	SW5_PG_EN
6E	SW5 CONFIG2	R/W	SW5_FLT_REN	—	SW5DVS_RAMP	SW5ILIM[1:0]		SW5PHASE[2:0]		
6F	SW5 PWRUP	R/W	SW5_SEQ[7:0]							
70	SW5 MODE1	R/W	—	—	SW5_PDGRP[1:0]		SW5_STBY_MODE[1:0]		SW5_RUN_MODE[1:0]	
71	SW5 RUN VOLT	R/W	VSW5_RUN[7:0]							
72	SW5 STBY VOLT	R/W	VSW5_STBY[7:0]							
75	SW6 CONFIG1	R/W	SW6_UV_BYPASS	SW6_OV_BYPASS	SW6_ILIM_BYPASS	SW6_UV_STATE	SW6_OV_STATE	SW6_ILIM_STATE	SW6_WDBYPASS	SW6_PG_EN
76	SW6 CONFIG2	R/W	SW6_FLT_REN	SW6_VTTEN	SW6DVS_RAMP	SW6ILIM[1:0]		SW6PHASE[2:0]		
77	SW6 PWRUP	R/W	SW6_SEQ[7:0]							
78	SW6 MODE1	R/W	—	—	SW6_PDGRP[1:0]		SW6_STBY_MODE[1:0]		SW6_RUN_MODE[1:0]	
79	SW6 RUN VOLT	R/W	VSW6_RUN[7:0]							
7A	SW6 STBY VOLT	R/W	VSW6_STBY[7:0]							
7D	SW7 CONFIG1	R/W	SW7_UV_BYPASS	SW7_OV_BYPASS	SW7_ILIM_BYPASS	SW7_UV_STATE	SW7_OV_STATE	SW7_ILIM_STATE	SW7_WDBYPASS	SW7_PG_EN
7E	SW7 CONFIG2	R/W	SW7_FLT_REN	—	—	SW7ILIM[1:0]		SW7PHASE[2:0]		
7F	SW7 PWRUP	R/W	SW7_SEQ[7:0]							
80	SW7 MODE1	R/W	—	—	SW7_PDGRP[1:0]		SW7_STBY_MODE[1:0]		SW7_RUN_MODE[1:0]	
81	SW7 RUN VOLT	R/W	—	—	—	VSW7[4:0]				
85	LDO1 CONFIG1	R/W	LDO1_UV_BYPASS	LDO1_OV_BYPASS	LDO1_ILIM_BYPASS	LDO1_UV_STATE	LDO1_OV_STATE	LDO1_ILIM_STATE	LDO1_WDBYPASS	LDO1_PG_EN
86	LDO1 CONFIG2	R/W	LDO1_FLT_REN	LDO1_PDGRP[1:0]		—	—	—	LDO1_RUN_EN	LDO1_STBY_EN
87	LDO1 PWRUP	R/W	LDO1_SEQ[7:0]							
88	LDO1 RUN VOLT	R/W	—	—	—	—	VLDO1_RUN[3:0]			
89	LDO1 STBY VOLT	R/W	—	—	—	—	VLDO1_STBY[3:0]			

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
8B	LDO2 CONFIG1	R/W	LDO2_UV_ BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_ BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_ILIM_STATE	LDO2_WDBYPASS	LDO2_PG_EN
8C	LDO2 CONFIG2	R/W	LDO2_FLT_ REN	LDO2_PDGRP[1:0]		LDO2HW_EN	VSELECT_EN	—	LDO2_RUN_EN	LDO2_STBY_EN
8D	LDO2 PWRUP	R/W	LDO2_SEQ[7:0]							
8E	LDO2 RUN VOLT	R/W	—	—	—	—	VLDO2_RUN[3:0]			
8F	LDO2 STBY VOLT	R/W	—	—	—	—	VLDO2_STBY[3:0]			
91	LDO3 CONFIG1	R/W	LDO3_UV_ BYPASS	LDO3_OV_BYPASS	LDO3_ILIM_ BYPASS	LDO3_UV_STATE	LDO3_OV_STATE	LDO3_ILIM_STATE	LDO3_WDBYPASS	LDO3_PG_EN
92	LDO3 CONFIG2	R/W	LDO3_FLT_ REN	LDO3_PDGRP[1:0]		—	—	—	LDO3_RUN_EN	LDO3_STBY_EN
93	LDO3 PWRUP	R/W	LDO3_SEQ[7:0]							
94	LDO3 RUN VOLT	R/W	—	—	—	—	VLDO3_RUN[3:0]			
95	LDO3 STBY VOLT	R/W	—	—	—	—	VLDO3_STBY[3:0]			
97	LDO4 CONFIG1	R/W	LDO4_UV_ BYPASS	LDO4_OV_BYPASS	LDO4_ILIM_ BYPASS	LDO4_UV_STATE	LDO4_OV_STATE	LDO4_ILIM_STATE	LDO4_WDBYPASS	LDO4_PG_EN
98	LDO4 CONFIG2	R/W	LDO4_FLT_ REN	LDO4_PDGRP[1:0]		—	—	—	LDO4_RUN_EN	LDO4_STBY_EN
99	LDO4 PWRUP	R/W	LDO4_SEQ[7:0]							
9A	LDO4 RUN VOLT	R/W	—	—	—	—	VLDO4_RUN[3:0]			
9B	LDO4 STBY VOLT	R/W	—	—	—	—	VLDO4_STBY[3:0]			
9D	VSNVS CONFIG1	R/W	—	—	—	—	—	—	VSNVSVOLT [1:0]	
9F	PAGE SELECT	R/TW	—	—	—	—	—	PAGE[2:0]		

16.2 PF8200 OTP mirror register map (page 1)

Reset types	
OFF_OTP	Register loads the OTP mirror register values during power up
OTP	Register available in OTP bank only, reset from fuses when VIN crosses UVDET threshold
VSNVS	Reset when BOS has no valid input. VIN < UVDET and coin cell < 1.8 V (VSNVS not present)

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A0	OTP FSOB SELECT	—	—	—	OTP_FSOB_ ASS_EN	OTP_FSOB_ SOFTFAULT	OTP_FSOB_ WDI	OTP_FSOB_ WDC	OTP_FSOB_ HARDFAULT
A1	OTP I2C	—	—	—	OTP_I2C_ SECURE_EN	OTP_I2C_ CRC_EN	OTP_I2C_ADD[2:0]		
A2	OTP CTRL1	—	—	OTP_EWARN_TIME[1:0]		OTP_FS_ BYPASS	OTP_ STANDBYINV	OTP_PG_ ACTIVE	OTP_PG_CHECK
A3	OTP CTRL2	OTP_FSS_EN	OTP_FSS_RANGE	—	OTP_XFAILB_EN	OTP_VIN_ OVLO_SDWN	OTP_VIN_ OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
A4	OTP CTRL3	OTP_VTT_PDOWN	OTP_SW6_VTTEN	OTP_SW5CONFIG[1:0]		OTP_SW4CONFIG[1:0]		OTP_SW1CONFIG[1:0]	
A5	OTP FREQ CTRL	OTP_SW_MODE	OTP_SYNCIN_ EN	OTP_SYNCOUT_ EN	OTP_FSYNC_ RANGE	OTP_CLK_FREQ[3:0]			
A6	OTP COI NCELL CTRL	—	—	—	—	OTP_VCOIN[3:0]			
A7	OTP PWRON	—	—	OTP_PWRON_ MODE	OTP_PWRON_DBNC[1:0]		OTP_PWRON_RST_ EN	OTP_TRESET[1:0]	
A8	OTP WD CONFIG	—	—	OTP_WDI_ MODE	OTP_WDI_INV	OTP_WD_EN	OTP_WD_ STBY_EN	OTP_WDI_ STBY_ACTIVE	OTP_ WDWINDOW
A9	OTP WD EXPIRE	—	—	—	—	—	OTP_WD_MAX_EXPIRE[2:0]		

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
AA	OTP WD COUNTER	OTP_WD_DURATION[3:0]				OTP_WD_MAX_CNT [3:0]			
AB	OTP FAULT COUNTERS	OTP_FS_MAX_CNT[3:0]				OTP_FAULT_MAX_CNT[3:0]			
AC	OTP FAULT TIMERS	—	OTP_FS_OK_TIMER[2:0]			OTP_TIMER_FAULT[3:0]			
AD	OTP PWRDN DLY1	OTP_GRP4_DLY[1:0]		OTP_GRP3_DLY[1:0]		OTP_GRP2_DLY[1:0]		OTP_GRP1_DLY[1:0]	
AE	OTP PWRDN DLY2	OTP_PD_SEQ_DLY[1:0]		—	—	—	—	OTP_RESETBMCU_DLY[1:0]	
AF	OTP PWRUP CTRL	—	OTP_PWRDWN_MODE	OTP_PGOOD_PDGRP[1:0]		OTP_RESETBMCU_PDGRP[1:0]		OTP_SEQ_TBASE[1:0]	
B0	OTP RES ETBMCU PWRUP	OTP_RESETBMCU_SEQ[7:0]							
B1	OTP PGOOD PWRUP	OTP_PGOOD_SEQ[7:0]							
B2	OTP SW1 VOLT	OTP_VSW1[7:0]							
B3	OTP SW1 PWRUP	OTP_SW1_SEQ[7:0]							
B4	OTP SW1 CONFIG1	OTP_SW1UV_TH[1:0]		OTP_SW1OV_TH[1:0]		OTP_SW1_PDGRP[1:0]		OTP_SW1ILIM[1:0]	
B5	OTP SW1 CONFIG2	OTP_SW1_LSELECT[1:0]		OTP_SW1PHASE[2:0]			OTP_SW1DVS_RAMP	OTP_SW1_PG_EN	OTP_SW1_WDBYPASS
B6	OTP SW2 VOLT	OTP_VSW2[7:0]							
B7	OTP SW2 PWRUP	OTP_SW2_SEQ[7:0]							
B8	OTP SW2 CONFIG1	OTP_SW2UV_TH[1:0]		OTP_SW2OV_TH[1:0]		OTP_SW2_PDGRP[1:0]		OTP_SW2ILIM[1:0]	
B9	OTP SW2 CONFIG2	OTP_SW2_LSELECT[1:0]		OTP_SW2PHASE[2:0]			OTP_SW2DVS_RAMP	OTP_SW2_PG_EN	OTP_SW2_WDBYPASS
BA	OTP SW3_VOLT	OTP_VSW3[7:0]							
BB	OTP SW3 PWRUP	OTP_SW3_SEQ[7:0]							
BC	OTP SW3 CONFIG1	OTP_SW3UV_TH[1:0]		OTP_SW3OV_TH[1:0]		OTP_SW3_PDGRP[1:0]		OTP_SW3ILIM[1:0]	
BD	OTP SW3 CONFIG2	OTP_SW3_LSELECT[1:0]		OTP_SW3PHASE[2:0]			OTP_SW3DVS_RAMP	OTP_SW3_PG_EN	OTP_SW3_WDBYPASS
BE	OTP SW4 VOLT	OTP_VSW4[7:0]							
BF	OTP SW4 PWRUP	OTP_SW4_SEQ[7:0]							
C0	OTP SW4 CONFIG1	OTP_SW4UV_TH[1:0]		OTP_SW4OV_TH[1:0]		OTP_SW4_PDGRP[1:0]		OTP_SW4ILIM[1:0]	
C1	OTP SW4 CONFIG2	OTP_SW4_LSELECT[1:0]		OTP_SW4PHASE[2:0]			OTP_SW4DVS_RAMP	OTP_SW4_PG_EN	OTP_SW4_WDBYPASS
C2	OTP SW5 VOLT	OTP_VSW5[7:0]							
C3	OTP SW5 PWRUP	OTP_SW5_SEQ[7:0]							
C4	OTP SW5 CONFIG1	OTP_SW5UV_TH[1:0]		OTP_SW5OV_TH[1:0]		OTP_SW5_PDGRP[1:0]		OTP_SW5ILIM[1:0]	
C5	OTP SW5 CONFIG2	OTP_SW5_LSELECT[1:0]		OTP_SW5PHASE[2:0]			OTP_SW5DVS_RAMP	OTP_SW5_PG_EN	OTP_SW5_WDBYPASS
C6	OTP SW6 VOLT	OTP_VSW6[7:0]							
C7	OTP SW6 PWRUP	OTP_SW6_SEQ[7:0]							
C8	OTP SW6 CONFIG1	OTP_SW6UV_TH[1:0]		OTP_SW6OV_TH[1:0]		OTP_SW6_PDGRP[1:0]		OTP_SW6ILIM[1:0]	
C9	OTP SW6 CONFIG2	OTP_SW6_LSELECT[1:0]		OTP_SW6PHASE[2:0]			OTP_SW6DVS_RAMP	OTP_SW6_PG_EN	OTP_SW6_WDBYPASS
CA	OTP SW7 VOLT	—	—	—	OTP_VSW7[4:0]				
CB	OTP SW7 PWRUP	OTP_SW7_SEQ[7:0]							

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CC	OTP SW7 CONFIG1	OTP_SW7UV_TH[1:0]		OTP_SW7OV_TH[1:0]		OTP_SW7_PDGRP[1:0]		OTP_SW7ILIM[1:0]	
CD	OTP SW7 CONFIG2	OTP_SW7_LSELECT[1:0]		OTP_SW7PHASE[2:0]			—	OTP_SW7_PG_EN	OTP_SW7_WDBYPASS
CE	OTP LDO1 VOLT	OTP_LDO1UV_TH[1:0]		OTP_LDO1OV_TH[1:0]		OTP_VLDO1[3:0]			
CF	OTP LDO1 PWRUP	OTP_LDO1_SEQ[7:0]							
D0	OTP LDO1 CONFIG	OTP_LDO1_PDGRP[1:0]		—	—	—	OTP_LDO1_PG_EN	OTP_LDO1_WDBYPASS	OTP_LDO1LS
D1	OTP LDO2 VOLT	OTP_LDO2UV_TH[1:0]		OTP_LDO2OV_TH[1:0]		OTP_VLDO2[3:0]			
D2	OTP LDO2 PWRUP	OTP_LDO2_SEQ[7:0]							
D3	OTP LDO2 CONFIG	OTP_LDO2_PDGRP[1:0]		OTP_VSELECT_EN	OTP_LDO2HW_EN	—	OTP_LDO2_PG_EN	OTP_LDO2_WDBYPASS	OTP_LDO2LS
D4	OTP LDO3 VOLT	OTP_LDO3UV_TH[1:0]		OTP_LDO3OV_TH[1:0]		OTP_VLDO3[3:0]			
D5	OTP LDO3 PWRUP	OTP_LDO3_SEQ[7:0]							
D6	OTP LDO3 CONFIG	OTP_LDO3_PDGRP[1:0]		—	—	—	OTP_LDO3_PG_EN	OTP_LDO3_WDBYPASS	OTP_LDO3LS
D7	OTP LDO4 VOLT	OTP_LDO4UV_TH[1:0]		OTP_LDO4OV_TH[1:0]		OTP_VLDO4[3:0]			
D8	OTP LDO4 PWRUP	OTP_LDO4_SEQ[7:0]							
D9	OTP LDO4 CONFIG	OTP_LDO4_PDGRP[1:0]		—	—	—	OTP_LDO4_PG_EN	OTP_LDO4_WDBYPASS	OTP_LDO4LS
DA	OTP VSNVS CONFIG	—	—	—	—	—	—	VSNVSVOLT [1:0]	
DB	OTP_OV_BYPASS1	—	OTP_SW7_OVBYPASS	OTP_SW6_OVBYPASS	OTP_SW5_OVBYPASS	OTP_SW4_OVBYPASS	OTP_SW3_OVBYPASS	OTP_SW2_OVBYPASS	OTP_SW1_OVBYPASS
DC	OTP_OV_BYPASS2	—	—	—	—	OTP_LDO4_OVBYPASS	OTP_LDO3_OVBYPASS	OTP_LDO2_OVBYPASS	OTP_LDO1_OVBYPASS
DD	OTP_UV_BYPASS1	—	OTP_SW7_UVBYPASS	OTP_SW6_UVBYPASS	OTP_SW5_UVBYPASS	OTP_SW4_UVBYPASS	OTP_SW3_UVBYPASS	OTP_SW2_UVBYPASS	OTP_SW1_UVBYPASS
DE	OTP_UV_BYPASS2	—	—	—	—	OTP_LDO4_UVBYPASS	OTP_LDO3_UVBYPASS	OTP_LDO2_UVBYPASS	OTP_LDO1_UVBYPASS
DF	OTP_ILIM_BYPASS1	—	OTP_SW7_ILIMBYPASS	OTP_SW6_ILIMBYPASS	OTP_SW5_ILIMBYPASS	OTP_SW4_ILIMBYPASS	OTP_SW3_ILIMBYPASS	OTP_SW2_ILIMBYPASS	OTP_SW1_ILIMBYPASS
E0	OTP_ILIM_BYPASS2	—	—	—	—	OTP_LDO4_ILIMBYPASS	OTP_LDO3_ILIMBYPASS	OTP_LDO2_ILIMBYPASS	OTP_LDO1_ILIMBYPASS
E3	OTP DEBUG1	—	—	—	—	—	—	—	BGMON_BYPASS

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

16.3 PF8100 functional register map

RESET SIGNALS	
UVDET	Reset when VIN crosses UVDET threshold
OFF_OTP	Bits are loaded with OTP values (mirror register)
OFF_TOGGLE	Reset when device goes to OFF mode
SC	Self-clear after write
NO_VSNVS	Reset when BOS has no valid input VIN < UVDET and coin cell < 1.8 V (VSNVS not present)

R/W types	
R	Read only
R/W	Read and Write
RW1C	Read, Write a 1 to clear
R/SW	Read/Secure Write
R/TW	Read/Write on TBB only

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	DEVICE ID	R	DEVICE_FAM[3:0]				DEVICE_ID[3:0]			
01	REV ID	R	FULL_LAYER_REV[3:0]				METAL_LAYER_REV[3:0]			
02	EMREV	R	PROG_ID[11-8]				—	EMREV[2:0]		
03	PROG ID	R	PROG_ID[7:0]							
04	INT STATUS1	RW1C	SDWN_I	FREQ_RDY_I	CRC_I	PWRUP_I	PWRDN_I	XINTB_I	FSOB_I	VIN_OVLO_I
05	INT MASK1	R/W	SDWN_M	FREQ_RDY_M	CRC_M	PWRUP_M	PWRDN_M	XINTB_M	FSOB_M	VIN_OVLO_M
06	INT SENSE1	R	—	—	—	—	—	XINTB_S	FSOB_S	VIN_OVLO_S
07	THERM INT	RW1C	WDI_I	FSYNC_FLT_I	THERM_155_I	THERM_140_I	THERM_125_I	THERM_110_I	THERM_95_I	THERM_80_I
08	THERM MASK	R/W	WDI_M	FSYNC_FLT_M	THERM_155_M	THERM_140_M	THERM_125_M	THERM_110_M	THERM_95_M	THERM_80_M
09	THERM SENSE	R	WDI_S	FSYNC_FLT_S	THERM_155_S	THERM_140_S	THERM_125_S	THERM_110_S	THERM_95_S	THERM_80_S
0A	SW MODE INT	RW1C	—	SW7_MODE_I	SW6_MODE_I	SW5_MODE_I	SW4_MODE_I	SW3_MODE_I	SW2_MODE_I	SW1_MODE_I
0B	SW MODE MASK	R/W	—	SW7_MODE_M	SW6_MODE_M	SW5_MODE_M	SW4_MODE_M	SW3_MODE_M	SW2_MODE_M	SW1_MODE_M
12	SW ILIM INT	RW1C	—	SW7_ILIM_I	SW6_ILIM_I	SW5_ILIM_I	SW4_ILIM_I	SW3_ILIM_I	SW2_ILIM_I	SW1_ILIM_I
13	SW ILIM MASK	R/W	—	SW7_ILIM_M	SW6_ILIM_M	SW5_ILIM_M	SW4_ILIM_M	SW3_ILIM_M	SW2_ILIM_M	SW1_ILIM_M
14	SW ILIM SENSE	R	—	SW7_ILIM_S	SW6_ILIM_S	SW5_ILIM_S	SW4_ILIM_S	SW3_ILIM_S	SW2_ILIM_S	SW1_ILIM_S
15	LDO ILIM INT	RW1C	—	—	—	—	LDO4_ILIM_I	LDO3_ILIM_I	LDO2_ILIM_I	LDO1_ILIM_I
16	LDO ILIM MASK	R/W	—	—	—	—	LDO4_ILIM_M	LDO3_ILIM_M	LDO2_ILIM_M	LDO1_ILIM_M
17	LDO ILIM SENSE	R	—	—	—	—	LDO4_ILIM_S	LDO3_ILIM_S	LDO2_ILIM_S	LDO1_ILIM_S
18	SW UV INT	RW1C	—	SW7_UV_I	SW6_UV_I	SW5_UV_I	SW4_UV_I	SW3_UV_I	SW2_UV_I	SW1_UV_I
19	SW UV MASK	R/W	—	SW7_UV_M	SW6_UV_M	SW5_UV_M	SW4_UV_M	SW3_UV_M	SW2_UV_M	SW1_UV_M
1A	SW UV SENSE	R	—	SW7_UV_S	SW6_UV_S	SW5_UV_S	SW4_UV_S	SW3_UV_S	SW2_UV_S	SW1_UV_S
1B	SW OV INT	RW1C	—	SW7_OV_I	SW6_OV_I	SW5_OV_I	SW4_OV_I	SW3_OV_I	SW2_OV_I	SW1_OV_I
1C	SW OV MASK	R/W	—	SW7_OV_M	SW6_OV_M	SW5_OV_M	SW4_OV_M	SW3_OV_M	SW2_OV_M	SW1_OV_M
1D	SW OV SENSE	R	—	SW7_OV_S	SW6_OV_S	SW5_OV_S	SW4_OV_S	SW3_OV_S	SW2_OV_S	SW1_OV_S
1E	LDO UV INT	RW1C	—	—	—	—	LDO4_UV_I	LDO3_UV_I	LDO2_UV_I	LDO1_UV_I
1F	LDO UV MASK	R/W	—	—	—	—	LDO4_UV_M	LDO3_UV_M	LDO2_UV_M	LDO1_UV_M
20	LDO UV SENSE	R	—	—	—	—	LDO4_UV_S	LDO3_UV_S	LDO2_UV_S	LDO1_UV_S
21	LDO OV INT	RW1C	—	—	—	—	LDO4_OV_I	LDO3_OV_I	LDO2_OV_I	LDO1_OV_I
22	LDO OV MASK	R/W	—	—	—	—	LDO4_OV_M	LDO3_OV_M	LDO2_OV_M	LDO1_OV_M
23	LDO OV SENSE	R	—	—	—	—	LDO4_OV_S	LDO3_OV_S	LDO2_OV_S	LDO1_OV_S
24	PWRON INT	RW1C	BGMON_I	PWRON_8S_I	PWRON_4S_I	PRON_3S_I	PWRON_2S_I	PWRON_1S_I	PWRON_REL_I	PWRON_PUSH_I
25	PWRON MASK	R/W	BGMON_M	PWRON_8S_M	PWRON_4S_M	PRON_3S_M	PWRON_2S_M	PWRON_1S_M	PWRON_REL_M	PWRON_PUSH_M
26	PWRON SENSE	R	BGMON_S	—	—	—	—	—	—	PWRON_S
27	SYS INT	R	EWARN_I	PWRON_I	OV_I	UV_I	ILIM_I	MODE_I	STATUS2_I	STATUS1_I
29	HARD FAULT FLAGS	RW1C	—	—	—	—	PU_FAIL	WD_FAIL	REG_FAIL	TSD_FAIL
2A	FSOB FLAGS	R/SW	—	—	—	—	FSOB_SFAULT_NOK	FSOB_WDI_NOK	FSOB_WDC_NOK	FSOB_HFAULT_NOK
2B	FSOB SELECT	R/W	—	—	—	—	FSOB_SOFTFAULT	FSOB_WDI	FSOB_WDC	FSOB_HARDFAULT
30	TEST FLAGS	R/TW	—	—	—	LDO2EN_S	VSELECT_S	—	TRIM_NOK	OTP_NOK
35	VMONEN1	R/SW	—	SW7VMON_EN	SW6VMON_EN	SW5VMON_EN	SW4VMON_EN	SW3VMON_EN	SW2VMON_EN	SW1VMON_EN

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
36	VMONEN2	R/SW	—	—	—	—	LDO4VMON_EN	LDO3VMON_EN	LDO2VMON_EN	LDO1VMON_EN
37	CTRL1	R/SW	VIN_OVLO_EN	VIN_OVLO_SDWN	WDI_MODE	TMP_MON_EN	WD_EN	WD_STBY_EN	WDI_STBY_ACTIVE	—
38	CTRL2	R/W	VIN_OVLO_DBNC[1:0]		—	TMP_MON_AON	LPM_OFF	STANDBYINV	RUN_PG_GPO	STBY_PG_GPO
39	CTRL3	R/W	OV_DB[1:0]		UV_DB[1:0]		—	—	PMIC_OFF	INTB_TEST
3A	PWRUP CTRL	R/W	—	PWRDWN_MODE	PGOOD_PDGRP[1:0]		RESETBMCU_PDGRP[1:0]		SEQ_TBASE[1:0]	
3C	RESETBMCU PWRUP	R/W	RESETBMCU_SEQ[7:0]							
3D	PGOOD PWRUP	R/W	PGOOD_SEQ[7:0]							
3E	PWRDN DLY1	R/W	GRP4_DLY[1:0]		GRP3_DLY[1:0]		GRP2_DLY[1:0]		GRP1_DLY[1:0]	
3F	PWRDN DLY2	R/W	—	—	—	—	—	—	RESETBMCU_DLY[1:0]	
40	FREQ CTRL	R/W	SYNCOUT_EN	FSYNC_RANGE	FSS_EN	FSS_RANGE	CLK_FREQ[3:0]			
41	COINCELL CTRL	R/W	—	—	COINCHG_EN	COINCHG_OFF	VCOIN[3:0]			
42	PWRON	R/W	—	—	—	PWRON_DBNC [1:0]		PWRON_RST_EN	TRESET[1:0]	
43	WD CONFIG	R/W	—	—	—	—	WD_DURATION[3:0]			
44	WD CLEAR	R/W1C	—	—	—	—	—	—	—	WD_CLEAR
45	WD EXPIRE	R/W	—	WD_MAX_EXPIRE[2:0]			—	WD_EXPIRE_CNT[2:0]		
46	WD COUNTER	R/W	WD_MAX_CNT [3:0]				WD_EVENT_CNT [3:0]			
47	FAULT COUNTER	R/W	FAULT_MAX_CNT[3:0]				FAULT_CNT [3:0]			
49	FAULT TIMERS	R/W	—	—	—	—	TIMER_FAULT[3:0]			
4A	AMUX	R/W	—	—	AMUX_EN	AMUX_SEL [4:0]				
4D	SW1 CONFIG1	R/W	SW1_UV_ BYPASS	SW1_OV_BYPASS	SW1_ILIM_BYPASS	SW1_UV_STATE	SW1_OV_STATE	SW1_ILIM_STATE	SW1_WDBYPASS	SW1_PG_EN
4E	SW1 CONFIG2	R/W	SW1_FLT_REN	—	SW1DVS_RAMP	SW1ILIM[1:0]		SW1PHASE[2:0]		
4F	SW1 PWRUP	R/W	SW1_SEQ[7:0]							
50	SW1 MODE	R/W	—	—	SW1_PDGRP[1:0]		SW1_STBY_MODE[1:0]		SW1_RUN_MODE[1:0]	
51	SW1 RUN VOLT	R/W	VSW1_RUN[7:0]							
52	SW1 STBY VOLT	R/W	VSW1_STBY[7:0]							
55	SW2 CONFIG1	R/W	SW2_UV_ BYPASS	SW2_OV_BYPASS	SW2_ILIM_BYPASS	SW2_UV_STATE	SW2_OV_STATE	SW2_ILIM_STATE	SW2_WDBYPASS	SW2_PG_EN
56	SW2 CONFIG2	R/W	SW2_FLT_REN	—	SW2DVS_RAMP	SW2ILIM[1:0]		SW2PHASE[2:0]		
57	SW2 PWRUP	R/W	SW2_SEQ[7:0]							
58	SW2 MODE1	R/W	—	—	SW2_PDGRP[1:0]		SW2_STBY_MODE[1:0]		SW2_RUN_MODE[1:0]	
59	SW2 RUN VOLT	R/W	VSW2_RUN[7:0]							
5A	SW2 STBY VOLT	R/W	VSW2_STBY[7:0]							
5D	SW3 CONFIG1	R/W	SW3_UV_ BYPASS	SW3_OV_BYPASS	SW3_ILIM_BYPASS	SW3_UV_STATE	SW3_OV_STATE	SW3_ILIM_STATE	SW3_WDBYPASS	SW3_PG_EN
5E	SW3 CONFIG2	R/W	SW3_FLT_REN	—	SW3DVS_RAMP	SW3ILIM[1:0]		SW3PHASE[2:0]		
5F	SW3 PWRUP	R/W	SW3_SEQ[7:0]							
60	SW3 MODE1	R/W	—	—	SW3_PDGRP[1:0]		SW3_STBY_MODE[1:0]		SW3_RUN_MODE[1:0]	
61	SW3 RUN VOLT	R/W	VSW3_RUN[7:0]							
62	SW3 STBY VOLT	R/W	VSW3_STBY[7:0]							
65	SW4 CONFIG1	R/W	SW4_UV_ BYPASS	SW4_OV_BYPASS	SW4_ILIM_BYPASS	SW4_UV_STATE	SW4_OV_STATE	SW4_ILIM_STATE	SW4_WDBYPASS	SW4_PG_EN
66	SW4 CONFIG2	R/W	SW4_FLT_REN	—	SW4DVS_RAMP	SW4ILIM[1:0]		SW4PHASE[2:0]		
67	SW4 PWRUP	R/W	SW4_SEQ[7:0]							
68	SW4 MODE1	R/W	—	—	SW4_PDGRP[1:0]		SW4_STBY_MODE[1:0]		SW4_RUN_MODE[1:0]	
69	SW4 RUN VOLT	R/W	VSW4_RUN[7:0]							
6A	SW4 STBY VOLT	R/W	VSW4_STBY[7:0]							
6D	SW5 CONFIG1	R/W	SW5_UV_ BYPASS	SW5_OV_BYPASS	SW5_ILIM_BYPASS	SW5_UV_STATE	SW5_OV_STATE	SW5_ILIM_STATE	SW5_WDBYPASS	SW5_PG_EN
6E	SW5 CONFIG2	R/W	SW5_FLT_REN	—	SW5DVS_RAMP	SW5ILIM[1:0]		SW5PHASE[2:0]		
6F	SW5 PWRUP	R/W	SW5_SEQ[7:0]							
70	SW5 MODE1	R/W	—	—	SW5_PDGRP[1:0]		SW5_STBY_MODE[1:0]		SW5_RUN_MODE[1:0]	
71	SW5 RUN VOLT	R/W	VSW5_RUN[7:0]							
72	SW5 STBY VOLT	R/W	VSW5_STBY[7:0]							

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register Name	R/W	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
75	SW6 CONFIG1	R/W	SW6_UV_BYPASS	SW6_OV_BYPASS	SW6_ILIM_BYPASS	SW6_UV_STATE	SW6_OV_STATE	SW6_ILIM_STATE	SW6_WDBYPASS	SW6_PG_EN
76	SW6 CONFIG2	R/W	SW6_FLT_REN	SW6_VTTEN	SW6DVS_RAMP	SW6ILIM[1:0]		SW6PHASE[2:0]		
77	SW6 PWRUP	R/W	SW6_SEQ[7:0]							
78	SW6 MODE1	R/W	—	—	SW6_PDGRP[1:0]		SW6_STBY_MODE[1:0]		SW6_RUN_MODE[1:0]	
79	SW6 RUN VOLT	R/W	VSW6_RUN[7:0]							
7A	SW6 STBY VOLT	R/W	VSW6_STBY[7:0]							
7D	SW7 CONFIG1	R/W	SW7_UV_BYPASS	SW7_OV_BYPASS	SW7_ILIM_BYPASS	SW7_UV_STATE	SW7_OV_STATE	SW7_ILIM_STATE	SW7_WDBYPASS	SW7_PG_EN
7E	SW7 CONFIG2	R/W	SW7_FLT_REN	—	—	SW7ILIM[1:0]		SW7PHASE[2:0]		
7F	SW7 PWRUP	R/W	SW7_SEQ[7:0]							
80	SW7 MODE1	R/W	—	—	SW7_PDGRP[1:0]		SW7_STBY_MODE[1:0]		SW7_RUN_MODE[1:0]	
81	SW7 RUN VOLT	R/W	—	—	—	VSW7[4:0]				
85	LDO1 CONFIG1	R/W	LDO1_UV_BYPASS	LDO1_OV_BYPASS	LDO1_ILIM_BYPASS	LDO1_UV_STATE	LDO1_OV_STATE	LDO1_ILIM_STATE	LDO1_WDBYPASS	LDO1_PG_EN
86	LDO1 CONFIG2	R/W	LDO1_FLT_REN	LDO1_PDGRP[1:0]		—	—	—	LDO1_RUN_EN	LDO1_STBY_EN
87	LDO1 PWRUP	R/W	LDO1_SEQ[7:0]							
88	LDO1 RUN VOLT	R/W	—	—	—	—	VLDO1_RUN[3:0]			
89	LDO1 STBY VOLT	R/W	—	—	—	—	VLDO1_STBY[3:0]			
8B	LDO2 CONFIG1	R/W	LDO2_UV_BYPASS	LDO2_OV_BYPASS	LDO2_ILIM_BYPASS	LDO2_UV_STATE	LDO2_OV_STATE	LDO2_ILIM_STATE	LDO2_WDBYPASS	LDO2_PG_EN
8C	LDO2 CONFIG2	R/W	LDO2_FLT_REN	LDO2_PDGRP[1:0]		LDO2HW_EN	VSELECT_EN	—	LDO2_RUN_EN	LDO2_STBY_EN
8D	LDO2 PWRUP	R/W	LDO2_SEQ[7:0]							
8E	LDO2 RUN VOLT	R/W	—	—	—	—	VLDO2_RUN[3:0]			
8F	LDO2 STBY VOLT	R/W	—	—	—	—	VLDO2_STBY[3:0]			
91	LDO3 CONFIG1	R/W	LDO3_UV_BYPASS	LDO3_OV_BYPASS	LDO3_ILIM_BYPASS	LDO3_UV_STATE	LDO3_OV_STATE	LDO3_ILIM_STATE	LDO3_WDBYPASS	LDO3_PG_EN
92	LDO3 CONFIG2	R/W	LDO3_FLT_REN	LDO3_PDGRP[1:0]		—	—	—	LDO3_RUN_EN	LDO3_STBY_EN
93	LDO3 PWRUP	R/W	LDO3_SEQ[7:0]							
94	LDO3 RUN VOLT	R/W	—	—	—	—	VLDO3_RUN[3:0]			
95	LDO3 STBY VOLT	R/W	—	—	—	—	VLDO3_STBY[3:0]			
97	LDO4 CONFIG1	R/W	LDO4_UV_BYPASS	LDO4_OV_BYPASS	LDO4_ILIM_BYPASS	LDO4_UV_STATE	LDO4_OV_STATE	LDO4_ILIM_STATE	LDO4_WDBYPASS	LDO4_PG_EN
98	LDO4 CONFIG2	R/W	LDO4_FLT_REN	LDO4_PDGRP[1:0]		—	—	—	LDO4_RUN_EN	LDO4_STBY_EN
99	LDO4 PWRUP	R/W	LDO4_SEQ[7:0]							
9A	LDO4 RUN VOLT	R/W	—	—	—	—	VLDO4_RUN[3:0]			
9B	LDO4 STBY VOLT	R/W	—	—	—	—	VLDO4_STBY[3:0]			
9D	VSNVS CONFIG1	R/W	—	—	—	—	—	—	VSNVSVOLT [1:0]	
9F	PAGE SELECT	R/TW	—	—	—	—	—	PAGE[2:0]		

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

16.4 PF8100 OTP mirror register map (page 1)

Reset types	
OFF_OTP	Register loads the OTP mirror register values during power up
OTP	Register available in OTP bank only, reset from fuses when VIN crosses UVDET threshold
VSNVS	Reset when BOS has no valid input. VIN < UVDET and coin cell < 1.8 V (VSNVS not present)

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
A0	OTP FSOB SELECT	—	—	—	—	OTP_FSOB_ SOFTFAULT	OTP_FSOB_WDI	OTP_FSOB_WDC	OTP_FSOB_ HARDFAULT
A1	OTP I2C	—	—	—	—	OTP_I2C_CRC_EN	OTP_I2C_ADD[2:0]		
A2	OTP CTRL1	—	—	OTP_EWARN_TIME[1:0]		—	OTP_STANDBYINV	OTP_PG_ACTIVE	OTP_PG_CHECK
A3	OTP CTRL2	OTP_FSS_EN	OTP_FSS_RANGE	—	OTP_XFAILB_EN	OTP_VIN_OVLO_ SDWN	OTP_VIN_OVLO_EN	OTP_VIN_OVLO_DBNC[1:0]	
A4	OTP CTRL3	OTP_VTT_PDOWN	OTP_SW6_VTTEN	OTP_SW5CONFIG[1:0]		OTP_SW4CONFIG[1:0]		OTP_SW1CONFIG[1:0]	
A5	OTP FREQ CTRL	OTP_SW_MODE	OTP_SYNCIN_EN	OTP_SYNCOUT_EN	OTP_FSYNC_ RANGE	OTP_CLK_FREQ[3:0]			
A6	OTP COINCELL CTRL	—	—	—	—	OTP_VCOIN[3:0]			
A7	OTP PWRON	—	—	OTP_PWRON_ MODE	OTP_PWRON_DBNC[1:0]		OTP_PWRON_ RST_EN	OTP_TRESET[1:0]	
A8	OTP WD CONFIG	—	—	OTP_WDI_MODE	OTP_WDI_INV	OTP_WD_EN	OTP_WD_STBY_EN	OTP_WDI_STBY_ ACTIVE	OTP_WDWINDOW
A9	OTP WD EXPIRE	—	—	—	—	—	OTP_WD_MAX_EXPIRE[2:0]		
AA	OTP WD COUNTER	OTP_WD_DURATION[3:0]				OTP_WD_MAX_CNT [3:0]			
AB	OTP FAULT COUNTERS	—	—	—	—	OTP_FAULT_MAX_CNT[3:0]			
AC	OTP FAULT TIMERS	—	—	—	—	OTP_TIMER_FAULT[3:0]			
AD	OTP PWRDN DLY1	OTP_GRP4_DLY[1:0]		OTP_GRP3_DLY[1:0]		OTP_GRP2_DLY[1:0]		OTP_GRP1_DLY[1:0]	
AE	OTP PWRDN DLY2	OTP_PD_SEQ_DLY[1:0]		—	—	—	—	OTP_RESETBMCU_DLY[1:0]	
AF	OTP PWRUP CTRL	—	OTP_PWRDWN_ MODE	OTP_PGOOD_PDGRP[1:0]		OTP_RESETBMCU_PDGRP[1:0]		OTP_SEQ_TBASE[1:0]	
B0	OTP RES ETBMCU PWRUP	OTP_RESETBMCU_SEQ[7:0]							
B1	OTP PGOOD PWRUP	OTP_PGOOD_SEQ[7:0]							
B2	OTP SW1 VOLT	OTP_VSW1[7:0]							
B3	OTP SW1 PWRUP	OTP_SW1_SEQ[7:0]							
B4	OTP SW1 CONFIG1	OTP_SW1UV_TH[1:0]		OTP_SW1OV_TH[1:0]		OTP_SW1_PDGRP[1:0]		OTP_SW1ILIM[1:0]	
B5	OTP SW1 CONFIG2	OTP_SW1_LSELECT[1:0]		OTP_SW1PHASE[2:0]			OTP_SW1DVS_RAMP	OTP_SW1_PG_EN	OTP_SW1_WDBYPASS
B6	OTP SW2 VOLT	OTP_VSW2[7:0]							
B7	OTP SW2 PWRUP	OTP_SW2_SEQ[7:0]							
B8	OTP SW2 CONFIG1	OTP_SW2UV_TH[1:0]		OTP_SW2OV_TH[1:0]		OTP_SW2_PDGRP[1:0]		OTP_SW2ILIM[1:0]	
B9	OTP SW2 CONFIG2	OTP_SW2_LSELECT[1:0]		OTP_SW2PHASE[2:0]			OTP_SW2DVS_RAMP	OTP_SW2_PG_EN	OTP_SW2_WDBYPASS
BA	OTP SW3_ VOLT	OTP_VSW3[7:0]							
BB	OTP SW3 PWRUP	OTP_SW3_SEQ[7:0]							

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BC	OTP SW3 CONFIG1	OTP_SW3UV_TH[1:0]		OTP_SW3OV_TH[1:0]		OTP_SW3_PDGRP[1:0]		OTP_SW3ILIM[1:0]	
BD	OTP SW3 CONFIG2	OTP_SW3_LSELECT[1:0]		OTP_SW3PHASE[2:0]			OTP_SW3DVS_RAMP	OTP_SW3_PG_EN	OTP_SW3_WDBYPASS
BE	OTP SW4 VOLT	OTP_VSW4[7:0]							
BF	OTP SW4 PWRUP	OTP_SW4_SEQ[7:0]							
C0	OTP SW4 CONFIG1	OTP_SW4UV_TH[1:0]		OTP_SW4OV_TH[1:0]		OTP_SW4_PDGRP[1:0]		OTP_SW4ILIM[1:0]	
C1	OTP SW4 CONFIG2	OTP_SW4_LSELECT[1:0]		OTP_SW4PHASE[2:0]			OTP_SW4DVS_RAMP	OTP_SW4_PG_EN	OTP_SW4_WDBYPASS
C2	OTP SW5 VOLT	OTP_VSW5[7:0]							
C3	OTP SW5 PWRUP	OTP_SW5_SEQ[7:0]							
C4	OTP SW5 CONFIG1	OTP_SW5UV_TH[1:0]		OTP_SW5OV_TH[1:0]		OTP_SW5_PDGRP[1:0]		OTP_SW5ILIM[1:0]	
C5	OTP SW5 CONFIG2	OTP_SW5_LSELECT[1:0]		OTP_SW5PHASE[2:0]			OTP_SW5DVS_RAMP	OTP_SW5_PG_EN	OTP_SW5_WDBYPASS
C6	OTP SW6 VOLT	OTP_VSW6[7:0]							
C7	OTP SW6 PWRUP	OTP_SW6_SEQ[7:0]							
C8	OTP SW6 CONFIG1	OTP_SW6UV_TH[1:0]		OTP_SW6OV_TH[1:0]		OTP_SW6_PDGRP[1:0]		OTP_SW6ILIM[1:0]	
C9	OTP SW6 CONFIG2	OTP_SW6_LSELECT[1:0]		OTP_SW6PHASE[2:0]			OTP_SW6DVS_RAMP	OTP_SW6_PG_EN	OTP_SW6_WDBYPASS
CA	OTP SW7 VOLT	—	—	—	OTP_VSW7[4:0]				
CB	OTP SW7 PWRUP	OTP_SW7_SEQ[7:0]							
CC	OTP SW7 CONFIG1	OTP_SW7UV_TH[1:0]		OTP_SW7OV_TH[1:0]		OTP_SW7_PDGRP[1:0]		OTP_SW7ILIM[1:0]	
CD	OTP SW7 CONFIG2	OTP_SW7_LSELECT[1:0]		OTP_SW7PHASE[2:0]			—	OTP_SW7_PG_EN	OTP_SW7_WDBYPASS
CE	OTP LDO1 VOLT	OTP_LDO1UV_TH[1:0]		OTP_LDO1OV_TH[1:0]		OTP_VLDO1[3:0]			
CF	OTP LDO1 PWRUP	OTP_LDO1_SEQ[7:0]							
D0	OTP LDO1 CONFIG	OTP_LDO1_PDGRP[1:0]		—	—	—	OTP_LDO1_PG_EN	OTP_LDO1_ WDBYPASS	OTP_LDO1LS
D1	OTP LDO2 VOLT	OTP_LDO2UV_TH[1:0]		OTP_LDO2OV_TH[1:0]		OTP_VLDO2[3:0]			
D2	OTP LDO2 PWRUP	OTP_LDO2_SEQ[7:0]							
D3	OTP LDO2 CONFIG	OTP_LDO2_PDGRP[1:0]		OTP_VSELECT_EN	OTP_LDO2HW_EN	—	OTP_LDO2_PG_EN	OTP_LDO2_ WDBYPASS	OTP_LDO2LS
D4	OTP LDO3 VOLT	OTP_LDO3UV_TH[1:0]		OTP_LDO3OV_TH[1:0]		OTP_VLDO3[3:0]			
D5	OTP LDO3 PWRUP	OTP_LDO3_SEQ[7:0]							
D6	OTP LDO3 CONFIG	OTP_LDO3_PDGRP[1:0]		—	—	—	OTP_LDO3_PG_EN	OTP_LDO3_ WDBYPASS	OTP_LDO3LS
D7	OTP LDO4 VOLT	OTP_LDO4UV_TH[1:0]		OTP_LDO4OV_TH[1:0]		OTP_VLDO4[3:0]			
D8	OTP LDO4 PWRUP	OTP_LDO4_SEQ[7:0]							
D9	OTP LDO4 CONFIG	OTP_LDO4_PDGRP[1:0]		—	—	—	OTP_LDO4_PG_EN	OTP_LDO4_ WDBYPASS	OTP_LDO4LS
DA	OTP VSNVS CONFIG	—	—	—	—	—	—	VSNVSVOLT [1:0]	
DB	OTP_OV_ BYPASS1	—	OTP_SW7_ OVBYPASS	OTP_SW6_ OVBYPASS	OTP_SW5_ OVBYPASS	OTP_SW4_ OVBYPASS	OTP_SW3_ OVBYPASS	OTP_SW2_ OVBYPASS	OTP_SW1_OVBYPASS
DC	OTP_OV_ BYPASS2	—	—	—	—	OTP_LDO4_ OVBYPASS	OTP_LDO3_ OVBYPASS	OTP_LDO2_ OVBYPASS	OTP_LDO1_ OVBYPASS

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DD	OTP_UV_BYPASS1	—	OTP_SW7_UVBYPASS	OTP_SW6_UVBYPASS	OTP_SW5_UVBYPASS	OTP_SW4_UVBYPASS	OTP_SW3_UVBYPASS	OTP_SW2_UVBYPASS	OTP_SW1_UVBYPASS
DE	OTP_UV_BYPASS2	—	—	—	—	OTP_LDO4_UVBYPASS	OTP_LDO3_UVBYPASS	OTP_LDO2_UVBYPASS	OTP_LDO1_UVBYPASS
DF	OTP_ILIM_BYPASS1	—	OTP_SW7_ILIMBYPASS	OTP_SW6_ILIMBYPASS	OTP_SW5_ILIMBYPASS	OTP_SW4_ILIMBYPASS	OTP_SW3_ILIMBYPASS	OTP_SW2_ILIMBYPASS	OTP_SW1_ILIMBYPASS
E0	OTP_ILIM_BYPASS2	—	—	—	—	OTP_LDO4_ILIMBYPASS	OTP_LDO3_ILIMBYPASS	OTP_LDO2_ILIMBYPASS	OTP_LDO1_ILIMBYPASS
E3	OTP DEBUG1	—	—	—	—	—	—	—	BGMOM_BYPASS

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

17 OTP/TBB and default configurations

The PF8100/PF8200 supports OTP fuse bank configuration and a predefined hardwire configurations to select the default power up configuration via the VDDOTP pin.

The default power up configuration is loaded into the functional I^2C registers based on the voltage on VDDOTP pin on register loading.

- If VDDOTP = GND, the device loads the configuration from the OTP mirror registers.
- If VDDOTP = V1P5D, the device loads the configuration from the default hardwire configuration.

When OTP configuration is selected, the register loading occurs in two stages:

- In the first stage, the fuses are loaded in the OTP Mirror registers every time VIN crosses the UVDET threshold in the rising edge.
- At the second stage, data from the mirror registers are loaded into the functional I^2C registers for device operation.

When VDDOTP = GND, the mirror registers hold the default configuration to be used on a power-on event. The mirror registers can be modified during the TBB mode in order to test a custom power up configuration and/or burn the configuration into the OTP fuses to generate a customized default power up configuration.

When VDDOTP = V1P5D, the I^2C functional register will always be loaded from the hardwire configuration every time a default loading is required. Therefore, no TBB operation is possible in this configuration.

In the event of a TRIM/OTP loading failure or a self-test failure, the corresponding fault flag is set and any PWRUP event is ignored until the flags are cleared by writing a 1 during the QPU_OFF state.

The TRIM_NOK, OTP_NOK and STEST_NOK flags can only be written when the TBBEN is set high (in TBB Mode). In normal operation, the TRIM_NOK, OTP_NOK and STEST_NOK flags can only be read, but not cleared.

17.1 TBB (Try Before Buy) operation

The PF8100/PF8200 allows temporary configuration (TBB) to debug or test a customized power up configuration in the system. In order to access the TBB mode, the TBBEN pin should be set high .

In this mode of operation, the device ignores the default value of the LPM_OFF bit and moves into the QPU_Off state, regardless of the result of the self-test. However, the actual result of the self-test is notified by the STEST_NOK flag.

- When the self-test is successful the STEST_NOK flag is set to 0
- When the self-test has failed, the STEST_NOK flag is set to 1

In the TBB mode, the following conditions are valid:

- I^2C communication uses standard communication with no CRC and secure write disabled.
- Default I^2C address is 0x08 regardless of the address configured by OTP.
- Watchdog monitoring is disabled (including WDI and internal watchdog timer).
- The PF8100/PF8200 can communicate through I^2C as long as V_{DDIO} is provided to the PMIC externally.

The PAGE[2:0] bits are provided to grant access to the mirror registers and other OTP dedicated bits. When device is in the TBB mode, it can access the mirror registers in the extended register Page 1. With the TBBEN pin pulled low, access to the extended register pages is not allowed.

The mirror registers are preloaded with the values form the OTP configuration. These may be modified to set the proper power up configuration during TBB operation.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

If a power up event is present with the TBBEN pin set high, device will power up with the proper configuration but limited functionality.

Limited functionality includes:

- Default I^2C address = 0x08
- CRC and secure write disabled
- Watchdog operation/monitoring disable

In order to allow TBB operation with full functionality, the TBBEN pin must be low when the power up event occurs.

The PF8100/PF8200 can operate normally using the TBB configuration, as long as VIN does not go below the UVDET threshold. If VIN is lost (VIN < UVDET) the mirror register will be reset and TBB configuration must be performed again.

17.2 OTP fuse programming

A permanent OTP configuration is possible by burning the OTP fuses. OTP fuse burning is performed in the TBBEN mode during the QPU_Off state. Contact your NXP representative for detailed information on OTP fuse programming.

17.3 Default hardwire configuration

If VDDOTP = V1P5D, the device loads the configuration from the default hardwire configuration directly into the corresponding I^2C functional registers every time the registers need to be reloaded.

When using the hardwire configuration, the TRIM values are still loaded from the OTP fuses. In the event of a TRIM loading failure, the corresponding fault flag is set to 1.

When the hardwire configuration is used, the PF8100/PF8200 does not allow TBB mode operation. When TBBEN = V1P5D, the device enters a debug mode. In this mode of operation, the device ignores the default value of the LPM_OFF bit and moves into the QPU_Off state, regardless of the result of the self-test. However, the actual result of the self-test is notified by the STEST_NOK flag.

- When the self-test is successful, the STEST_NOK flag is set to 0
- When the self-test has failed, the STEST_NOK flag is set to 1

During hardwire configuration, the OTP_NOK flag is always set to 0.

When any of the TRIM_NOK, OTP_NOK or STEST_NOK flags is set, any PWRUP event is ignored until the flags are cleared by writing a 0. These flags can only be written when the system is in the debug mode, (TBBEN = V1P5D). In normal operation, the TRIM_NOK, OTP_NOK and STEST_NOK flags are read only.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

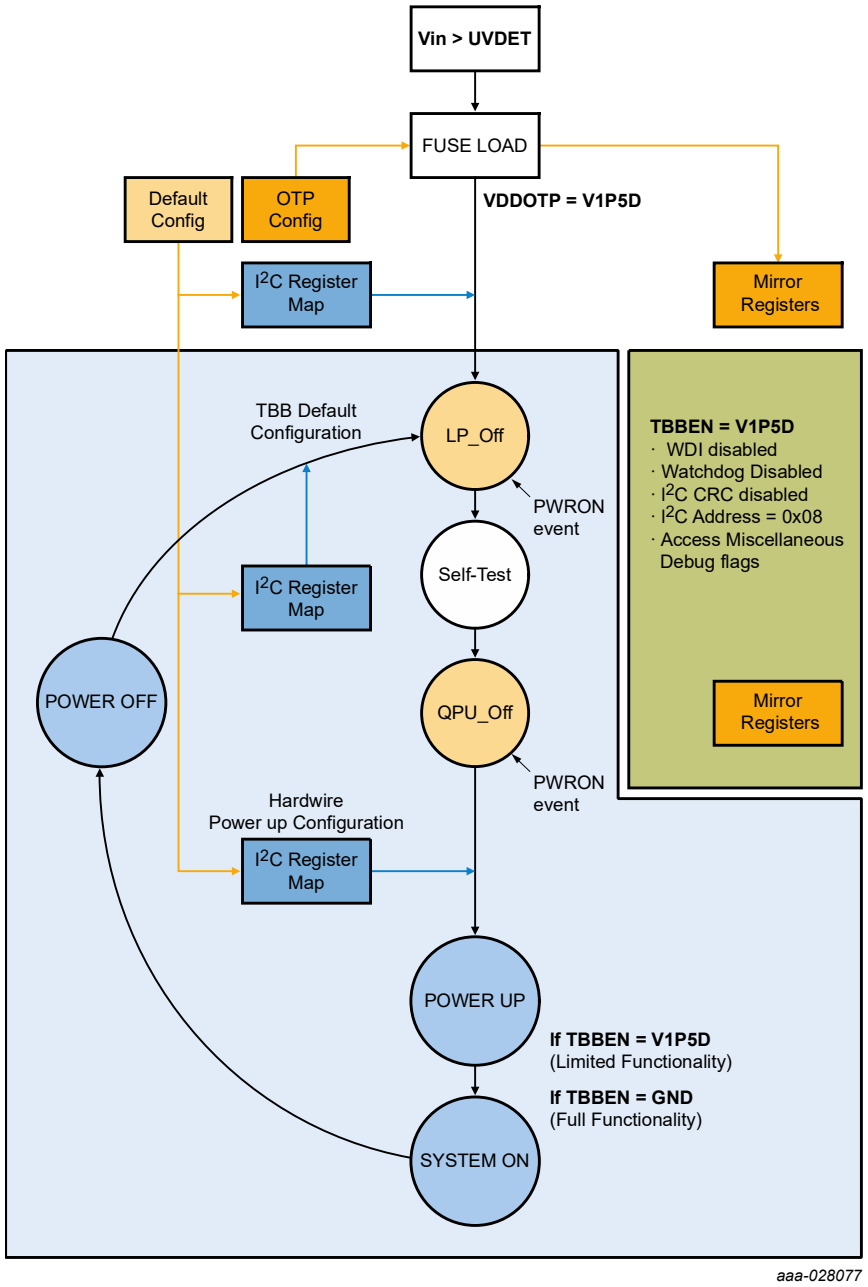


Figure 39. Hardwire operation diagram

For simplicity, the default hardwire configuration in PF8100/PF8200 is organized based on the OTP register map as shown in Table 78.

Table 78. Default hardwire configuration

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
A0	OTP FSOB SELECT	0	0	0	0	0	0	0	0	*Active Safe State disabled* | FSOB pin not used
A1	OTP I2C	0	0	0	0	0	0	0	0	*Secured I2C disabled* | I2C CRC disabled | I2C address = 0x08
A2	OTP CTRL1	0	0	0	0	0	0	1	0	*100 µs EWARN* | *Fail-safe State enabled* | STANDBY active high | PGOOD indicator | PG not Check on power up
A3	OTP CTRL2	0	0	0	0	0	1	0	1	FSS disabled | FSS Range = 5 % | XFAILB Disabled | VIN_OVLO shutdown disabled | VIN_OVLO enabled | VIN_OVLO debounce = 100 µs
A4	OTP CTRL3	0	0	0	0	0	0	0	1	VTT Hi-Z off | Single phase: SW6, SW5, SW4, SW3 | Dual phase: SW1/SW2

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 78. Default hardwire configuration*...continued*

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
A5	OTP FREQ CTRL	0	0	0	0	0	0	0	0	SWx in APS | SYNCIN = Disabled | SYNCOUT disabled | SYNCIN range = 2 MHz – 3 MHz | CLK Frequency = 2.5 MHz
A6	OTP COINCELL CTRL	0	0	0	0	1	0	1	1	VCOIN = 3.0 V
A7	OTP PWRON	0	0	0	0	0	0	0	0	PWRON = Level sensitive
A8	OTP WD CONFIG	0	0	0	1	0	0	0	0	WDI generates soft WD reset | WDI detect on rising edge | WD timer disabled | WD Timer in standby disabled |WDI detect in standby disabled | WD windows = 100 %
A9	OTP WD EXPIRE	0	0	0	0	0	1	1	1	Max WD expire count = 8
AA	OTP WD COUNTER	1	0	1	0	1	1	1	1	WD duration = 1024 ms | Max WD count = 16
AB	OTP FAULT COUNTERS	1	1	1	1	1	1	1	1	*Fail Safe MAX counter = 16* | Regulator fault max counter = 16
AC	OTP FAULT TIMERS	0	0	0	0	1	1	1	1	*Fail safe OK timer = 1 minute* | Regulator fault timer = Disabled
AD	OTP PWRDN DLY1	0	0	0	0	0	0	0	0	GRP4 delay = 125 µs | GRP 3 delay = 125 µs | GRP 2 delay = 125 µs | GRP 1 delay = 125 µs
AE	OTP PWRDN DLY2	0	0	0	0	0	0	0	1	No power down delay | RESETBMCU delay = 10 µs
AF	OTP PWRUP CTRL	0	0	0	0	0	0	1	0	PD mirror sequence | RESETBMCU PD Group2 | TBASE = 250 µs
B0	OTP RESETBMCU PWRUP	0	0	0	0	0	1	1	1	RESETBMCU SEQ = Slot 6
B1	OTP PGOOD PWRUP	0	0	0	0	0	0	0	0	PGOOD SEQ = OFF
B2	OTP SW1 VOLT	0	1	1	0	0	0	0	0	Voltage = 1.0 V
B3	OTP SW1 PWRUP	0	0	0	0	0	0	0	1	SEQ = Slot 0
B4	OTP SW1 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM typ 4.5 A
B5	OTP SW1 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
B6	OTP SW2 VOLT	0	1	1	0	0	0	0	0	Voltage = 1.0 V
B7	OTP SW2 PWRUP	0	0	0	0	0	0	0	1	SEQ = Slot 0
B8	OTP SW2 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM typ 4.5 A
B9	OTP SW2 CONFIG2	0	0	0	1	1	1	1	0	L = 1 µH | Phase = 180º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
BA	OTP SW3_VOLT	0	1	1	1	0	0	0	0	Voltage = 1.1 V
BB	OTP SW3 PWRUP	0	0	0	0	0	1	0	1	SEQ = Slot 4
BC	OTP SW3 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 4.5 A
BD	OTP SW3 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
BE	OTP SW4 VOLT	0	1	1	1	0	0	0	0	Voltage = 1.1 V
BF	OTP SW4 PWRUP	0	0	0	0	0	1	0	1	SEQ = Slot 4
C0	OTP SW4 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 4.5 A
C1	OTP SW4 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
C2	OTP SW5 VOLT	0	1	1	1	0	0	0	0	Voltage = 1.1 V
C3	OTP SW5 PWRUP	0	0	0	0	0	0	1	1	SEQ = Slot 2 (TBASE x 2 = 500 µs)
C4	OTP SW5 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 4.5 A
C5	OTP SW5 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/us | PG = EN | WDBYPASS = Disable
C6	OTP SW6 VOLT	1	0	1	1	0	0	0	1	Voltage = 1.8 V
C7	OTP SW6 PWRUP	0	0	0	0	0	0	1	1	SEQ = Slot 2 (TBASE x 2 = 500 µs)
C8	OTP SW6 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 4.5 A
C9	OTP SW6 CONFIG2	0	0	1	1	1	1	1	0	L = 1 µH | Phase = 0º | DVS Ramp = 12.5 mV/µs | PG = EN | WDBYPASS = Disable
CA	OTP SW7 VOLT	0	0	0	1	0	1	0	1	Voltage = 3.3 V
CB	OTP SW7 PWRUP	0	0	0	0	0	0	1	1	SEQ = Slot 2 (TBASE x 2 = 500 µs)
CC	OTP SW7 CONFIG1	0	1	0	1	0	0	1	1	UV mon = 7 % | OV mon = 7 % | SW PD Group4 | ILIM min 4.5 A
CD	OTP SW7 CONFIG2	0	0	1	1	1	0	1	0	L = 1 µH | Phase = 0º | PG = EN | WDBYPASS = Disable
CE	OTP LDO1 VOLT	0	1	0	1	0	0	0	1	Voltage = 1.8 V
CF	OTP LDO1 PWRUP	0	0	0	0	0	0	0	1	SEQ = Slot 0
D0	OTP LDO1 CONFIG	0	0	0	0	0	1	0	0	LDO PD Group 4 | PG = EN | WDBYPASS = Disable | LDO Mode

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 78. Default hardwire configuration*...continued*

ADDR	Register name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Configuration
D1	OTP LDO2 VOLT	0	1	0	1	1	0	1	1	Voltage = 3.3 V
D2	OTP LDO2 PWRUP	0	0	0	0	0	0	1	1	SEQ = Slot 2 (TBASE x 2 = 500 µs)
D3	OTP LDO2 CONFIG	0	0	1	1	0	1	0	0	LDO PD Group 4 | VSELECT = EN | LDO2HW = EN | PG = EN | WDBYPASS = Disable | LDO Mode
D4	OTP LDO3 VOLT	0	1	0	1	1	0	1	1	Voltage = 3.3 V
D5	OTP LDO3 PWRUP	0	0	0	0	0	0	0	0	SEQ = OFF
D6	OTP LDO3 CONFIG	0	0	0	0	0	1	0	0	LDO PD Group 4 | PG = EN | WDBYPASS = Disable | LDO Mode
D7	OTP LDO4 VOLT	0	1	0	1	1	0	1	1	Voltage = 3.3 V
D8	OTP LDO4 PWRUP	0	0	0	0	0	0	0	0	SEQ = OFF
D9	OTP LDO4 CONFIG	0	0	0	0	0	1	0	0	LDO PD Group 4 | PG = EN | WDBYPASS = Disable | LDO Mode
DA	OTP VSNVS CONFIG	0	0	0	0	0	0	1	0	Voltage = 3.0 V
DB	OTP OV BYPASS1	0	0	0	0	0	0	0	0	OV bypass disabled on all SW regulators
DC	OTP OV BYPASS2	0	0	0	0	0	0	0	0	OV bypass disabled on all LDO regulators
DD	OTP UV BYPASS1	0	0	0	0	0	0	0	0	UV bypass disabled on all SW regulators
DE	OTP UV BYPASS2	0	0	0	0	0	0	0	0	UV bypass disabled on all LDO regulators
DF	OTP ILIM BYPASS1	0	0	0	0	0	0	0	0	ILIM bypass disabled on all SW regulators
E0	OTP ILIM BYPASS2	0	0	0	0	0	0	0	0	ILIM bypass disabled on all LDO regulators
E1	OTP PROG IDH	0	0	0	0	1	1	1	1	Prog ID = 0xFFF
E2	OTP PROG IDL	1	1	1	1	1	1	1	1	Prog ID = 0xFFF

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

18 Functional safety

18.1 System safety strategy

The PF8200 is defined in a context of safety and shall provide a set of features to achieve the safety goals on such context. It provides a flexible yet complete safety architecture to comply with ASILB systems providing full programmability to enable or disable features to address the safety goal. This architecture includes protective mechanisms to avoid unwanted modification on the respective safety features, as required by the system.

The following are features considered to be critical for the functional safety strategy:

- Internal watchdog timer
- External watchdog monitoring input (WDI)
- Fail -safe output (FSOB)
- Output voltage monitoring with dedicated bandgap reference
- Protected I^2C protocol with CRC verification
- Input overvoltage protection
- Analog built-in self-test (ABIST)

18.2 Output voltage monitoring with dedicated bandgap reference

For the type 2 buck regulator and LDOs, the OV/UV monitors operate from a dedicated bandgap reference for voltage monitoring.

For the type 1 buck regulators, the OV/UV monitor operate from the same reference as the regulator. To ensure the integrity of the type 1 buck regulators, a comparison between the regulator bandgap and the monitoring bandgap is performed. A 4 % to 12 % difference between the two bandgaps is an indicator of a potential regulation or monitoring fault and is considered as a critical issue. Therefore, the device prevents the switching regulators from powering up.

In PF8200, if a bandgap error is detected during a power up event, the self-test will fail and prevent the device from powering up regardless of the value of the OTP_BGMON_BYPASS bit.

During system-on states a drift between the two bandgaps is detected:

- when OTP_BGMON_BYPASS = 0, the power stage of the voltage regulators will be shutdown
- when OTP_BGMON_BYPASS = 1, the bandgap monitor only sends an interrupt to the system to announce the bandgap failure

The BGMON_I is asserted when a bandgap failure occurs, provided it is not masked.

The BGMON_S bit is set to 0 when the bandgaps are within range, and set to 1 when the bandgaps are out of range.

18.3 ABIST verification

The PF8200 implements an ABIST verification of all output voltage monitors. The ABIST verification on the output voltage monitoring behaves as follows:

- Device test the OV comparators for each individual SWx and LDOx supply during the self-test routine
- Device test the UV comparators for each individual SWx and LDOx supply during the self-test routine
- During the ABIST verification, it is required to ensure the corresponding OV/UV comparators are able to toggle, which in turn is a sign of the integrity of these functions
- If any of the comparators is not able to toggle, a warning bit is set on the I^2C register map:
  - The ABIST_OV1 register contain the AB_SWx_OV bits for all external regulators

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

  - The ABIST_OV2 register contain the AB_LDOx_OV bits for all external regulators
  - The ABIST_UV1 register contain the AB_SWx_UV bits for all external regulators
  - The ABIST_UV2 register contain the AB_LDOx_UV bits for all external regulators
- The ABIST registers are cleared or overwritten every time the ABIST check is performed
- The ABIST registers are part of the secure registers and will require an I^2C secure write to be cleared if this feature is enabled.

Once ABIST check is performed, the PF8200 can proceed with the power up sequence and the MCU should be able to request the value of these registers and learn if ABIST failed for any of the voltage monitors.

The AB_RUN bit is provided to perform an ABIST verification on demand.

When the AB_RUN bit is set to 1, the control logic performs an ABIST verification on all OV/UV monitoring circuits. When the ABIST verification is finished, the AB_RUN bit self-clear to 0 and a new ABIST verification can be commanded as needed.

When the secure write feature is enabled, the system must perform a secure write sequence in order to start an ABIST verification on demand.

When the PF8200 performs an ABIST verification on demand, the OV/UV fault monitoring is blanked for a maximum period of 200 µs. During this time, the system must ensure it is in a safe state, or it is safe to perform this action without violating the safety goals of the system.

If a failure on the OV/UV monitor is detected during the ABIST on demand request, the PMIC will assert the corresponding ABIST flags. It is responsibility of the system to perform a diagnostic check after each ABIST verification to ensure it places the system in safe state if an ABIST fault is detected.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

19 IC level quiescent current requirements

Table 79. Quiescent current requirements

All parameters are specified at T_A = −40 to 105 °C, unless otherwise noted. Typical values are characterized at V_{IN} = 5.0 V and T_A = 25 °C, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
I_{LICELL}	Coin cell mode VIN < UVDET VSNVS = 3.0 V or 3.3 V	—	1.0	3.0	µA
I_{LICELL}	Coin cell mode VIN < UVDET VSNVS = 1.8 V	—	5.0	7.0	µA
I_{LPOFF}	LP_Off state LPM_OFF = 0 VIN > UVDET VSNVS = ON	—	40	150	µA
I_{QPUOFF}	QPU_Off LPM_OFF = 1 System ready to power on	—	750	1000	µA
I_{SYSON}	System on core current Run or standby and all regulators disabled Coin cell charger disabled AMUX disabled	—	750	1000	µA
I_{FSAFE}	Fail-safe mode VIN > UVDET VSNVS = ON	—	40	150	µA

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

20 Typical applications

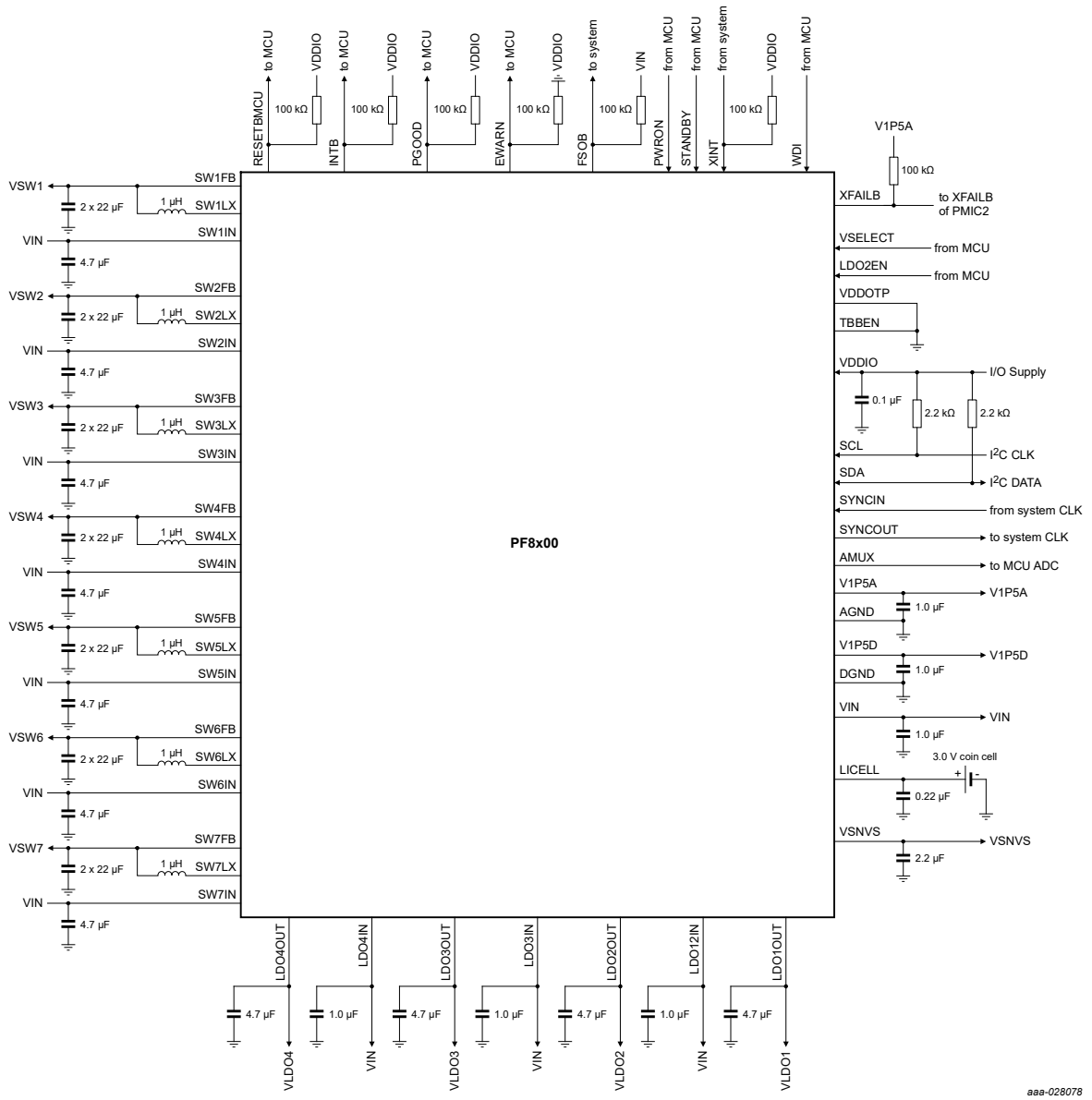


Figure 40. Typical application diagram

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21 Package information

21.1 Package outline for step-cut WF-type HVQFN56 (Automotive grade)

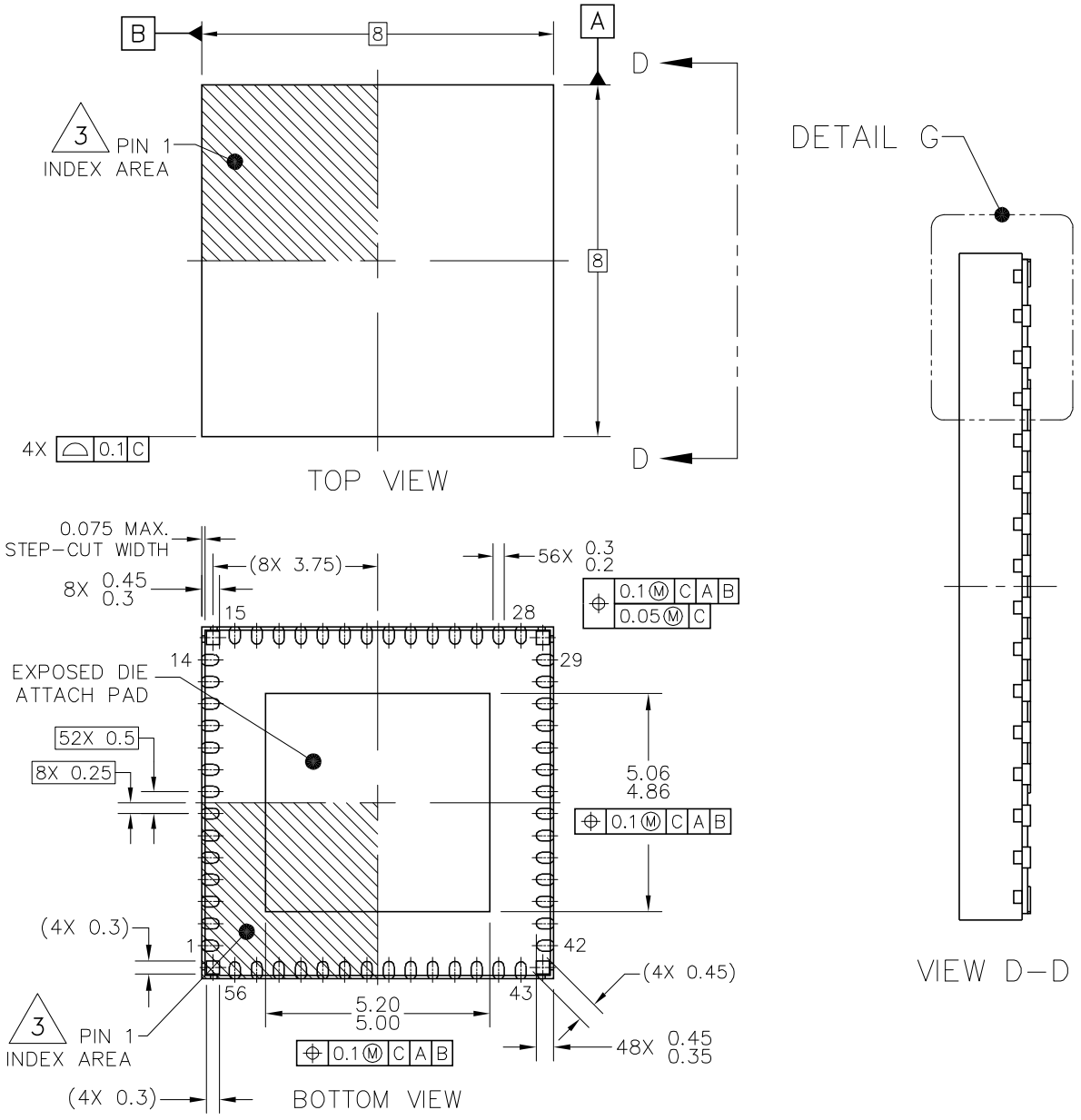


Figure 41. Package outline for WF-type HVQFN56 (Automotive grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

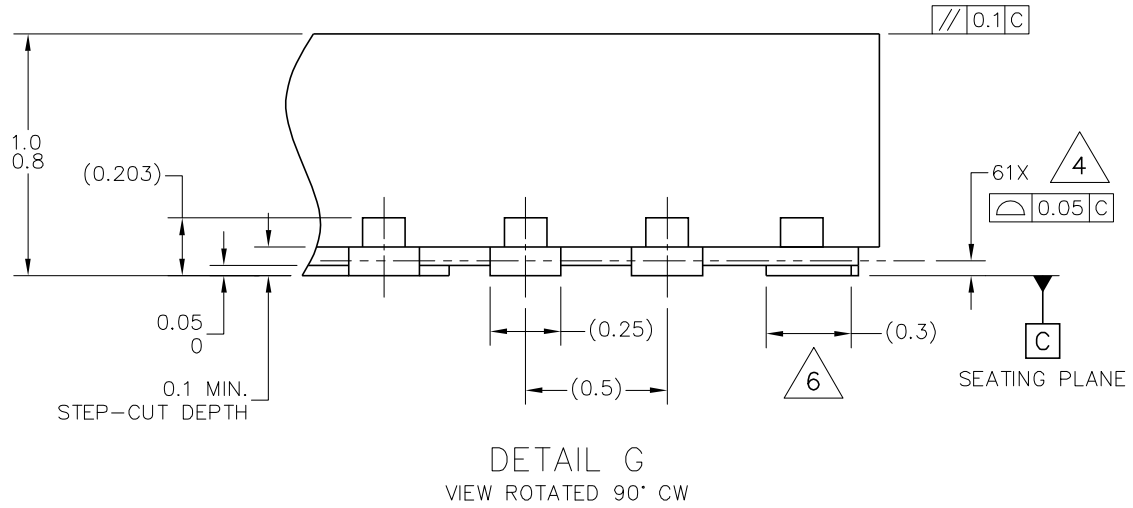


Figure 42. Package outline detail for WF-type HVQFN56 (Automotive grade)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN ONE CONFIGURATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 43. Package outline notes for WF-type HVQFN56 (Automotive grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21.2 PCB design guidelines for step-cut WF-type HVQFN56

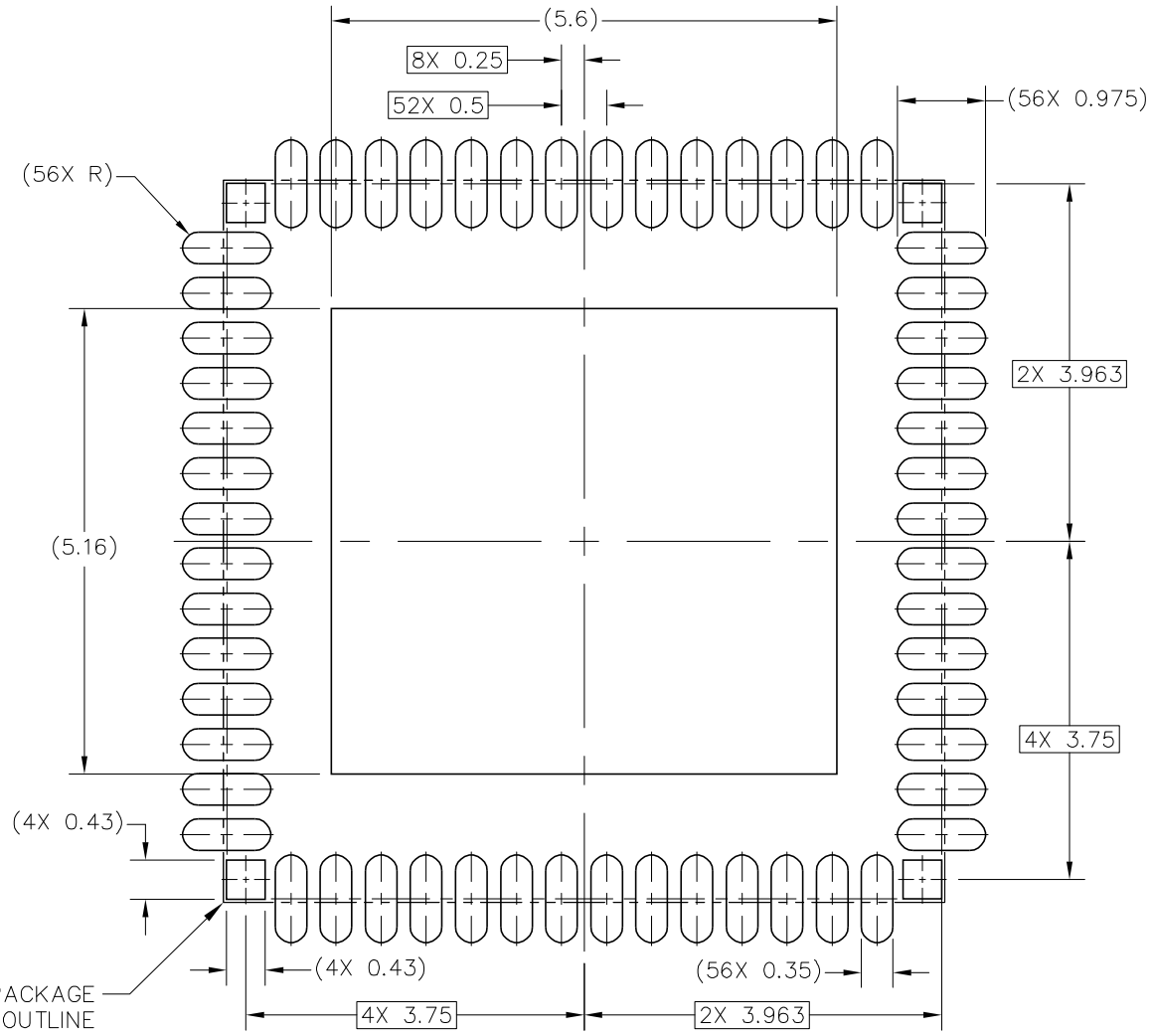


Figure 44. Solder mask pattern for WF-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

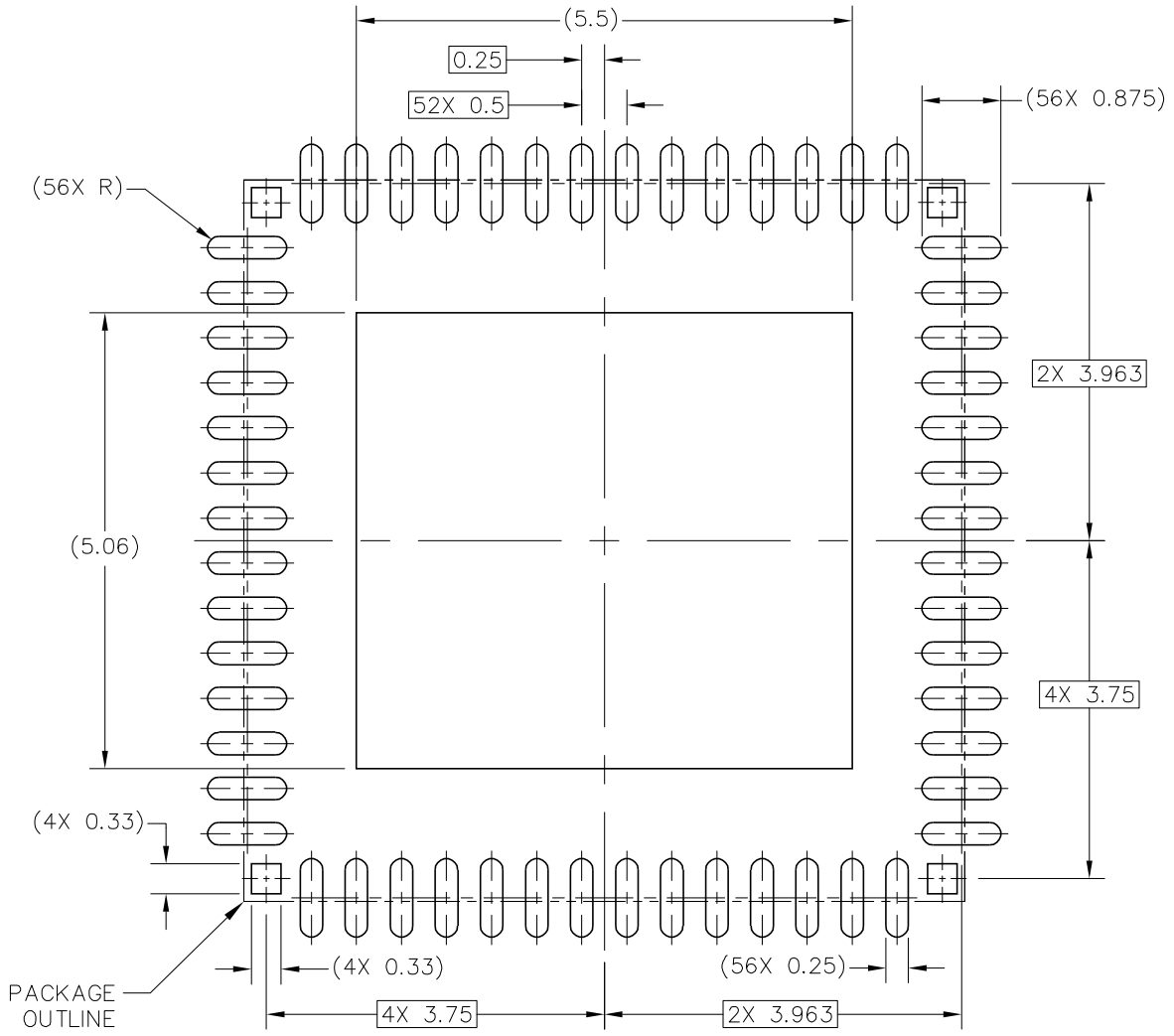


Figure 45. I/O pads and solderable areas for WF-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

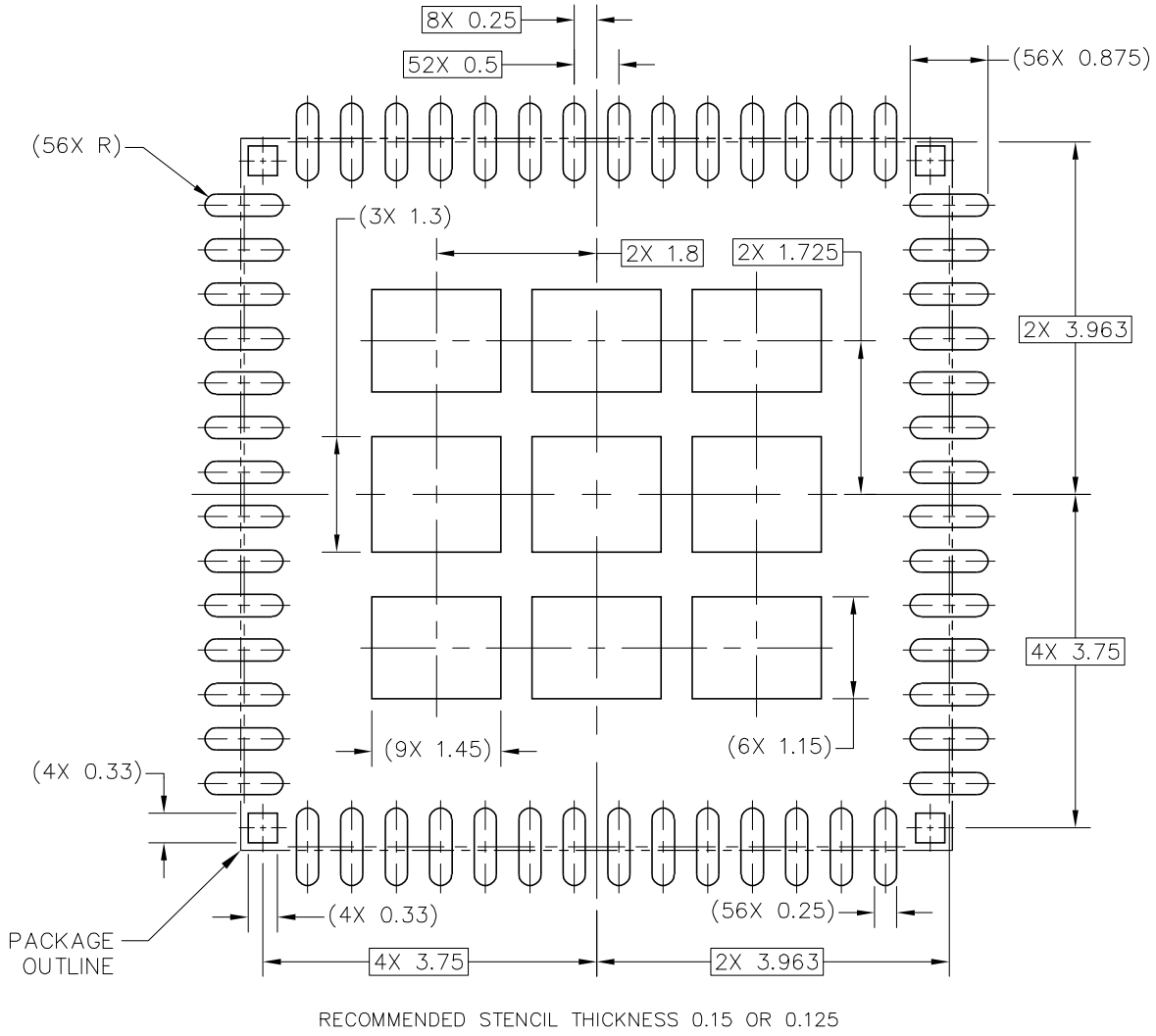


Figure 46. Solder paste stencil for WF-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21.3 Package outline for E-type HVQFN56 (Industrial grade)

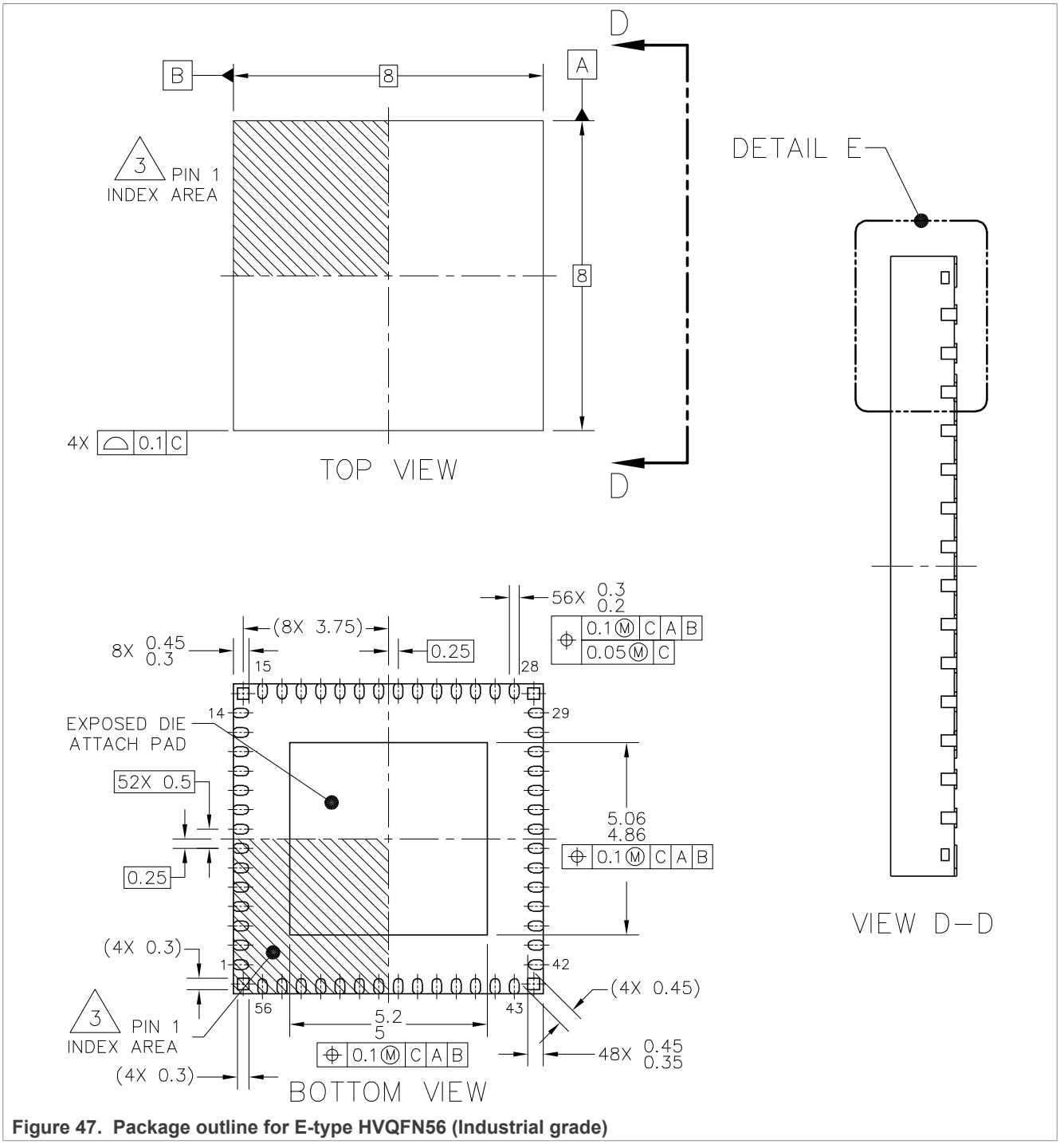


Figure 47. Package outline for E-type HVQFN56 (Industrial grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

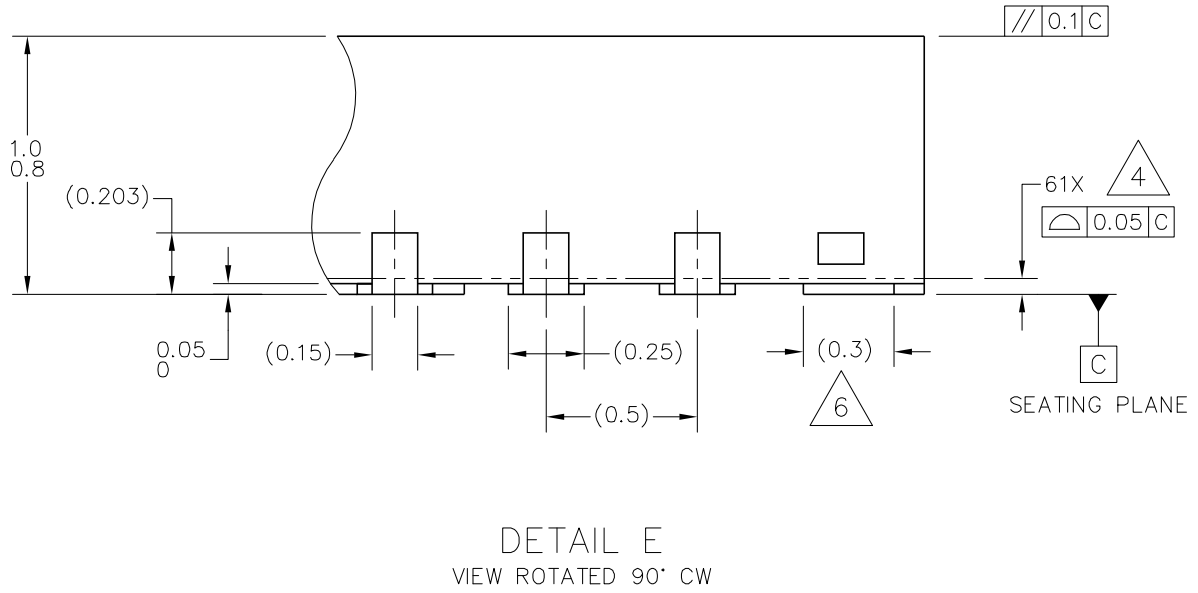


Figure 48. Package outline detail for E-type HVQFN56 (Industrial grade)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

Figure 49. Package outline notes for E-type HVQFN56 (Industrial grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21.4 PCB design guidelines for E-type HVQFN56

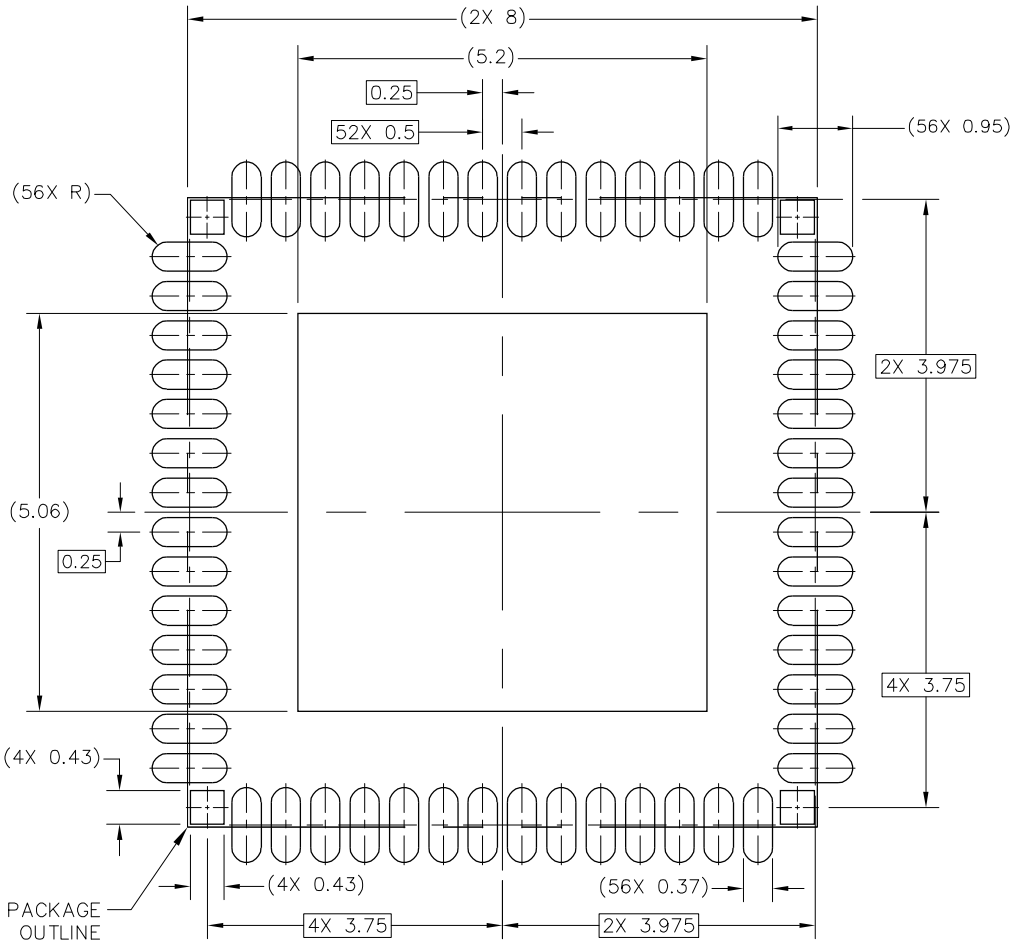


Figure 50. Solder mask pattern for E-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

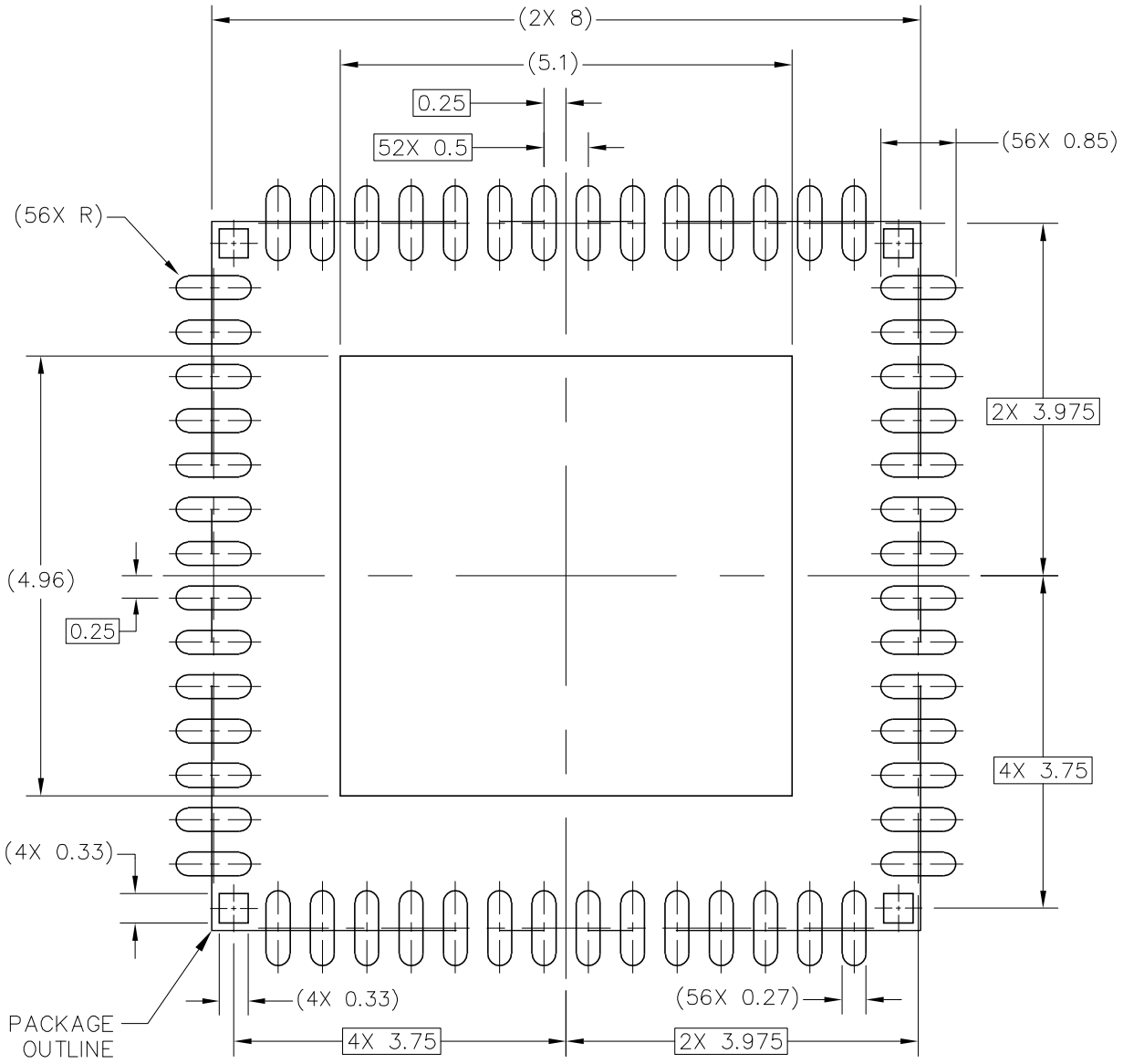


Figure 51. I/O pads and solderable areas for E-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

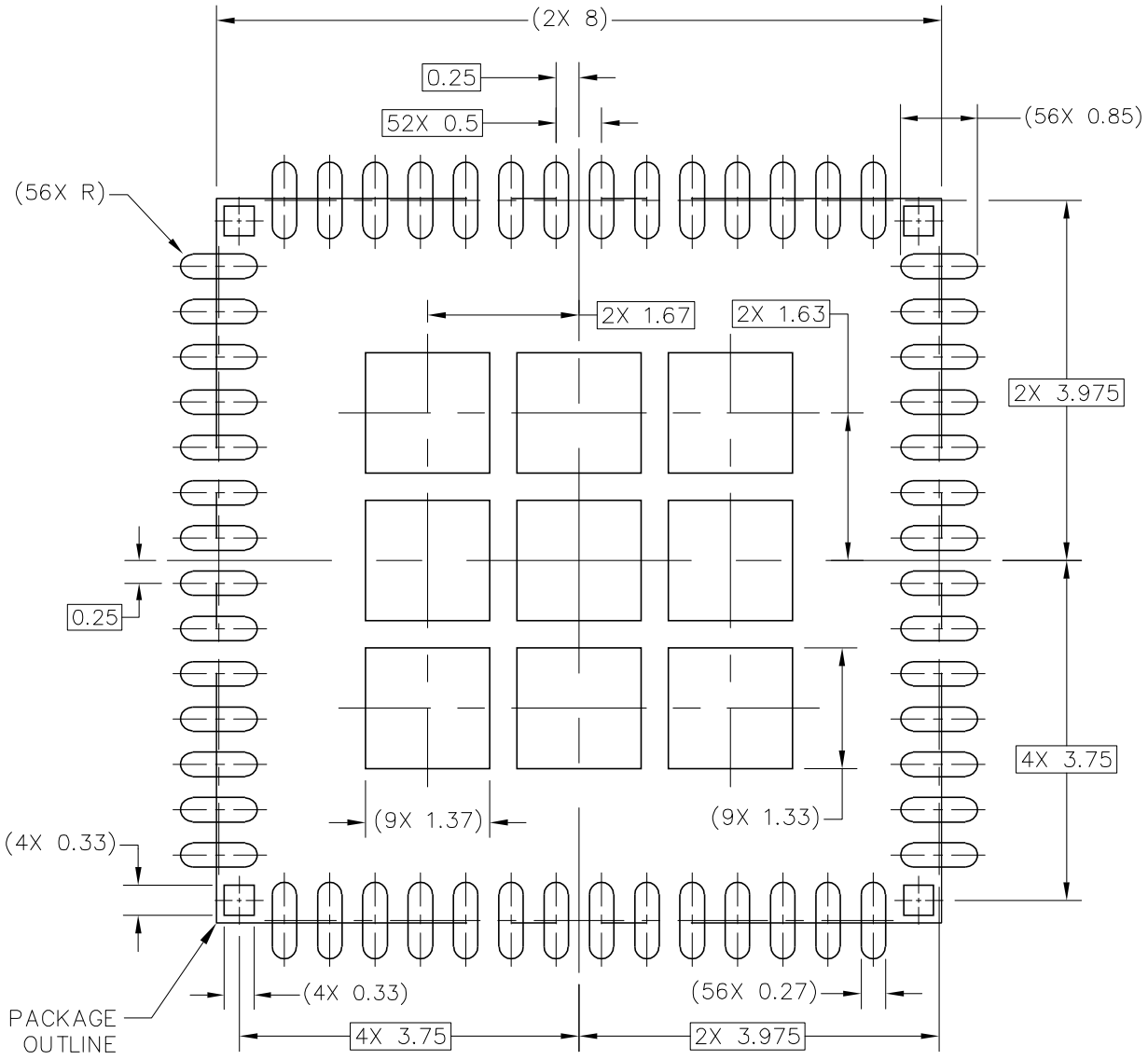


Figure 52. Solder paste stencil for E-type HVQFN56

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21.5 Package outline for dimple WF-type HVQFN56 (automotive/industrial grade)

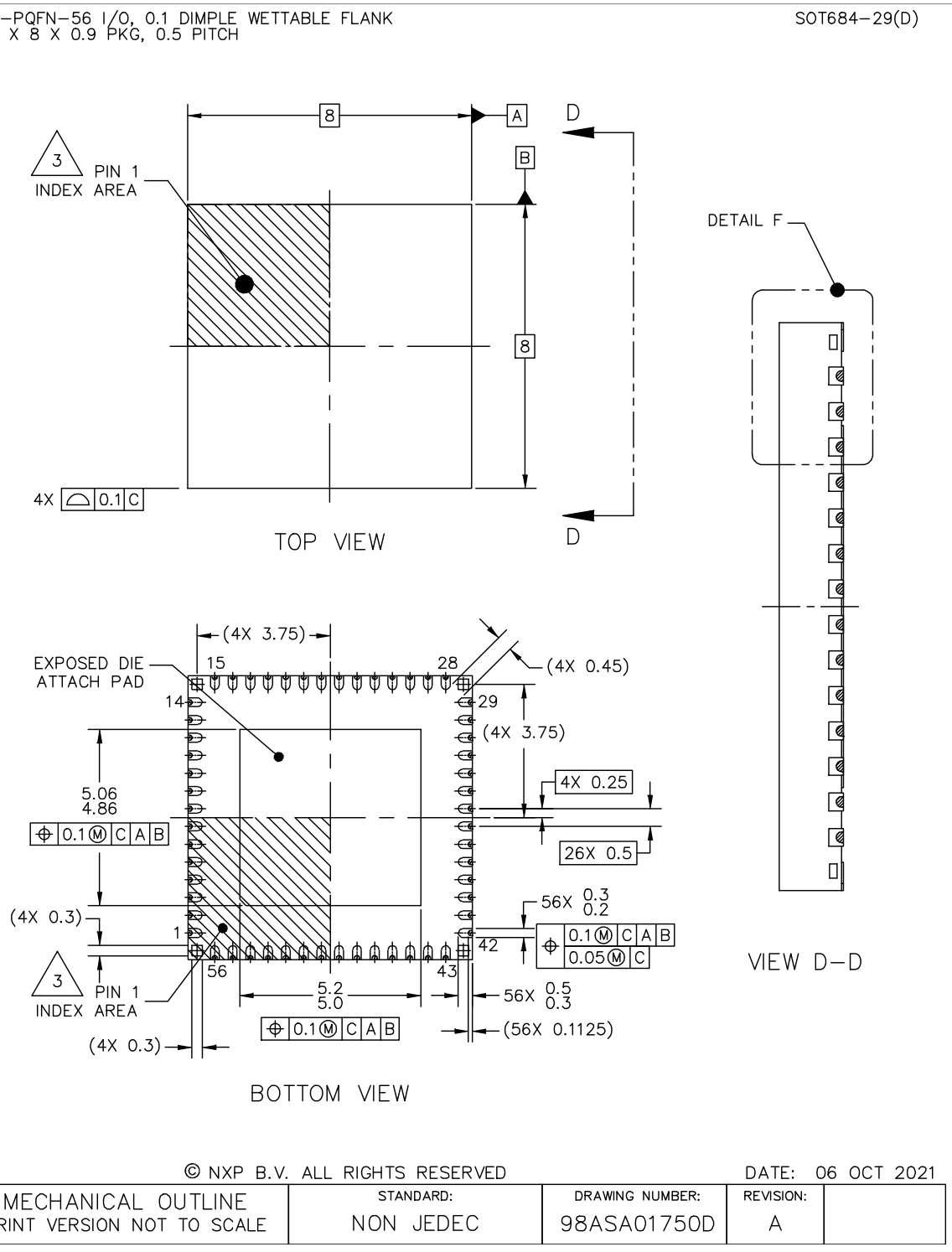


Figure 53. Package outline for dimple WF-type HVQFN56 (automotive/industrial grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

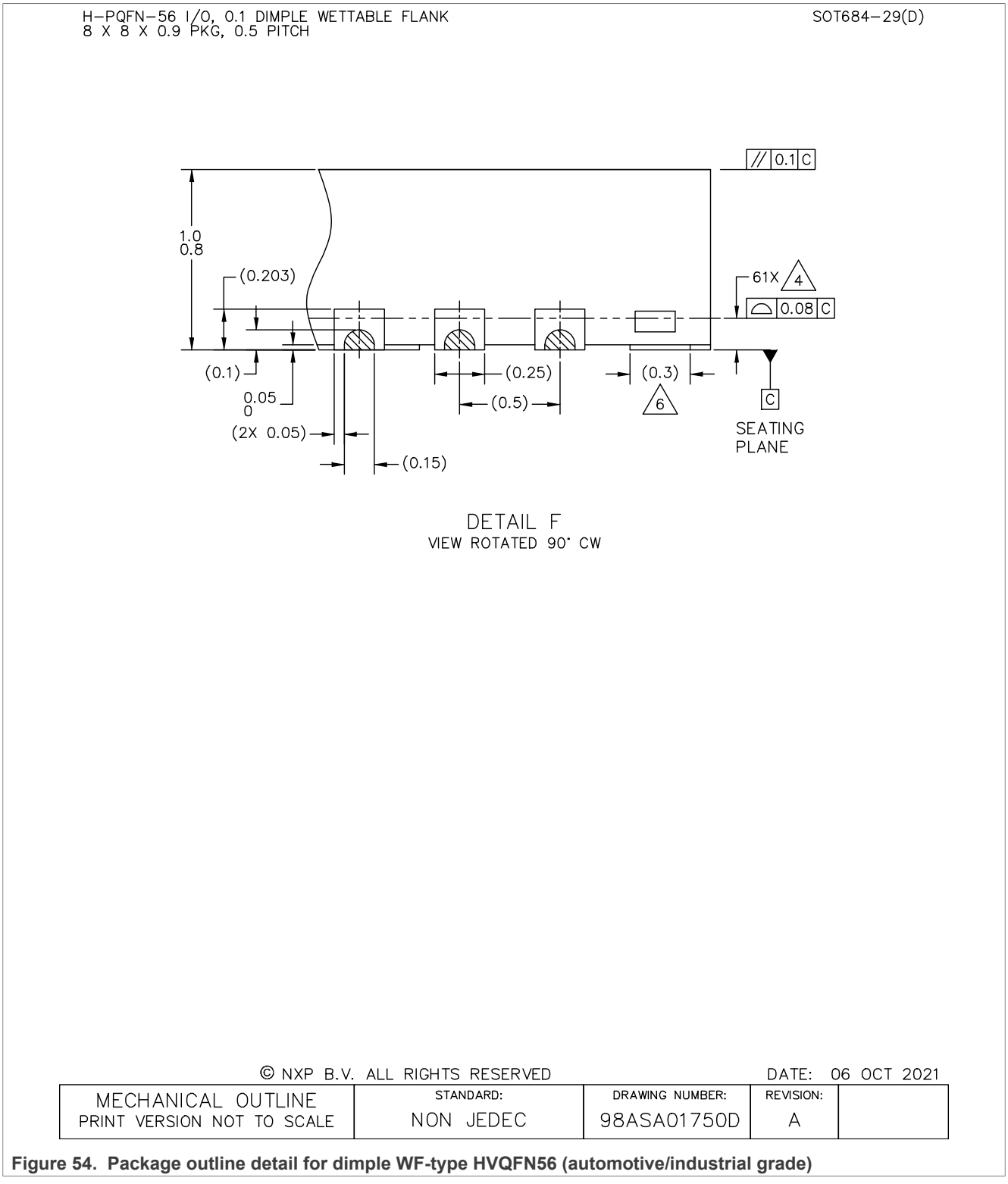


Figure 54. Package outline detail for dimple WF-type HVQFN56 (automotive/industrial grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

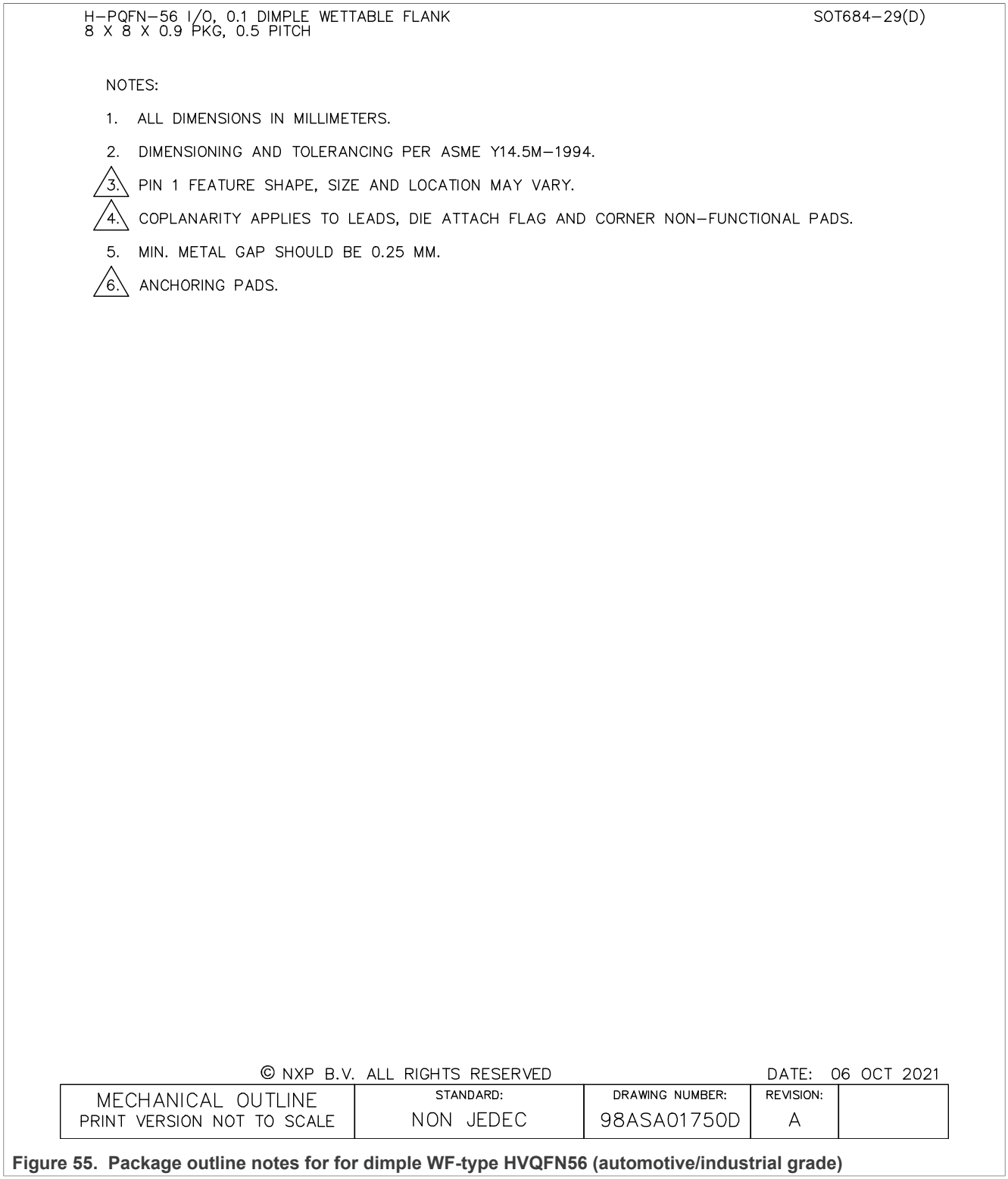


Figure 55. Package outline notes for for dimple WF-type HVQFN56 (automotive/industrial grade)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21.6 PCB design guidelines for dimple WF-type HVQFN56

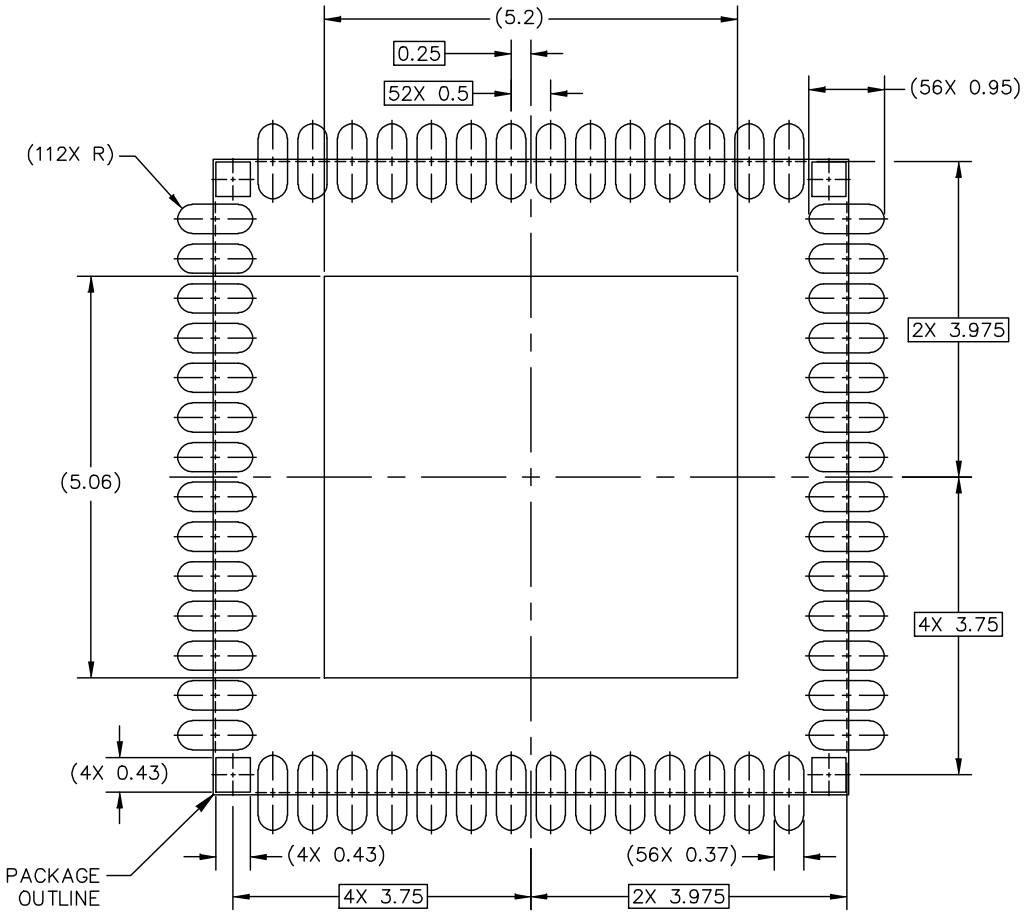


Figure 56. PCB design guidelines - solder mask opening pattern

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

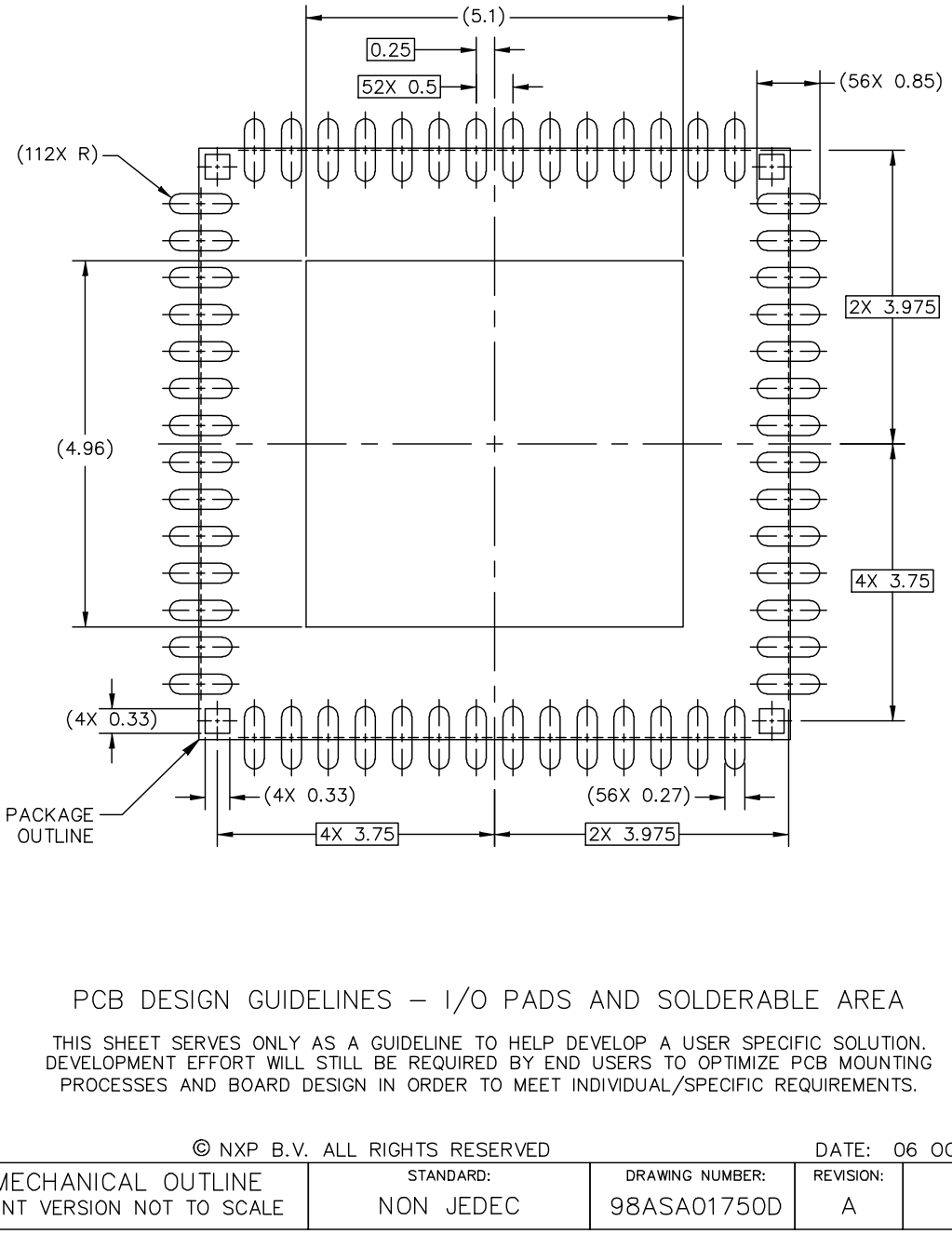


Figure 57. PCB design guidelines - I/O pads and solderable areas

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

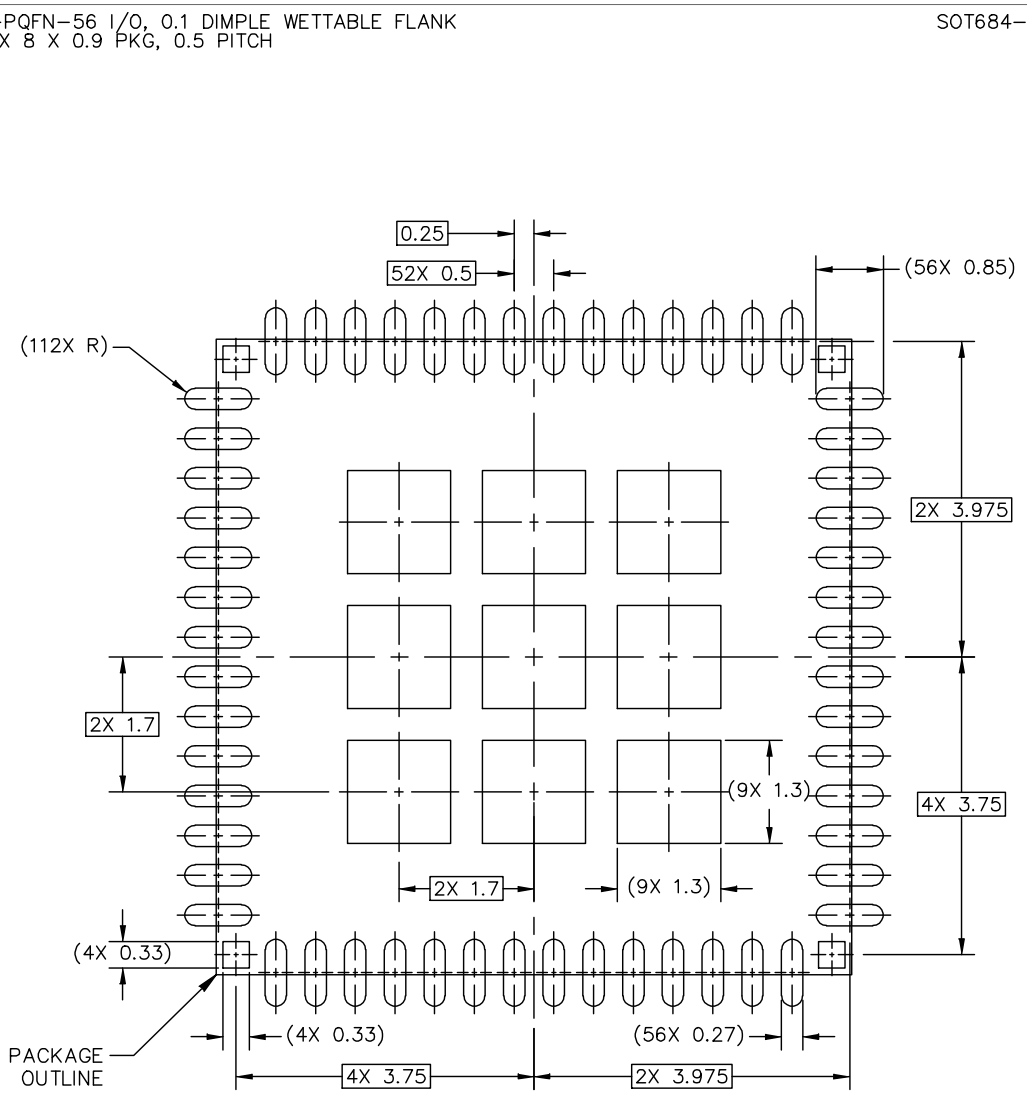


Figure 58. PCB design guidelines - Solder paste stencil

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

22 Revision history

Table 80. Revision history

Document ID	Release date	Description
PF8100_PF8200 v.12	18 Oct 2024	• CIN 202404027I • Updated front page graphics • Global: replaced *master* with *primary* and *slave* with *secondary* • Revised Section 2 and renamed to conform to current template • Revised Table 1 to add types with package data SOT684-29(D) • Revised Table 2, adding parts with IDs ending in *TS* • Revised Table 67 to correct heading from OV to UV • Added Section 21.5 – SOT684-29(D) • Added Section 21.6 – SOT684-29(D) • Updated legal information
PF8100_PF8200 v.11	24 Feb 2021	• CIN 202102036I • Table 6: updated storage temperature (replaced −40 by −55) • Table 53: changed output accuracy from ±2.0% to ±1.5% for V_{SWxACC} (0.8 V ≤ VSWxFB ≤ 1.0 V) • Section 14.9.13: updated Figure 21
PF8100_PF8200 v.10	5 Oct 2020	• CIN 202009036I • Table 3: added note for pins SW1LX, SW2LX, SW3LX, SW4LX, SW5LX, SW6LX, and SW7LX (additional note added to clarify that the SWxLX pins are tolerant to negative transient spike during the dead band time with expectable fast transients as low as −3.0 V) • Table 11: added new transitions to the State machine transition definition table in order to clarify missing conditions related to the XFAILB during power up and power down events • Section 15.4, Section 15.5: added a section for current limit specification (The current limit specification is given with respect to the inductor ……) • Section 15.4.3 (I_{SWx}, I_{SWx_DP}): added note "The Type 1 buck regulator in single or dual phase configuration is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken to prevent reaching PMIC thermal shutdown during high ambient temperature conditions" • Section 15.4.3: updated V_{SWxACC} values and conditions • Section 15.5.1 (I_{SW7}): added note "The Type 2 buck regulator is capable of providing output current above the nominal max current specification as long as it does not reach the current limitation. However, if operating above the nominal maximum current, overall thermal considerations must be taken to prevent reaching PMIC thermal shutdown during high ambient temperature conditions" • Section 15.8.5: added a section to provide clarification on the system level implementation to handle an external clock failure (Upon an external clock failure, the MCU must proof…..)
PF8100_PF8200 v.9.0	9 Nov 2019	• CIN 201909005I • Table 53: added values for I_{SW5LIM} and added note "Current limit applicable to SW5 to ensure maximum power requirement for the MEMC rail in i.MX8QM systems" • Table 53: added note "Current limit applicable to SW1, SW2, SW3, SW4 and SW6" for I_{SWxLIM} (SWxILIM[1:0] = 11) • Section 14.9.11.1, Section 14.9.11.2: divided Section 14.9.11 content into two subtopics to clarify FSOB configuration differences between PF8200 and PF8100 devices
PF8100_PF8200 v.8.0	20 Sept 2019	• CIN 201909005I • Table 2: added MC33PF8100FJES and MC34PF8100FJEP, deleted MC33PF8200DMES and MC33PF8200DNES, added "not recommended for new designs" note for MC33PF8100CCES and MC34PF8100CCEP parts • Table 53: updated description (replaced "VSWxIN = UVDET to 5.5 V" by "VIN = VSWxIN = UVDET to 5.5 V" and "VSWxIN = 5.0 V" by "VIN = VSWxIN = 5.0 V"), added note "VSWxIN must be connected to VIN to ensure proper device operation" • Table 60: updated description (replaced "VSW7IN = 5.0 V" by "VIN = VSW7IN = 5.0 V"), added note "VSW7IN must be connected to VIN to ensure proper operation" • Table 9: Added note "Input supply for switching regulators must be capable to sink current to avoid overvoltage condition during the power down sequence of the device"
PF8100_PF8200 v.7.0	29 April 2019	• Global: changed document status from Preliminary to Product

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 80. Revision history...*continued*

Document ID	Release date	Description
PF8100_PF8200 v.6.0	19 April 2019	• Preliminary data sheet • Section 4: updated Table 1 and added Table 2 • Table 3: updated description for V1P5D AND V1P5A (replaced 1.5 by 1.6) • Table 3: updated description for VDDIO (replaced 1.7 V by 1.6 V) • Section 12.1: added "SW1, SW2 and SW3 configurable as a triple phase regulator with up to 7.5 A current capability" to features list • Section 15.4.2: updated description and added Figure 26 • Table 53: added values for I_{SWx_TP} and $I_{SWxILIM_TP}$ and conditions for $V_{SWxLOTR}$ and $V_{SWxLOTR}$ • Table 37: updated min and typical values for V_{1P5D} and V_{1P5A} (replaced 1.35 by 1.50 and 1.50 by 1.60) • Figure 6 and Figure 7: replaced 1.5 V by 1.6 V) • Table 39: updated the max value for $V_{COINRLHYS}$ (replaced 150 by 170) • Table 15: updated VIN_OVLO min value (replaced 5.6 by 5.55) • Table 42: updated max value for $V_{COINHYS}$ (replaced 140 by 200) • Section 21: updated package drawings and added drawings for industrial grade
PF8100_PF8200 v.5.0	1 Oct 2018	• Objective data sheet • Updated max value for VIN_OVLO_HYS in Table 15 (replaced 100 by 200)
PF8100_PF8200 v.4.0	28 Sept 2018	• Advance information • Changed document status from technical data to advance information
PF8100_PF8200 v.3.0	26 Sept 2018	• Technical data • Updated description for RESETBMCU_ V_{OL}, INTB_ V_{OL}, PGOOD_ V_{OL}, XFAILB_V_{OL} in Table 28 (replaced −2.0 mA by 10 mA) • Updated max value for VSELECT_ V_{IL} and LDO2EN_ V_{IL} in Table 28 (replaced 0.4 by 0. 3*VDDIO) • Updated min value for VSELECT_ V_{IH} and LDO2EN_ V_{IH} in Table 28 (replaced 1.4 by 0. 7*VDDIO) • Updated max value for V_{SNVS_ILIM} in Table 42 (replaced 60 by 70) • Updated clock frequency tolerance (replaced ±5 % by ±6 %) in Table 44 description • Updated min value for $t_{PFMtoPWM}$ in Table 53 (replaced 10 by 30) • Updated min and max values for $I_{SWxNLIM}$ in Table 53 (replaced 0.7 by 0.6 and 1.3 by 1.4) • Updated max value for $t_{ONSWxMAX}$ in Table 53 (replaced 279 by 310) • Updated description and min value for t_{ONSWx_MIN} in Table 53 (replaced 36 by 34.2) • Updated typical value for I_{SWxQ} in Table 53 (replaced 12 by 14) • Updated min and max values for V_{SWxACC} in Table 53 • Updated R_{SWxDIS} values in Table 53 • Added $V_{SWxACCPFM}$ values to Table 53 • Updated description for V_{SW7IN} in Table 60 (replaced 4.5 by 4.1) • Updated min and max values for V_{SW7ACC} in Table 60 (replaced −3.0 by −4.0 and 3.0 by 4.0) • Updated $R_{dischLDOx}$ values in Table 64 (replaced 45 by 50 and 500 by 300) • Updated values for $t_{SW7RAMP}$, t_{ONSW7}, I_{SW7Q} in Table 60 • Updated typical and max values for $I_{LDOxLIM}$ and I_{LSxLIM} in Table 64 (replaced 800 by 850 and 1200 to 1400) • Updated typical and max values for I_{LDOxQ} in Table 64 (replaced 9.4 by 7.0 and 12.5 to 10) • Updated max values for t_{ONLDOx} and $t_{OFFLDOx}$ in Table 64 (replaced 500 by 300 and 2500 by 3500) • Updated min and max values for $V_{LDOxLOTR}$ in Table 64 (replaced −3.0 by −6.0 and 3.0 by 6.0) • Updated typical and max values for $T_{onLDOxLS}$ in Table 64 (replaced 100 by 150 and 500 by 300) • Updated min and max values for $R_{dischLDOx}$ in Table 64 (replaced 45 by 50 and 500 by 300) • Updated description and values for t_{UV_DB} and t_{OV_DB} in Table 69 • Updated min and max values for $f_{20MzACC}$ in Table 71 (replaced −5.0 by −6.0 and 5.0 by 6.0) • Updated values in Table 75 • Updated package outline
PF8100_PF8200 v.2.2	11June 2018	• Product preview • Minor typo corrections
PF8100_PF8200 v.2.1	22 May 2018	• Product preview • Changed document id from PF8x00 to PF8100_PF8200 • Updated PF8200 OTP mirror register table (deleted E0, E1 and added E3) • Updated PF8100 OTP mirror register table (deleted E0, E1 and added E3)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 80. Revision history...*continued*

Document ID	Release date	Description
PF8100_PF8200 v.2.0	16 Jan 2018	• Product preview • Updates to reflect silicon B0
PF8100_PF8200 v.1.0	12 May 2017	• Product preview

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Tables

Tab. 1. Device options 4
Tab. 2. Ordering information 4
Tab. 3. HVQFN56 pin description 8
Tab. 4. Absolute maximum ratings 11
Tab. 5. ESD ratings 12
Tab. 6. Thermal characteristics 13
Tab. 7. QFN56 thermal resistance and package dissipation ratings 13
Tab. 8. Operating conditions 14
Tab. 9. Voltage supply summary 16
Tab. 10. Device differences 17
Tab. 11. State machine transition definition 20
Tab. 12. Fail-safe OK timer configuration 27
Tab. 13. UVDET threshold 28
Tab. 14. VIN_OVLO debounce configuration 28
Tab. 15. VIN_OVLO specifications 28
Tab. 16. Startup timing requirements (PWRON pulled up) 29
Tab. 17. Startup with PWRON driven high externally and LPM_OFF = 0 30
Tab. 18. Power up time base register 31
Tab. 19. Power up sequence registers 32
Tab. 20. Power down regulator group bits 35
Tab. 21. Power down counter delay 35
Tab. 22. Programmable delay after RESETBMCU is asserted 36
Tab. 23. Power down delay selection 37
Tab. 24. Regulator control during fault event bits 38
Tab. 25. Fault timer register configuration 40
Tab. 26. Fault bypass bits 40
Tab. 27. Interrupt registers 45
Tab. 28. I/O electrical specifications 46
Tab. 29. PWRON debounce configuration in edge detection mode 48
Tab. 30. TRESET configuration 48
Tab. 31. Standby pin polarity control 48
Tab. 32. EWARN time configuration 50
Tab. 33. Early warning threshold 50
Tab. 34. LDO control in run or standby mode 52
Tab. 35. I2C address configuration 57
Tab. 36. Secure bits 58
Tab. 37. Internal supplies electrical characteristics 60
Tab. 38. Coin cell charger voltage level 61
Tab. 39. Coin cell electrical characteristics 61
Tab. 40. VSNVS operation description 62
Tab. 41. VSNVS output voltage configuration 63
Tab. 42. VSNVS electrical characteristics 63
Tab. 43. DVS ramp speed configuration 64
Tab. 44. Ramp rates 64
Tab. 45. Output voltage configuration 65
Tab. 46. SW regulator mode configuration 65
Tab. 47. SWx current limit selection 66
Tab. 48. SWx phase configuration 66
Tab. 49. SWx inductor selection bits 66
Tab. 50. OTP_SW1CONFIG register description 68
Tab. 51. OTP SW4CONFIG register description 68
Tab. 52. OTP_SW5CONFIG register description 68
Tab. 53. Type 1 buck regulator electrical characteristics 70
Tab. 54. Recommended external components 72
Tab. 55. SW7 output voltage configuration 74
Tab. 56. SW7 regulator mode configuration 75
Tab. 57. SW7 current limit selection 76
Tab. 58. SW7 phase configuration 76
Tab. 59. SW7 inductor selection bits 76
Tab. 60. Type 2 buck regulator electrical characteristics 77
Tab. 61. Recommended external components 78
Tab. 62. LDO operation description 79
Tab. 63. LDO output voltage configuration 79
Tab. 64. LDO regulator electrical characteristics 80
Tab. 65. UV threshold configuration register 81
Tab. 66. OV threshold configuration register 82
Tab. 67. UV debounce timer configuration 82
Tab. 68. OV debounce timer configuration 82
Tab. 69. VMON Electrical characteristics 84
Tab. 70. Manual frequency tuning configuration 86
Tab. 71. Clock management specifications 88
Tab. 72. Thermal monitor specifications 90
Tab. 73. Thermal monitor bit description 91
Tab. 74. AMUX channel selection 92
Tab. 75. AMUX specifications 93
Tab. 76. Watchdog duration register 93
Tab. 77. Soft WD register reset 96
Tab. 78. Default hardwire configuration 114
Tab. 79. Quiescent current requirements 119
Tab. 80. Revision history 137

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Figures

Fig. 1. Simplified application diagram 3
Fig. 2. Internal block diagram 7
Fig. 3. Pin configuration for HVQFN56 8
Fig. 4. Functional block diagram 16
Fig. 5. State diagram 19
Fig. 6. Startup with PWRON pulled up 29
Fig. 7. Startup with PWRON driven high externally and bit LPM_OFF = 0 30
Fig. 8. Power up/down sequence between off and system-on states 33
Fig. 9. Power up/down sequence between run and standby 33
Fig. 10. Group power down sequence example 36
Fig. 11. Power down delay 37
Fig. 12. Regulator turned off with RegX_STATE = 0 and FLT_REN = 0 38
Fig. 13. Regulator turned off with RegX_STATE = 0 and FLT_REN = 1 39
Fig. 14. Correct power up (no fault during power up) 42
Fig. 15. Power up sequencer with a temporary failure 43
Fig. 16. Power up sequencer aborted as fault persists for longer than 2.0 ms 44
Fig. 17. I/O interface diagram 46
Fig. 18. XFAILB behavior during a power up sequence 55
Fig. 19. XFAILB behavior during a power down sequence 55
Fig. 20. Behavior during an external XFAILB event 56
Fig. 21. External XFAILB event during a power up sequence 56
Fig. 22. 8 bit SAE J1850 CRC polynomial 57
Fig. 23. VSNVS block diagram 62
Fig. 24. Buck regulator block diagram 64
Fig. 25. Dual phase configuration 69
Fig. 26. Triple phase configuration 69
Fig. 27. Quad phase configuration 70
Fig. 28. Type 2 buck regulator block diagram 74
Fig. 29. LDOx regulator block diagram 79
Fig. 30. Voltage monitoring architecture 83
Fig. 31. Clock management architecture 85
Fig. 32. Spread-spectrum waveforms 87
Fig. 33. Thermal monitoring architecture 90
Fig. 34. Thermal sensor voltage characteristics 91
Fig. 35. Watchdog timer operation 95
Fig. 36. Soft WD reset behavior 97
Fig. 37. Hard WD reset behavior 98
Fig. 38. Watchdog event counter 99
Fig. 39. Hardwire operation diagram 114
Fig. 40. Typical application diagram 120
Fig. 41. Package outline for WF-type HVQFN56 (Automotive grade) 121
Fig. 42. Package outline detail for WF-type HVQFN56 (Automotive grade) 122
Fig. 43. Package outline notes for WF-type HVQFN56 (Automotive grade) 122
Fig. 44. Solder mask pattern for WF-type HVQFN56 123
Fig. 45. I/O pads and solderable areas for WF-type HVQFN56 124
Fig. 46. Solder paste stencil for WF-type HVQFN56 .. 125
Fig. 47. Package outline for E-type HVQFN56 (Industrial grade) 126
Fig. 48. Package outline detail for E-type HVQFN56 (Industrial grade) 127
Fig. 49. Package outline notes for E-type HVQFN56 (Industrial grade) 127
Fig. 50. Solder mask pattern for E-type HVQFN56 128
Fig. 51. I/O pads and solderable areas for E-type HVQFN56 129
Fig. 52. Solder paste stencil for E-type HVQFN56 130
Fig. 53. Package outline for dimple WF-type HVQFN56 (automotive/industrial grade) 131
Fig. 54. Package outline detail for dimple WF-type HVQFN56 (automotive/industrial grade) 132
Fig. 55. Package outline notes for for dimple WF-type HVQFN56 (automotive/industrial grade) 133
Fig. 56. PCB design guidelines - solder mask opening pattern 134
Fig. 57. PCB design guidelines - I/O pads and solderable areas 135
Fig. 58. PCB design guidelines - Solder paste stencil 136

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Contents

1 Overview 1
2 Features and benefits 2
3 Simplified application diagram 3
4 Ordering information 4
5 Applications 6
6 Internal block diagram 7
7 Pinning information 8
7.1 Pinning 8
7.2 Pin description 8
8 Absolute maximum ratings 11
9 ESD ratings 12
10 Thermal characteristics 13
11 Operating conditions 14
12 General description 15
12.1 Features 15
12.2 Functional block diagram 16
12.3 Power tree summary 16
12.4 Device differences 17
13 State machine 18
13.1 State descriptions 22
13.1.1 OTP/TRIM load 22
13.1.2 LP_Off state 23
13.1.3 Self-test routine (PF8200 only) 23
13.1.4 QPU_Off state 23
13.1.5 Power up sequence 24
13.1.6 System-on states 24
13.1.6.1 Run state 24
13.1.6.2 Standby state 25
13.1.7 WD_Reset 26
13.1.8 Power down state 26
13.1.9 Fail-safe transition 26
13.1.10 Fail-safe state (PF8200 only) 26
13.1.11 Coin cell state 27
14 General device operation 28
14.1 UVDET 28
14.2 VIN OVLO condition 28
14.3 IC startup timing with PWRON pulled up 29
14.4 IC startup timing with PWRON pulled low during VIN application 30
14.5 Power up 31
14.5.1 Power up events 31
14.5.2 Power up sequencing 31
14.6 Power down 34
14.6.1 Turn off events 34
14.6.2 Power down sequencing 34
14.6.2.1 Sequential power down 34
14.6.2.2 Group power down 35
14.6.2.3 Power down delay 36
14.7 Fault detection 37
14.7.1 Fault monitoring during power up state 41
14.8 Interrupt management 44
14.9 I/O interface pins 46
14.9.1 PWRON 47
14.9.2 STANDBY 48
14.9.3 RESETBMCU 49
14.9.4 INTB 49
14.9.5 XINTB 49
14.9.6 WDI 49
14.9.7 EWARN 50
14.9.8 PGOOD 51
14.9.9 VSELECT 51
14.9.10 LDO2EN 52
14.9.11 FSOB (safety output) 52
14.9.11.1 FSOB fault safe state 52
14.9.11.2 FSOB active safe state (PF8200 only) 53
14.9.12 TBBEN 54
14.9.13 XFAILB 54
14.9.14 SDA and SCL (I2C bus) 56
14.9.14.1 I2C CRC verification 57
14.9.14.2 I2C secure write 58
15 Functional blocks 60
15.1 Analog core and internal voltage references 60
15.2 Coin cell charger 60
15.3 VSNVS LDO/switch 61
15.4 Type 1 buck regulators (SW1 to SW6) 63
15.4.1 SW6 VTT operation 67
15.4.2 Multiphase operation 67
15.4.3 Electrical characteristics 70
15.5 Type 2 buck regulator (SW7) 74
15.5.1 Electrical characteristics 77
15.6 Linear regulators 78
15.6.1 LDO load switch operation 80
15.6.2 LDO regulator electrical characteristics 80
15.7 Voltage monitoring 81
15.7.1 Electrical characteristics 84
15.8 Clock management 84
15.8.1 Low frequency clock 85
15.8.2 High frequency clock 85
15.8.3 Manual frequency tuning 85
15.8.4 Spread-spectrum 86
15.8.5 Clock Synchronization 87
15.9 Thermal monitors 89
15.10 Analog multiplexer 92
15.11 Watchdog event management 93
15.11.1 Internal watchdog timer 93
15.11.2 Watchdog reset behaviors 95
16 I2C register map 100
16.1 PF8200 functional register map 100
16.2 PF8200 OTP mirror register map (page 1) 103
16.3 PF8100 functional register map 106
16.4 PF8100 OTP mirror register map (page 1) 109
17 OTP/TBB and default configurations 112
17.1 TBB (Try Before Buy) operation 112
17.2 OTP fuse programming 113
17.3 Default hardwire configuration 113
18 Functional safety 117
18.1 System safety strategy 117
18.2 Output voltage monitoring with dedicated bandgap reference 117
18.3 ABIST verification 117
19 IC level quiescent current requirements 119
20 Typical applications 120

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

21 Package information 121
21.1 Package outline for step-cut WF-type HVQFN56 (Automotive grade) 121
21.2 PCB design guidelines for step-cut WF-type HVQFN56 123
21.3 Package outline for E-type HVQFN56 (Industrial grade) 126
21.4 PCB design guidelines for E-type HVQFN56 128
21.5 Package outline for dimple WF-type HVQFN56 (automotive/industrial grade) 131
21.6 PCB design guidelines for dimple WF-type HVQFN56 134
22 Revision history 137
Legal information 140

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2024 NXP B.V. **All rights reserved.**