NTB0104

Dual supply translating transceiver; auto direction sensing; 3-state

Rev. 4.1 — 17 October 2024 Product data sheet

1 General description

The NTB0104 is a 4-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 4-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.2 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V).

Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 1.2 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - HBM JESD22-A114E Class 2 exceeds 2500 V for A port
  - HBM JESD22-A114E Class 3B exceeds 15000 V for B port
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1500 V (For NTB0104UK 1000 V)
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

3 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTB0104BQ	B0104	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
NTB0104GU12	t4	XQFN12	plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 × 2.0 × 0.50 mm	SOT1174-1
NTB0104UK	t04	WLCSP12	wafer level chip-size package, 12 bumps; body 1.20 × 1.60 × 0.56 mm. (Backside Coating included)	NTB0104UK

3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NTB0104BQ	NTB0104BQ,115	DHVQFN14	REEL 7" Q1/T1 *STANDARD MARK SMD	3000	T_{amb} = -40 °C to +125 °C
NTB0104GU12	NTB0104GU12,115	XQFN12	REEL 7" Q1/T1 *STANDARD MARK SMD	4000	T_{amb} = -40 °C to +125 °C
NTB0104UK[1]	NTB0104UK,012	WLCSP12	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	5000	T_{amb} = -40 °C to +125 °C

[1] Discontinued with last time buy date of 3/22/2024 and last time ship date of 9/27/2024.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

4 Functional diagram

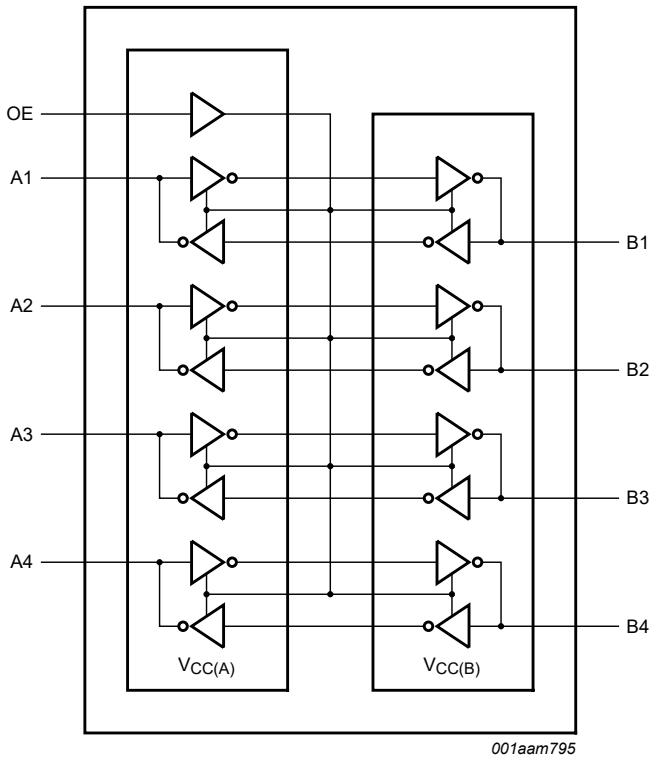


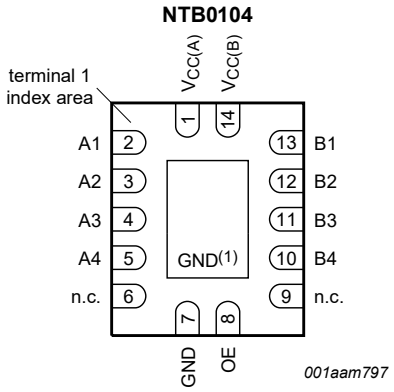
Figure 1. Logic symbol

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

5 Pinning information

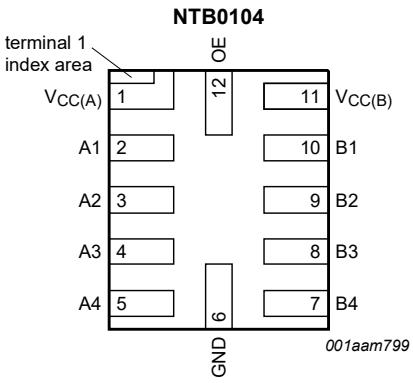
5.1 Pinning



Transparent top view

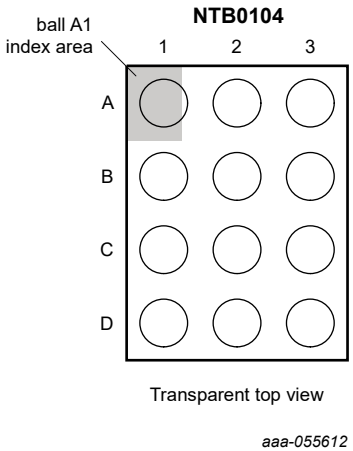
1. This is not a supply pin, the substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad, however if it is soldered the solder land should remain floating or be connected to GND

Figure 2. Pin configuration DHVQFN14 (SOT762-1)



Transparent top view

Figure 3. Pin configuration XQFN12 (SOT1174-1)



Transparent top view

Figure 4. Pin configuration WLCSP12 package

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

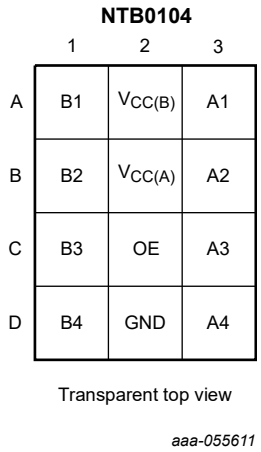


Figure 5. Ball mapping for WLCSP12

5.2 Pin description

Table 3. Pin description

Symbol	Pin		Ball	Description
	SOT762-1	SOT1174-1	WLCSP12	
$V_{CC(A)}$	1	1	B2	supply voltage A
A1, A2, A3, A4	2, 3, 4, 5	2, 3, 4, 5	A3, B3, C3, D3	data input or output (referenced to $V_{CC(A)}$)
n.c.	6, 9	-	-	not connected
GND	7	6	D2	ground (0 V)
OE	8	12	C2	output enable input (active HIGH; referenced to $V_{CC(A)}$)
B4, B3, B2, B1	10, 11, 12, 13	7, 8, 9, 10	D1, C1, B1, A1	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	14	11	A2	supply voltage B

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

6 Functional description

Table 4. Function table[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	L	Z	Z
1.2 V to $V_{CC(B)}$	1.65 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

7 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			-0.5	+6.5	V
V_I	input voltage		[1]	-0.5	+6.5	V
V_O	output voltage	Active mode	[1][2][3]	-0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	V_O = 0 V to V_{CCO}	[2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] V_{CCO} + 0.5 V should not exceed 6.5 V.
[4] For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.
For XQFN12 packages: above 128 °C the value of P_{tot} derates linearly with 11.5 mW/K.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

8 Recommended operating conditions

Table 6. Recommended operating conditions[1][2]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			1.2	3.6	V
$V_{CC(B)}$	supply voltage B			1.65	5.5	V
V_I	input voltage			0	5.5	V
V_O	output voltage	Power-down or 3-state mode; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V				
		A port		0	3.6	V
		B port		0	5.5	V
T_{amb}	ambient temperature			-40	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	40	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.
[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

9 Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = -20 µA		-	1.1	-	V
V_{OL}	LOW-level output voltage	A port; $V_{CC(A)}$ = 1.2 V; I_O = 20 µA		-	0.09	-	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	-	±1	µA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V to V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[1]	-	-	±1	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	-	±1	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		-	-	±1	µA
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[2]				
		$I_{CC(A)}$; $V_{CC(A)}$ = 1.2 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.05	-	µA
		$I_{CC(B)}$; $V_{CC(A)}$ = 1.2 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	3.3	-	µA
		$I_{CC(A)}$ + $I_{CC(B)}$; $V_{CC(A)}$ = 1.2 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	3.5	-	µA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	2.8	-	pF
$C_{I/O}$	input/output capacitance	A port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	4.0	-	pF
		B port; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	7.5	-	pF

[1] V_{CCO} is the supply voltage associated with the output.
[2] V_{CCI} is the supply voltage associated with the input.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.8 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.2 V	10	10	10	10	10	20	10	1050	nA
1.5 V	10	10	10	10	10	10	10	650	nA
1.8 V	10	10	10	10	10	10	10	350	nA
2.5 V	-	-	10	10	10	10	10	40	nA
3.3 V	-	-	-	-	10	10	10	10	nA

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A or B port and OE input	[1]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		0.65V_{CCI}	-	0.65V_{CCI}	-	V
V_{IL}	LOW-level input voltage	A or B port and OE input	[1]					
		$V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.35V_{CCI}	-	0.35V_{CCI}	V
V_{OH}	HIGH-level output voltage	A or B port; I_O = -20 µA	[2]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V		V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V		V_{CCO} - 0.4	-	V_{CCO} - 0.4	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 20 µA	[2]					
		A port; $V_{CC(A)}$ = 1.4 V to 3.6 V		-	0.4	-	0.4	V
		B port; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.4	-	0.4	V
$R_{O(ser)}$	serial output resistance	A port		3	5	3	5	kΩ
		B port		3	5	3	5	kΩ
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	±2	-	±5	µA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.2 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[2]	-	±2	-	±10	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		-	±2	-	±10	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		-	±2	-	±10	µA
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[1]					
		$I_{CC(A)}$						
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	15	µA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	20	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	2	-	15	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	-2	-	-15	µA
		$I_{CC(B)}$						
		OE = LOW; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	15	µA
		OE = HIGH; $V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	5	-	20	µA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	-2	-	-15	µA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	2	-	15	µA

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 9. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)}$ = 1.4 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	10	-	40	µA

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

10 Dynamic characteristics

Table 10. Typical dynamic characteristics for temperature 25 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for waveforms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$				Unit
				1.8 V	2.5 V	3.3 V	5.0 V	
$V_{CC(A)}$ = 1.2 V; T_{amb} = 25 °C								
t_{pd}	propagation delay	A to B		5.9	4.8	4.4	4.2	ns
		B to A		5.6	4.8	4.5	4.4	ns
t_{en}	enable time	OE to A, B		0.5	0.5	0.5	0.5	µs
t_{dis}	disable time	OE to A; no external load	[2]	8.3	8.3	8.3	8.3	ns
		OE to B; no external load	[2]	10.4	9.4	9.3	8.8	ns
		OE to A		81	69	83	68	ns
		OE to B		81	69	83	68	ns
t_t	transition time	A port		4.0	4.0	4.1	4.1	ns
		B port		2.6	2.0	1.7	1.4	ns
$t_{sk(o)}$	output skew time	between channels	[3]	0.2	0.2	0.2	0.2	ns
t_W	pulse width	data inputs		15	13	13	13	ns
f_{data}	data rate			70	80	80	80	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}
[2] Delay between OE going LOW and when the outputs are actually disabled.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V												
t_{pd}	propagation delay	A to B		1.4	12.9	1.2	10.1	1.1	10.0	0.8	9.9	ns
		B to A		0.9	14.2	0.7	12.0	0.4	11.7	0.3	13.7	ns
t_{en}	enable time	OE to A, B		-	1.0	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	1.0	12.9	1.0	12.9	1.0	12.9	1.0	12.9	ns
		OE to B; no external load	[2]	1.0	18.7	1.0	15.8	1.0	15.1	1.0	14.4	ns
		OE to A		-	320	-	260	-	260	-	280	ns
		OE to B		-	200	-	200	-	200	-	200	ns

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_t	transition time	A port		0.9	5.1	0.9	5.1	0.9	5.1	0.9	5.1	ns
		B port		0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		25	-	25	-	25	-	25	-	ns
f_{data}	data rate			-	40	-	40	-	40	-	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{pd}	propagation delay	A to B		1.6	11.0	1.4	7.7	1.3	6.8	1.2	6.5	ns
		B to A		1.5	12.0	1.3	8.4	1.0	7.6	0.9	7.1	ns
t_{en}	enable time	OE to A, B		-	1.0	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	1.0	11.7	1.0	11.7	1.0	11.7	1.0	11.7	ns
		OE to B; no external load	[2]	1.0	16.9	1.0	14.5	1.0	13.7	1.0	12.7	ns
		OE to A		-	260	-	230	-	230	-	230	ns
		OE to B		-	200	-	200	-	200	-	200	ns
t_t	transition time	A port		0.8	4.1	0.8	4.1	0.8	4.1	0.8	4.1	ns
		B port		0.9	4.7	0.6	3.2	0.5	2.5	0.4	2.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		20	-	17	-	17	-	17	-	ns
f_{data}	data rate			-	49	-	60	-	60	-	60	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{pd}	propagation delay	A to B		-	-	1.1	6.3	1.0	5.2	0.9	4.7	ns
		B to A		-	-	1.2	6.6	1.1	5.1	0.9	4.4	ns
t_{en}	enable time	OE to A, B		-	-	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	-	-	1.0	9.7	1.0	9.7	1.0	9.7	ns
		OE to B; no external load	[2]	-	-	1.0	12.9	1.0	12.0	1.0	11.0	ns
		OE to A		-	-	-	200	-	200	-	200	ns
		OE to B		-	-	-	200	-	200	-	200	ns
t_t	transition time	A port		-	-	0.7	3.0	0.7	3.0	0.7	3.0	ns
		B port		-	-	0.7	3.2	0.5	2.5	0.4	2.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		-	-	12	-	10	-	10	-	ns
f_{data}	data rate			-	-	-	85	-	100	-	100	Mbps

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 11. Dynamic characteristics for temperature range -40 °C to +85 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{pd}	propagation delay	A to B		-	-	-	-	0.9	4.7	0.8	4.0	ns
		B to A		-	-	-	-	1.0	4.9	0.9	3.8	ns
t_{en}	enable time	OE to A, B		-	-	-	-	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	-	-	-	-	1.0	9.4	1.0	9.4	ns
		OE to B; no external load	[2]	-	-	-	-	1.0	11.3	1.0	10.4	ns
		OE to A		-	-	-	-	-	260	-	260	ns
		OE to B		-	-	-	-	-	200	-	200	ns
t_t	transition time	A port		-	-	-	-	0.7	2.5	0.7	2.5	ns
		B port		-	-	-	-	0.5	2.5	0.4	2.7	ns
$t_{sk(o)}$	putput skew time	between channels	[3]	-	-	-	-	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		-	-	-	-	10	-	10	-	ns
f_{data}	data rate			-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}
[2] Delay between OE going LOW and when the outputs are actually disabled.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.5 V ± 0.1 V												
t_{pd}	propagation delay	A to B		1.4	15.9	1.2	13.1	1.1	13.0	0.8	12.9	ns
		B to A		0.9	17.2	0.7	15.0	0.4	14.7	0.3	16.7	ns
t_{en}	enable time	OE to A, B		-	1.0	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	1.0	13.5	1.0	13.5	1.0	13.5	1.0	13.5	ns
		OE to B; no external load	[2]	1.0	19.9	1.0	16.8	1.0	16.1	1.0	15.2	ns
		OE to A		-	340	-	280	-	280	-	300	ns
		OE to B		-	220	-	220	-	220	-	220	ns

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
t_t	transition time	A port		0.9	7.1	0.9	7.1	0.9	7.1	0.9	7.1	ns
		B port		0.9	6.5	0.6	5.2	0.5	4.8	0.4	4.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		25	-	25	-	25	-	25	-	ns
f_{data}	data rate			-	40	-	40	-	40	-	40	Mbps
$V_{CC(A)}$ = 1.8 V ± 0.15 V												
t_{pd}	propagation delay	A to B		1.6	14.0	1.4	10.7	1.3	9.8	1.2	9.5	ns
		B to A		1.5	15.0	1.3	11.4	1.0	10.6	0.9	10.1	ns
t_{en}	enable time	OE to A, B		-	1.0	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	1.0	12.3	1.0	12.3	1.0	12.3	1.0	12.3	ns
		OE to B; no external load	[2]	1.0	18.1	1.0	15.3	1.0	14.5	1.0	13.5	ns
		OE to A		-	280	-	250	-	250	-	250	ns
		OE to B		-	220	-	220	-	220	-	220	ns
t_t	transition time	A port		0.8	6.2	0.8	6.1	0.8	6.1	0.8	6.1	ns
		B port		0.9	5.8	0.6	5.2	0.5	4.8	0.4	4.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	0.5	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		22	-	19	-	19	-	19	-	ns
f_{data}	data rate			-	45	-	55	-	55	-	55	Mbps
$V_{CC(A)}$ = 2.5 V ± 0.2 V												
t_{pd}	propagation delay	A to B		-	-	1.1	9.3	1.0	8.2	0.9	7.7	ns
		B to A		-	-	1.2	9.6	1.1	8.1	0.9	7.4	ns
t_{en}	enable time	OE to A, B		-	-	-	1.0	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	-	-	1.0	10.1	1.0	10.1	1.0	10.1	ns
		OE to B; no external load	[2]	-	-	1.0	13.5	1.0	12.7	1.0	11.7	ns
		OE to A		-	-	-	220	-	220	-	220	ns
		OE to B		-	-	-	220	-	220	-	220	ns
t_t	transition time	A port		-	-	0.7	5.0	0.7	5.0	0.7	5.0	ns
		B port		-	-	0.7	4.6	0.5	4.8	0.4	4.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	0.5	-	0.5	-	0.5	ns
t_W	pulse width	data inputs;		-	-	14	-	13	-	10	-	ns
f_{data}	data rate			-	-	-	75	-	80	-	100	Mbps

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 12. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8; for wave forms see Figure 6 and Figure 7.

Symbol	Parameter	Conditions		$V_{CC(B)}$								Unit
				1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
				Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V												
t_{pd}	propagation delay	A to B		-	-	-	-	0.9	7.7	0.8	7.0	ns
		B to A		-	-	-	-	1.0	7.9	0.9	6.8	ns
t_{en}	enable time	OE to A, B		-	-	-	-	-	1.0	-	1.0	µs
t_{dis}	disable time	OE to A; no external load	[2]	-	-	-	-	1.0	9.9	1.0	9.9	ns
		OE to B; no external load	[2]	-	-	-	-	1.0	12.1	1.0	10.9	ns
		OE to A		-	-	-	-	-	280	-	280	ns
		OE to B		-	-	-	-	-	220	-	220	ns
t_t	transition time	A port		-	-	-	-	0.7	4.5	0.7	4.5	ns
		B port		-	-	-	-	0.5	4.1	0.4	4.7	ns
$t_{sk(o)}$	output skew time	between channels	[3]	-	-	-	-	-	0.5	-	0.5	ns
t_W	pulse width	data inputs		-	-	-	-	10	-	10	-	ns
f_{data}	data rate			-	-	-	-	-	100	-	100	Mbps

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
t_t is the same as t_{THL} and t_{TLH}
[2] Delay between OE going LOW and when the outputs are actually disabled.
[3] Skew between any two outputs of the same package switching in the same direction.

Table 13. Typical power dissipation capacitance

Voltages are referenced to GND (ground = 0 V).[1][2]

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			$V_{CC(B)}$							
			1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V	
T_{amb} = 25 °C										
C_{PD}	power dissipation capacitance	outputs enabled; OE = $V_{CC(A)}$								
		A port: (direction A to B)	5	5	5	5	5	5	5	pF
		A port: (direction B to A)	8	8	8	8	8	8	8	pF
		B port: (direction A to B)	18	18	18	18	18	18	18	pF
		B port: (direction B to A)	13	16	12	12	12	12	13	pF

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Table 13. Typical power dissipation capacitance...*continued*

Voltages are referenced to GND (ground = 0 V).[1][2]

Symbol	Parameter	Conditions	$V_{CC(A)}$							Unit
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			$V_{CC(B)}$							
			1.8 V	5.0 V	1.8 V	1.8 V	2.5 V	5.0 V	3.3 V to 5.0 V	
		outputs disabled; OE = GND								
		A port: (direction A to B)	0.12	0.12	0.04	0.05	0.08	0.08	0.07	pF
		A port: (direction B to A)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction A to B)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B port: (direction B to A)	0.07	0.09	0.07	0.07	0.05	0.09	0.09	pF

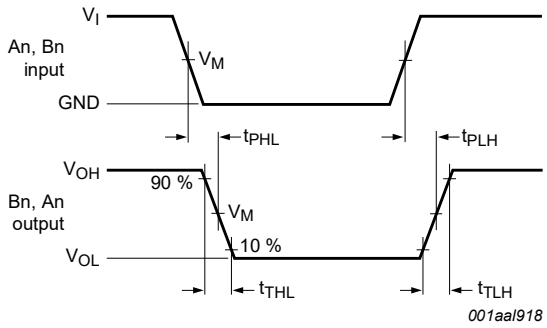
[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; R_L = ∞ Ω.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

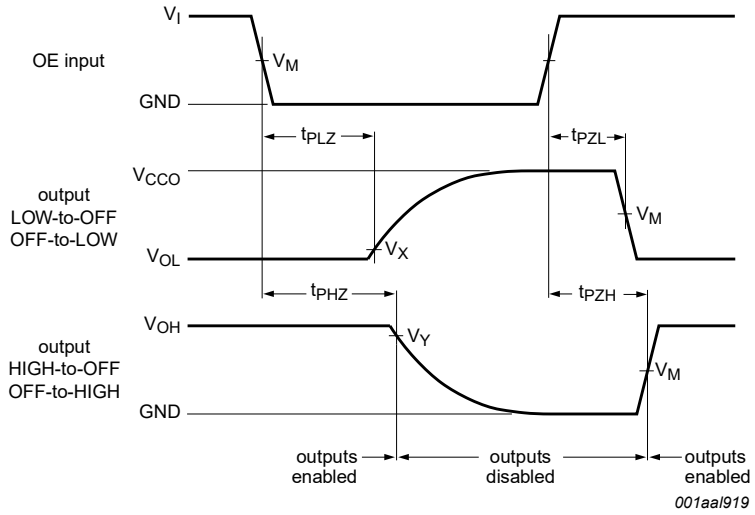
11 Waveforms



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. The data input (An, Bn) to data output (Bn, An) propagation delay times



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and disable times

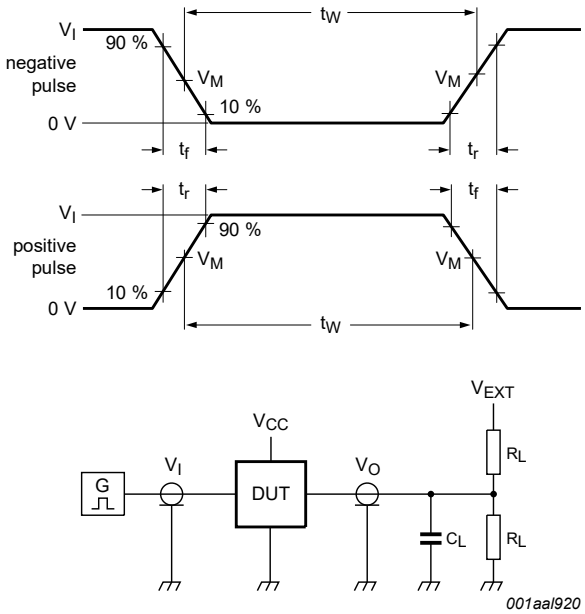
Table 14. Measurement points[1]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.5 V ± 0.1 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the input and V_{CCO} is the supply voltage associated with the output.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.



Test data is given in Table 15.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 8. Test circuit for measuring switching times

Table 15. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I[1]	Δt/ΔV	C_L	R_L[2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.
[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 kΩ.
[3] V_{CCO} is the supply voltage associated with the output.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

12 Application information

12.1 Applications

Voltage level-translation applications. The NTB0104 can be used to interface between devices or systems operating at different supply voltages. See Figure 9 for a typical operating circuit using the NTB0104.

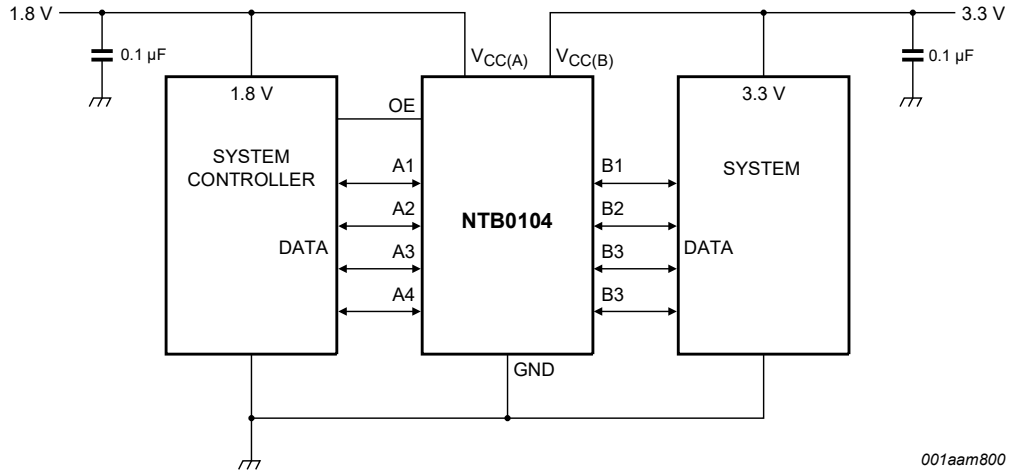


Figure 9. Typical operating circuit

12.2 Architecture

The architecture of the NTB0104 is shown in Figure 10. The device does not require an extra input signal to control the direction of data flow from A to B or from B to A. In a static state, the output drivers of the NTB0104 can maintain a defined output level, but the output architecture is designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing in the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shots turn on the PMOS transistors (T1, T3) for a short duration, accelerating the low-to-high transition. Similarly, during a falling edge, the one shots turn on the NMOS transistors (T2, T4) for a short duration, accelerating the high-to-low transition. During output transitions the typical output impedance is 70 Ω at V_{CCO} = 1.2 V to 1.8 V, 50 Ω at V_{CCO} = 1.8 V to 3.3 V and 40 Ω at V_{CCO} = 3.3 V to 5.0 V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

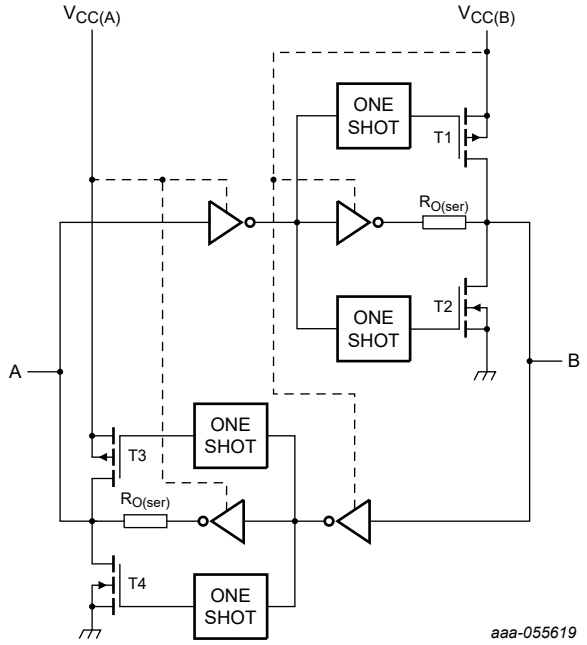
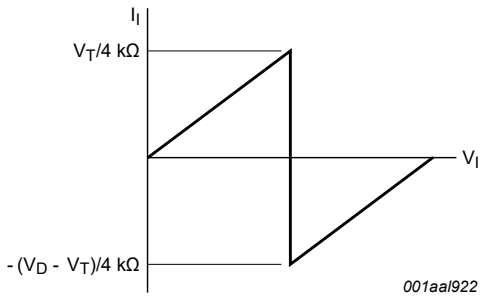


Figure 10. Architecture of NTB0104 I/O cell (one channel)

12.3 Input driver requirements

For correct operation, the device driving the data I/Os of the NTB0104 must have a minimum drive capability of ±2 mA See Figure 11 for a plot of typical input current versus input voltage.



V_T: input threshold voltage of the NTB0104 (typically V_{CCI} / 2).

V_D: supply voltage of the external driver.

Figure 11. Typical input current versus input voltage graph

12.4 Power up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTB0104 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

12.5 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor, the minimum value of the resistor is determined by the current-sourcing capability of the driver.

12.6 Pull-up or pull-down resistors on I/O lines

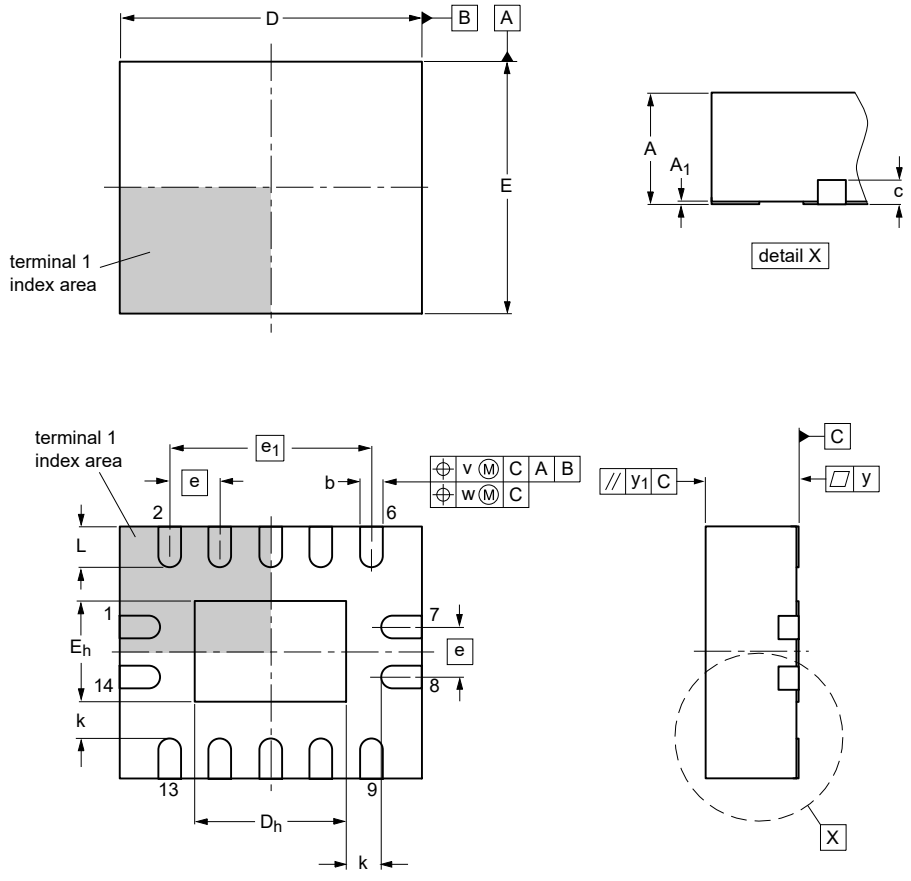
As mentioned previously the NTB0104 is designed with low static drive strength to drive capacitive loads of up to 70 pF. To avoid output contention issues, any pull-up or pull-down resistors used must be kept higher than 50 kΩ. For this reason the NTB0104 is not recommended for use in open drain driver applications such as 1-Wire or I^2C. For these applications, the NTS0104 level translator is recommended.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

13 Package outline

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

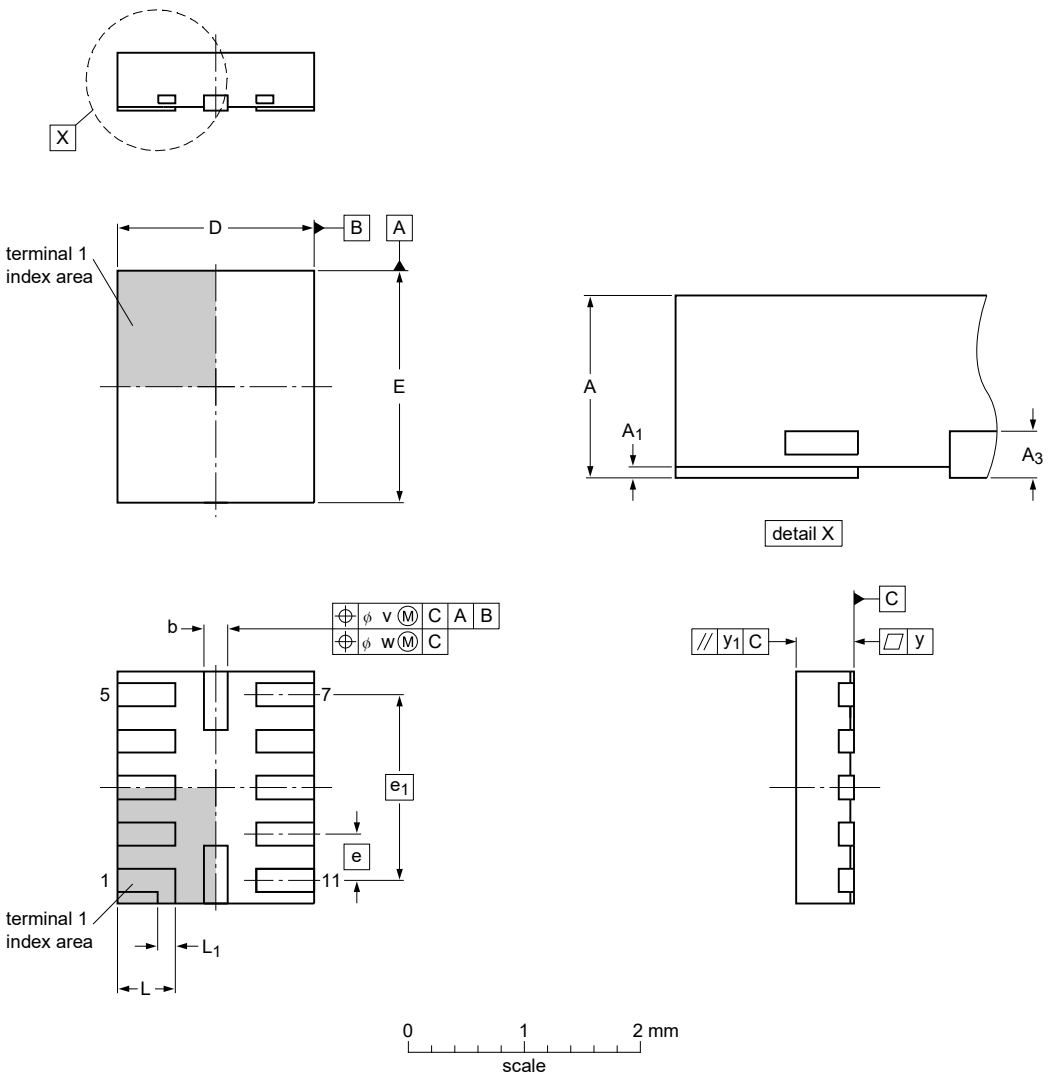
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Figure 12. Package outline SOT762-1 (DHVQFN14)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

XQFN12: plastic, extremely thin quad flat package; no leads; 12 terminals; body 1.70 x 2.00 x 0.50 mm **SOT1174-1**



Dimensions

Unit(1)		A	A_1	A_3	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05		0.25	1.8	2.1			0.55					
	nom			0.127	0.20	1.7	2.0	0.4	1.6	0.50	0.15	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.6	1.9			0.45					

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1174-1_po

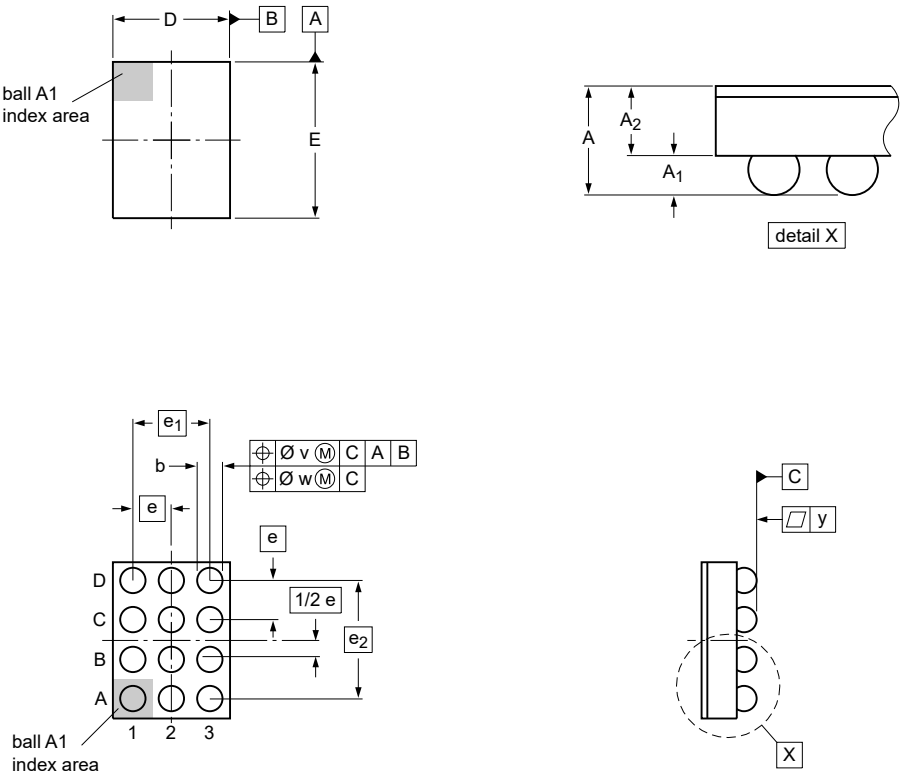
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1174-1	- - -	MO-288	- - -			10-04-07 10-04-21

Figure 13. Package outline SOT1174-1 (XQFN12)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

WLCSP12: wafer level chip-size package,
12 bumps; body 1.20 x 1.60 x 0.56 mm. (Backside Coating included) **NTB0104UK**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.615	0.23	0.385	0.29	1.23	1.63						
	nom	0.560	0.20	0.360	0.26	1.20	1.60	0.40	0.80	1.20	0.05	0.015	0.03
	min	0.505	0.17	0.335	0.23	1.17	1.57						

ntb0104uk_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
NTB0104UK						~~11-05-23~~ 11-06-16

Figure 14. Package outline WLCSP12 package

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

14 Footprint information

Footprint information for reflow soldering of DHVQFN14 package **SOT762-1**

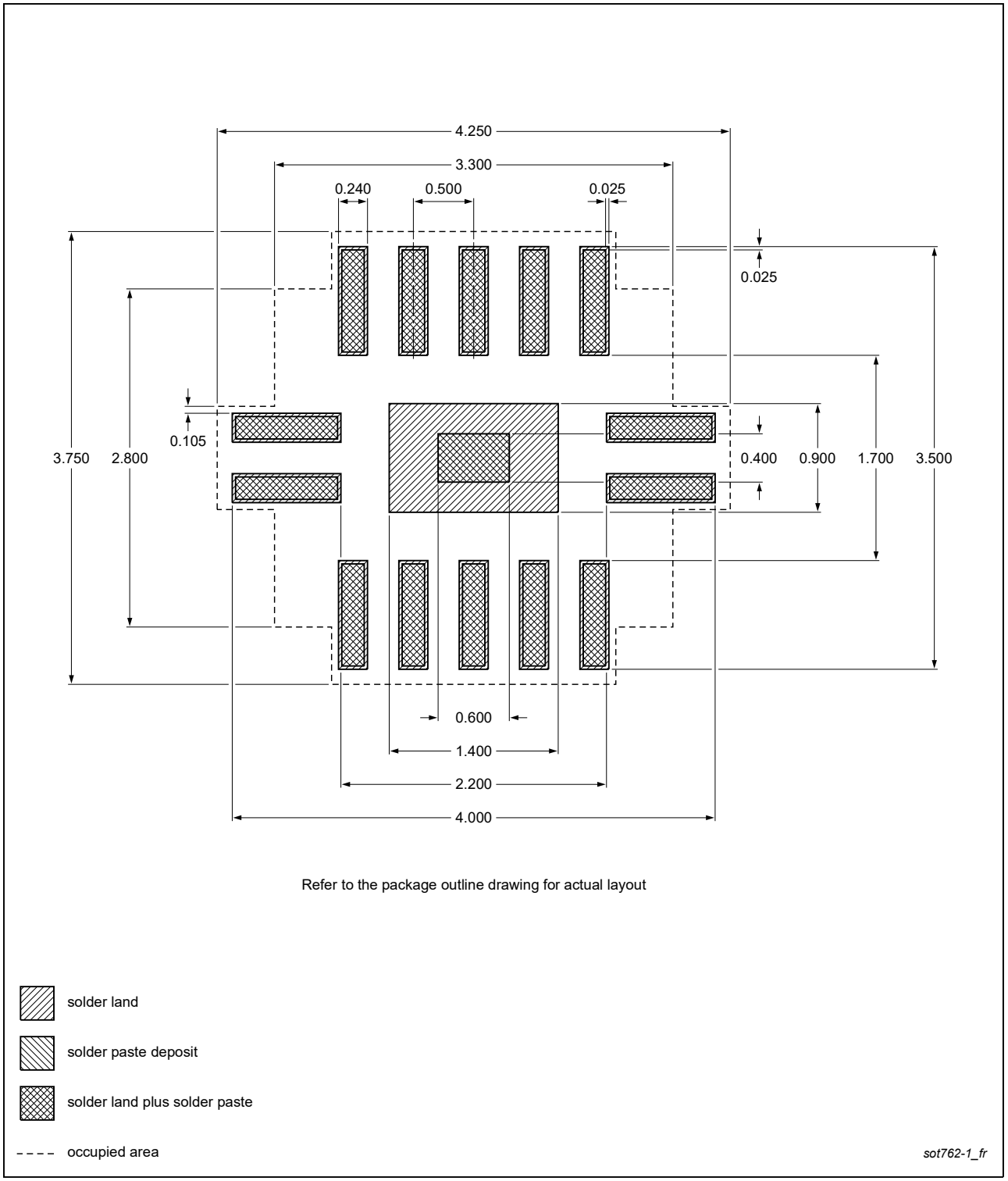


Figure 15. Footprint information for reflow soldering of SOT762-1 (DHVQFN14)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Footprint information for reflow soldering of XQFN12 package **SOT1174-1**

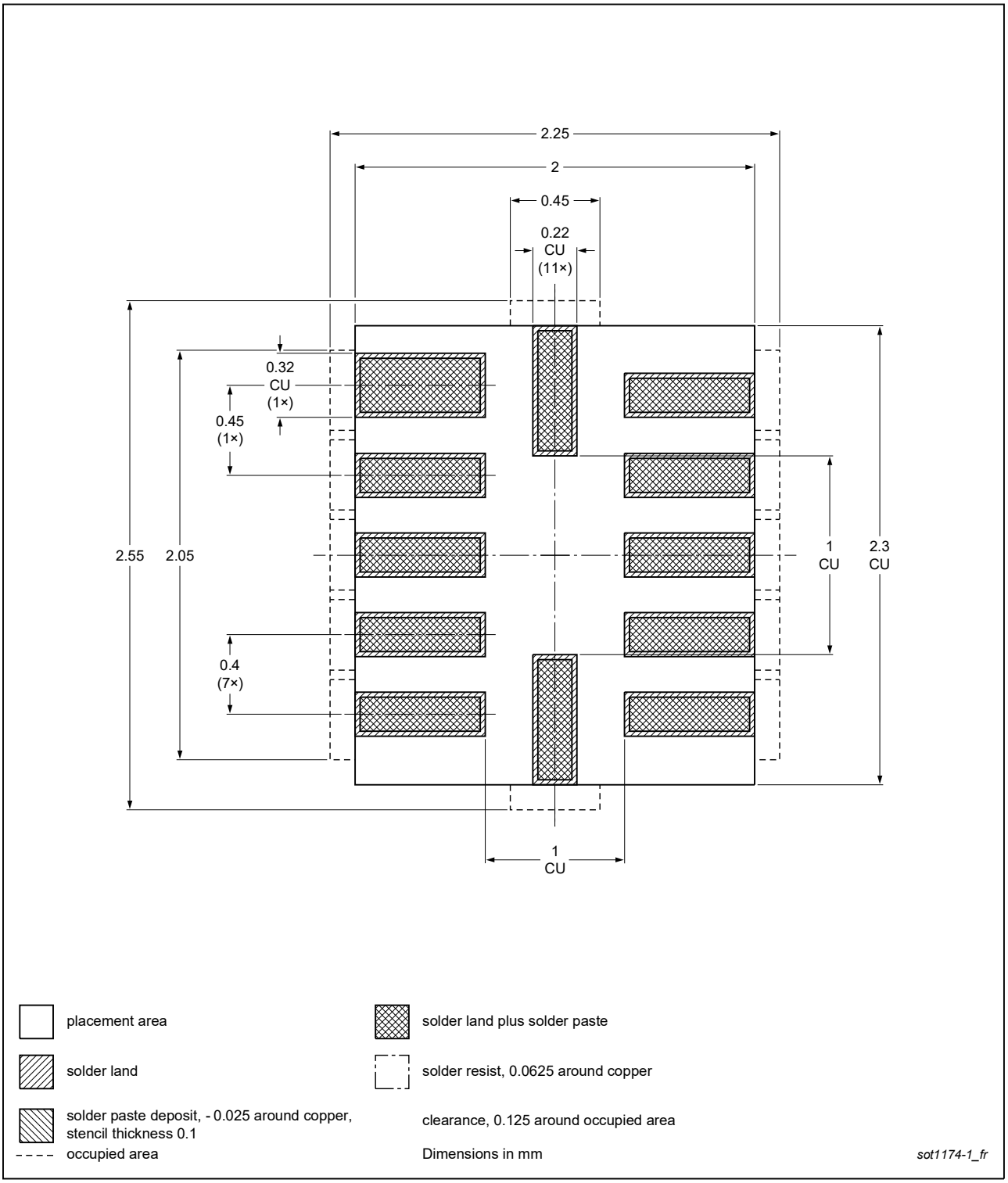


Figure 16. Footprint information for reflow soldering of SOT1174-1 (XQFN12)

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

15 Abbreviations

Table 16. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

16 Revision history

Table 17. Revision history

Document ID	Release date	Description
NTB0104 v.4.1	17 October 2024	• Table 2: Added last time buy/ship date for NTB0104UK • Table 9: Added internal 4 kΩ resistor min/max parameters
NTB0104 v.4	19 April 2018	• Figure 12: Added "k" heat pad to pin minimum gap dimension • Added Section 3.1, Section 14 • Removed Section 4 "Marking" • Added topside marking to Table 1
NTB0104 v.3	10 November 2011	• Legal pages updated.
NTB0104 v.2	9 November 2011	Product data sheet
NTB0104 v.1	26 October 2010	Product data sheet

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Tables

Tab. 1. Ordering information 3
Tab. 2. Ordering options 3
Tab. 3. Pin description 6
Tab. 4. Function table 7
Tab. 5. Limiting values 8
Tab. 6. Recommended operating conditions 9
Tab. 7. Typical static characteristics 10
Tab. 8. Typical supply current 10
Tab. 9. Static characteristics 11
Tab. 10. Typical dynamic characteristics for temperature 25 °C 13
Tab. 11. Dynamic characteristics for temperature range -40 °C to +85 °C 13
Tab. 12. Dynamic characteristics for temperature range -40 °C to +125 °C 15
Tab. 13. Typical power dissipation capacitance 17
Tab. 14. Measurement points 19
Tab. 15. Test data 20
Tab. 16. Abbreviations 29
Tab. 17. Revision history 30

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Figures

Fig. 1. Logic symbol 4
Fig. 2. Pin configuration DHVQFN14 (SOT762-1) 5
Fig. 3. Pin configuration XQFN12 (SOT1174-1) 5
Fig. 4. Pin configuration WLCSP12 package 5
Fig. 5. Ball mapping for WLCSP12 6
Fig. 6. The data input (An, Bn) to data output (Bn, An) propagation delay times 19
Fig. 7. Enable and disable times 19
Fig. 8. Test circuit for measuring switching times 20
Fig. 9. Typical operating circuit 21
Fig. 10. Architecture of NTB0104 I/O cell (one channel) 22
Fig. 11. Typical input current versus input voltage graph 22
Fig. 12. Package outline SOT762-1 (DHVQFN14) 24
Fig. 13. Package outline SOT1174-1 (XQFN12) 25
Fig. 14. Package outline WLCSP12 package 26
Fig. 15. Footprint information for reflow soldering of SOT762-1 (DHVQFN14) 27
Fig. 16. Footprint information for reflow soldering of SOT1174-1 (XQFN12) 28

All information provided in this document is subject to legal disclaimers.

© 2024 NXP B.V. All rights reserved.

Contents

1 General description 1
2 Features and benefits 2
3 Ordering information 3
3.1 Ordering options 3
4 Functional diagram 4
5 Pinning information 5
5.1 Pinning 5
5.2 Pin description 6
6 Functional description 7
7 Limiting values 8
8 Recommended operating conditions 9
9 Static characteristics 10
10 Dynamic characteristics 13
11 Waveforms 19
12 Application information 21
12.1 Applications 21
12.2 Architecture 21
12.3 Input driver requirements 22
12.4 Power up 22
12.5 Enable and disable 22
12.6 Pull-up or pull-down resistors on I/O lines 23
13 Package outline 24
14 Footprint information 27
15 Abbreviations 29
16 Revision history 30
Legal information 31

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© 2024 NXP B.V. **All rights reserved.**