74AHC123A; 74AHCT123A

Dual retriggerable monostable multivibrator with reset

Rev. 7 — 28 February 2024 Product data sheet

1. General description

The 74AHC123A; 74AHCT123A is a dual retriggerable monostable multivibrator with reset. The basic output pulse width is programmed by selection of external components (R_{EXT} and C_{EXT}). Once triggered this basic pulse width may be extended by retriggering either of the edge triggered inputs (n$\overline{A}$ or (nB). By repeating this process, the output pulse period (nQ = HIGH, n$\overline{Q}$ = LOW) can be made as long as desired. Alternatively, an output delay can be terminated at any time by a LOW-going edge on input n$\overline{R}$D. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses up to 100 % duty factor
- Direct reset terminates output pulse
- Overvoltage tolerant inputs to 5.5 V
- All inputs have a Schmitt-trigger action
- High noise immunity
- Input levels:
  - For 74AHC123A: CMOS level
  - For 74AHCT123A: TTL level
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC123AD 74AHCT123AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC123APW 74AHCT123APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC123ABQ 74AHCT123ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

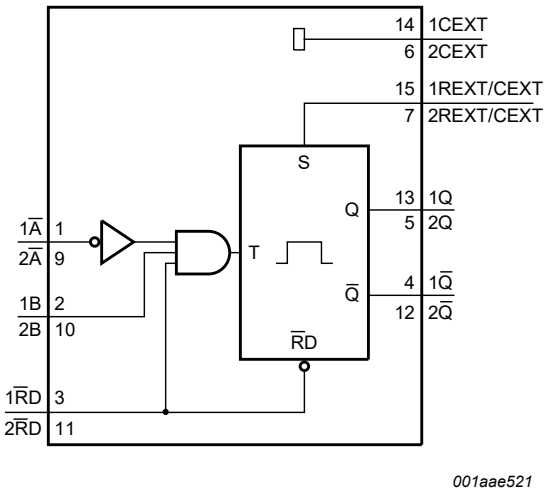


Fig. 1. Logic symbol

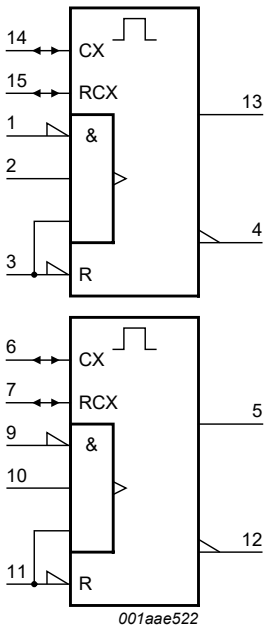


Fig. 2. IEC logic symbol

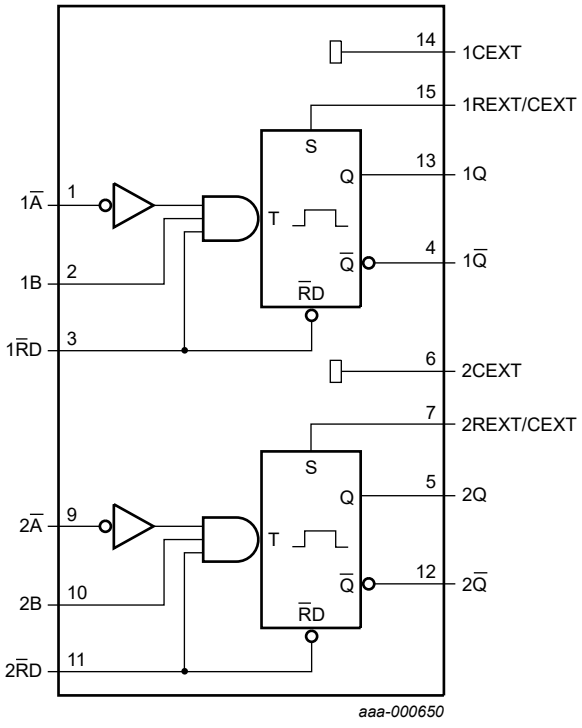
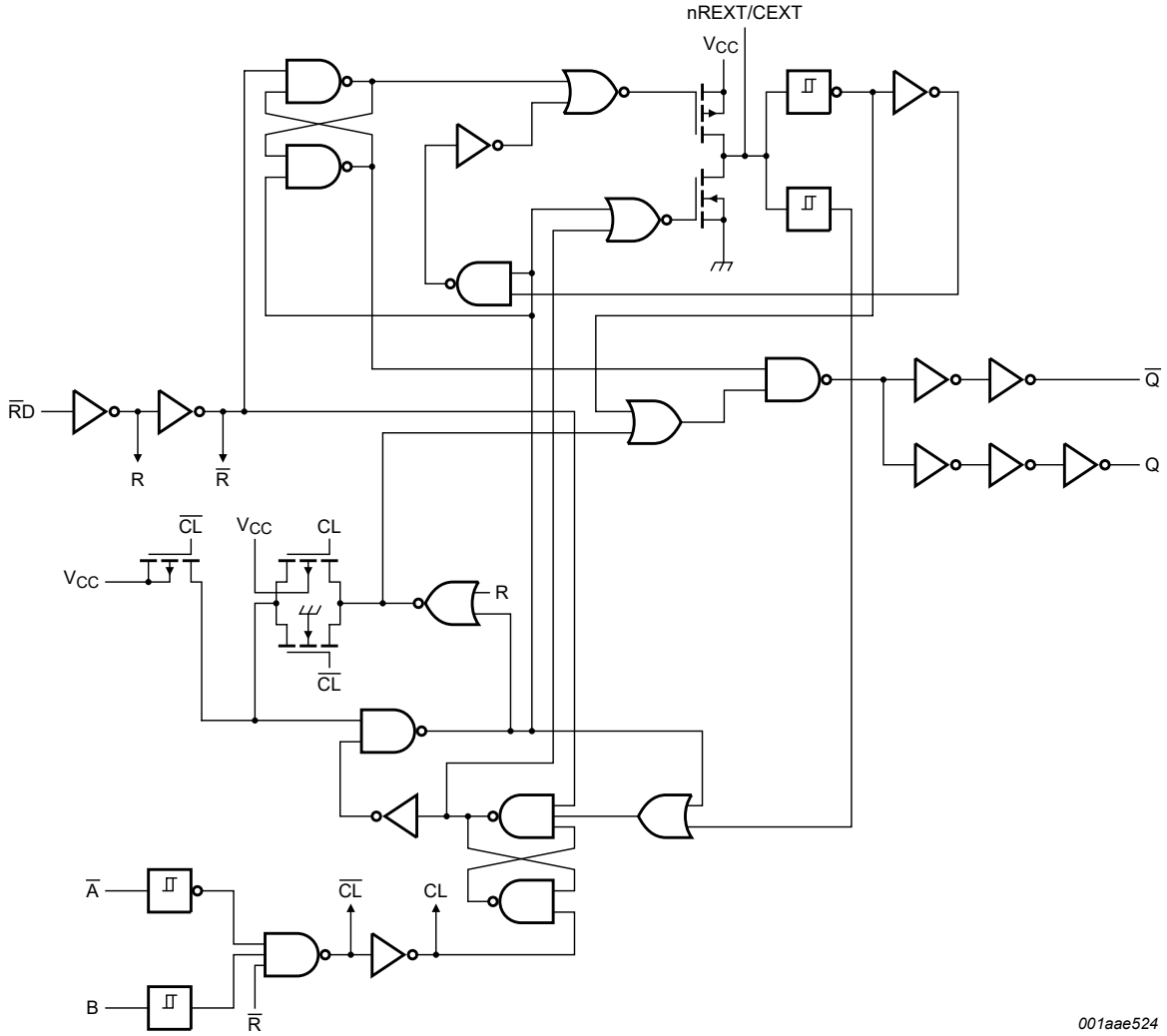


Fig. 3. Functional diagram

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For minimum noise generation it is recommended to ground pins 6 (2CEXT) and 14 (1CEXT) externally to pin 8 (GND).

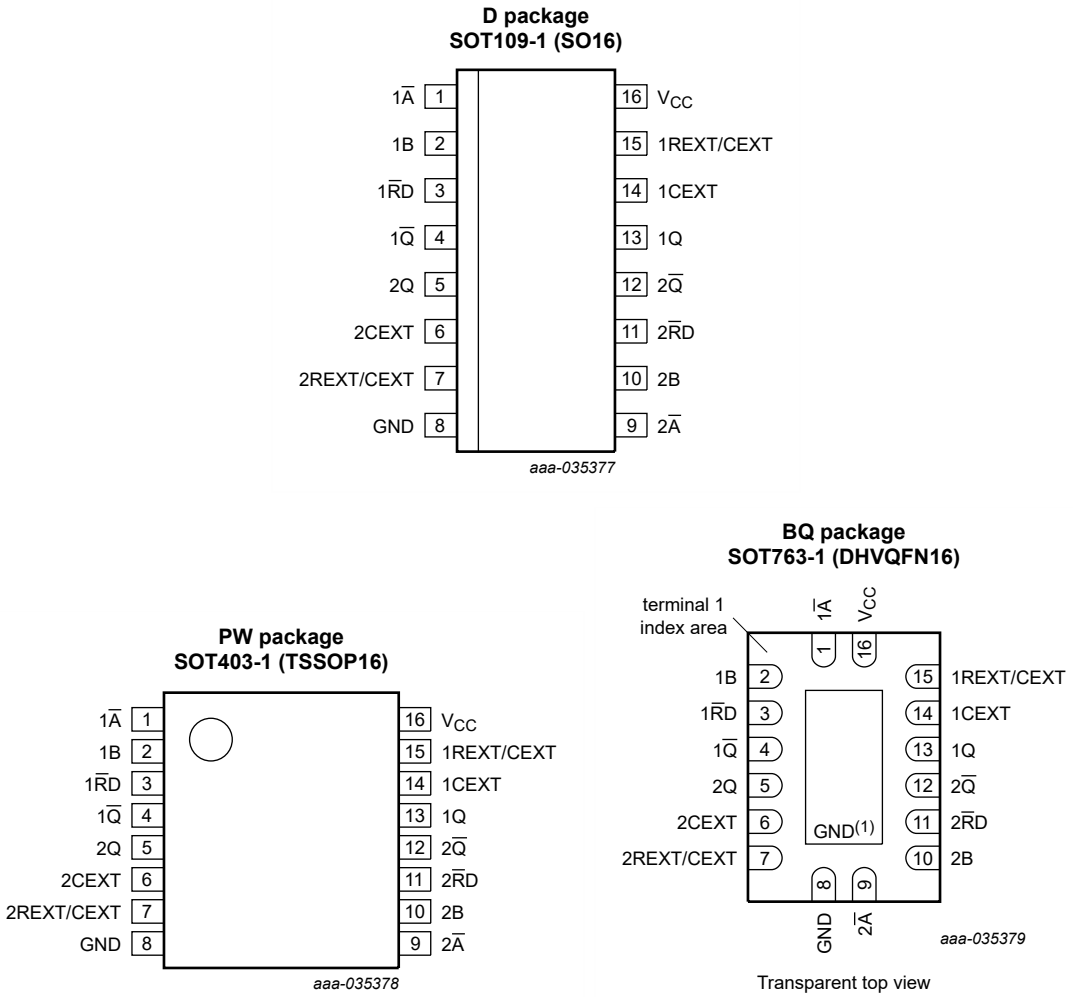
Fig. 4. Functional diagram

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5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

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5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{A}$	1	negative-edge triggered input 1
1B	2	positive-edge triggered input 1
$1\overline{R}D$	3	direct reset LOW and positive-edge triggered input 1
$1\overline{Q}$	4	active LOW output 1
2Q	5	active HIGH output 2
2CEXT	6	external capacitor connection 2
2REXT/CEXT	7	external resistor and capacitor connection 2
GND	8	ground (0 V)
$2\overline{A}$	9	negative-edge triggered input 2
2B	10	positive-edge triggered input 2
$2\overline{R}D$	11	direct reset LOW and positive-edge triggered input 2
$2\overline{Q}$	12	active LOW output 2
1Q	13	active HIGH output 1
1CEXT	14	external capacitor connection 1
1REXT/CEXT	15	external resistor and capacitor connection 1
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH transition;

↓ = HIGH-to-LOW transition;

⎍ *= one HIGH level output pulse;*

⎎ *= one LOW level output pulse.*

Input			Output	
n$\overline{R}$D	**n$\overline{A}$**	**nB**	**nQ**	**n$\overline{Q}$**
L	X	X	L	H
X	H	X	L [1]	H [1]
X	X	L	L [1]	H [1]
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

[1] If the monostable multivibrator was triggered before this condition was established, the pulse will continue as programmed.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC123A			74AHCT123A			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

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9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC123A										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V								
		nREXT/CEXT [1]	-	-	±0.25	-	±2.5	-	±10.0	µA
		pins nA, nB, nRD	-	-	±0.1	-	±1.0	-	±2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
		active state (per circuit); [1] V_I = V_{CC} or GND								
		V_{CC} = 3.0 V	-	160	250	-	280	-	280	µA
		V_{CC} = 4.5 V	-	380	500	-	650	-	650	µA
		V_{CC} = 5.5 V	-	560	750	-	975	-	975	µA
C_I	input capacitance		-	5.0	10	-	10	-	10	pF
C_O	output capacitance		-	4.0	-	-	-	-	-	pF

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Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHCT123A										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	nREXT/CEXT; [1] V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±0.25	-	±2.5	-	±10.0	µA
		pins n$\overline{A}$, nB, n$\overline{RD}$; V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±2.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
		active state (per circuit); [1] V_I = V_{CC} or GND								
		V_{CC} = 4.5 V	-	380	500	-	650	-	650	µA
		V_{CC} = 5.5 V	-	560	750	-	975	-	975	µA
C_I	input capacitance		-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4.0	-	-	-	-	-	pF

[1] Voltage on nREXT/CEXT = 0.5 × V_{CC} and pin nREXT/CEXT in OFF-state during test.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; For test circuit see Fig. 10.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC123A										
t_{pd}	propagation delay	$n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	7.4	20.6	1.0	24.0	1.0	26.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	10.5	24.1	1.0	27.5	1.0	30.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	5.1	12.0	1.0	14.0	1.0	15.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	7.3	14.0	1.0	16.0	1.0	17.5	ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$; see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	8.2	22.4	1.0	26.0	1.0	28.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	11.7	25.9	1.0	29.5	1.0	32.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	5.6	12.9	1.0	15.0	1.0	16.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	8.1	14.9	1.0	17.0	1.0	19.0	ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$ (reset); see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V; C_L = 15 pF	-	6.4	15.8	1.0	18.5	1.0	20.0	ns
		V_{CC} = 3.0 V to 3.6 V; C_L = 50 pF	-	9.2	19.3	1.0	22.0	1.0	24.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.4	9.4	1.0	11.0	1.0	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	6.3	11.4	1.0	13.0	1.0	14.5	ns
t_W	pulse width	inputs; $n\overline{A}$ = LOW; see Fig. 5								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nB = HIGH; see Fig. 5								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; $n\overline{R}D$ = LOW; see Fig. 5								
		V_{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		outputs; $n\overline{Q}$ = LOW and nQ = HIGH; C_L = 50 pF; see Fig. 5, Fig. 6, Fig. 7 and Fig. 8 [3]								
		C_{EXT} = 28 pF; R_{EXT} = 2 kΩ								
		V_{CC} = 3.0 V to 3.6 V	-	115	240	-	300	-	300	ns
		V_{CC} = 4.5 V to 5.5 V	-	100	200	-	240	-	240	ns
		C_{EXT} = 0.01 µF; R_{EXT} = 10 kΩ								
		V_{CC} = 3.0 V to 3.6 V	90	100	110	90	110	85	115	µs
		V_{CC} = 4.5 V to 5.5 V	90	100	110	90	110	85	115	µs
		C_{EXT} = 0.1 µF; R_{EXT} = 10 kΩ;								
		V_{CC} = 3.0 V to 3.6 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms
		V_{CC} = 4.5 V to 5.5 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms

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Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rtrig}	retrigger time	$n\overline{A}$ to nB; C_{EXT} = 100 pF; R_{EXT} = 1 kΩ; C_L = 50 pF; see Fig. 6 and Fig. 8								
		V_{CC} = 3.0 V to 3.6 V	-	60	-	-	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	-	39	-	-	-	-	-	ns
		$n\overline{A}$ to nB; C_{EXT} = 0.01 µF; R_{EXT} = 1 kΩ; C_L = 50 pF; see Fig. 6 and Fig. 8								
		V_{CC} = 3.0 V to 3.6 V	-	1.5	-	-	-	-	-	µs
		V_{CC} = 4.5 V to 5.5 V	-	1.2	-	-	-	-	-	µs
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	57	-	-	-	-	-	pF
74AHCT123A										
t_{pd}	propagation delay	$n\overline{A}$ and nB to nQ and $n\overline{Q}$; see Fig. 5 [2]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	5.0	12.0	1.0	14.0	1.0	15.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	7.1	14.0	1.0	16.0	1.0	17.5	ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$; see Fig. 5 [2]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	5.2	12.9	1.0	15.0	1.0	16.5	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	7.5	14.9	1.0	17.0	1.0	18.5	ns
		$n\overline{R}D$ to nQ and $n\overline{Q}$ (reset); see Fig. 5 [2]								
		V_{CC} = 4.5 V to 5.5 V; C_L = 15 pF	-	4.7	9.4	1.0	11.0	1.0	12.0	ns
		V_{CC} = 4.5 V to 5.5 V; C_L = 50 pF	-	6.7	11.4	1.0	13.0	1.0	14.5	ns
t_W	pulse width	inputs; $n\overline{A}$ = LOW; C_L = 50 pF; see Fig. 5								
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; nB = HIGH; C_L = 50 pF; see Fig. 5								
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		inputs; $n\overline{R}D$ = LOW; C_L = 50 pF; see Fig. 5								
		V_{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
		outputs; $n\overline{Q}$ = LOW and nQ = HIGH; C_L = 50 pF; C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; see Fig. 5, Fig. 6, Fig. 7 and Fig. 8 [3]								
		V_{CC} = 4.5 V to 5.5 V	-	100	200	-	240	-	240	ns
		C_{EXT} = 0.01 µF; R_{EXT} = 10 kΩ								
		V_{CC} = 4.5 V to 5.5 V	90	100	110	90	110	85	115	µs
		C_{EXT} = 0.1 µF; R_{EXT} = 10 kΩ								
		V_{CC} = 4.5 V to 5.5 V	0.9	1	1.1	0.9	1.1	0.85	1.15	ms

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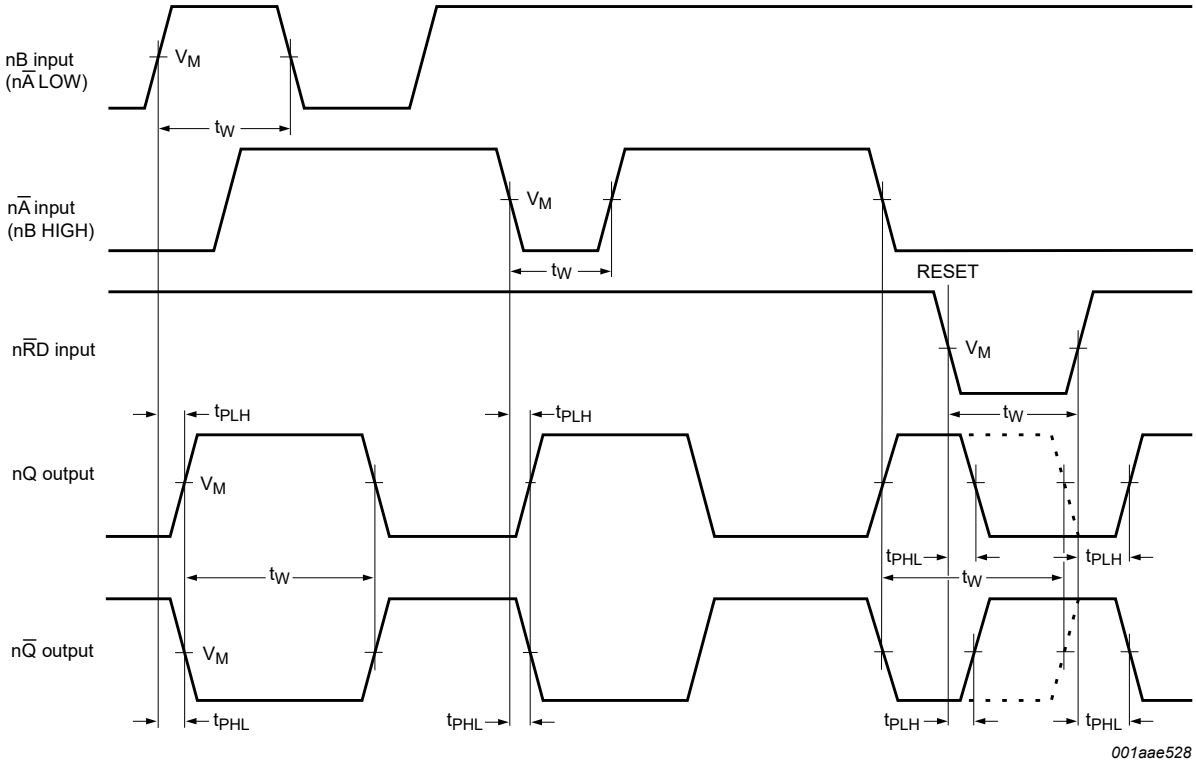
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rtrig}	retrigger time	$n\overline{A}$ to nB; C_{EXT} = 100 pF; R_{EXT} = 1 kΩ; C_L = 50 pF; see Fig. 6 and Fig. 8								
		V_{CC} = 4.5 V to 5.5 V	-	60	-	-	-	-	-	ns
		$n\overline{A}$ to nB; C_{EXT} = 0.01 µF; R_{EXT} = 1 kΩ; C_L = 50 pF; see Fig. 6 and Fig. 8								
		V_{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	-	-	µs
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [4]	-	58	-	-	-	-	-	pF
External components										
R_{EXT}	external resistance	V_{CC} = 2.0 V	5	-	-	-	-	-	-	kΩ
		V_{CC} > 3.0 V	1	-	-	-	-	-	-	kΩ
C_{EXT}	external capacitance	V_{CC} = 2.0 V [5]	-	-	-	-	-	-	-	pF
		V_{CC} > 3.0 V [5]	-	-	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}; C_{EXT} = 0 pF; R_{EXT} = 5 kΩ.
[3] For $C_{EXT} \geq 10$ nF the typical value of the pulse width t_W (µs) = C_{EXT} (nF) × R_{EXT} (kΩ).
[4] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.
[5] C_{EXT} has no limits.

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10.1. Waveforms and test circuit

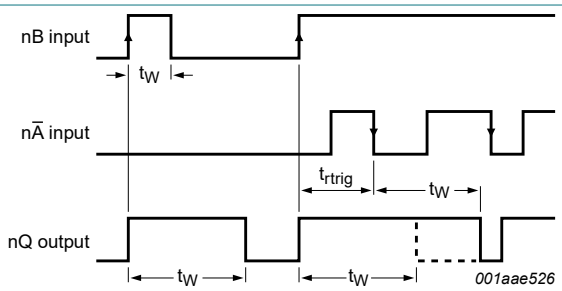


Measurement points are given in Table 8.

Fig. 5. Propagation delay input (nA, nB, nRD) to output (nQ, nQ)

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC123A	0.5 × V_{CC}	0.5 × V_{CC}
74AHCT123A	1.5 V	0.5 × V_{CC}

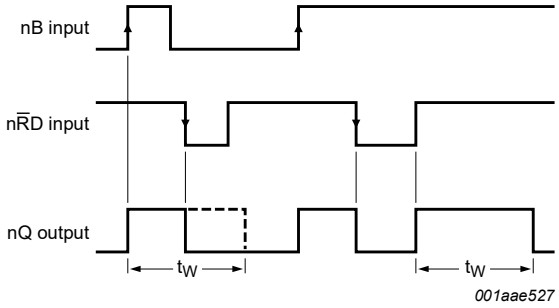


nRD = HIGH

Fig. 6. Output pulse control using retrigger pulse

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nA̅ = LOW

Fig. 7. Output pulse control using reset input nR̄D

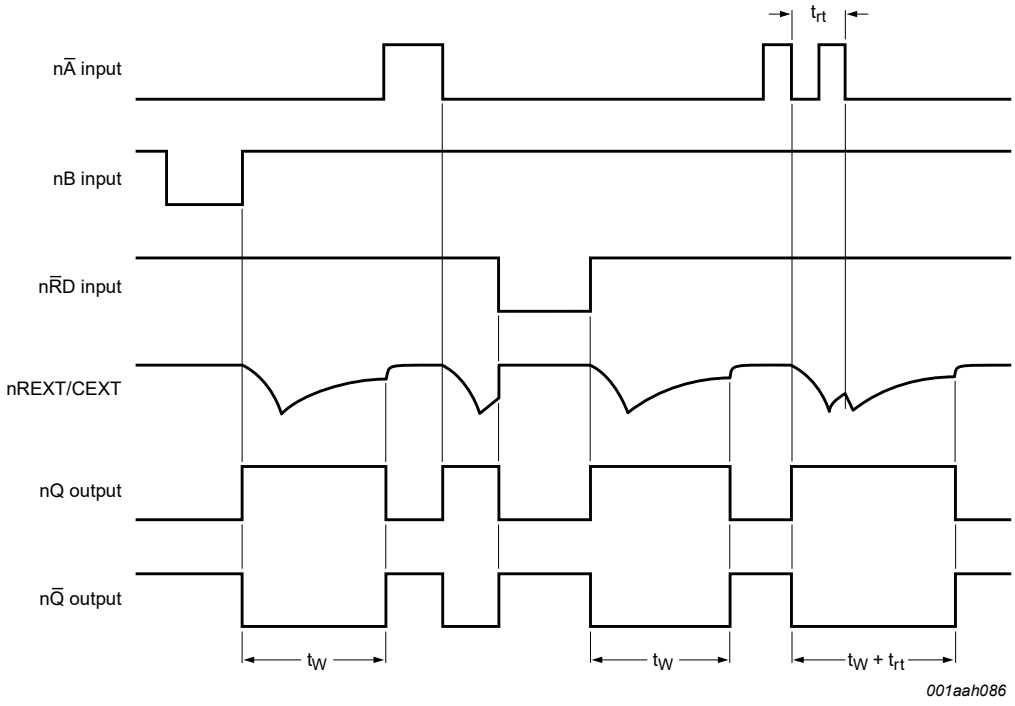


Fig. 8. Input and output timing

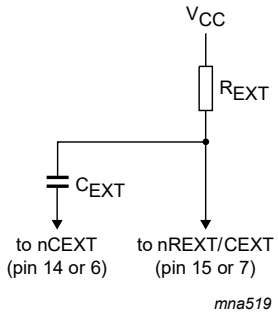
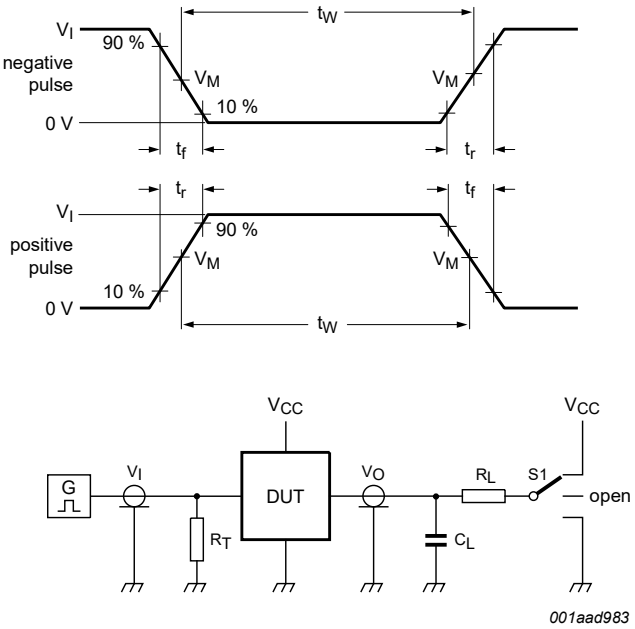


Fig. 9. Timing component connections

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Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance

S1 = Test selection switch

Fig. 10. Test circuit for measuring switching times

Table 9. Test data

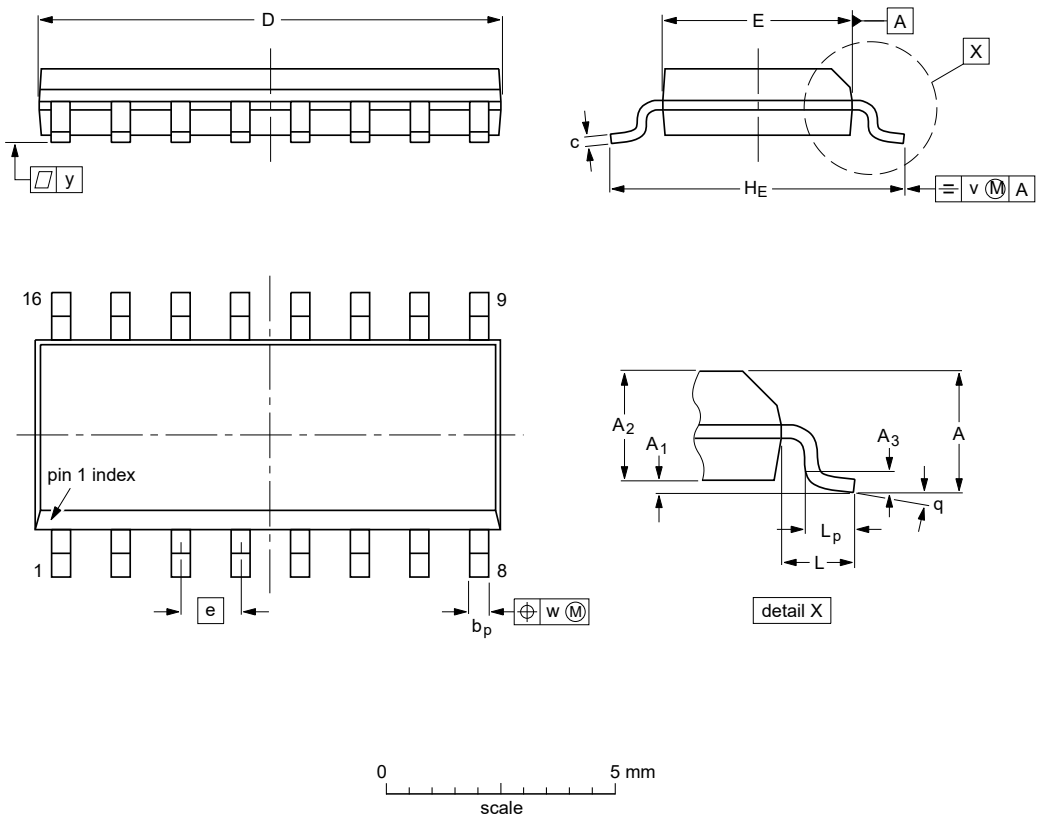
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC123A	V_{CC}	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT123A	3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

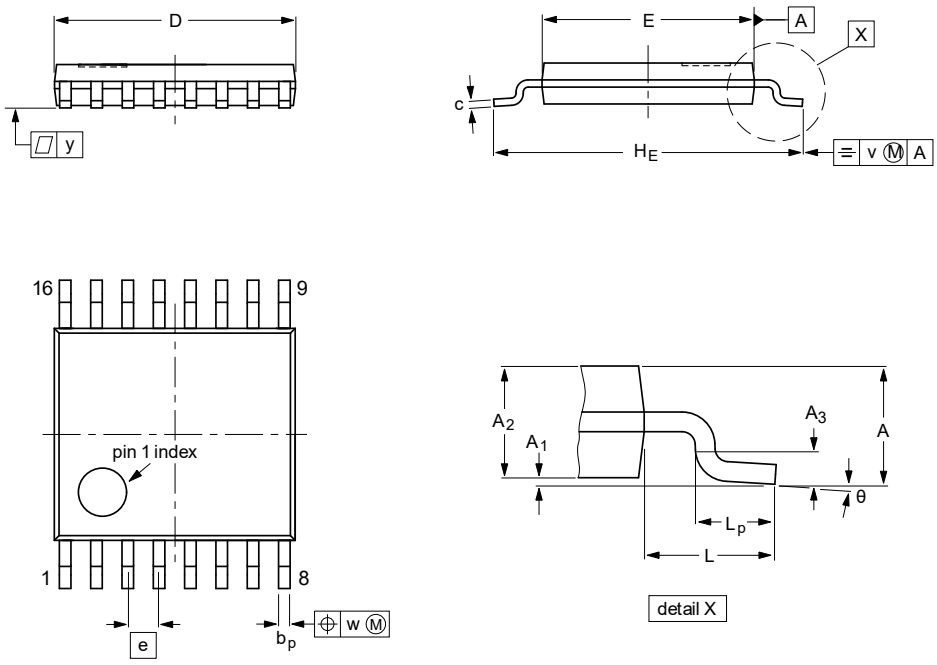
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

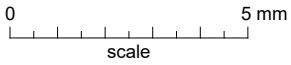
Fig. 11. Package outline SOT109-1 (SO16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

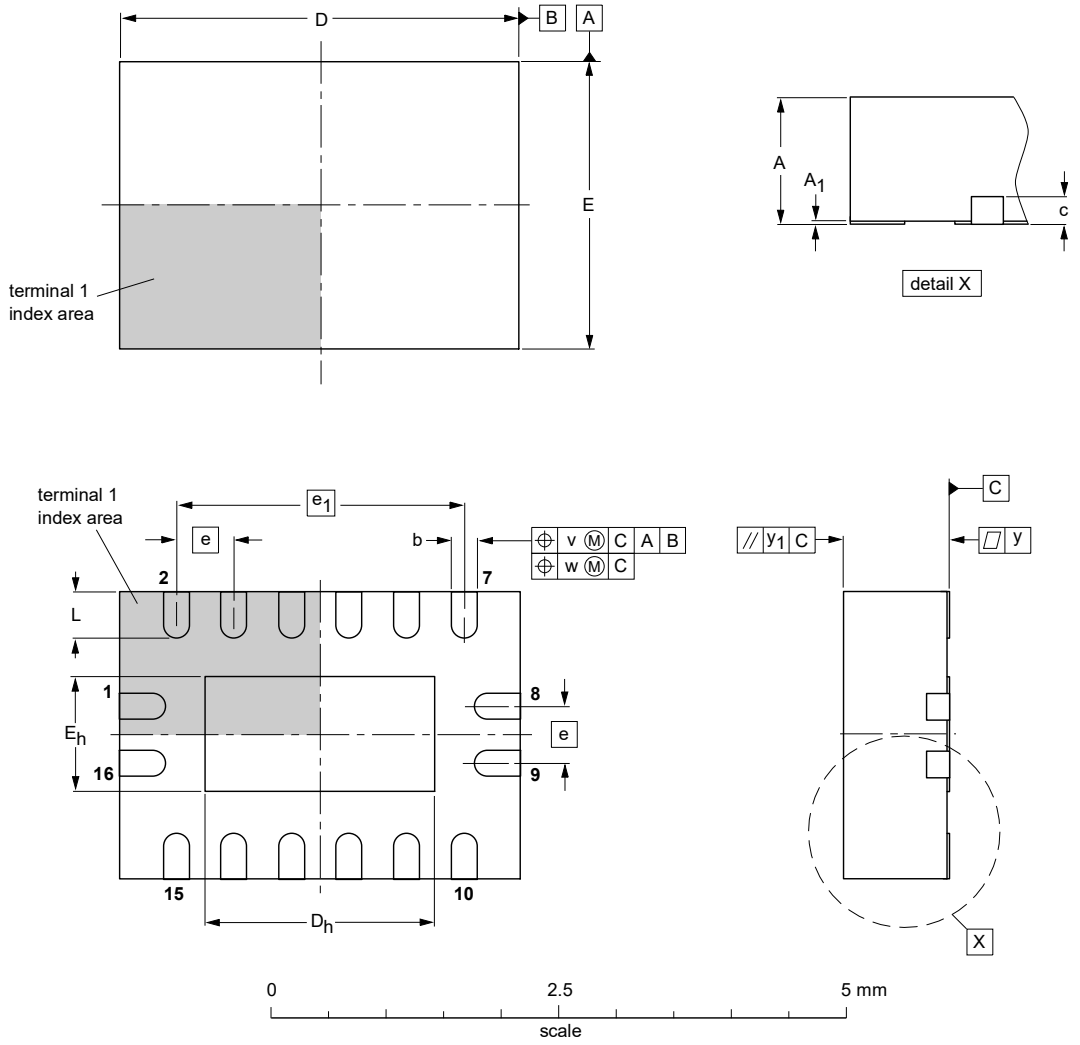
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 12. Package outline SOT403-1 (TSSOP16)

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DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 13. Package outline SOT763-1 (DHVQFN16)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT123A v.7	20240228	Product data sheet	-	74AHC_AHCT123A v.6
Modifications:	• Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74AHC_AHCT123A v.6	20230904	Product data sheet	-	74AHC_AHCT123A v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AHC_AHCT123A v.5	20200617	Product data sheet	-	74AHC_AHCT123A v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74AHC_AHCT123A v.4	20111108	Product data sheet	-	74AHC_AHCT123A v.3
Modifications:	• Legal pages updated.			
74AHC_AHCT123A v.3	20110908	Product data sheet	-	74AHC_AHCT123A v.2
74AHC_AHCT123A v.2	20080118	Product data sheet	-	74AHC_AHCT123A v.1
74AHC_AHCT123A v.1	20000315	Product specification	-	-

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Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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