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# PDTA115EMB

## PNP resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ

Rev. 1 — 1 June 2012 Product data sheet

## 1. Product profile

### 1.1 General description

PNP Resistor-Equipped Transistor (RET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC115EMB.

### 1.2 Features and benefits

- 20 mA output current capability
- Reduces component count
- Built-in bias resistors
- Reduces pick and place costs
- Simplifies circuit design
- AEC-Q101 qualified
- Leadless ultra small SMD plastic package
- Low package height of 0.37 mm

### 1.3 Applications

- Low-current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications
- Mobile applications

### 1.4 Quick reference data

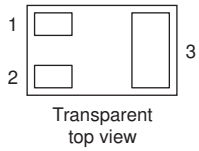
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | -50 | V |
| $I_O$ | output current | | - | - | -20 | mA |
| R1 | bias resistor 1 (input) | $T_{amb}$ = 25 °C | 70 | 100 | 130 | kΩ |
| R2/R1 | bias resistor ratio | | 0.8 | 1 | 1.2 | |

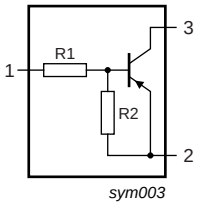
## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | I | input (base) | | |
| 2 | G | GND (emitter) | | |
| 3 | O | output (collector) | | |




**SOT883B (DFN1006B-3)**




## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PDTA115EMB | DFN1006B-3 | Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm | SOT883B |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PDTA115EMB | 0010 0000 |

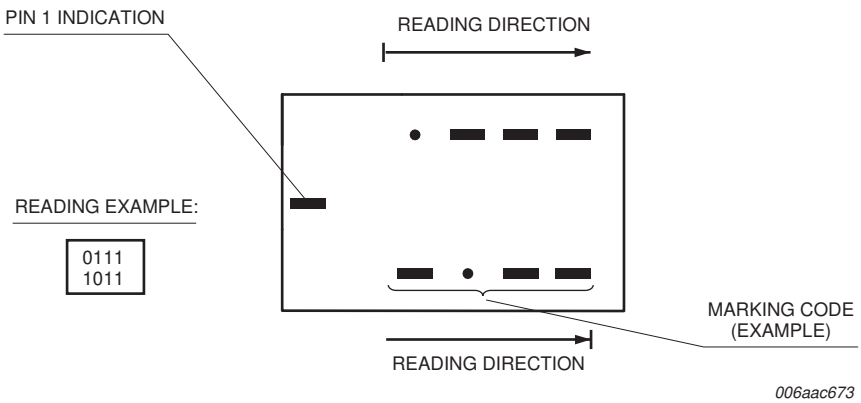



**Fig 1. DFN1006B-3 (SOT883B) binary marking code description**


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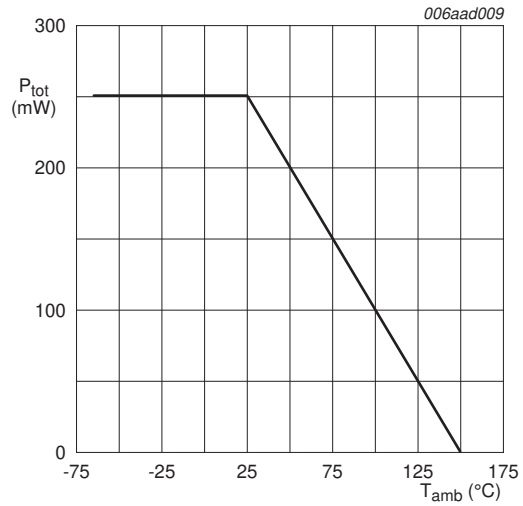
# 5. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CBO}$ | collector-base voltage | open emitter | | - | -50 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | -50 | V |
| $V_{EBO}$ | emitter-base voltage | open collector | | - | -10 | V |
| $V_I$ | input voltage | positive | | - | 10 | V |
| | | negative | | - | -40 | V |
| $I_O$ | output current | | | - | -20 | mA |
| $I_{CM}$ | peak collector current | pulsed; $t_p \leq 1$ ms | | - | -100 | mA |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 250 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | -65 | 150 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.




FR4 PCB, standard footprint

**Fig 2. Power derating curve for DFN1006B-3 (SOT883B)**

# 6. Thermal characteristics

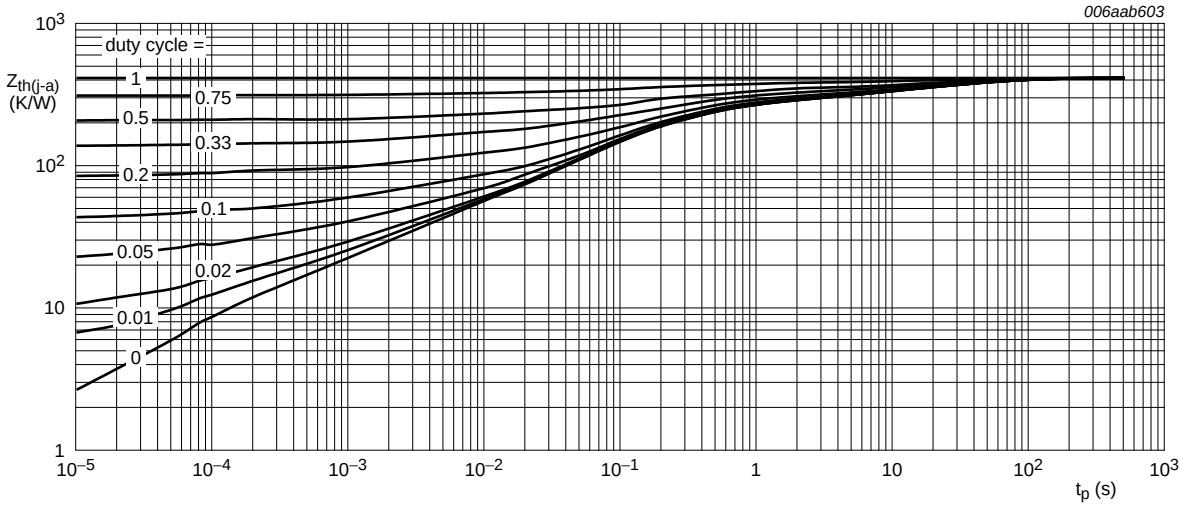
**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 500 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.


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FR4 PCB, standard footprint

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

# 7. Characteristics

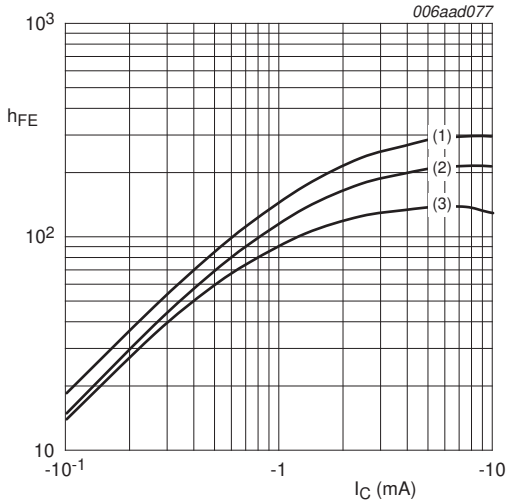
**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = -50 V; $I_E$ = 0 A; $T_{amb}$ = 25 °C | | - | - | -100 | nA |
| $I_{CEO}$ | collector-emitter cut-off current | $V_{CE}$ = -30 V; $I_B$ = 0 A; $T_{amb}$ = 25 °C | | - | - | -1 | µA |
| | | $V_{CE}$ = -30 V; $I_B$ = 0 A; $T_j$ = 150 °C | | - | - | -5 | µA |
| $I_{EBO}$ | emitter-base cut-off current | $V_{EB}$ = -5 V; $I_C$ = 0 A; $T_{amb}$ = 25 °C | | - | - | -50 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = -5 V; $I_C$ = -5 mA; $T_{amb}$ = 25 °C | | 80 | - | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = -5 mA; $I_B$ = -0.25 mA; $T_{amb}$ = 25 °C | | - | - | -150 | mV |
| $V_{I(off)}$ | off-state input voltage | $V_{CE}$ = -5 V; $I_C$ = -100 µA; $T_{amb}$ = 25 °C | | - | -1.2 | -0.5 | V |
| $V_{I(on)}$ | on-state input voltage | $V_{CE}$ = -0.3 V; $I_C$ = -1 mA; $T_{amb}$ = 25 °C | | -3 | -1.6 | - | V |
| R1 | bias resistor 1 (input) | $T_{amb}$ = 25 °C | | 70 | 100 | 130 | kΩ |
| R2/R1 | bias resistor ratio | | | 0.8 | 1 | 1.2 | |
| $C_C$ | collector capacitance | $V_{CB}$ = -10 V; $I_E$ = 0 A; $i_e$ = 0 A; f = 1 MHz; $T_{amb}$ = 25 °C | | - | - | 3 | pF |
| $f_T$ | transition frequency | $V_{CE}$ = -5 V; $I_C$ = -10 mA; f = 100 MHz; $T_{amb}$ = 25 °C | [1] | - | 180 | - | MHz |

[1] Characteristics of built-in transistor.


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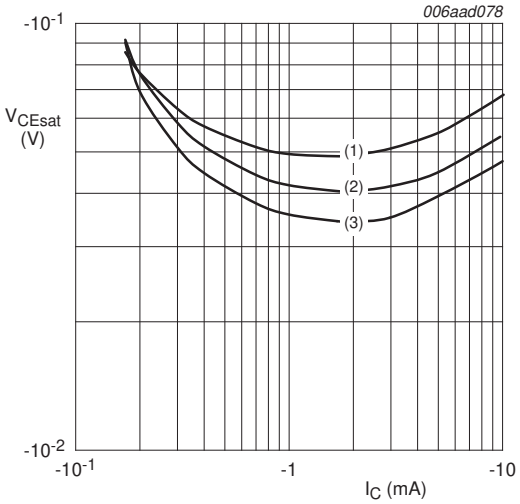

$V_{CE}$ = -5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = -40 °C

**Fig 4. DC current gain as a function of collector current; typical values**



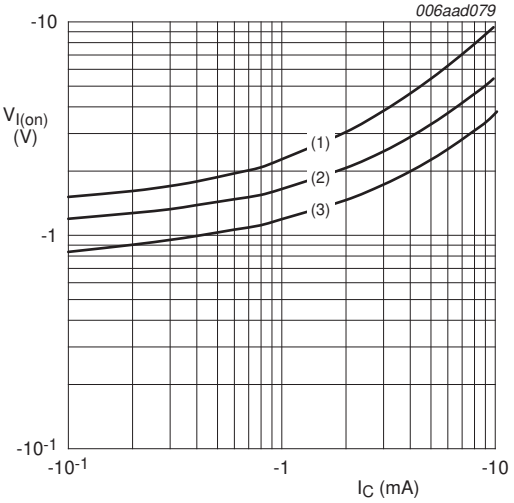

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = -40 °C

**Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values**



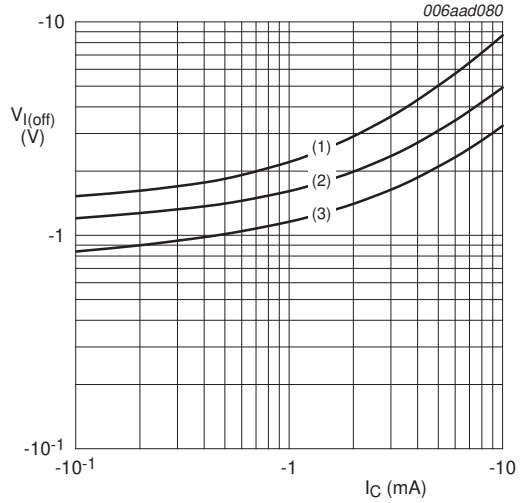

$V_{CE}$ = -0.3 V

(1) $T_{amb}$ = -40 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 6. On-state input voltage as a function of collector current; typical values**




$V_{CE}$ = -5 V

(1) $T_{amb}$ = -40 °C

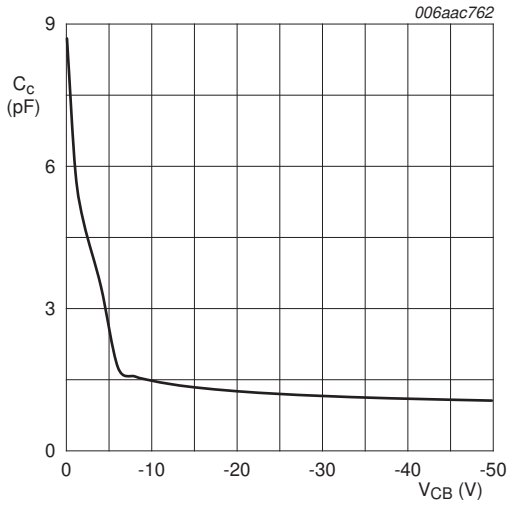
(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 7. Off-state input voltage as a function of collector current; typical values**

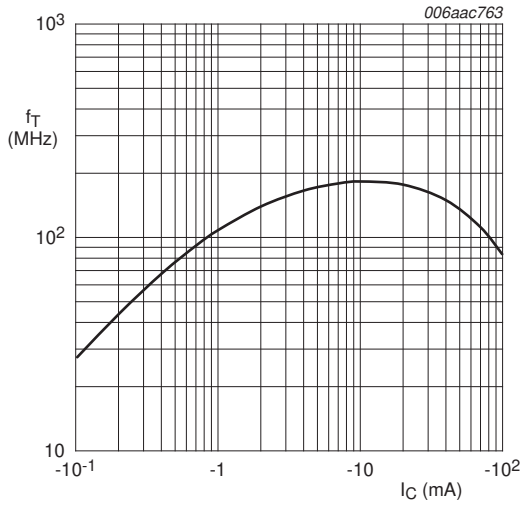

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f = 1 MHz; $T_{amb}$ = 25 °C

**Fig 8. Collector capacitance as a function of collector-base voltage; typical values of built-in transistor**




$V_{CE}$ = -5 V; $T_{amb}$ = 25 °C

**Fig 9. Transition frequency as a function of collector current; typical values of built-in transistor**

# 8. Test information

## 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.


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## 9. Package outline

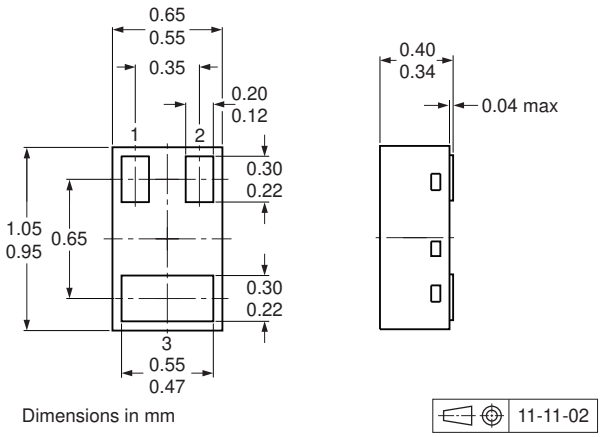



**Fig 10. Package outline SOT883B (DFN1006B-3)**

## 10. Soldering

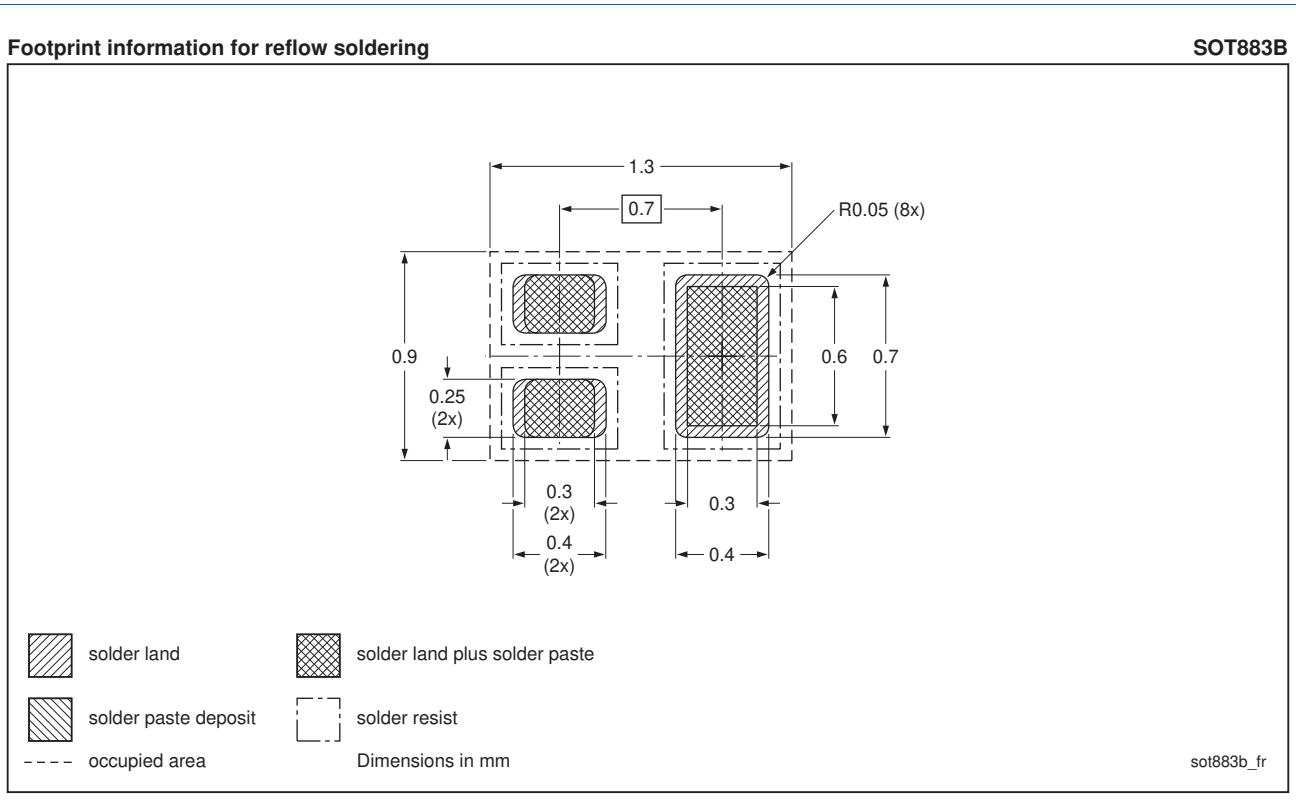



**Fig 11. Reflow soldering footprint for SOT883B (DFN1006B-3)**


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## 11. Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PDTA115EMB v.1 | 20120601 | Product data sheet | - | - |


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