## Description

The PI4IOE5V96224 provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I²C-bus) and is a part of the Fast-mode Plus family.

The PI4IOE5V96224 supports high I²C-bus drive (25mA) so that many more devices can be on the bus without the need for bus buffers, high total package sink capacity (600mA) that supports having all 25mA LEDs on at the same time and more device addresses (64) are available to allow many more devices on the bus without address conflicts.

The device consists of a 24-bit quasi-bidirectional port and an I²C-bus interface. The PI4IOE5V96224 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs.

It also possesses an interrupt line ( $\overline{\text{INT}}$ ) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I²C-bus. The internal Power-On Reset (POR) or software reset sequence initializes the I/Os as inputs.

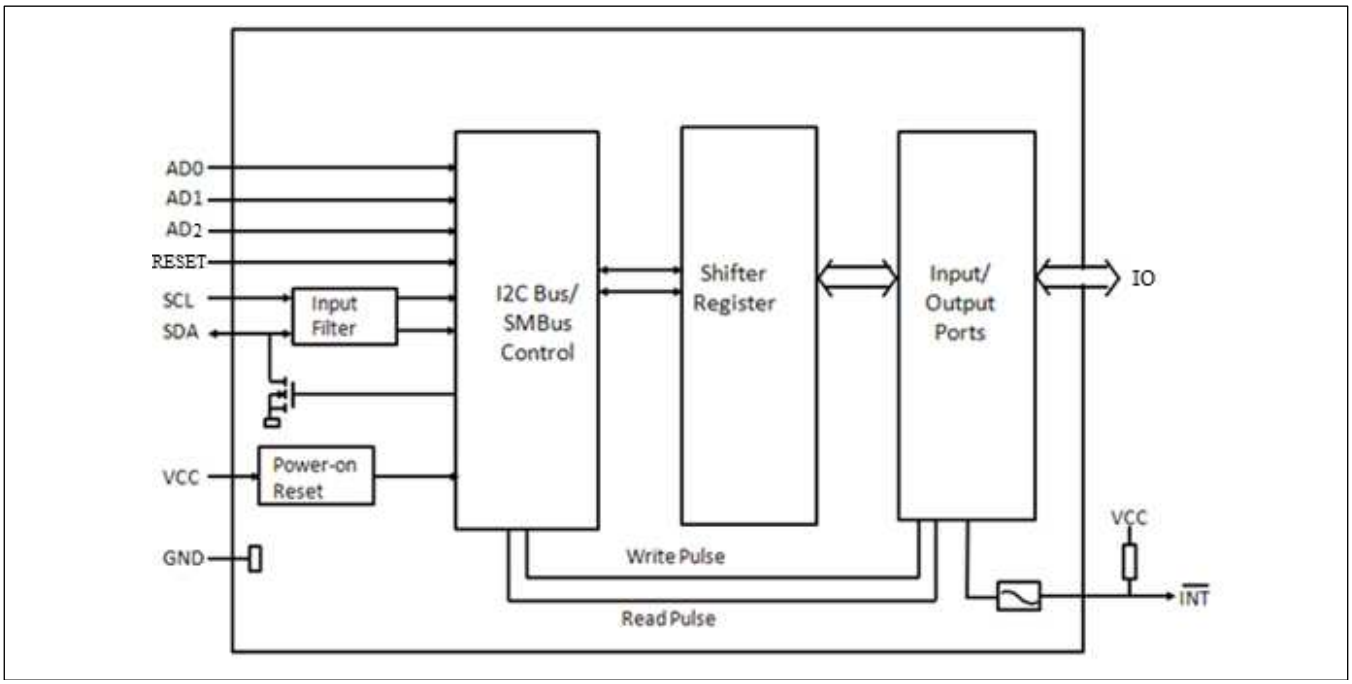
## Features

- Operation power supply voltage from 2.3V to 5.5V
- 24-bit remote I/O pins that default to inputs at power-up
- 1MHz I²C-bus interface
- Compliant with the I²C-bus Fast and Standard modes
- 5.0V tolerant I/Os
- SDA with 30mA sink capability for 4000pF buses
- Latched outputs with 25mA sink capability for directly driving LEDs
- Total package sink capability of 600mA
- Active LOW open-drain interrupt output
- Low standby current
- 64 programmable slave addresses using 3 address pins
- ESD protection (4KV HBM and 1KV CDM)
- Latch-up tested (exceeds 100mA)
- Packaging (Pb-free & Green):
  - 32-Pin, 3mm x 6mm, TQFN (ZL)
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

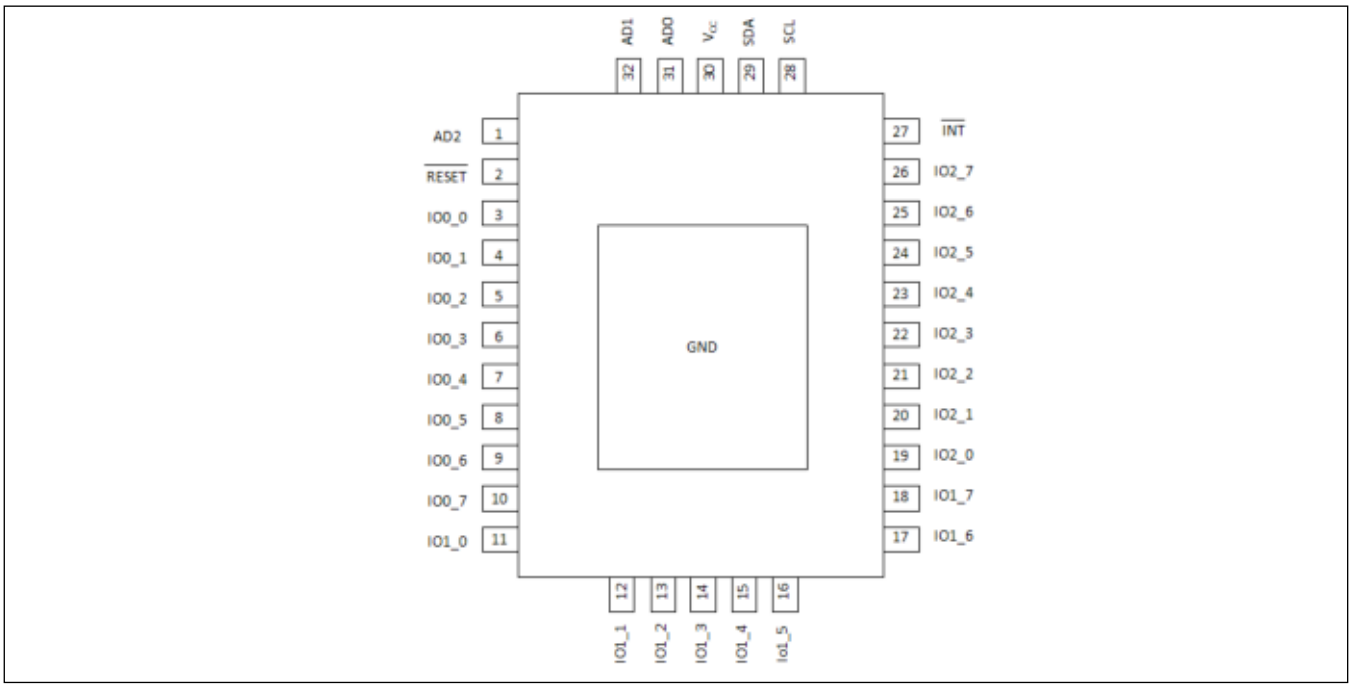
## Block Diagram




Note: All I/Os are set to inputs at reset.


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Pin Configuration




## Pin Description

| Pin Number | Name | Type | Description |
|---|---|---|---|
| 1 | AD2 | I | Address input 2 |
| 2 | $\overline{\text{RESET}}$ | I | RESET |
| 3 - 10 | IO0_0 – IO0_7 | I/O | Port 0 input/output 0 - 7 |
| 11 – 18 | IO1_0 – IO1_7 | I/O | Port 1 input/output 0 - 7 |
| 19 - 26 | IO2_0 – IO2_7 | I/O | Port 2 input/output 0 - 7 |
| 27 | $\overline{\text{INT}}$ | O | Interrupt output (open-drain) |
| 28 | SCL | I | Serial clock line input |
| 29 | SDA | I | Serial data line open-drain |
| 30 | VCC | P | Supply voltage |
| 31 | AD0 | I | Address input 0 |
| 32 | AD1 | I | Address input 1 |
| Thermal Pad | GND | G | Ground |

* I = Input; O = Output; P = Power; G = Ground


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Maximum Ratings

| | |
|---|---|
| Power Supply | -0.5V to +6.0V |
| Voltage on an I/O Pin | GND-0.5V to +6.0V |
| Input Current | ±20mA |
| Output Current on an I/O Pin | ±50mA |
| Supply Current | ±160mA |
| Ground Supply Current | 800mA |
| Total Power Dissipation | 600mW |
| Operation Temperature | -40~85°C |
| Storage Temperature | -65~150°C |
| Maximum Junction Temperature, Tj (max) | 125°C |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Static characteristics

$V_{CC}$ = 2.3V to 5.5V; GND = 0; $T_{amb}$ = -40°C to +85°C; unless otherwise specified.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Power supply** | | | | | | |
| VCC | Supply voltage | | 2.3 | | 5.5 | V |
| $I_{CC}$ | Supply current | Operating mode; $V_{CC}$ = 5.5V; no load; $f_{SCL}$ = 1MHz | | 250 | 500 | μA |
| $I_{stb}$ | Standby current | Standby mode; $V_{CC}$ = 5.5V; no load; $V_I$ = VCC; $f_{SCL}$ = 0; I/O = inputs | | 0.25 | 1 | uA |
| $V_{POR}$ | Power-on reset voltage(1) | | | 1.16 | 1.41 | V |
| **Input SCL, Input/Output SDA** | | | | | | |
| $V_{IL}$ | Low level input voltage | | -0.5 | | +0.3$V_{CC}$ | V |
| $V_{IH}$ | High level input voltage | | 0.7$V_{CC}$ | | 5.5 | V |
| $I_{OL}$ | Low level output current | $V_{OL}$=0.4 | 20 | | | mA |
| $I_L$ | Leakage current | $V_I$ = VCC = GND | -1 | | 1 | μA |
| $C_i$ | Input capacitance | $V_I$ = GND | | 5 | 10 | pF |
| **I/Os** | | | | | | |
| $I_{OL}$ | Low level output current | $V_{CC}$ = 2.3V; $V_{OL}$ = 0.5V(2) | 12 | 28 | | mA |
| | | $V_{CC}$ = 3.0V; $V_{OL}$ = 0.5V(2) | 17 | 35 | | mA |
| | | $V_{CC}$ = 4.5V; $V_{OL}$ = 0.5V(2) | 25 | 42 | | mA |
| $I_{OL}$(tot) | Total LOW-level output current | $V_{OL}$ = 0.5V; $V_{CC}$ = 4.5V | | | 600 | mA |
| $I_{OH}$ | HIGH-level output current | $V_{OH}$ = GND | -30 | -359 | -480 | uA |
| Itrt(pu) | Transient boosted pull-up current | $V_{OH}$ = GND | -0.5 | -1.0 | | mA |
| $C_i$ | Off-state Input capacitance | (3) | | 9 | 10 | pF |
| $C_o$ | Off-state Output capacitance | (3) | | 9 | 10 | pF |
| **Interrupt $\overline{INT}$** | | | | | | |
| $I_{OL}$ | Low level output current | $V_{OL}$ = 0.4V | 6 | | | mA |
| $C_o$ | Output capacitance | | | 2.1 | 10 | pF |
| **Select inputs AD2, AD1, AD0 and $\overline{RESET}$** | | | | | | |
| $V_{IL}$ | Low level input voltage | | -0.5 | | +0.81 | V |
| $V_{IH}$ | High level input voltage | $V_{CC}$ = 3.3V | +1.8 | | 5.5 | V |


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_L$ | Input leakage current | | -1 | | 1 | μA |
| Ci | Input capacitance | | | 2.4 | 10 | pF |

**Note:**
1. VCC must be lowered to 0.2 V for at least 20us in order to reset part.
2. Each I/O must be externally limited to a maximum of 25mA and the total package limited to 600 mA due to internal busing limits.
3. The value is not tested, but verified on sampling basis.

## Dynamic Characteristics

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C | | Fast mode Plus I²C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $t_{BUF}$ | bus free time between a STOP and START condition | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{HD;STA}$ | hold time (repeated) START condition | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | 4.7 | | 0.6 | | 0.26 | | μs |
| $t_{SU;STO}$ | set-up time for STOP condition | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_{VD;ACK}$[1] | data valid acknowledge time | | 3.45 | | 0.9 | | 0.45 | μs |
| $t_{HD;DAT}$[2] | data hold time | 0 | | 0 | | 0 | | ns |
| $t_{VD;DAT}$ | data valid time | | 3.45 | | 0.9 | | 0.45 | ns |
| $t_{SU;DAT}$ | data set-up time | 250 | | 100 | | 50 | | ns |
| $t_{LOW}$ | LOW period of the SCL clock | 4.7 | | 1.3 | | 0.5 | | μs |
| $t_{HIGH}$ | HIGH period of the SCL clock | 4.0 | | 0.6 | | 0.26 | | μs |
| $t_f$ | fall time of both SDA and SCL signals | | 300 | | 300 | | 120 | ns |
| $t_r$ | rise time of both SDA and SCL signals | | 1000 | | 300 | | 120 | ns |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | 50 | | 50 | | 50 | ns |
| **Port timing $C_L$≤100pF** | | | | | | | | |
| $t_{v(Q)}$ | Data output valid time(3) | | 200 | | 200 | | 200 | ns |
| $t_{su(D)}$ | Data input set-up time | 0 | | 0 | | 0 | | ns |
| $t_{h(D)}$ | Data input hold time | 4 | | 4 | | 4 | | μs |
| **Interrupt timing $C_L$≤100pF** | | | | | | | | |
| $t_{v(D)}$ | Valid time on pin $\overline{INT}$ | | 4 | | 4 | | 4 | μs |
| td(rst) | Reset time on pin $\overline{INT}$ | | 4 | | 4 | | 4 | μs |
| **Reset timing** | | | | | | | | |
| $t_{w(rst)}$ | Reset pulse width | | 25 | | 25 | | 25 | ns |
| $t_{vrec(rst)}$ | Reset recovery time(4) | | 0 | | 0 | | 0 | ns |
| $t_{rst}$ | Reset time | | 1 | | 1 | | 1 | μs |

**Note:**
1. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA (out) LOW.
2. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.
3. $t_{v(Q)}$measured from 0.7VCC on SCL to 50% I/O output.


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Details Description

### a. Device Address

Following a START condition, the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PI4IOE5V96224 is shown in below. Slave address pins AD2, AD1, and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1, and AD0. Address values depending on AD2, AD1, and AD0 can be found in Table 2 "PI4IOE5V96224 address map".

**Table 1. PI4IOE5V96224 Address**

| | b7(MSB) | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|
| Address Byte | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

**Table 2. PI4IOE5V96224 Address Maps**

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address (Write) | Address (Read) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | SCL | GND | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 20h | 21h |
| GND | SCL | VDD | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 22h | 23h |
| GND | SDA | GND | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 24h | 25h |
| GND | SDA | VDD | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 26h | 27h |
| VDD | SCL | GND | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 28h | 29h |
| VDD | SCL | VDD | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 2Ah | 2Bh |
| VDD | SDA | GND | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 2Ch | 2Dh |
| VDD | SDA | VDD | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 2Eh | 2Fh |
| GND | SCL | SCL | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 30h | 31h |
| GND | SCL | SDA | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 32h | 33h |
| GND | SDA | SCL | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 34h | 35h |
| GND | SDA | SDA | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 36h | 37h |
| VDD | SCL | SCL | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 38h | 39h |
| VDD | SCL | SDA | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 3Ah | 3Bh |
| VDD | SDA | SCL | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 3Ch | 3Dh |
| VDD | SDA | SDA | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 3Eh | 3Fh |
| GND | GND | GND | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 40h | 41h |
| GND | GND | VDD | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 42h | 43h |
| GND | VDD | GND | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 44h | 45h |
| GND | VDD | VDD | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 46h | 47h |
| VDD | GND | GND | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 48h | 49h |
| VDD | GND | VDD | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 4Ah | 4Bh |
| VDD | VDD | GND | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 4Ch | 4Dh |
| VDD | VDD | VDD | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 4Eh | 4Fh |
| GND | GND | SCL | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 50h | 51h |
| GND | GND | SDA | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 52h | 53h |
| GND | VDD | SCL | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 54h | 55h |
| GND | VDD | SDA | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 56h | 57h |
| VDD | GND | SCL | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 58h | 59h |
| VDD | GND | SDA | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 5Ah | 5Bh |


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address (Write) | Address (Read) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VDD | VDD | SCL | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 5Ch | 5Dh |
| VDD | VDD | SDA | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 5Eh | 5Fh |
| SCL | SCL | GND | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A0h | A1h |
| SCL | SCL | VDD | 1 | 0 | 1 | 0 | 0 | 0 | 1 | A2h | A3h |
| SCL | SDA | GND | 1 | 0 | 1 | 0 | 0 | 1 | 0 | A4h | A5h |
| SCL | SDA | VDD | 1 | 0 | 1 | 0 | 0 | 1 | 1 | A6h | A7h |
| SDA | SCL | GND | 1 | 0 | 1 | 0 | 1 | 0 | 0 | A8h | A9h |
| SDA | SCL | VDD | 1 | 0 | 1 | 0 | 1 | 0 | 1 | AAh | ABh |
| SDA | SDA | GND | 1 | 0 | 1 | 0 | 1 | 1 | 0 | ACh | ADh |
| SDA | SDA | VDD | 1 | 0 | 1 | 0 | 1 | 1 | 1 | AEh | AFh |
| SCL | SCL | SCL | 1 | 0 | 1 | 1 | 0 | 0 | 0 | B0h | B1h |
| SCL | SCL | SDA | 1 | 0 | 1 | 1 | 0 | 0 | 1 | B2h | B3h |
| SCL | SDA | SCL | 1 | 0 | 1 | 1 | 0 | 1 | 0 | B4h | B5h |
| SCL | SDA | SDA | 1 | 0 | 1 | 1 | 0 | 1 | 1 | B6h | B7h |
| SDA | SCL | SCL | 1 | 0 | 1 | 1 | 1 | 0 | 0 | B8h | B9h |
| SDA | SCL | SDA | 1 | 0 | 1 | 1 | 1 | 0 | 1 | BAh | BBh |
| SDA | SDA | SCL | 1 | 0 | 1 | 1 | 1 | 1 | 0 | BCh | BDh |
| SDA | SDA | SDA | 1 | 0 | 1 | 1 | 1 | 1 | 1 | BEh | BFh |
| SCL | GND | GND | 1 | 1 | 0 | 0 | 0 | 0 | 0 | C0h | C1h |
| SCL | GND | VDD | 1 | 1 | 0 | 0 | 0 | 0 | 1 | C2h | C3h |
| SCL | VDD | GND | 1 | 1 | 0 | 0 | 0 | 1 | 0 | C4h | C5h |
| SCL | VDD | VDD | 1 | 1 | 0 | 0 | 0 | 1 | 1 | C6h | C7h |
| SDA | GND | GND | 1 | 1 | 0 | 0 | 1 | 0 | 0 | C8h | C9h |
| SDA | GND | VDD | 1 | 1 | 0 | 0 | 1 | 0 | 1 | CAh | CBh |
| SDA | VDD | GND | 1 | 1 | 0 | 0 | 1 | 1 | 0 | CCh | CDh |
| SDA | VDD | VDD | 1 | 1 | 0 | 0 | 1 | 1 | 1 | CEh | CFh |
| SCL | GND | SCL | 1 | 1 | 1 | 0 | 0 | 0 | 0 | E0h | E1h |
| SCL | GND | SDA | 1 | 1 | 1 | 0 | 0 | 0 | 1 | E2h | E3h |
| SCL | VDD | SCL | 1 | 1 | 1 | 0 | 0 | 1 | 0 | E4h | E5h |
| SCL | VDD | SDA | 1 | 1 | 1 | 0 | 0 | 1 | 1 | E6h | E7h |
| SDA | GND | SCL | 1 | 1 | 1 | 0 | 1 | 0 | 0 | E8h | E9h |
| SDA | GND | SDA | 1 | 1 | 1 | 0 | 1 | 0 | 1 | EAh | EBh |
| SDA | VDD | SCL | 1 | 1 | 1 | 0 | 1 | 1 | 0 | ECh | Edh |
| SDA | VDD | SDA | 1 | 1 | 1 | 0 | 1 | 1 | 1 | EEh | EFh |


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Quasi-bidirectional I/O Architecture

The PI4IOE5V96224's 24 ports (see Figure 1) are entirely independent and can be used either as input or output ports. Input data is transferred from the ports to the microcontroller in the Read mode. Output data is transmitted to the ports in the Write mode.

Every data transmission from the PI4IOE5V96224 must consist of a multiple of three bytes, the first byte will be referred to as IO1_7 to IO1_0, and the second byte as IO2_7 to IO2_0. The third will be referred to as P2_7 to IO_0.

This quasi-bidirectional I/O can be used as an input or output without the use of a control signal for data directions. At power-on the I/Os are HIGH. In this mode only a current source ($I_{OH}$) to VCC is active. An additional strong pull-up to VCC (Itrt(pu)) allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The I/Os should be HIGH before being used as inputs. After power-on, as all the I/Os are set HIGH, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode.

Remark: If a HIGH is applied to an I/O which has been written earlier to LOW, a large current ($I_{OL}$) will flow to GND.

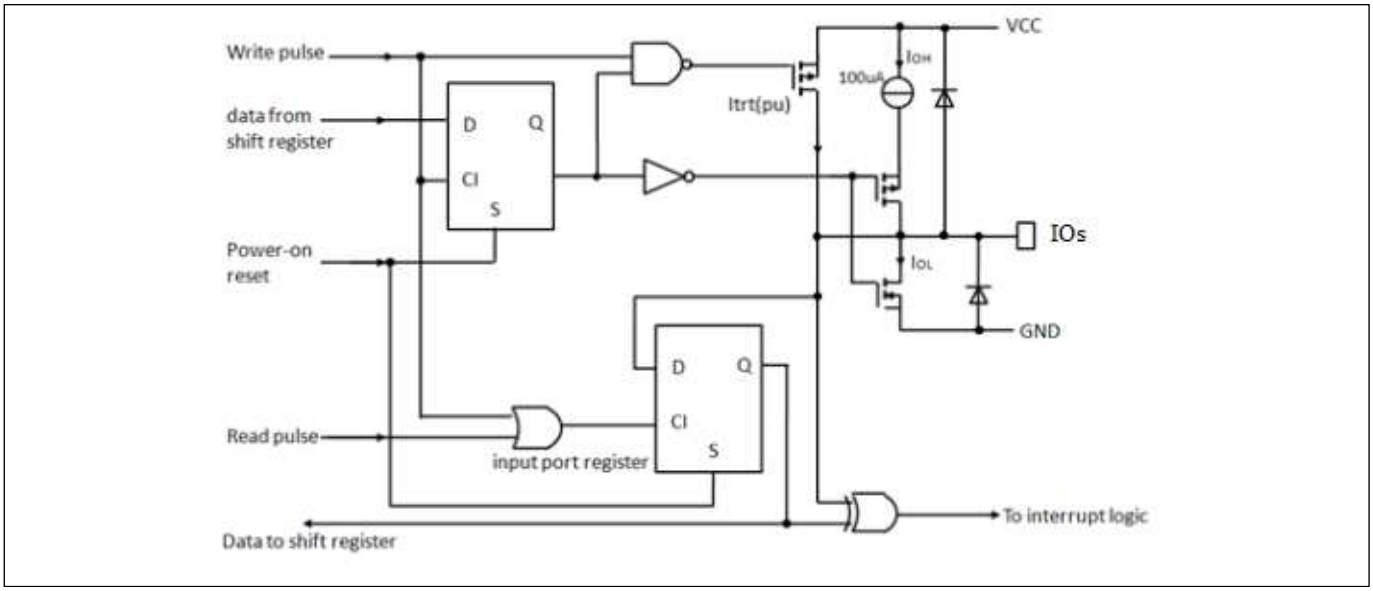



**Figure 1. Simplified Schematic Diagram of IOX_0 to IOX_7**

## Writing to the Port (Output Mode)

To write, the master (microcontroller) first addresses the slave device. By setting the last bit of the byte containing the slave address to logic 0 the Write mode is entered. The PI4IOE5V96224 acknowledges and the master sends the first data byte for IO0_7 to IO0_0. After the first data byte is acknowledged by the PI4IOE5V96224, the second data byte IO1_7 to IO1_0 is sent by the master. After the second data byte is acknowledged by the PI4IOE5V96224, the three data byte IO2_7 to IO2_0 is sent by the master. Once again, the PI4IOE5V96224 acknowledges the receipt of the data. Each 8-bit data is presented on the port lines after it has been acknowledged by the PI4IOE5V96224.

The number of data bytes that can be sent successively is not limited. After every three bytes, the previous data is overwritten.

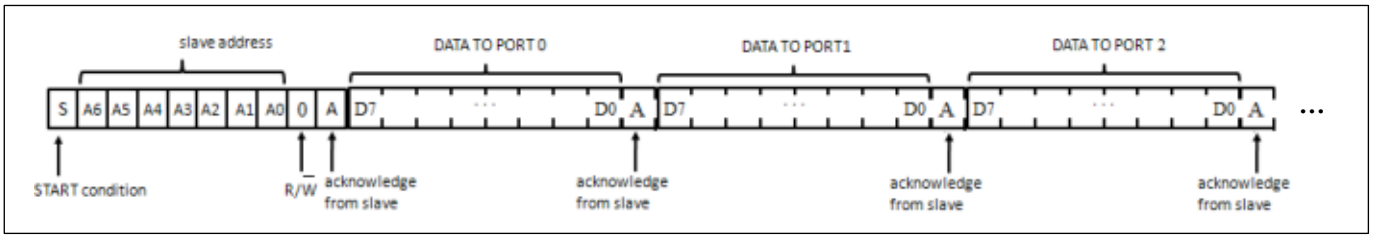



**Figure 2. Write Mode**


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Reading from a Port (Input Mode)

All ports programmed as input should be set to logic 1. To read, the master (microcontroller) first addresses the slave device after it receives the interrupt. By setting the last bit of the byte containing the slave address to logic 1 the Read mode is entered. The data bytes that follow on the SDA are the values on the ports.
If the data on the input port changes faster than the master can read, this data may be lost. Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid.

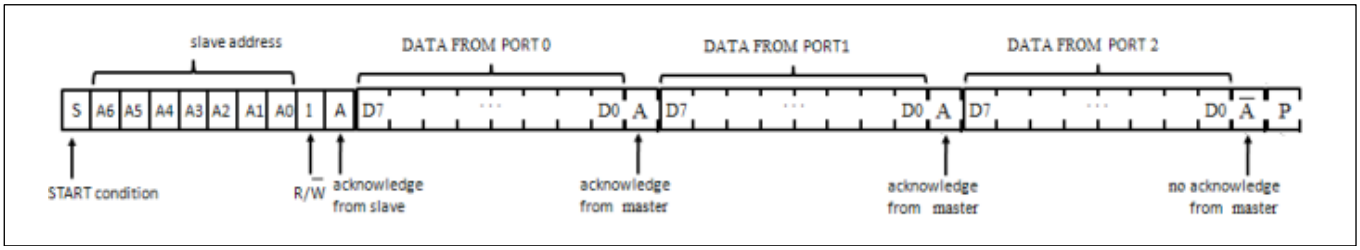



**Figure 3. Read Input Port Register**

## Power-On Reset

When power is applied to VCC, an internal Power-On Reset (POR) holds the PI4IOE5V96224 in a reset condition until VCC has reached VPOR. At that point, the reset condition is released and the PI4IOE5V96224 registers and I²C-bus state machine will initialize to their default states. Thereafter VCC must be lowered below 0.2 V to reset the device.

## Interrupt Output (INT)

The PI4IOE5V96224 provides an open-drain interrupt ( $\overline{\text{INT}}$ ) which can be fed to a corresponding input of the microcontroller. This gives these chips a kind of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the port inputs. After time $t_{(V)D}$ the signal $\overline{\text{INT}}$ is valid.

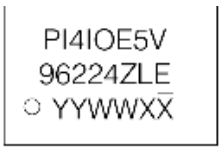
The interrupt disappears when data on the port is changed to the original setting or data is read from or written to the device which has generated the interrupt.
In the write mode, the interrupt may become deactivated (HIGH) on the rising edge of the write to port pulse. On the falling edge of the write to port pulse the interrupt is definitely deactivated (HIGH).
The interrupt is reset in the read mode on the rising edge of the read from port pulse.
During the resetting of the interrupt itself, any changes on the I/Os may not generate an interrupt. After the interrupt is reset any change in I/Os will be detected and transmitted as an INT.

## $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PI4IOE5V96224 registers and I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Part Marking

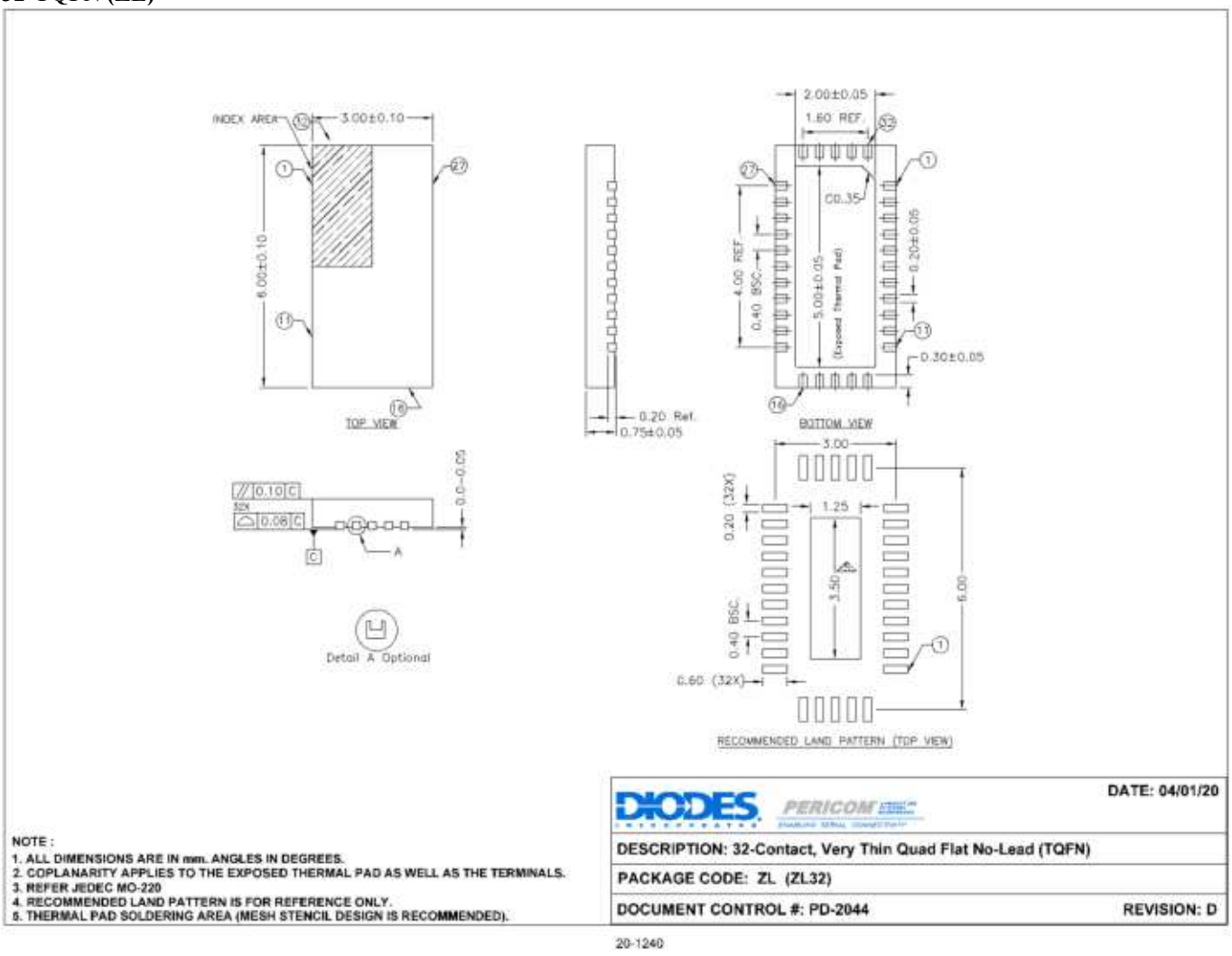



YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

## Packaging Mechanical

**32-TQFN (ZL)**




**For latest package info.**
**please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/**

## Mechanical Data

- Surface Mount Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Case Material: Molded Plastic, UL Flammability Rating 94V-0
- Terminals: Finish - NiPdAu Nickel Palladium Gold, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.046 grams (Approximate)

## Ordering Information

| Orderable Part Number | Package Code | Package Description |
|---|---|---|
| PI4IOE5V96224ZLEX | ZL | 32-contact, Very Thin Quad Flat No-Lead (TQFN) |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel


© 2025 Copyright Diodes Incorporated. All Rights Reserved.

**IMPORTANT NOTICE**

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.

5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

9. This Notice may be periodically updated with the most recent version available at https://www.diodes.com/about/company/terms-and-conditions/important-notice

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.
All other trademarks are the property of their respective owners.
© 2025 Diodes Incorporated. All Rights Reserved.

**www.diodes.com**


© 2025 Copyright Diodes Incorporated. All Rights Reserved.