6-Bit Bi-directional Level Shifter for Open-Drain and Push-Pull Application

Features

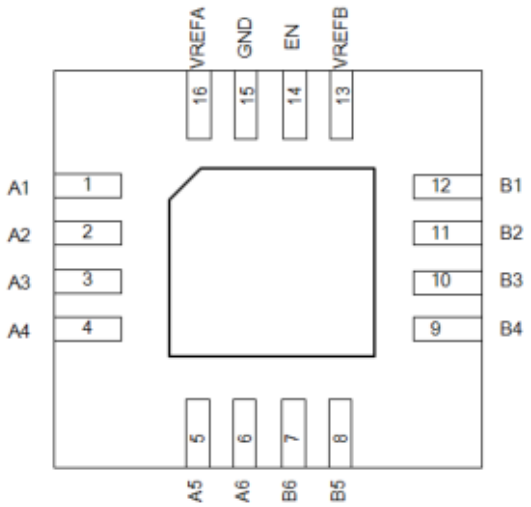
- Provides Bidirectional Voltage Translation With No Direction Pin
- Supports Up to 100 MHz Up Translation and Greater Than 100 MHz Down Translation at≤ 30pF Cap Load and Up To 40 MHz Up/Down Translation at 50 pF Cap Load
- Supports Hot Insertion
- Allow Bidirectional Voltage Level Translation Between
  - 0.95 V ↔ 1.8/2.5/3.3/5 V
  - 1.2 V ↔ 1.8/2.5/3.3/5 V
  - 1.8 V ↔ 2.5/3.3/5 V
  - 2.5 V ↔ 3.3/5 V
  - 3.3 V ↔ 5 V
- Low Standby Current
- 5 V Tolerance I/O Port to Support TTL
- Low Ron Provides Less Signal Distortion
- High-Impedance I/O pins For EN = Low
- Flow-Through Pin out for Ease PCB Trace Routing
- ESD protection (8KV HBM and 1KV CDM)
- Latch-Up Performance Exceeds 100 mA Per JESD 17
- –40°C to 125°C Operating Temperature Range
- Package: UQFN-16

Description

The PI4ULS5V106 supports up to 100 MHz up translation and greater than 100 MHz down translation at ≤ 30pF cap load and up to 40 MHz up/down translation at 50pF cap load which allows the LSF family to support more consumer or telecom interfaces (MDIO or SDIO). It has bidirectional voltage translation without the need for DIR pin which minimizes system effort (for PMBus, I2C, or SMbus).

ThePI4ULS5V106 supports 5 V tolerance on IO port which makes it compatible with TTL levels in industrial and telecom applications. It is able to set up different voltage translation levels on each channel which makes it very flexible.

Pin Configuration



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Pin Description

Pin Name	Pin No.	Description
GND	15	Ground.
VREFA	16	Reference supply voltage A
An	1-6	Data port A
Bn	7-12	Data port B
VREFB	13	Reference supply voltage B
EN	14	Enable. Connect to VREFB and pull-up through a 200kΩresistor

Block Diagram

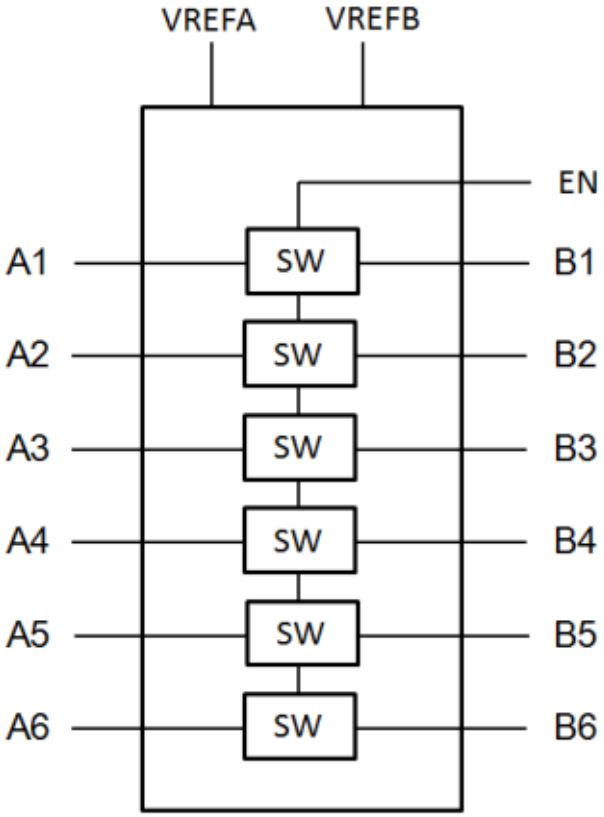


Figure 1: Block Diagram

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Maximum Ratings

Storage Temperature	-65°C to +150°C
Tj, Junction temperature	125℃
Reference Voltage	-0.5V to +7.0V
I/O Input Voltage	-0.5V to +7.0V
channel current (DC)	128mA
Input clamping Current	-50Ma

Note:
Stresses greater than those listed under MAXIMUMRATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{I/O}$	Voltage on an input/output pin	0	-	5	V
VREFA	Reference voltage	0	-	5	V
VREFB	Reference bias voltage	0	-	5	V
VEN	Input voltage on pin EN	0	-	5	V
$I_{(pass)}$	Pass switch current	-	-	64	mA
T_A	Ambient temperature	-40	-	85	°C

DC Electrical Characteristics

(T_A = –40°C to 85°C, unless otherwise noted. Typical values are at 3.3V Vdd and +25°C.)

Parameter	Description	Test Conditions[1]		Min	Typ.[2]	Max	Unit
Input and output SDAB and SCLB							
V_{IK}	input clamping voltage	I_I = -18mA; VEN= 0 V		-	-	-1.2	V
I_{IH}	HIGH-level input current	V_I = 5 V; VEN= 0 V		-	-	5	µA
ICC	Supply Current	VREFB = VEN = 5.5 V, VREFA = 4.5 V or 1 V, IO = 0, VI = VCC or GND			1		µA
$C_{i(refA/refB/EN)}$	input capacitance on pinVREFA,VREFB, EN	V_I = 3 V or 0 V		-	11	-	pF
$C_{io(off)}$	off-state input/output capacitance	V_O = 3 V or 0 V; VEN= 0 V		-	4	-	pF
$C_{io(on)}$	on-state input/output capacitance	V_O = 3 V or 0 V; VEN= 3 V		-	10.5	-	pF
Ron	ON-state resistance	V_I= 0V; I_O = 64mA; VREFB ,VEN connect to 5 V through 200k Ω	VREFA = 3.3 V;		8		Ω
			VREFA = 1.8 V;		9		Ω
			VREFA = 1.0 V;		10		Ω
		V_I= 0V; I_O = 32mA VREFB ,VEN connect to 5 V through 200k Ω	VREFA = 1.8 V;		10		Ω
			VREFA = 2.5 V;		15		Ω
		V_I= 1.8V; I_O = 15mA VREFB ,VEN connect to 5V through 200k Ω	VREFA = 3.3 V;		9		Ω
		V_I= 1.0V; I_O = 10mA VREFB ,VEN connect to 3.3V through 200k Ω	VREFA = 1.8 V;		18		Ω
		V_I= 0V; I_O = 10mA VREFB ,VEN connect to 3.3V through 200k Ω	VREFA = 1.0 V;		20		Ω
		V_I= 0V; I_O = 10mA VREFB ,VEN connect to 1.8V through 200k Ω	VREFA = 1.0 V;		30		Ω

Notes:

1) All typical values are at T_A = 25 °C.

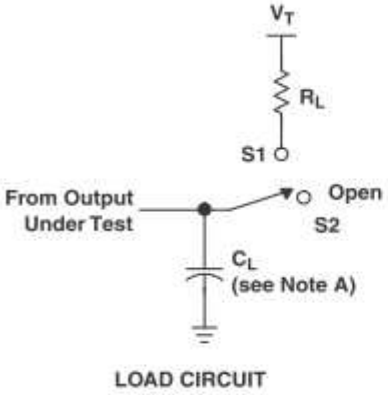
2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

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Dynamic characteristics

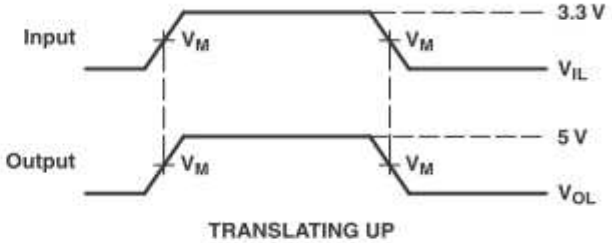
T_A= -40°Cto +85°C; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
Dynamic characteristics (translating down)									
VEN= 3.3 V; V_{IH} = 3.3 V; V_{IL} = 0 V; V_M = 1.15 V									
t_{PLH}	LOW-to-HIGH propagation delay	From A→B or B→A	1.9		1.4		0.78		ns
t_{PHL}	HIGH-to-LOW propagation delay		2		1.5		0.85		ns
VEN= 2.5 V; V_{IH} = 2.5 V; V_{IL} = 0 V; V_M = 0.75 V									
t_{PLH}	LOW-to-HIGH propagation delay	From A→B or B→A	2		1.45		0.8		ns
t_{PHL}	HIGH-to-LOW propagation delay		2.1		1.55		0.9		ns
Dynamic characteristics (translating up)									
VEN= 3.3 V; V_{IH} = 2.3 V; V_{IL} = 0 V; V_T = 3.3 V; V_M = 1.15 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay		2.1		1.55		0.9		ns
t_{PHL}	HIGH-to-LOW propagation delay		2.2		1.65		1		ns
VEN= 2.5 V; V_{IH} = 1.5 V; V_{IL} = 0 V; V_T = 2.5 V; V_M = 0.75 V; R_L = 300 Ω									
t_{PLH}	LOW-to-HIGH propagation delay		1.8		1.35		0.8		ns
t_{PHL}	HIGH-to-LOW propagation delay		1.9		1.45		0.9		ns

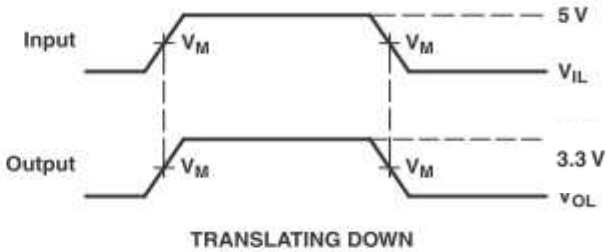


LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



TRANSLATING UP



TRANSLATING DOWN

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 2: Test Circuit

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Function Description

The PI4ULS5V106 is bidirectional voltage level translators operational from 0.95 to 4.5 V (VREFA) and 1.8 to 5.5 V(VREFB). This allows bidirectional voltage translations between 1 V and 5 V without the need for a direction pin in open-drain or push-pull applications. It supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pull-up resistor.

When the A or B port is LOW, the switch is in the ON-state and a low resistance connection exists between the A and B ports. The low Ron of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the B port when the B port is HIGH, the voltage on the A port is limited to the voltage set by VREFA When the A port is HIGH, the B port is pulled to the drain pull-up supply voltage by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control.

The supply voltage for each channel can be individually set up with a pull-up resistor. For example, channel 1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and channel 2 in down-translation mode (2.5 V ↔ 1.8 V).When EN is HIGH, the translator switch is on, and the An is connected to the Bn, respectively, allowing bidirectional data flow between ports.

When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by VREFB To ensure the high-impedance state during power-up or power-down, EN must be LOW.

Application Information

The PI4ULS5V106 are able to perform voltage translation for open-drain or push-pull interface.

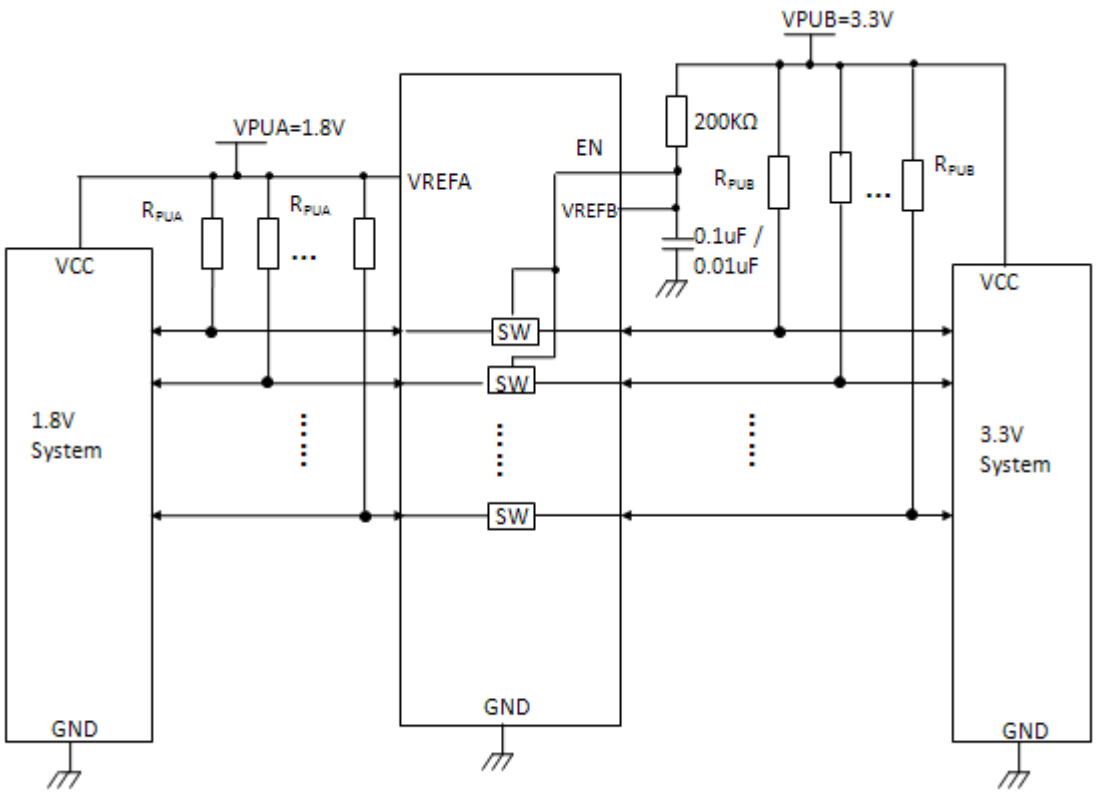


Figure 3: Typical Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREFB and both pins pulled to HIGH through a pull-up resistor (typically 200 k). This allows VREFB to regulate the EN input.

A filter capacitor on VREFB is recommended.

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The master output driver can be totem pole or open-drain (pull-up resistors may be required) and the slave device output can be totem pole or open-drain (pull-up resistors are required to pull the Bn outputs to VPUB. However, if either output is totem-pole, data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contentions in either direction. If both outputs are open-drain, no direction control is needed.
When VREFB is connected through a 200k ohm resistor to a 3.3 V to 5.5 V power supply, and VREFA is set between 1.0 V and VPUB-1V, the output of each An has a maximum output voltage equal to VREFA, and the output of each Bn has a maximum output voltage equal to VPUB.

Pull-up resistors and minimum values

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The V_{OL} of driver
- The V_{OL} of thePI6ULS5V108
- The V_{IL} of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.
Tables in bellow contain suggested minimum values of pull-up resistors for the PI6UILS5V9306 with typical voltage translation levels and drive currents.
The calculated values assume that both drive currents are the same.
V_{OL} = V_{IL} = 0.1*VCC and accounts for a 5 % VCC tolerance of the supplies, 1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in the table to ensure that the pass voltage is less than 10 % of the VCC voltage, and the external driver should be able to sink the total current from both pull-up resistors.

Pull-up resistor minimum values, 3 mA driver sink current for PI6ULS5V108

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPUA}= 859Ω R_{RPUB}= 859Ω	R_{RPUA}= 970Ω R_{RPUB}= 970Ω	R_{RPUA}= none R_{RPUB}= 896Ω Or both 1.23kΩ	R_{RPUA}= none R_{RPUB}= 1.19kΩ Or both 1.53kΩ	R_{RPUA}= none R_{RPUB}= 1.82kΩ Or both 2.16kΩ
1.2V		R_{RPUA}= 1.07kΩ R_{RPUB}= 1.07kΩ	R_{RPUA}= none R_{RPUB}= 886Ω Or both 1.33kΩ	R_{RPUA}= none R_{RPUB}= 1.18kΩ Or both 1.63kΩ	R_{RPUA}= none R_{RPUB}= 1.81kΩ Or both 2.26kΩ
1.5V			R_{RPUA}= none R_{RPUB}= 875Ω Or both 1.43kΩ	R_{RPUA}= none R_{RPUB}= 1.17kΩ Or both 1.73kΩ	R_{RPUA}= none R_{RPUB}= 1.8kΩ Or both 2.36kΩ
1.8V			R_{RPUA}= 1.53kΩ R_{RPUB}= 1.53kΩ	R_{RPUA}= none R_{RPUB}= 1.16kΩ Or both 1.82kΩ	R_{RPUA}= none R_{RPUB}= 1.79kΩ Or both 2.46kΩ
2.5V				R_{RPUA}= 2.06kΩ R_{RPUB}= 2.06kΩ	R_{RPUA}= none R_{RPUB}= 1.77kΩ Or both 2.69kΩ
3.3V					R_{RPUA}= none R_{RPUB}= 1.74kΩ Or both 2.96kΩ

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Pull-up resistor minimum values, 10 mA driver sink current for PI6ULS5V108

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPUA}= 258Ω R_{RPUB}= 258Ω	R_{RPUA}= 291Ω R_{RPUB}= 291Ω	R_{RPUA}= none R_{RPUB}= 269Ω Or both 369Ω	R_{RPUA}= none R_{RPUB}= 358Ω Or both 458Ω	R_{RPUA}= none R_{RPUB}= 546Ω Or both 646Ω
1.2V		R_{RPUA}= 321Ω R_{RPUB}= 321Ω	R_{RPUA}= none R_{RPUB}= 266Ω Or both 399Ω	R_{RPUA}= none R_{RPUB}= 355Ω Or both 488Ω	R_{RPUA}= none R_{RPUB}= 543Ω Or both 677Ω
1.5V			R_{RPUA}= none R_{RPUB}= 263Ω Or both 429Ω	R_{RPUA}= none R_{RPUB}= 352Ω Or both 518Ω	R_{RPUA}= none R_{RPUB}= 540Ω Or both 707Ω
1.8V			R_{RPUA}= 460Ω R_{RPUB}= 460Ω	R_{RPUA}= none R_{RPUB}= 348Ω Or both 548Ω	R_{RPUA}= none R_{RPUB}= 537Ω Or both 737Ω
2.5V				R_{RPUA}= 619Ω R_{RPUB}= 619Ω	R_{RPUA}= none R_{RPUB}= 521Ω Or both 808Ω
3.3V					R_{RPUA}= none R_{RPUB}= 522Ω Or both 889Ω

Pull-up resistor minimum values, 15 mA driver sink current for PI6ULS5V108

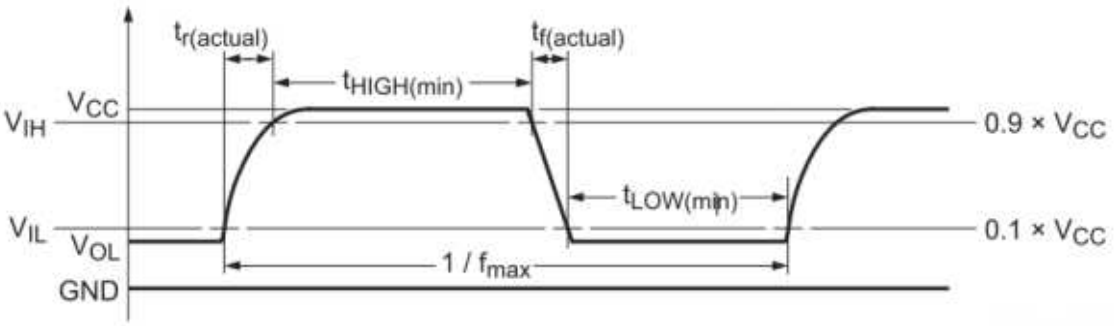
A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	R_{RPUA}= 172Ω R_{RPUB}= 172Ω	R_{RPUA}= 194Ω R_{RPUB}= 194Ω	R_{RPUA}= none R_{RPUB}= 179Ω Or both 246Ω	R_{RPUA}= none R_{RPUB}= 238Ω Or both 305Ω	R_{RPUA}= none R_{RPUB}= 364Ω Or both 431Ω
1.2V		R_{RPUA}= 214Ω R_{RPUB}= 214Ω	R_{RPUA}= none R_{RPUB}= 177Ω Or both 266Ω	R_{RPUA}= none R_{RPUB}= 236Ω Or both 325Ω	R_{RPUA}= none R_{RPUB}= 362Ω Or both 451Ω
1.5V			R_{RPUA}= none R_{RPUB}= 175Ω Or both 286Ω	R_{RPUA}= none R_{RPUB}= 234Ω Or both 345Ω	R_{RPUA}= none R_{RPUB}= 360Ω Or both 471Ω
1.8V			R_{RPUA}= 306Ω R_{RPUB}= 306Ω	R_{RPUA}= none R_{RPUB}= 232Ω Or both 366Ω	R_{RPUA}= none R_{RPUB}=358Ω Or both 492Ω
2.5V				R_{RPUA}= 413Ω R_{RPUB}= 413Ω	R_{RPUA}= none R_{RPUB}= 354Ω Or both 539Ω
3.3V					R_{RPUA}= none R_{RPUB}= 348Ω Or both 593Ω

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Max Frequency Application

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\max) = \frac{1}{\text{tLOW(min)} + \text{tHIGH(min)} + \text{tr(actual)} + \text{tf(actual)}}$$



The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.

Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PI6ULS5V108 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

Part Marking

ZHD Package

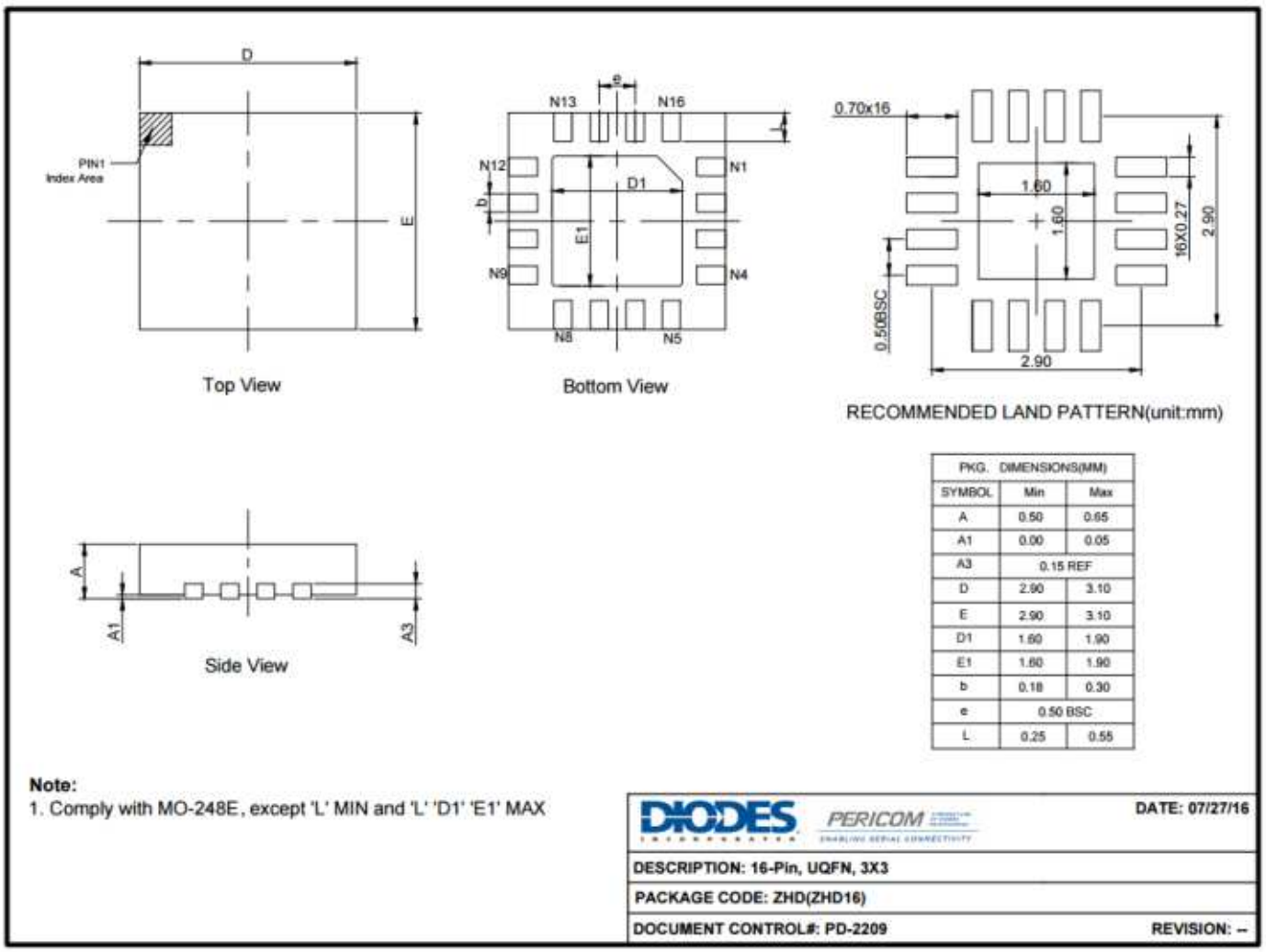


Y: Date Code (Year)
W: Date Code (Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above fab code means Cu wire

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Packaging Mechanical

16-UQFN (ZHD)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.50	0.65
A1	0.00	0.05
A3	0.15 REF	
D	2.90	3.10
E	2.90	3.10
D1	1.60	1.90
E1	1.60	1.90
b	0.18	0.30
e	0.50 BSC	
L	0.25	0.55

Note:
1. Comply with MO-248E, except 'L' MIN and 'L' 'D1' 'E1' MAX

DATE: 07/27/16

DESCRIPTION: 16-Pin, UQFN, 3X3

PACKAGE CODE: ZHD(ZHD16)

DOCUMENT CONTROL#: PD-2209 REVISION: --

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Part No.	Package Code	Package
PI4ULS5V106ZHDEX	ZHD	16-Pin, 3x3 (UQFN)

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3).compliant.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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