PL360

PL360 Datasheet

Description

The PL360 is a programmable modem for narrow-band Power Line Communication (PLC), able to run any PLC protocol in the frequency band below 500 kHz.

This device has been designed to comply with FCC, ARIB, KN60 and CENELEC EN50065 regulations matching requirements of Internet of Things and Smart Energy applications. It supports state-of-the-art narrow-band PLC standards such as ITU G.9903 (G3-PLC®), ITU G.9904 (PRIME) as well as any other narrowband PLC protocols, being at the same time a future-proof platform able to support the evolution of these standards.

The PL360 has been conceived to be driven by external Microchip host devices, thus providing an additional level of flexibility on the host side. The Microchip host device loads the proper PLC-protocol firmware before modem operation and controls the PL360 modem.

Features

- Programmable Narrow-Band Power Line Communication (PLC) Modem
- Integrated PLC Front End:
  - PGA with automatic gain control and ADC
  - DAC and transmission driver supports direct line driving or external Class-D amplifier driving
  - Digital transmission level control
  - Supports two independent transmission branches for the PLC signal
  - Up to 500 kHz PLC signal bandwidth
- Architecture
  - High performance architecture combining CPU, specific co-processors for digital signal processing and dedicated hardware accelerators for common narrow-band PLC tasks
  - Dedicated SRAM memories for code and data
- ARM® 32-bit Cortex®-M7 Core Managing PL360 System: Co-Processors, Hardware Accelerators and Peripherals
  - 216 MHz maximum frequency
  - 192 kB of SRAM for data and code
  - Bootloader allows loading plain programs or authenticated and encrypted programs
  - 12 multiplexed GPIOs
  - 1 SPI, 1 UART, 2 PWM
  - Serial wire debug port
  - Zero-Crossing Detection on the mains
- Cryptographic Engine and Secure Boot
  - AES 128, 192, 256 supported
  - Secure boot: supports AES-128 CMAC for authentication, AES-128 CBC for decryption
  - Fuse programming control for decryption and authentication 128-bit keys
- Clock Management
  - 24 MHz external crystal for system clock
- Power Management

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  - 3.3 V external supply voltage for I/O, digital and analog
  - 1.25 V internal voltage regulator for the core
  - Optimized power modes for specific operation profiles, including Low Power mode
- Available in TQFP-48 and QFN-48 Packages
- -40ºC to +85ºC Temperature Range

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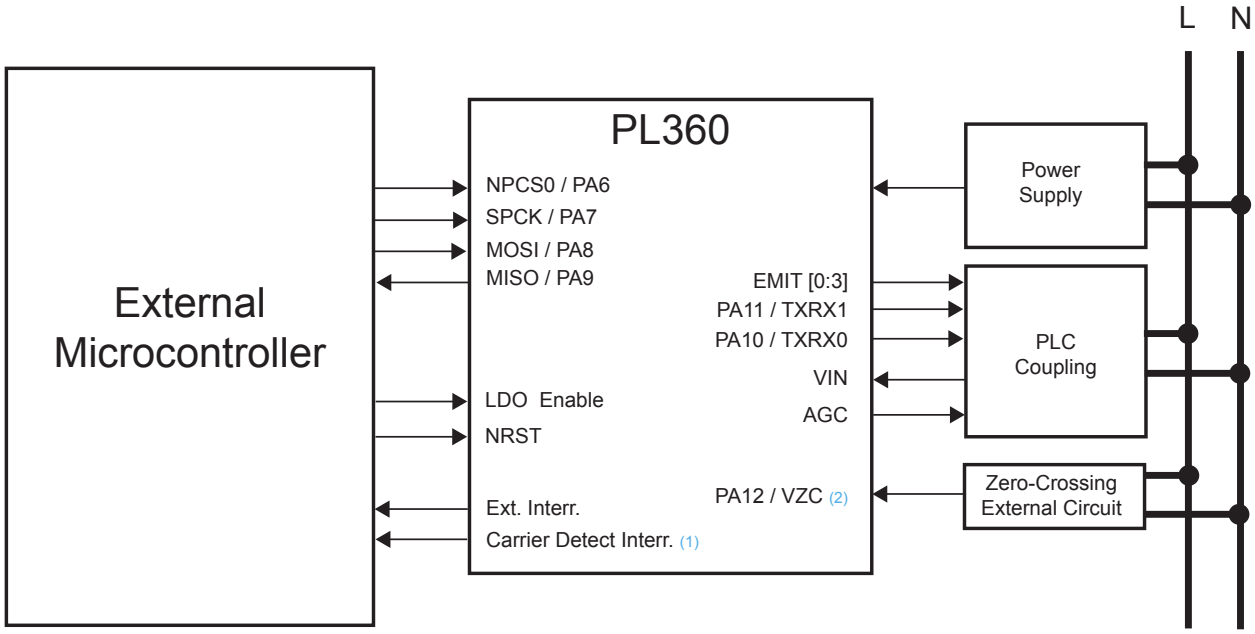
1. PL360 Application Block Diagram

PL360 transceiver has been conceived to be easily managed by an external microcontroller through a 4-line standard Serial Peripheral Interface (SPI). By means of the SPI, the external microcontroller can fully manage and control the PL360 by accessing the internal peripheral registers.

Two additional signals are used by the host to control the PL360: LDO enable and NRST.

Some GPIOs can be used as interrupt signals from the PL360 to the external microcontroller depending on the requirements of the protocol being used.

Figure 1-1. PL360 Application Example

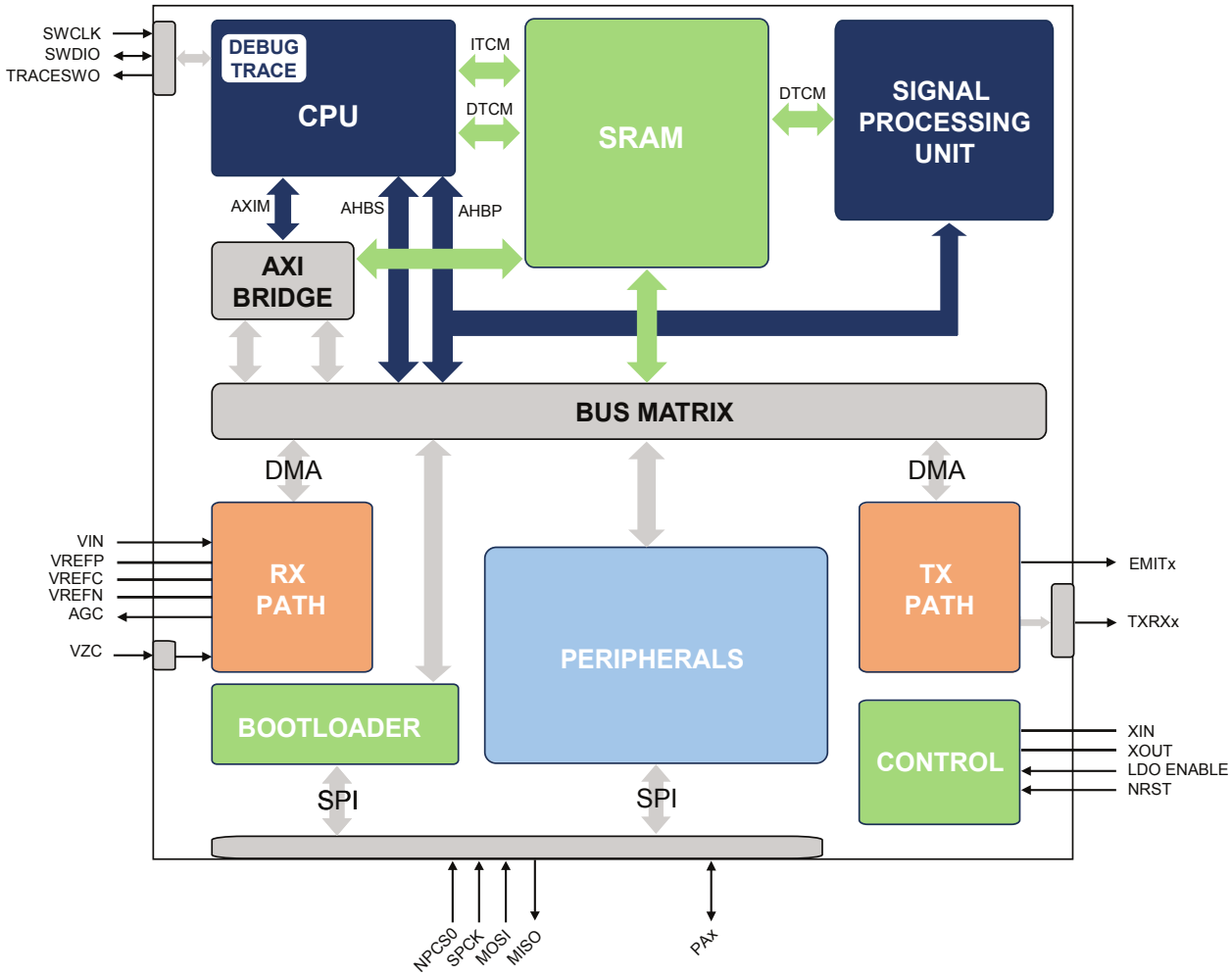


Notes:

1. Used by protocols requiring carrier detection signaling
2. Used by applications requiring phase detection

2. Block Diagram

Figure 2-1. PL360 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	3.3V Digital supply. Digital power supply must be decoupled by external capacitors	Power			3.0V to 3.6V
VDDIN	3.3V Voltage Regulator Input	Power			3.0V to 3.6V
VDDIN_AN	3.3V Analog supply (ADC + PGA)	Power			3.0V to 3.6V
VDDCORE	1.25V Voltage Regulator Output with internal connection to Core power supply. Decoupling capacitors must be placed in VDDCORE pins	Power			1.25V
VDDPLL	1.25V PLL power supply input. Must be connected to pin 7 (VDDCORE) through a LP filter	Power			1.25V
GND	Digital Ground	Power			(1)
AGND	Analog Ground	Power			(1)
Clocks, Oscillators and PLLs					
XIN	Crystal Oscillator Input	Input		VDDIO	
XOUT	Crystal Oscillator Output	Output		VDDIO	
Reset/Test					
NRST	System Reset	Input	Low	VDDIO	
TST	Test Mode	Input	High	VDDIO	
LDO ENABLE	Enable Internal LDO regulator	Input			
Power Line Communications					
EMIT [0:3]	PLC Tri-state Transmission ports	Output		VDDIO	
VIN	PLC signal reception input	Input		VDDIN_AN	
AGC	Automatic Gain Control: • This digital tri-state output is managed by AGC hardware logic to drive external circuitry when input signal attenuation is needed	Output		VDDIO	(3)
VZC	Mains Zero-Cross Detection Signal: • This input detects the zero-crossing of the mains voltage	Input		VDDIO	External Protection Resistor (2) (3)

TXRX0	Analog Front-End Transmission/Reception for TXDRV0 • This digital output is used to modify external coupling behavior in Transmission/ Reception	Output		VDDIO	
TXRX1	Analog Front-End Transmission/Reception for TXDRV1 • This digital output is used to modify external coupling behavior in Transmission/ Reception. The suitable value depends on the external circuitry configuration. The polarity of this pin can be inverted by software	Output		VDDIO	
VREFP	Internal Reference “Plus” Voltage. Bypass to analog ground with an external decoupling capacitor. Connect an external decoupling capacitor between VREFP and VREFN.	Analog		VDDIN_AN	
VREFN	Internal Reference “Minus” Voltage. Bypass to analog ground with an external decoupling capacitor. Connect an external decoupling capacitor between VREFP and VREFN.	Analog		VDDIN_AN	
VREFC	Internal Reference Common-mode Voltage. Bypass to analog ground with an external decoupling capacitor.	Analog		VDDIN_AN	
General Purpose I/Os					
PA [0:11]	General Purpose Input / Output	I/O		VDDIO	(4)
PA [12]	General Purpose Input	Input		VDDIO	(4)
Serial Wire - Debug Port – SW-DP					
SWDIO	Serial Wire Input/Output	I/O		VDDIO	
SWCLK	Serial Wire Clock	Input		VDDIO	
TRACESWO	Trace Asynchronous Data Out	Output		VDDIO	
Serial Peripheral Interface - SPI					
NPCS	SPI Chip Select	Input	Low	VDDIO	Internal pull up (4)
SPCK	SPI Clock signal	Input		VDDIO	Internal pull up (4)
MOSI	SPI Master Out Slave In	Input		VDDIO	Internal pull up (4)
MISO	SPI Master In Slave Out	Output		VDDIO	

Notes:

1. Separate pins are provided for GND and AGND grounds. Layout considerations should be taken into account to reduce interference. Ground pins should be connected as short as possible to the system ground plane. For more details about EMC Considerations, please refer to AVR040 application note
2. Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design. Please refer to the Reference Design for further information
3. See Table 13-4
4. See Table 13-5

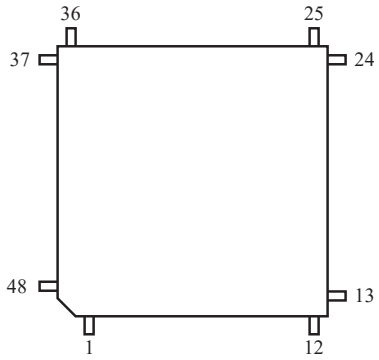
4. Package and Pinout

4.1 48–Lead TQFP Package Outline

The 48-lead TQFP package has a 0.5 mm pitch and respects Green standards.

Figure 4-1 shows the orientation of the 48-lead TQFP package. Refer to the section 14. Mechanical Characteristics for the 48-lead TQFP package mechanical drawing.

Figure 4-1. Orientation of the 48-Lead TQFP Package



4.2 48–Lead TQFP Pinout

Table 4-1. 48 - Lead TQFP Pinout

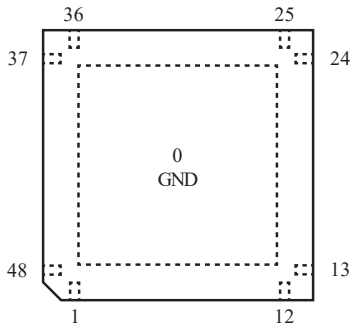
1	NRST	13	PA0	25	EMIT1	37	GND
2	XIN	14	PA1	26	VDDIO	38	AGND
3	XOUT	15	PA2/TRACESWO	27	EMIT2	39	VIN
4	VDDIO	16	PA3	28	VDDIO	40	VDDIN_AN
5	VDDPLL	17	PA6/NPCS0	29	VDDCORE	41	VREFP
6	GND	18	PA7/SPCK	30	GND	42	VREFC
7	VDDCORE	19	PA8/MOSI	31	EMIT3	43	VREFN
8	VDDIN	20	PA9/MISO	32	VDDIO	44	AGND
9	LDO ENABLE	21	VDDIO	33	PA11/TXRX1	45	VDDIN_AN
10	PA4/SWDIO	22	GND	34	PA10/TXRX0	46	VDDIO
11	PA5/SWCLK	23	EMIT0	35	AGC	47	PA12/VZC
12	VDDIO	24	VDDIO	36	VDDIO	48	TST

4.3 48–Lead QFN Package Outline

The 48-lead QFN package has a 0.4 mm pitch and respects Green standards.

Figure 4-1 shows the orientation of the 48-lead QFN package. Refer to the section 14. Mechanical Characteristics for the 48-lead QFN package mechanical drawing.

Figure 4-2. Orientation of the 48-Lead QFN Package



4.4 48–Lead QFN Pinout

Table 4-2. 48 - Lead QFN Pinout

0	GND						
1	NRST	13	PA0	25	EMIT1	37	GND
2	XIN	14	PA1	26	VDDIO	38	AGND
3	XOUT	15	PA2/TRACESWO	27	EMIT2	39	VIN
4	VDDIO	16	PA3	28	VDDIO	40	VDDIN_AN
5	VDDPLL	17	PA6/NPCS0	29	VDDCORE	41	VREFP
6	GND	18	PA7/SPCK	30	GND	42	VREFC
7	VDDCORE	19	PA8/MOSI	31	EMIT3	43	VREFN
8	VDDIN	20	PA9/MISO	32	VDDIO	44	AGND
9	LDO ENABLE	21	VDDIO	33	PA11/TXRX1	45	VDDIN_AN
10	PA4/SWDIO	22	GND	34	PA10/TXRX0	46	VDDIO
11	PA5/SWCLK	23	EMIT0	35	AGC	47	PA12/VZC
12	VDDIO	24	VDDIO	36	VDDIO	48	TST

4.5 Pinout Specification

Table 4-3. Pinout Specification

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
1	VDDIO	RST	NRST	I			I, Hiz
2	VDDIO	CLOCK	XIN	I			I, Hiz
3	VDDIO	CLOCK	XOUT	O			O
4	VDDIO	Power	VDDIO	-			
5	VDDPLL	Power	VDDPLL	-			
6	GNDOSC	Power	GNDOSC	-			

.....continued

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
7	VDDCORE	Power	VDDCORE	-			
8	VDDIN	Power	VDDIN	-			
9	VDDIO	LDO	LDO ENABLE	I			I, Hiz
10	VDDIO	GPIO	PA4	I/O	SWDIO	I/O	SWDIO, I, Hiz
11	VDDIO	GPIO	PA5	I/O	SWCLK	I	SWCLK, I, Hiz
12	VDDIO	Power	VDDIO	-			
13	VDDIO	GPIO	PA0	I/O			PIO, I, Hiz
14	VDDIO	GPIO	PA1	I/O			PIO,I, Hiz
15	VDDIO	GPIO	PA2	I/O	TRACESWO	O	PIO, I, Hiz
16	VDDIO	GPIO	PA3	I/O			PIO, I, Hiz
17	VDDIO	GPIO	PA6	I/O	NPCS0	I	NPCS0, I, Hiz
18	VDDIO	GPIO	PA7	I/O	SPCK	I	SPCK, I, Hiz
19	VDDIO	GPIO	PA8	I/O	MOSI	I	MOSI, I, Hiz
20	VDDIO	GPIO	PA9	I/O	MISO	O	MISO, O, ST1
21	VDDIO	Power	VDDIO	-			
22	GND	Power	GND	-			
23	VDDIO	PLC	EMIT0	O			O, Hiz
24	VDDIO	Power	VDDIO	-			
25	VDDIO	PLC	EMIT1	O			O, Hiz
26	VDDIO	Power	VDDIO	-			
27	VDDIO	PLC	EMIT2	O			O, Hiz
28	VDDIO	Power	VDDIO	-			
29	VDDCORE	Power	VDDCORE	-			
30	GND	Power	GND	-			
31	VDDIO	PLC	EMIT3	O			O, Hiz
32	VDDIO	Power	VDDIO	-			
33	VDDIO	GPIO	PA11	I/O	TXRX1	O	PIO, I, Hiz
34	VDDIO	GPIO	PA10	I/O	TXRX0	O	PIO, I, Hiz
35	VDDIO	AGC	AGC	O			O, ST0
36	VDDIO	Power	VDDIO	-			
37	GND	Power	GND	-			
38	AGND	Ground	AGND	-			
39	VDDIN_AN	PLC	VIN	I			I, Hiz

.....continued

Pin	Power Rail	I/O Type	Primary		PIO Peripheral A		Reset State
			Signal	Dir	Signal	Dir	Signal, Dir, Hiz, ST
40	VDDIN_AN	Power	VDDIN_AN	-			
41	VDDIN_AN	Analog	VREFP	-			
42	VDDIN_AN	Analog	VREFC	-			
43	VDDIN_AN	Analog	VREFN	-			
44	AGND	Ground	AGND	-			
45	VDDIN_AN	Power	VDDIN_AN	-			
46	VDDIO	Power	VDDIO	-			
47	VDDIO	GPIO	VZC/PA12	I			VZC/PIO, I, Hiz
48	VDDIO	TST	TST	I			

Note:

HiZ = High Impedance, ST = Set To.

5. Analog Front-End

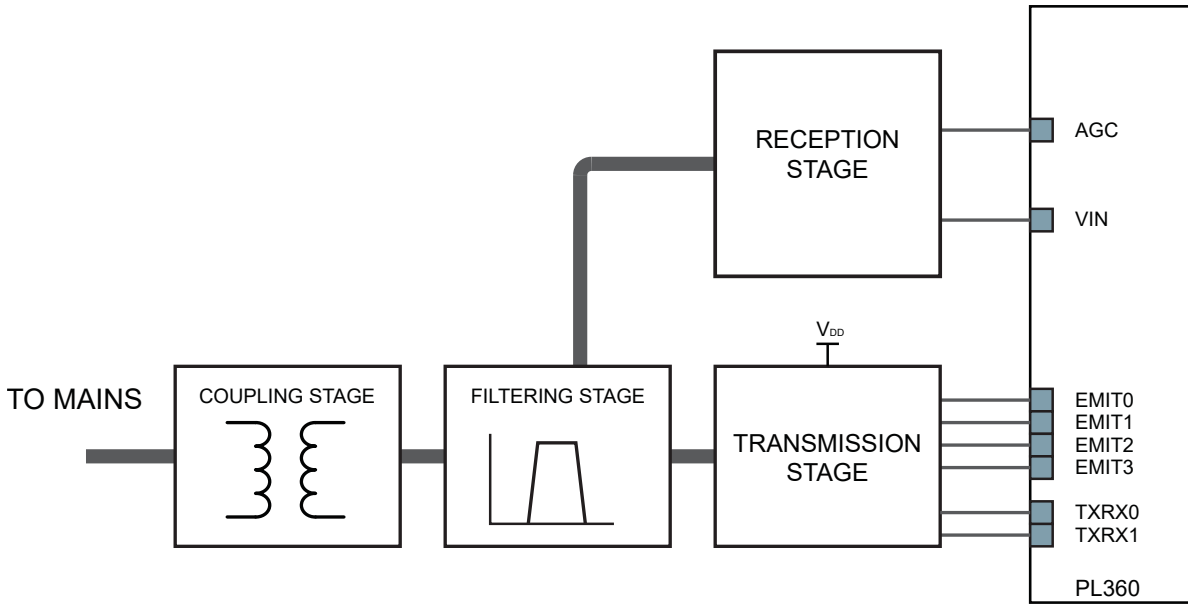
5.1 PLC Coupling Circuitry Description

Microchip PLC technology is purely digital and does not require external DAC/ADC, thus simplifying the external required circuitry. Generally, Microchip PLC coupling reference designs make use of few passive components plus a Class D amplification stage for transmission.

All PLC coupling reference designs are generally composed by the same sub-circuits:

- Transmission Stage
- Reception Stage
- Filtering Stage
- Coupling Stage

Figure 5-1. PLC Coupling Block Diagram



5.1.1 Transmission Stage

The transmission stage adapts the EMIT signals and amplifies them if required. It can be composed by:

- Driver: It adapts the EMIT signals to either control the amplifier or to be filtered by the next stage
- Amplifier: If required, a Class-D amplifier which generates a square waveform from 0 to VDD is included
- Bias and protection: It provides a DC component and provides protection from received disturbances

The transmission stage must be always followed by a filtering stage.

5.1.2 Filtering Stage

The in-band flat response filtering stage does not distort the injected signal, it reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels.

The filtering stage has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage
- Adapt Input/Output impedance for optimal reception/transmission. This is controlled by TXRX0 and TXRX1 signals

- In some cases, Band-pass filtering for received signals

When the system is intended to be connected to a physical channel with high voltage or which is not electrically referenced to the same point, then the filtering stage must be always followed by a coupling stage.

5.1.3 Coupling Stage

The coupling stage blocks the DC component of the line to/from which the signal is injected/received (i.e. 50/60 Hz of the mains). This is typically carried out by a high voltage capacitor.

The coupling stage can also electrically isolate the coupling circuitry from the external world by means of a 1:1 signal transformer.

5.1.4 Reception Stage

The reception stage adapts the received analog signal to be properly captured by the PL360 internal reception chain. The reception circuit is independent of the PLC channel which is being used. It basically consists of:

- Anti aliasing filter (RC Filter)
- Attenuation resistor for AGC circuit
- Driver of the internal ADC

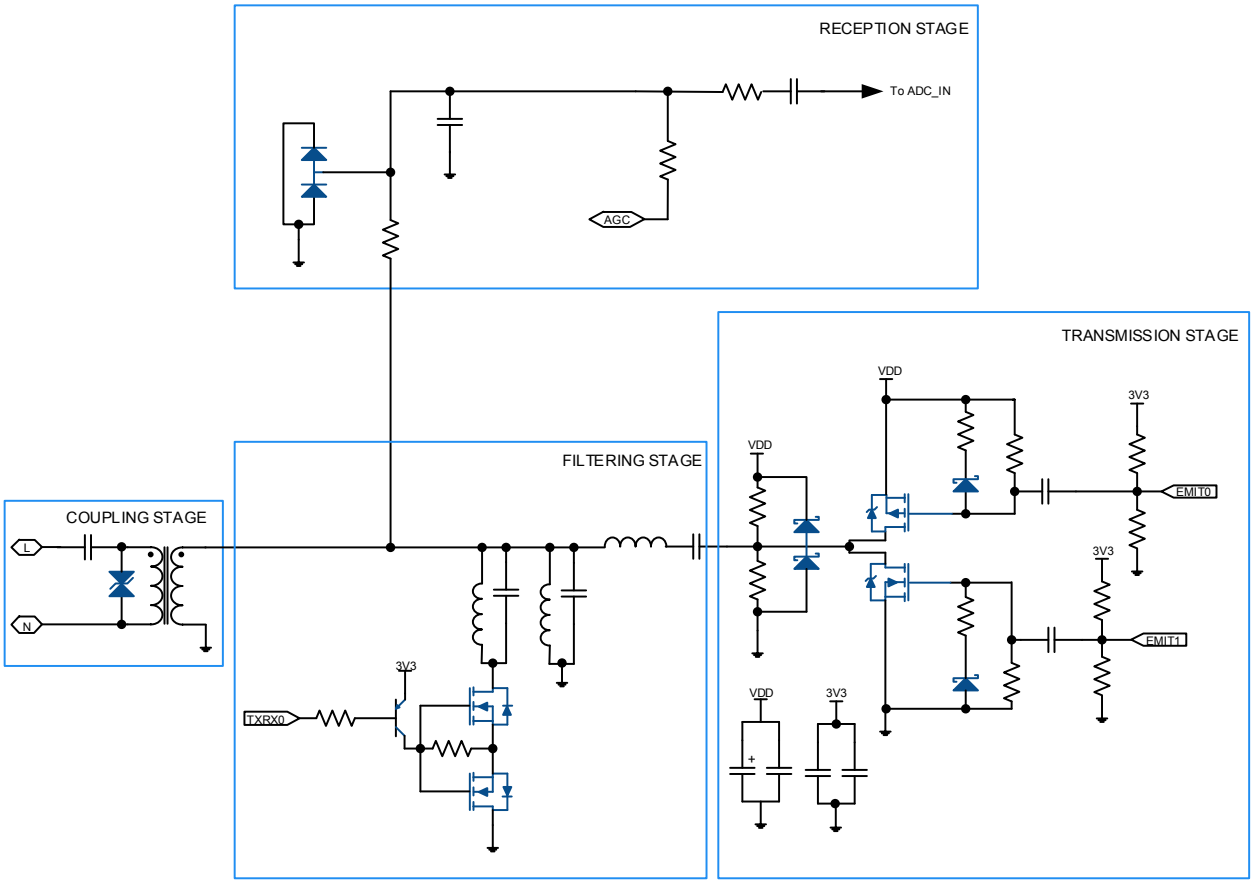
The AGC circuit avoids distortion on the received signal that may arise when the input signal is high enough to polarize the protection diodes in direct region.

The driver to the internal ADC comprises several resistors and capacitors, which provide a DC component and adapt the received signal to be converted by the internal reception chain.

5.1.5 Generic PLC Coupling

The figure below shows an example of a typical PLC coupling circuit, including all the stages previously described.

Figure 5-2. Single Branch PLC Coupling Block Diagram Example



5.2 Coupling Reference Designs

Microchip provides PLC coupling reference designs (usually refered to as ATPLCOUPxxx) for different applications and frequency bands up to 500 kHz, which have been designed to achieve high performance, low cost and simplicity.

6. Power Considerations

6.1 Power Supplies

The following table defines the power supply requirements of the PL360.

Table 6-1. Power Supplies

Name	Associated Ground	Powers
VDDCORE	GND	Core power supply with internal connection to 1.25V voltage regulator output. Decoupling capacitors required.
VDDIO	GND	3.3V Digital supply. Digital power supply must be decoupled by external capacitors.
VDDIN	GND	3.3V Voltage regulator input.
VDDIN_AN	AGND	3.3V Analog supply (ADC + PGA).
VDDPLL	GND	1.25V Voltage Regulator Output. Connected to VDDCORE through a LP filter.

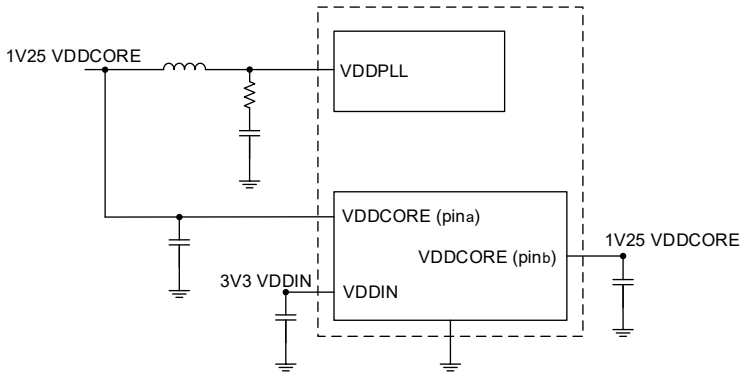
The PL360 embeds a voltage regulator to supply the core. The Voltage Regulator state is controlled by the external LDO ENABLE pin. The two VDDCORE pins in the package must be populated with external decoupling capacitors, the VDDCORE pin close to the VDDPLL pin should be populated with a 4.7µF low ESR capacitor, an 1.0µF or 2.2µF capacitor should be connected to the second VDDCORE pin.

6.2 Power Constraints

The following power constraints apply to PL360 device. Deviating from these constraints may lead to unwanted device behavior.

- VDDIN and VDDIO must have the same level, 3.3V
- VDDPLL voltage must be derived from VDDCORE through a low-pass filter. A second order LC with cutoff frequency equal to 25 KHz should be used. The inductor can be replaced by a ferrite bead, then a cutoff frequency equal to 75 KHz could be acceptable. In those cases, it is mandatory to check the communication performances of the system to detect problems originated from poor PLL supply filtering

Figure 6-1. Voltage Regulator Connectivity(1)



Note:

1. Please refer to the schematics of the evaluation board for further information about correct values of decoupling capacitors and low-pass filter components

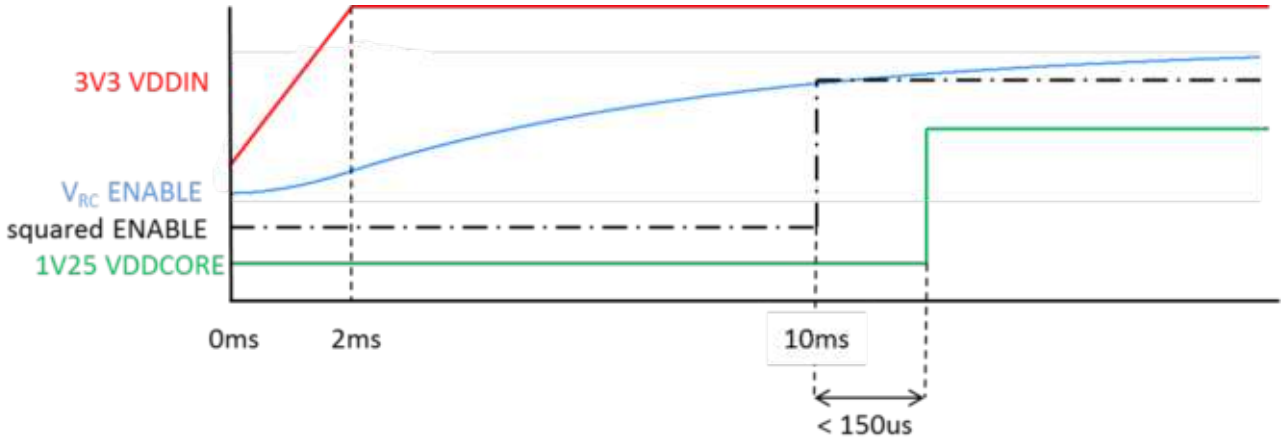
For more information on power considerations, refer to section 13.8 Power On Considerations.

6.2.1 Power-up

VDDIO and VDDIN must rise simultaneously, prior to VDDCORE and VDDPLL rising. This is respected if VDDCORE and VDDPLL are supplied by the embedded voltage regulator and the voltage regulator is turned on after VDDIN reaches 3.3V.

The figure below shows system response when an RC delay line (R = 6K8Ω, C = 1µF) is used to derive ENABLE control from VDDIN.

Figure 6-2. Power-up Sequence



6.2.2 Power-down

VDDIO and VDDIN should fall simultaneously, VDDCORE and VDDPLL will fall later as the regulator VDDIN decreases.

7. Input/Output Lines

The PL360 has several kinds of input/output (I/O) lines such as general purpose I/Os (PA) and system I/Os. PAs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral.

7.1 General-Purpose I/O Lines

PA Lines are managed and configured internally.

7.2 System I/O Lines

System I/O lines are pins used by oscillators, Test mode and Reset.

7.2.1 Test Mode (TST) Pin

The TST pin is used to set the circuit in manufacturing Test mode. It must be tied to ground for normal operation.

7.2.2 Reset (NRST) Pin

The NRST pin is unidirectional. It is controlled externally and can be driven low to provide a Reset signal to reset the PL360. It resets the core and the peripherals. There is no constraint on the length of the Reset pulse.

8. Bootloader

8.1 Description

The bootloader loads the program from an external master to the internal memory of PL360. It allows loading of plain programs or secured programs. When a secured program is loaded, the original program length must be padded to become a multiple of 16 bytes, and the length (number of blocks, where a block is a 16 bytes set) must be specified for a correct signature validation and decryption.

Signature uses AES128 CMAC. Signature can be calculated over the {Encrypted Software} or over {Encrypted Software + Initialization Vector + Number of Blocks-1}. The number of blocks for signature calculation will be specified as a 16 bytes integer number in the {image}, although the number is programmed as a 16-bit integer in the corresponding register of the bootloader.

Decryption of the secured program uses AES128 CBC.

When secured software transfer has been selected, system operation will not start unless signature validation and decryption pass correctly.

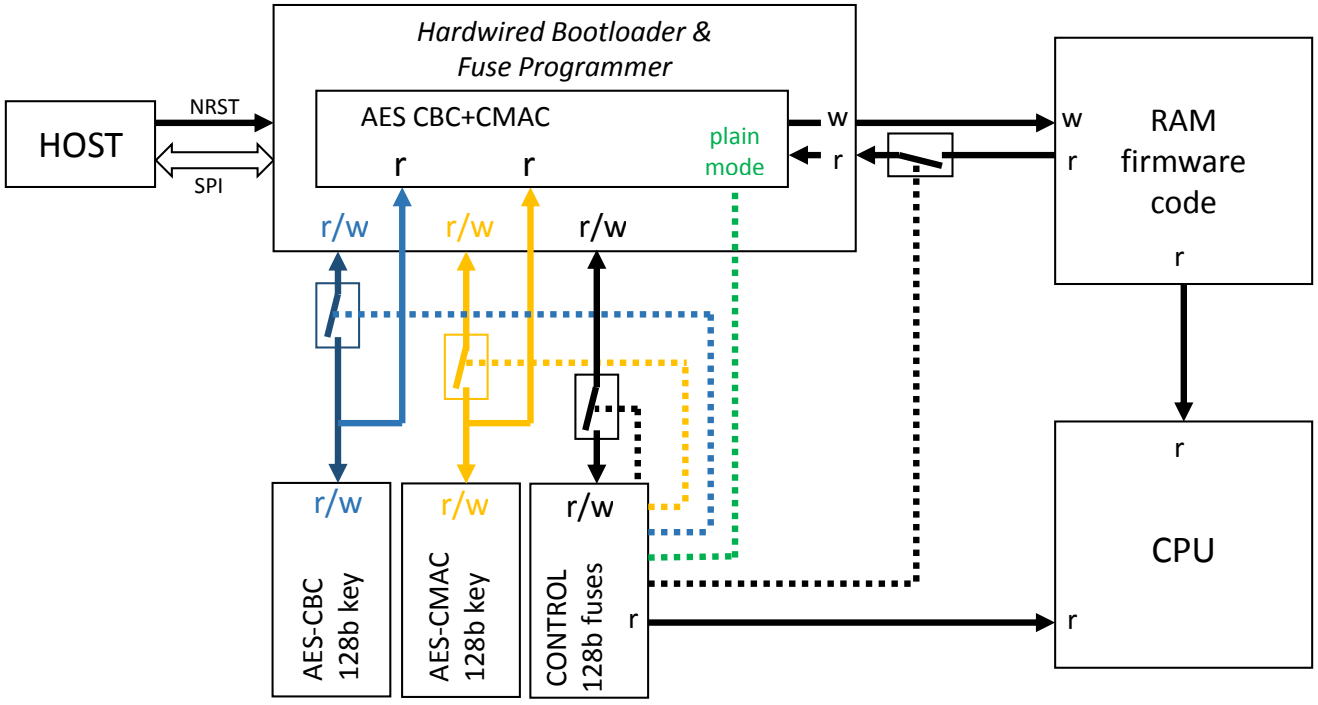
The bootloader also allows programming of security keys and security control fuses.

8.2 Embedded Characteristics

- Bootloader operates on SCK (typ.freq. 12Mhz, max.freq≤16Mhz), synchronously with core and bus clocks
- Fixed phase and polarity SPI control protocol
- Password to unlock bootloader
- Fuse programming control

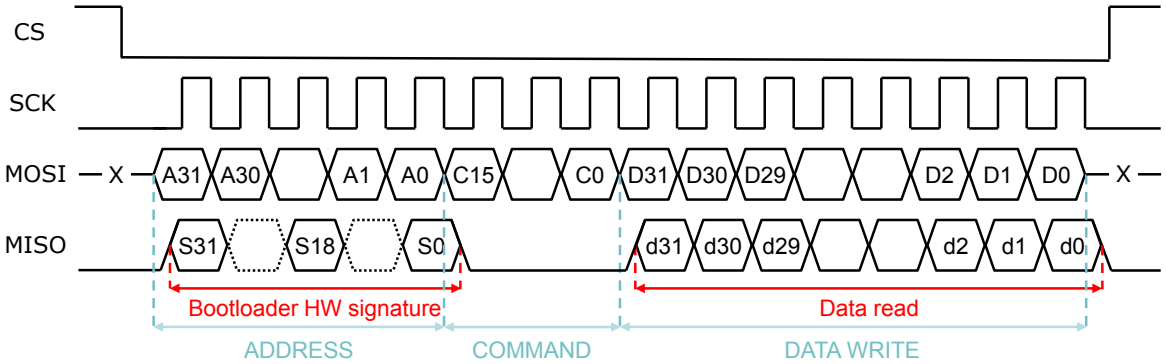
8.3 Block Diagram

Figure 8-1. Block Diagram



8.4 Functional Description

The bootloader loads the program from an external master to the internal memory of PL360. The external master can access instruction memory, data memory and registers through SPI. The bootloader only works in SPI Mode 0 (CPHA=1 and CPOL=0). The basic data transfer is:



The basic frame sent from the master through the MOSI signal is composed as shown in the following table:

Address	Command	Data
32-bit block	16-bit block	n blocks of 32 bits

All the blocks in the basic frame sent by MOSI use little-endian format.

Each frame received from the master will be acknowledged with a 32 bits signature through the MISO signal.

There is a series of SPI commands supported by the bootloader. The commands are:

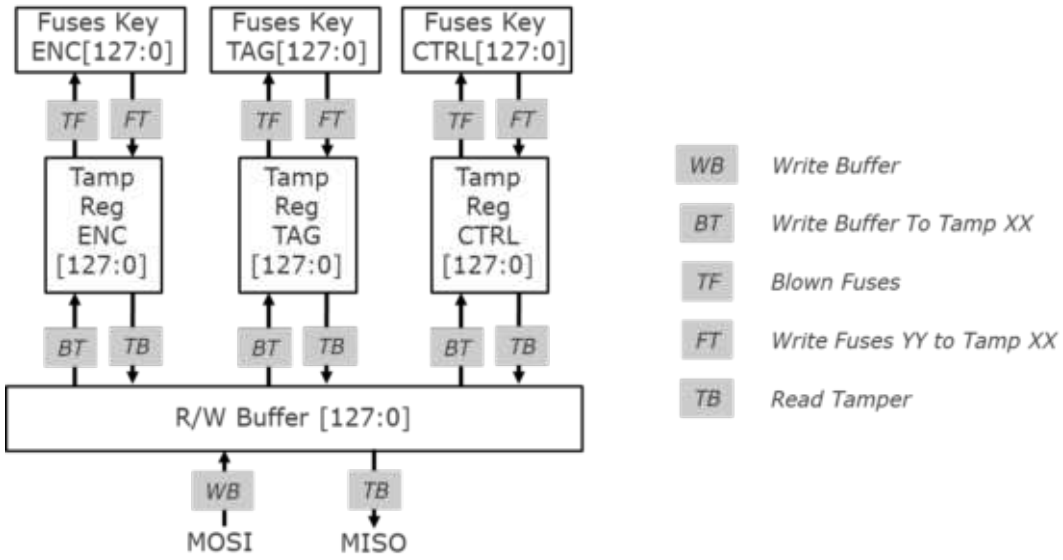
Command	Description	addr(31:0)	data(n*32-1:0)
0x0000	Write word on one address	0xAAAAAAAA(1)	0xDDDDDDDD(2)
0x0001	Write words on consecutive address	0xAAAAAAAA(1)	0xDDD…DDD(2) (3)
0x0002	Read words on consecutive address	0xAAAAAAAA(1)	0x000…000(4)
0x0003	Read word on one address	0xAAAAAAAA(1)	0x00000000
0x0004	Write number of decryption packets	0x00000000	0x0000DDDD(2)
0x0005	Write decryption initial vector	0x00000000	0xDDD…DDD(2) (3)
0x0006	Write decryption signature	0x00000000	0xDDD…DDD(2) (3)
0x0007	Write 128 bits fuses value to Buffer register	0x00000000	0xDDD…DDD(2) (3)
0x0008	Write Buffer register to Tamper register for KEY_ENC_FUSES	0x00000000	0x00000000
0x0009	Write Buffer register to Tamper register for KEY_TAG_FUSES	0x00000000	0x00000000
0x000B	Write Buffer register to Tamper register for CONTROL_FUSES	0x00000000	0x00000000
0x000C	Blow desired fuses	0x00000000	0x00000000
0x000D	Write KEY_ENC_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x000E	Write KEY_TAG_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0010	Write CONTROL_FUSES to the corresponding Tamper register	0x00000000	0x00000000
0x0011	Read Tamper register	0x00000000	0x000…000(4)
0x0012	Read bootloader status	0x00000000	0x00000000
0x0013	Start Decryption	0x00000000	0x00000000

.....continued			
Command	**Description**	**addr(31:0)**	**data(n*32-1:0)**
0x0014	Start/Stop BOOTLOADER access window in Master mode	0x00000000	0x00000000
0x0015	Start Decryption Plus	0x00000000	0x00000000
0xA55A	Control of MISO signal transferred to M7-SPI	0x00000000	0x00000000
0xA66A	Control of MISO signal transferred to M7-SPI and Bootloader clock disabled	0x00000000	0x00000000
0xDE05	Unblock bootloader	0x00000000	0xDDDDDDDD(2)

Notes:

1. 'AA' is an address byte
2. 'DD' is a data byte
3. Command contains as many bytes as needed to send
4. Command contains as many '00's as bytes wanted to be read

The figure below shows the structure of the registers and data transfers for fuses and their control logic.



8.4.1 Unlock, Load Program and Start Loaded Program

After Reset, the bootloader is locked, and the master must send two frames as password to unlock the bootloader. These frames are:

Order	Address	Command	Data
1	0x00000000	0xDE05	0x5345ACBA
2	0x00000000	0xDE05	0xACBA5345

At this point, the master sends commands to the bootloader and it can start loading the program to PL360. The program must be loaded starting in address 0x00000000.

After loading the program, it must be started. To start the loaded program requires clearing of the CPUWAIT bit of MSSC Miscellaneous register (Address 0x400E1800) and transferring the control of MISO signal to M7-SPI peripheral:

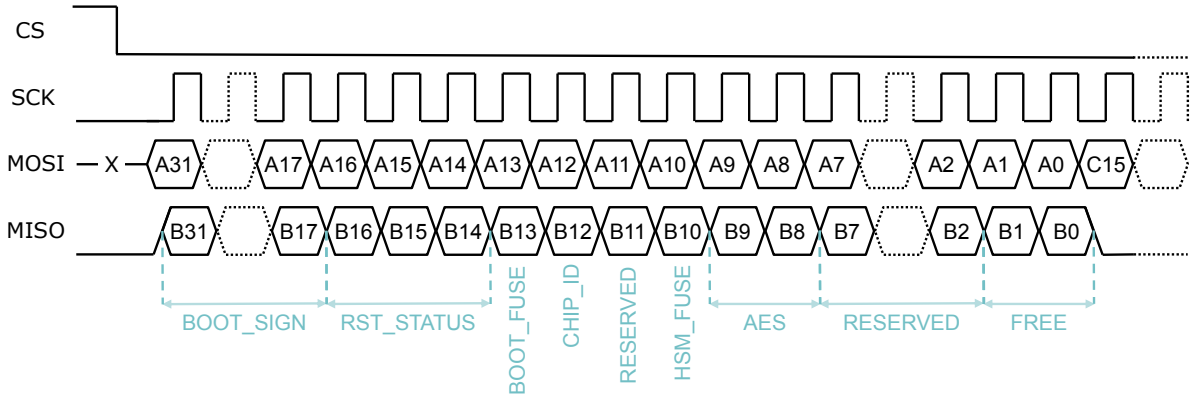
Order	Address	Command	Data
1	0x400E1800	0x0000	0x00000000
2	0x00000000	0xA66A	0x00000000

If this action is not done, the MISO signal will remain controlled by the BOOTLOADER.

8.4.2 Bootloader Hardware Signature

Each frame received from the master (write or read frame), will be acknowledged with a 32 bits signature through the MISO signal. This is used to give the bootloader's signature and the state of the system to the master.

This frame is composed of:



Bit	Name	Value
31..17	BOOT_SIGN	010101100011010
16	RST_STATUS	USER_RST
15		CM7_RESET
14		WDT_RESET
13	BOOT_FUSE	
12	CHIP_ID	
11	RESERVED	
10	HSM_FUSE	
9	AES_FUSES	AES_DIS
8		AES_128
7..2	RESERVED	
1..0	FREE_FUSES	

8.4.3 Write Process

The command used to write on a unique address is CMD=0x0000.

The command used to write on several consecutive addresses is CMD=0x0001. In this case, it will be sent the 32 bits of the initial address, 16 bits of command (0x0001) and as many consecutive words (32 bits) as are wanted to write.

Regarding the decryption packets, the commands to write the number of decryption packets (CMD=0x0004), the initial vector of decryption (CMD=0x0005) or the decryption signature to test if decryption is correct (CMD=0x0006), the address of the frame is not taken into account and it can be composed with any address value. To write the decryption packet, only the last 15 bits are taken into account. In the case of decryption initial vector and decryption

signature where it is necessary to send as data the 128 bit value, it is made in the same way than the write process at consecutive addresses, sending 4 consecutive words (32 bits).

To write a fuse box, the Buffer register must be written in advance (CMD=0x0007) and then the Tamper registers of KEY_ENC_BOX, KEY_TAG_BOX or CONTROL_BOX must be written with the content of the buffer (CMD=0x0008, CMD=0x0009 and CMD=0x000B respectively). Finally, to blow the desired fuses with the values in the corresponding Tamper register, the command (CMD=0x000C) must be sent with any address and any data value.

The end of this writing process is indicated in the answer of the bootloader status command (CMD=0x0012). If the writing process is active, bit 0 of the answer is '1'. In other case, all data of the answer is 0.

In the case of CONTROL_BOX, to activate the new values, it is also necessary to write the CONTROL_FUSES values to the corresponding Tamper register (CMD=0x0010).

8.4.4 Read Process

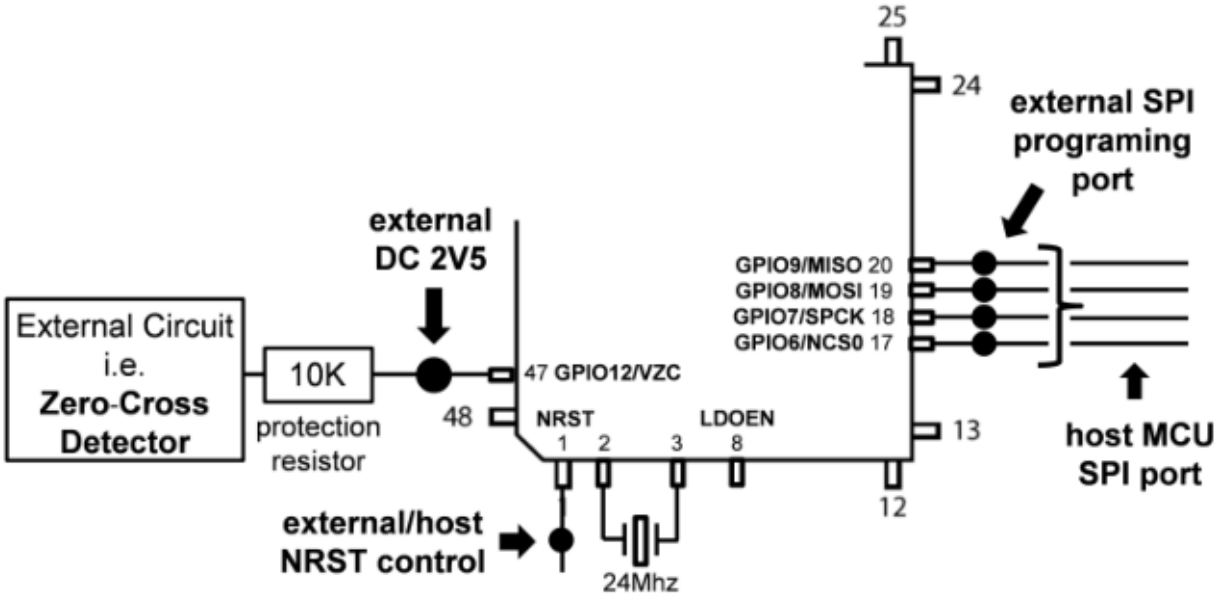
The command used to read an unique address is CMD=0x0003.

The command used to read several consecutive addresses is CMD=0x0002. In this case the frame will be composed of 32 bits for the address, 16 bits for the command and as many SCK pulses (always multiple of 32) as needed to read data.

To read a fuse box, it must be written previously in the corresponding Tamper register. The content of Tamper registers KEY_ENC_BOX, KEY_TAG_BOX or CONTROL_BOX are written to the buffer with the commands CMD=0x000D, CMD=0x000E and CMD=0x0010 respectively. Once the Tamper register is written, it can be read with the command CMD=0x0011.

8.4.5 Fuse Programming

To write control or key fuses, an external supply of 2.5V ±10% DC 50mA supply must be connected to VZC pin. If fuses are programmed in system, the appropriate protection of VZC circuitry by means of a 10K resistor must be implemented, as it is shown in the figure below.



The fuse programming commands are sent through SPI. In case of using an external fuses programming controller, the host MCU SPI ports must be left in High Impedance mode to allow the connection between PL360 and external fuses programming controller.

8.4.6 Control Fuses

The control fuse box includes 128 fuse bits. Only some of them are used to configure software security features, see table below. Reserved bits in the range 0 to 17 must not be modified. Bits from 18 to 128 are not used.

The default value of all fuses is not set.

Fuse Bit	Name	Description
0	ENCRNOTPLAIN	If it is set, Secure mode is active
1	READ_AES_KEY	If it is set, KEY_ENC and KEY_TAG can't be read
2	WRITE_AES_KEY	If it is set, KEY_ENC and KEY_TAG can't be written
5	READ_CONTROL	If it is set, CONTROL_FUSES can't be read
6	WRITE_CONTROL	If it is set, CONTROL_FUSES can't be written
7	READ_RAM	If it is set, memory ram can't be read
8	RESERVED	Reserved
9	RESERVED	Reserved
10	FORCE_IVNBINC	If it is set, initialization vector and number of blocks must be used in the calculation of the signature
11	RESERVED	Reserved
12	RESERVED	Reserved
13	RESERVED	Reserved
14	RESERVED	Reserved
15	RESERVED	Reserved
16	DBG_DISABLE	If it is set, JTAG debug is disabled
17	DBG_DISABLE_SE	Reserved

8.4.7 Decryption

After writing the full encrypted binary in the program RAM, decryption of the program is launched. There are two options depending on the content of the encrypted program which has been loaded.

If the KEY_TAG includes only the program, basic decryption is required (CMD=0x0013).

If the KEY_TAG includes the program plus initial vector and total number of packets, decryption plus is required (CMD=0x0015).

In both cases, neither address nor data are considered.

If FORCE_IVNBINC fuse is set to '1', both decryption commands (CMD=0x0013 and CMD=0x0015) will calculate the signature over SOFT+IV+NB.

8.4.8 Examples

8.4.8.1 Write a Non-encrypted Program

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0001_DDDDDDDD…	Write the program at consecutive addresses from 0x00000000
0x00000000_0002_XXXXXXXX…	(Optional) Read the program to validate it (READ_RAM fuse must be not set)
0x400E1800_0000_00000000	Clear CPUWAIT to start program operation
0x00000000_A66A_00000000	Give control of the MISO signal to M7-SPI and disable bootloader clock

8.4.8.2 Write an Encrypted Program when Keys are already Written

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0004_0000XXXX	Set the number of blocks of the encrypted program
0x00000000_0005_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Set the initialization vector of the encrypted program
0x00000000_0006_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Set signature of the encrypted program
0x00000000_0001_EEEEEEEE…	Write the program at consecutive addresses from 0x00000000
0x00000000_0013_00000000	Launch code decryption
0x00000000_0012_00000000	Check bootloader status to know if decrypt process has finished. Answers: • 0x”Bootloader Hardware signature”_0000_ 00000002 (aes_active) • 0x”Bootloader Hardware signature”_0000_ 00000000 (bootloader ready)
0x00000000_0002_XXXXXXXX…	(Optional) Read the decrypted program to validate it (READ_RAM fuse must not be set)
0x400E1800_0000_00000000	Clear CPUWAIT to start program operation
0x00000000_A66A_00000000	Give control of the MISO signal to M7-SPI and disable bootloader clock

8.4.8.3 Write Decryption Keys, or Control Bits, in the Fuse Boxes

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the decryption key KEY_ENC in the Buffer register
0x00000000_0008_00000000	Write the buffer register to the Tamper register for KEY_ENC_FUSES
0x00000000_000C_00000000	Blow fuses at corresponded fuse box
0x00000000_0012_00000000	Check bootloader status to know if process of blowing fuses has finished. Answers: • 0x”Bootloader Hardware signature”_0000_ 00000001 (fuse blowing active) • 0x”Bootloader Hardware signature”_0000_ 00000000 (bootloader ready)
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the signature/authentication key KEY_TAG in the Buffer register
0x00000000_0009_00000000	Write the buffer register to the Tamper register for KEY_TAG_FUSES
0x00000000_000C_00000000	Blow fuses at corresponded fuse box

.....continued	
Command	**Description**
0x00000000_0012_00000000	Check bootloader status to know if process of blowing fuses has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000001 (fuse blowing active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0007_XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX	Write the signature/authentication key KEY_TAG in the buffer register
0x00000000_000B_00000000	Write the Buffer register to the Tamper register for CONTROL_FUSES
0x00000000_000C_00000000	Blow fuses at corresponded fuse box
0x00000000_0012_00000000	Check bootloader status to know if process of blowing fuses has finished. Answers: • 0x"Bootloader Hardware signature"_0000_ 00000001 (fuse blowing active) • 0x"Bootloader Hardware signature"_0000_ 00000000 (bootloader ready)
0x00000000_0010_00000000	Read CONTROL_FUSES fuse value to its Tamper register to load the new value at system

8.4.8.4 Read Decryption Keys, or Control Bits, from the Fuse Boxes

Command	Description
0x00000000_DE05_5345ACBA	After Reset, unblock the bootloader
0x00000000_DE05_ACBA5345	
0x00000000_000D_00000000	Read fuse box values for KEY_ENC and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI
0x00000000_000E_00000000	Read fuse box values for KEY_TAG and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI
0x00000000_0010_00000000	Read fuse box values for CONTROL_FUSES and write them to the corresponding Tamper register
0x00000000_0011_00000000 00000000 00000000 00000000	Read the Tamper register through the SPI

9. Serial Peripheral Interface (SPI)

9.1 Description

The SPI circuit is a synchronous serial data link that provides communication with external devices in Slave mode. The Serial Peripheral Interface is essentially a Shift register that serially transmits data bits to a Master SPI device. During a data transfer, SPI master controls the data flow, while the slave device has data shifted into and out by the master.

The SPI system consists of two data lines and two control lines:

- Master Out Slave In (MOSI): This data line supplies the output data from the master shifted into the input(s) of the slave(s)
- Master In Slave Out (MISO): This data line supplies the output data from a slave to the input of the master. There may be no more than one slave transmitting data during any particular transfer
- Serial Clock (SPCK): This control line is driven by the master and regulates the flow of the data bits. The master can transmit data at a variety of baud rates; there is one SPCK pulse for each bit that is transmitted
- Peripheral Chip Select (NPCS): This control line allows slaves to be turned on and off by hardware

9.2 Embedded Characteristics

- Slave Serial Peripheral Bus Interface
  - 8-bit to 16-bit data length
- Slave Mode Operates on SPCK, Asynchronously with Core and Bus Clock

9.3 Signal Description

The pins used for interfacing the compliant external devices are multiplexed with PIO lines.

Table 9-1. I/O Lines

Instance	Signal	Pin Description	Slave	I/O Line
SPI0	SPI0_MISO	Master In Slave Out	Output	PA9
SPI0	SPI0_MOSI	Master Out Slave In	Input	PA8
SPI0	SPI0_NSS	Peripheral Chip Select/Slave Select	Input	PA6
SPI0	SPI0_SPCK	Serial Clock	Input	PA7

9.4 Functional Description

9.4.1 Data Transfer

Four combinations of polarity and phase are available for data transfers. Consequently, a master/slave pair must use the same parameter pair values to communicate.

Table 9-2 shows the four modes and corresponding parameter settings.

Table 9-2. SPI Bus Protocol Modes

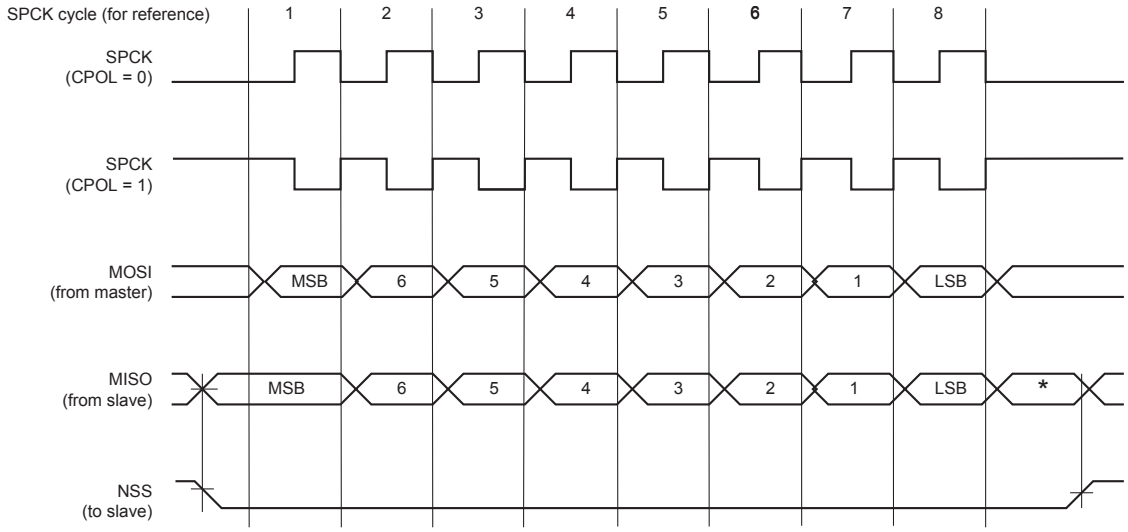
SPI Mode	Shift SPCK Edge	Capture SPCK Edge	SPCK Inactive Level
0	Falling	Rising	Low

.....continued

SPI Mode	Shift SPCK Edge	Capture SPCK Edge	SPCK Inactive Level
1	Rising	Falling	Low
2	Rising	Falling	High
3	Falling	Rising	High

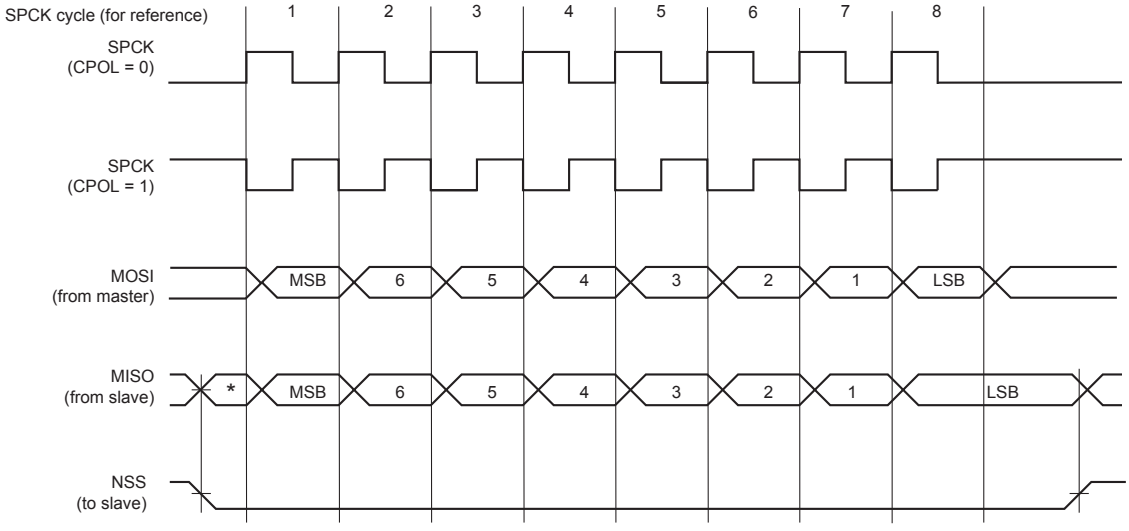
Figure 9-1 and Figure 9-2 show examples of data transfers.

Figure 9-1. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)



* Not defined.

Figure 9-2. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined.

9.4.2 SPI Slave Mode

When operating in Slave mode, the SPI processes data bits on the clock provided on the SPI clock pin (SPCK). The SPI waits until NSS goes active before receiving the serial clock from an external master. When NSS falls, the clock is validated and the data is loaded.

The bits are shifted out on the MISO line and sampled on the MOSI line.

When a transfer starts, the data shifted out is the data present in the internal Shift register. If no data has been written, the last data received is transferred. If no data has been received since the last reset, all bits are transmitted low, as the internal Shift register resets to 0.

When a first data is written, it is transferred immediately in the internal Shift register. If new data is written, it remains until a transfer occurs, i.e., NSS falls and there is a valid clock on the SPCK pin. When the transfer occurs, the last data written is transferred in the internal Shift register. This enables frequent updates of critical variables with single transfers.

If no character is ready to be transmitted, i.e., no character has been written since the last load to the internal Shift register, last character is retransmitted.

9.4.3 SPI Typical Frequencies

Table 9-3. Typical Operating Frequency

Application case	Typical frequency
CENELEC A / CENELEC B	8MHz
FCC (transmission band above 150 kHz)	12MHz
Bootloader	12MHz

10. Transmission Path

10.1 Description

The Transmission Path adapts input digital signal to a bit-stream emitted through the EMIT pins which inputs the PLC Coupling. The Transmission Control block manages the start and the end of any transmission.

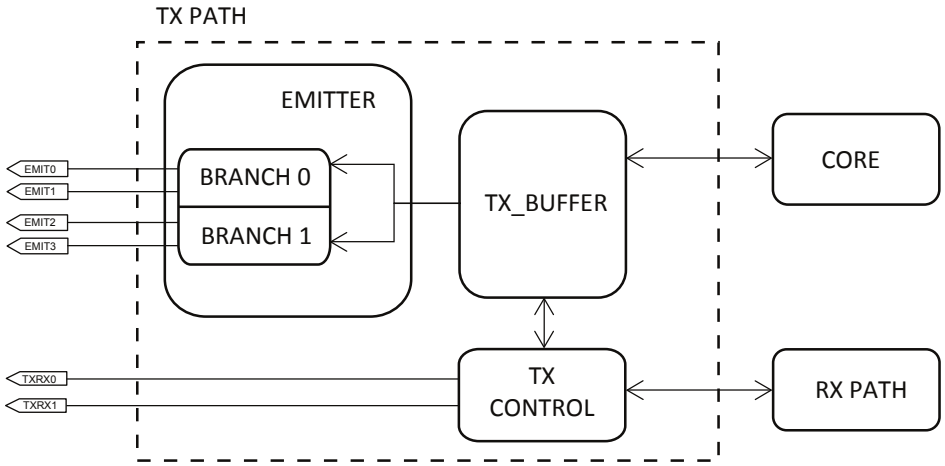
The Emitter block allows to emit bit-stream through two different pair of EMIT pins, managed independently one from the other with different TXRX pins, which indicate which pair of EMIT pins is transmitting.

10.2 Embedded Characteristics

- Able to transmit using two independent transmission branches
- Supports driving of external amplifier (”external driver”)
- Supports configuration without external driver (”internal driver”)

10.3 Block Diagram

Figure 10-1. Block Diagram



10.4 Product Dependencies

10.4.1 I/O Lines

The TXRX0 and TXRX1 pins are multiplexed with PIO lines. TXRX pins indicate if the associated branch is transmitting or not.

In case of using a coupling with internal driver, only one branch is allowed and all the four EMIT pins must be connected to the same point and transmission control is indicated by TXRX0.

In case of using a coupling with external driver:

- if the coupling uses only one branch, EMIT0-EMIT1 pins are used and transmission control is indicated by TXRX0
- if the coupling uses two branches, EMIT and TXRX pins are used as is indicated by Table 10-1

Table 10-1. I/O Lines

Branch	EMIT		Control Signal	
	Signal	Pinout	Control Signal	I/O Line
1	EMIT0	23	TXRX0	PA10
	EMIT1	25		
2	EMIT2	27	TXRX1	PA11
	EMIT3	31		

11. Reception Path

11.1 Description

The Reception Path has two main purposes:

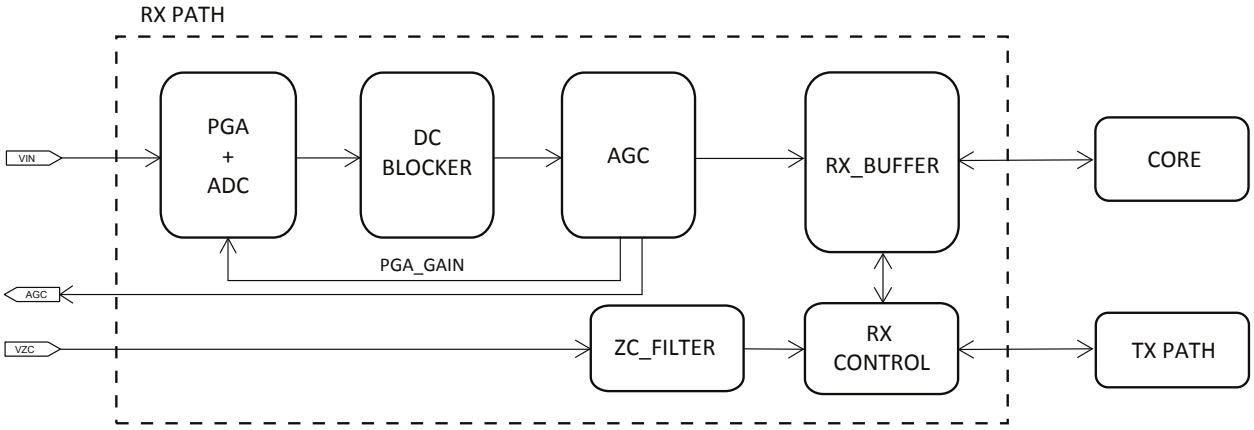
- Adapting the input signal from external coupling stage to downsample a digital signal in order to obtain received data
- Calculating zero-crossing from an adapted signal obtained from mains

11.2 Embedded Characteristics

- AGC for maintaining constant level of energy at input
- Zero-Cross Detection

11.3 Block Diagram

Figure 11-1. Block Diagram

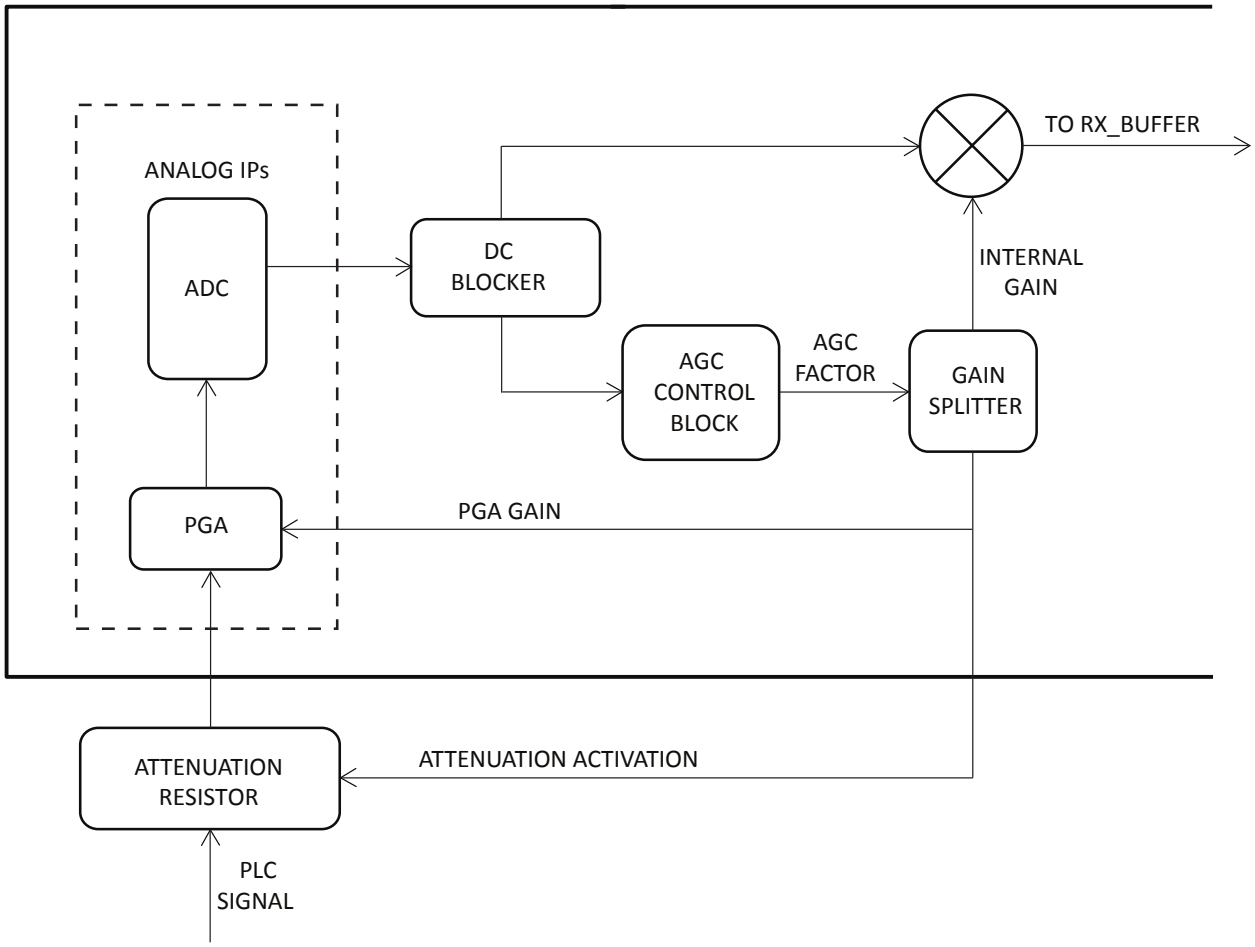


11.4 Functional Description

11.4.1 Automatic Gain Control (AGC)

AGC peripheral adapts the input PLC signal to accomplish the requirements of PL360 core.

Figure 11-2. Block Diagram

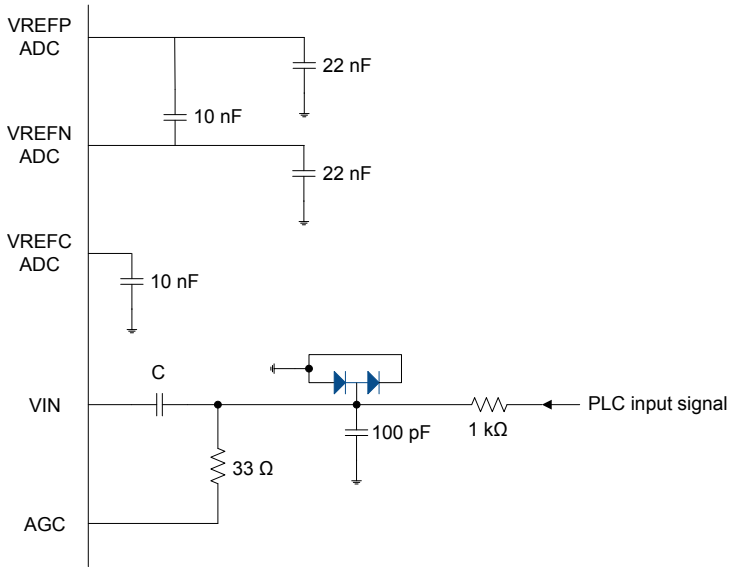


The DC blocker removes a possible existing DC offset after the ADC. It calculates the average value of DC and subtracts it from the input signal. It is done by means of a very narrow low pass filter.

Once the DC has been removed, the signal enters into the AGC Block. The objective of the AGC block is to maintain a constant level of energy at the core input. In case of detecting impulsive noise, the AGC maintains the amplifying factor. However, if the amplitude of the incoming signal decreases, the AGC reacts quickly and amplifies the signal.

The output AGC signal is used to activate an external resistor, which attenuates the input signal. The target is to avoid the saturation of the ADC.

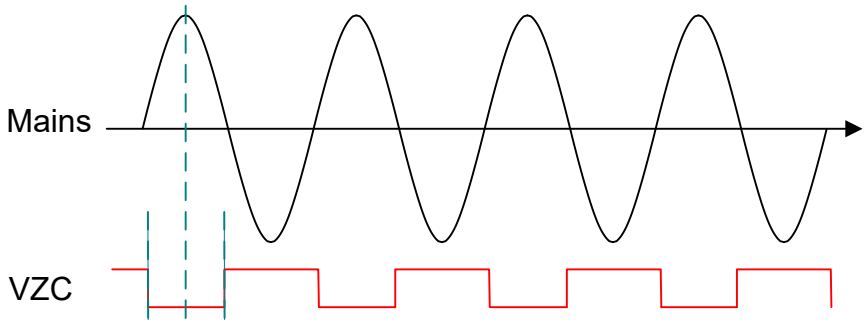
Figure 11-3. Electrical Connections for PLC Reception



11.4.2 Zero-crossing detection

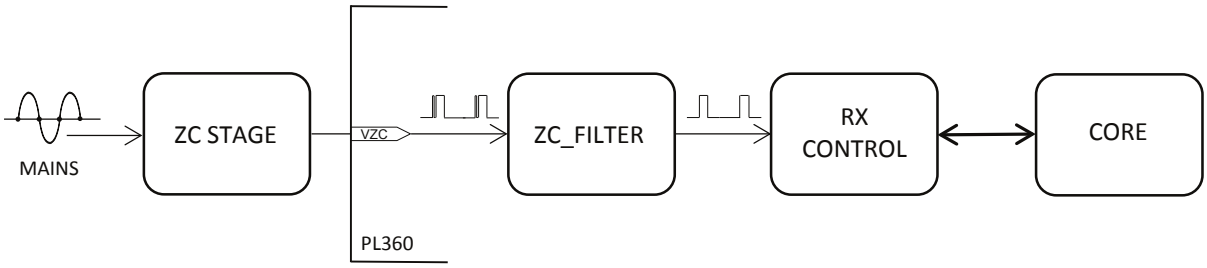
In the PL360, the Zero-Crossing Detection strategy is based on a digital filter circuitry to eliminate quick transitions after the zero-cross input stage. Rising and falling edges times are measured also by hardware and then a PLL software algorithm is applied. The center of the low level pulse input must be aligned with the peak of the mains wave, although some adjustment can be made on the application to correct the delay between pulse and wave.

Figure 11-4. Zero-Crossing Signal



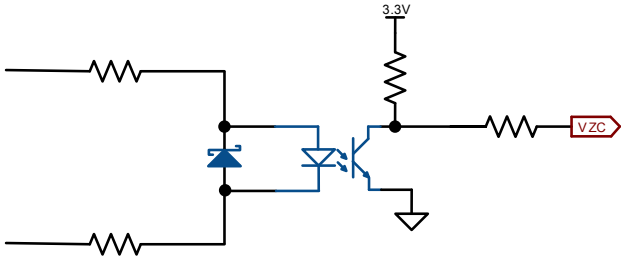
The achieved precision meets the standard requirements to track 50Hz or 60Hz ±10% mains.

Figure 11-5. Block Diagram



A simple external circuit is required to adapt the mains signal to VZC input. A typical application circuit for unidirectional topologies is shown in Figure 11-6.

Figure 11-6. Typical Circuit, Using a Unidirectional Optocoupler



11.4.3 Dumping Buffer

In parallel with RX Buffer, a Dumping Buffer (DP Buffer) is implemented. The main purpose of DP Buffer is to store samples to be analyzed for channel characterization purposes. The content of DP Buffer is accessible via SPI.

12. Advanced Encryption Standard (AES)

12.1 Description

PL360 includes a dedicated peripheral to perform AES operations. The AES algorithm is a symmetric block cipher that can encrypt (encipher) and decrypt (decipher) information.

The AES algorithm supports the use of cryptographic keys of 128, 192 and 256 bits to encrypt and decrypt data in blocks of 128 bits.

13. Electrical Characteristics

13.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

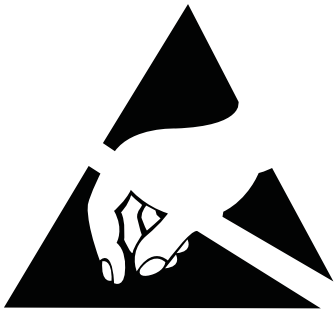
Table 13-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDIO	-0.5 to 4.0	V
Input Voltage	VI	-0.5 to VDDIO +0.5 (≤ 4.0V)	
Output Voltage	VO	-0.5 to VDDIO +0.5 (<4.0V)	
Storage Temperature	T_{ST}	-55 to 125	ºC
Junction Temperature	T_J	-40 to 125	
Output Current(1)	IO	±8(2)	mA

Notes:

1. DC current that continuously flows for 10 ms or more, or average DC current
2. Applies to all the pins except EMIT and AGC pins. EMIT and AGC pins should only be used according to circuit configurations recommended by Microchip

ATTENTION observe ESD precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection.

13.2 Recommended Operating Conditions

Table 13-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VDDIO	3.00	3.30	3.60	V
	VDDIN_AN	3.00	3.30	3.60	
	VDDIN	3.00	3.30	3.60	
	VDDPLL	1.15	1.25	1.32	

.....continued

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Junction Temperature	T_J	-40	25	125	ºC
Ambient Temperature	T_A	-40	-	85	

Table 13-3. Thermal Resistance Data

Package	Symbol	Parameter	Condition	Typ	Unit
TQFP48	θ_{JA}	Junction-to-ambient thermal resistance	Still Air	57.5	ºC/W
			1m/s	50.3	
			2m/s	48.1	
	θ_{JC}	Junction-to-case thermal resistance	-	14.1	
QFN48	θ_{JA}	Junction-to-ambient thermal resistance	Still Air	45.4	ºC/W
			1m/s	39.5	
			2m/s	37.9	
	θ_{JC}	Junction-to-case thermal resistance	-	13.5	

θ_{JA} is calculated based on a standard JEDEC JESD51-5 defined environment (1.6mm thickness PCB, 4 copper layers, 76.2mm x 114.3mm board) and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

13.3 Electrical Pinout

Table 13-4. 48 - Lead TQFP/QFN Electrical Pinout

Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
1	NRST	I	-	-	Y	25	EMIT1	OT	± 60(1)	-	-
2	XIN	I	-	-	-	26	VDDIO	P	-	-	-
3	XOUT	O	-	-	-	27	EMIT2	OT	± 60(1)	-	-
4	VDDIO	P	-	-	-	28	VDDIO	P	-	-	-
5	VDDPLL	P	-	-	-	29	VDDCORE	P	-	-	-
6	GND	P	-	-	-	30	GND	P	-	-	-
7	VDDCORE	P	-	-	-	31	EMIT3	OT	± 60(1)	-	-
8	VDDIN	P	-	-	-	32	VDDIO	P	-	-	-
9	LDO ENABLE	I	-	-	-	33	PA11/TXRX1	I/O	± 2/4	PU/PD/-	Y/-
10	PA4/SWDIO	I/O	± 2/4	PU/PD/-	Y/-	34	PA10/TXRX0	I/O	± 2/4	PU/PD/-	Y/-
11	PA5/SWCLK	I/O	± 2/4	PU/PD/-	Y/-	35	AGC	OT	± 20(2)	PU/-	-
12	VDDIO	P	-	-	-	36	VDDIO	P	-	-	-
13	PA0	I/O	± 2/4	PU/PD/-	Y/-	37	GND	P	-	-	-
14	PA1	I/O	± 2/4	PU/PD/-	Y/-	38	AGND	P	-	-	-

.....continued

Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
15	PA2/TRACESWO	I/O	± 2/4	PU/PD/-	Y/-	39	VIN	I	-	-	-
16	PA3	I/O	± 2/4	PU/PD/-	Y/-	40	VDDIN_AN	P	-	-	-
17	PA6/NPCS0	I/O	± 2/4	PU/PD/-	Y/-	41	VREFP(4)	-	-	-	-
18	PA7/SPCK	I/O	± 2/4	PU/PD/-	Y/-	42	VREFC(4)	-	-	-	-
19	PA8/MOSI	I/O	± 2/4	PU/PD/-	Y/-	43	VREFN(4)	-	-	-	-
20	PA9/MISO	I/O	± 2/4	PU/PD/-	Y/-	44	AGND	P	-	-	-
21	VDDIO	P	-	-	-	45	VDDIN_AN	P	-	-	-
22	GND	P	-	-	-	46	VDDIO	P	-	-	-
23	EMIT0	OT	± 60(1)	-	-	47	PA12/VZC	I	-	(3)	Y
24	VDDIO	P	-	-	-	48	TST	I	-	-	Y

I/O = pin direction (I = input, O = output, T = tri-state, P = power)

I(mA) = nominal current (+ = source, - = sink)

Res = pin pull up/pull down resistor (PU = pull up, PD = pull down (70 - 140 kΩ, typical 100 kΩ))

HY = Input Hysteresis (Y = yes)

Notes:

1. Selectable from 15mA to 60mA in 10 steps of 5mA
2. Selectable from 5mA to 20mA in 4 steps of 5mA
3. In case of fuse programming, an external 10kΩ serial resistor is needed. See 8.4.5 Fuse Programming
4. VREFP, VREFC and VREFN are analog signals

13.4 DC Characteristics

Table 13-5. PL360 DC Characteristics

Parameter	Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Supply Voltage		VDDIO	3.00	3.30	3.60	V
H-level Input Voltage (3.3V CMOS)		VIH	2.0	-	VDDIO +0.3	
L-level Input Voltage (3.3V CMOS)		VIL	-0.3	-	0.8	
H-level Output Voltage	3.3V I/O IOH = -100 µA	VOH	VDDIO -0.2	-	VDDIO	
L-level Output Voltage	3.3V I/O IOL = 100 µA	VOL	0	-	0.2	
Internal Pull Up Resistor(1)	3.3V I/O	Rpu	70	100	140	kΩ
Internal Pull Down Resistor(1)	3.3V I/O	Rpd	70	100	140	

Note:

1. Only applicable to pins with internal pulling

13.5 Power Consumption

The table below shows power consumption of the system (digital and analog) when it is used with typical AMR protocols. However, it is important to remember that different protocols, or even the same protocols used with different clock schemes or with different software implementations, can lead to other consumption figures.

Table 13-6. Full System Power Consumption

Frequency band	Application Case	Rating		Unit
		Typ(1)	Max(2)	
CENELEC-A CENELEC-B	Reception waiting for preamble detection	112	-	mW
	Reception processing incoming frames	146	-	
	Transmission with external driver and coupling board	164	-	
	90% time in transmission with external driver and coupling board and 10% time waiting for preamble detection	-	210	
FCC	Reception waiting for preamble detection	211	-	
	Reception processing incoming frames	286	-	
	Transmission with external driver and coupling board	327	-	
	90% time in transmission with external driver and coupling board and 10% time waiting for preamble detection	-	396	

Notes:

1. T_{AMB} = 25ºC, VDDIO = 3.3V, VDDIN = 3.3V and VDDIN_AN = 3.3V, G3-PLC
2. T_{AMB} = 85ºC, VDDIO = 3.6V, VDDIN = 3.6V and VDDIN_AN = 3.6V, G3-PLC

The table below shows power consumption of the analog IPs in the system. Analog parts are the PLL used for internal clock generation (supplied from VDDPLL pin) and the conversion module composed of the Programmable Gain Amplifier (PGA) and the Analog-to-Digital Converter (ADC), both supplied from VDDIN_AN pins.

Maximum consumption cases should be taken into account for supply filter calculation. Supply voltage drop after the filters must be small enough to guarantee correct operation of the analog IPs. Voltage applied to VDDPLL and VDDIN_AN must always be greater than Vtypical-10%, VDDPLL > 1.08V and VDDIN_AN > 3.0V.

Table 13-7. Analog Power Consumption

Supply	Block	Application Case	Rating			Unit
			Min	Typ	Max	
VDDPLL	**PLL**	-	-	1.7(1)	2.1(2)	mA
VDDIN_AN	**PGA**	-	-	1.5(3)	2.2(4)	
	ADC	CENELEC-A / CENELEC-B	-	7.5(3)	10.8(4)	
		FCC	-	14.4(3)	20.9(4)	

Notes:

1. Typical case conditions: freq=216Mhz, T_{AMB} = 25ºC, VDDPLL = 1.2V
2. Worst case conditions: freq=216Mhz, T_{AMB} = 125ºC, VDDPLL = 1.32V
3. Typical case conditions: T_J = 25ºC, VDDIN_AN = 3.3V
4. Worst case conditions: T_J = 125ºC, VDDIN_AN = 3.6V

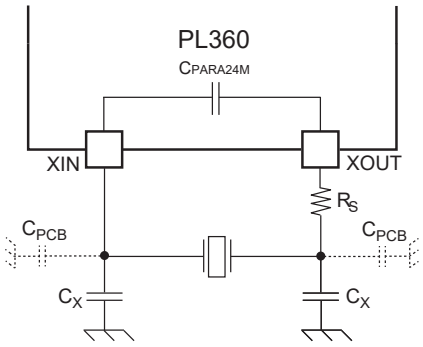
13.6 Crystal Oscillator

Table 13-8. PL360 24 MHz Crystal Oscillator Characteristics

Parameter	Test Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Crystal Oscillator frequency	Fundamental	X_{tal}		24		MHz
Internal parasitic capacitance	Between XIN and XOUT	$C_{PARA24M}$	0.6	0.7	0.8	pF
Start-up time		t_{ON}	-	-	1	ms
Drive level		P_{ON}	-	-	400	µW
Load capacitance		C_{LOAD}	4	-	18	pF

Note: The crystal should be located as close as possible to XOUT and XIN pins.

Figure 13-1. 24 MHz Crystal Oscillator Schematic



$$C_X = 2 \times (C_{XTAL} - C_{PARA24M} - C_{PCB}/2)$$

where C_{PCB} is the ground referenced parasitic capacitance of the printed circuit board (PCB) on XIN and XOUT tracks.

Table 13-9 summarizes recommendations to be followed when choosing a crystal.

Table 13-9. Recommended Crystal Characteristics

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Equivalent Series Resistor	ESR	-	-	100	Ω
Motional capacitance	C_M	2	-	3.2	fF
Shunt capacitance	C_{SHUNT}	-	-	1.3	pF

13.7 PGA and ADC

Table 13-10. PL360 PGA and ADC Input Characteristics

Parameter	Typical Value	Unit
VIN input impedance	10	kΩ
VIN max voltage dynamic range	± 0.75	V

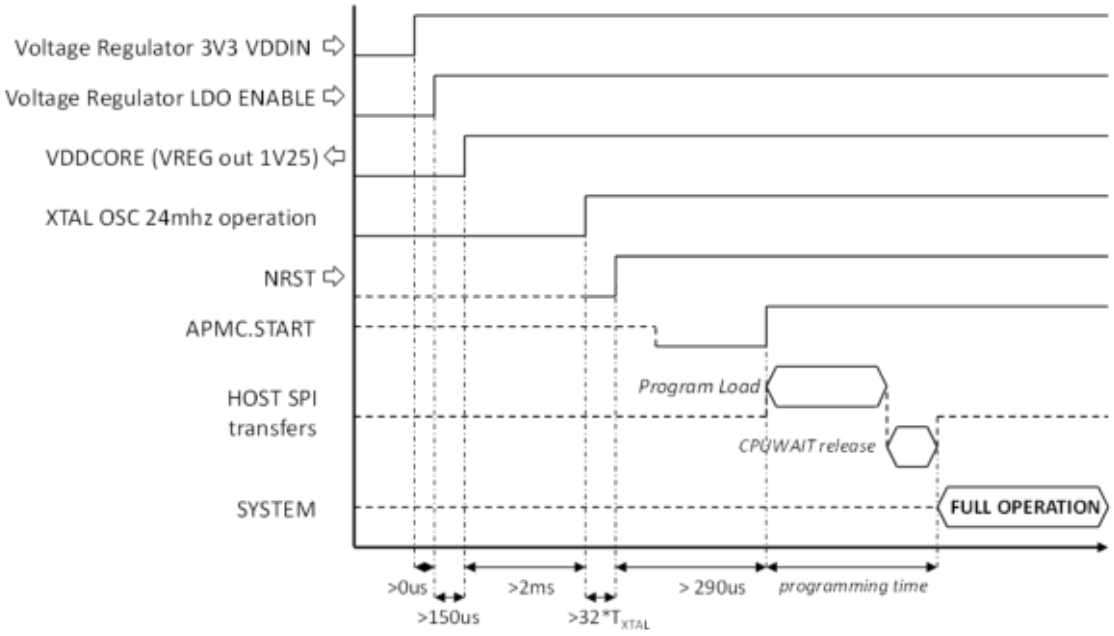
Note: Although the maximum VIN range is 0 - 3.3V, the PGA has been designed to saturate with any input value greater than VCM ±0.75V. To clamp the input signal, a pair of series diodes can be used to easily achieve it.

13.8 Power On Considerations

The Power On procedure starts after enabling the embedded voltage regulator. It is mandatory to wait for a stable 3V3 supply input to the voltage regulator before enabling it.

Crystal oscillator starts automatically after VDDCORE is stable, it takes a maximum of 2ms to get stable operation. The NRST pin must be tied to '0' during crystal oscillation startup, and it must be released to '1' after, at least, 32 X_{tal} clock periods. The clock signals will start operation ≈290µs after NRST release. Then the external host CPU will access to Bootloader logic to transfer the program and release the system for operation.

Figure 13-2. Power On Timing Diagram

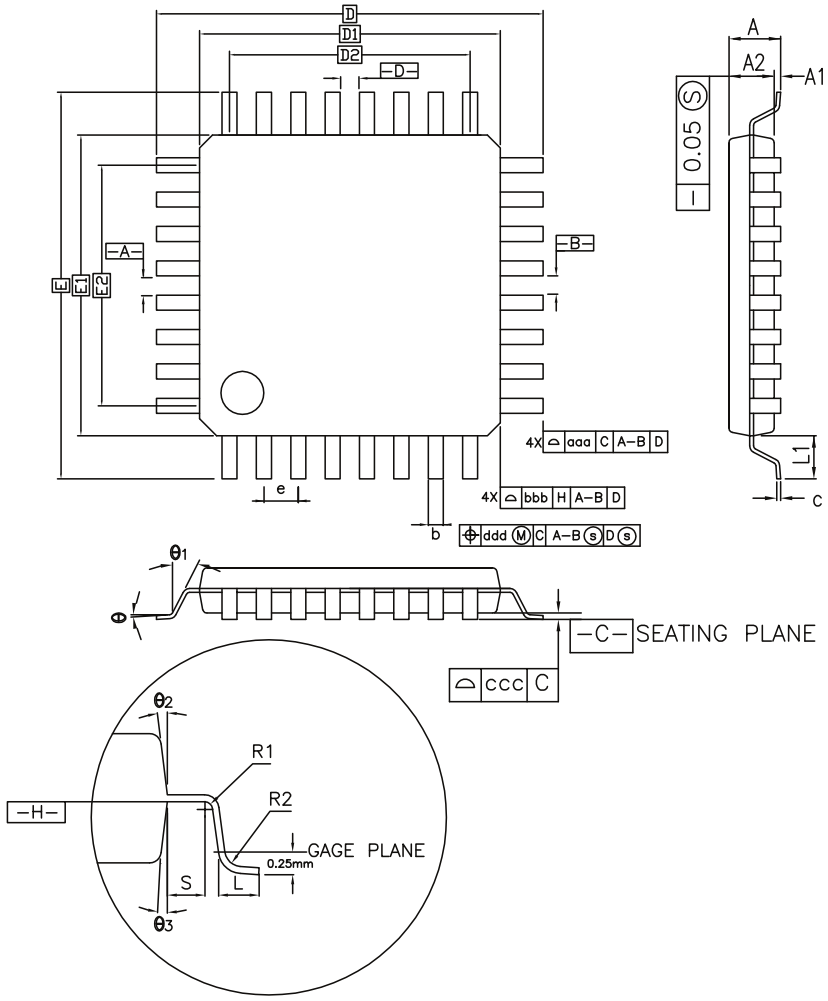


Timing between LDO ENABLE active and NRST release must always be greater than {150µs + 2ms + 32Tx_{tal}} as it is shown in previous figure.

14. Mechanical Characteristics

14.1 TQFP48 Mechanical Characteristics

Figure 14-1. 48 TQFP Package Dimensions



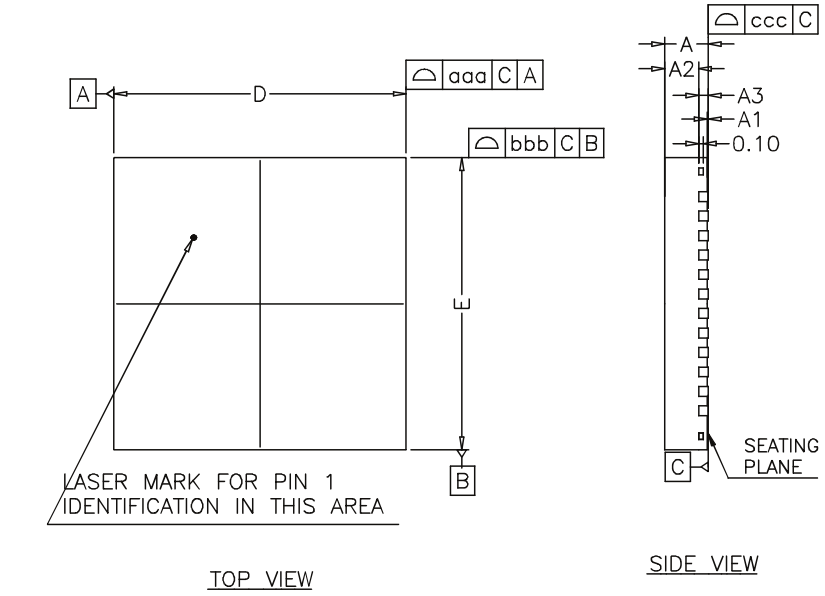
CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BSC.			0.354 BSC.		
D_1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E_1	7.00 BSC.			0.276 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	48L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

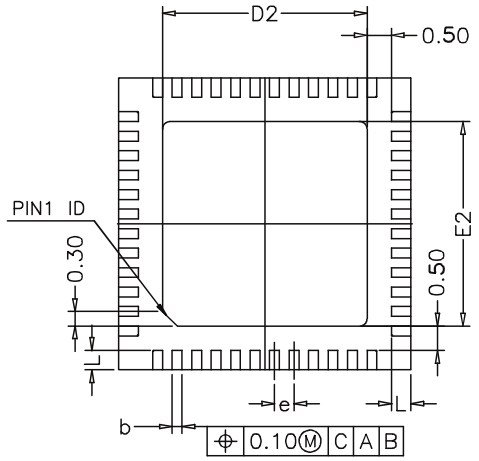
14.2 QFN48 Mechanical Characteristics

Figure 14-2. 48 QFN Package Dimensions



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D2	4.10	4.20	4.30	0.161	0.165	0.169
E	6.00 bsc			0.236 bsc		
E2	4.10	4.20	4.30	0.161	0.165	0.169
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.08			0.003		



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. –1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.

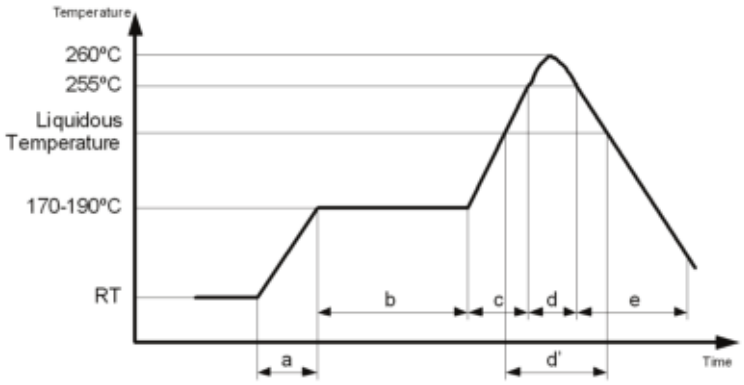
15. Recommended Mounting Conditions

15.1 Conditions of Standard Reflow

Table 15-1. Recommended Mounting Conditions of Standard Reflow

Items	Contents	
Method	IR (Infrared Reflow) / Convection	
Times	2	
Floor Life	Before unpacking	Please use within 2 years after production
	From unpacking to second reflow	Within 8 days
	In case over period of floor life	Baking with 125ºC +/- 3ºC for 24hrs +2hrs/-0hrs is required. Then please use within 8 days (please remember baking is up to 2 times)
Floor Life Condition	Between 5ºC and 30ºC and also below 70% RH required. (It is preferred lower humidity in the required temp. range)	

Figure 15-1. TQFP Package Soldering Profile



Notes:

H rank: 260ºC Max

a: Average ramp-up rate:	1ºC/s to 4ºC/s
b: Preheat & Soak:	170ºC to 190ºC, 60s to 180s
c: Average ramp-up rate:	1ºC/s to 4ºC/s
d: Peak temperature:	260ºC Max, up to 255ºC within 10s
d': Liquidous temperature:	Up to 230ºC within 40s or
	Up to 225ºC within 60s or
	Up to 220ºC within 80s
e: Cooling:	Natural cooling or forced cooling

15.2 Manual Soldering

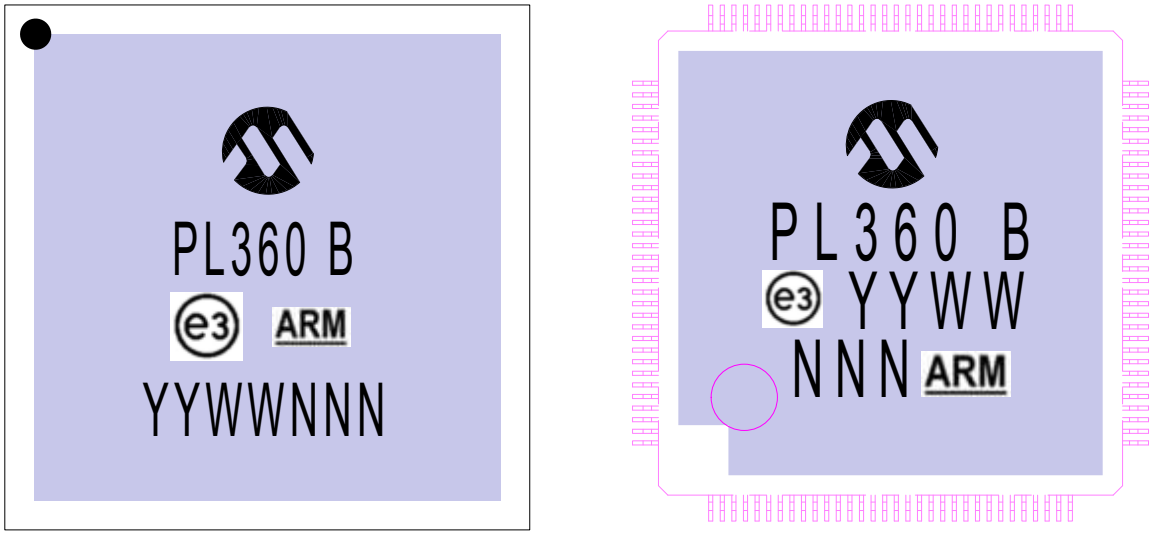
Table 15-2. Recommended Mounting Conditions of Manual Soldering

Items	Contents	
Floor Life	Before unpacking	Please use within 2 years after production
	From unpacking to Manual Soldering	Within 2 years after production (No control required for moisture adsorption because it is partial heating)
Floor Life Condition	Between 5°C and 30°C and also below 70% RH required. (It is preferred lower humidity in the required temp. range)	
Solder Condition	Temperature of soldering iron: Max 400°C, Time: Within 5 seconds/pin. *Be careful touching package body with iron	

16. Marking

All devices are marked with the Microchip logo and the ordering code.

Figure 16-1. QFN48 and TQFP48 Marking



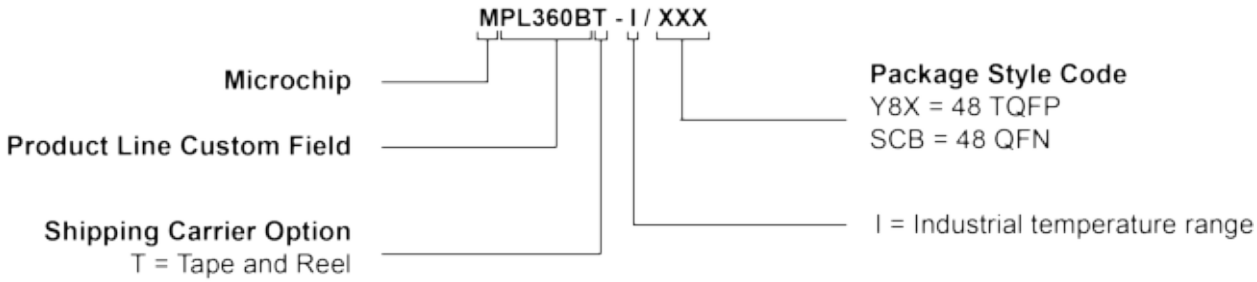
Where:

- M: Microchip logo
- PL360 B: Product name
- e3: Jedec code
- YYWW: Traceability code
- NNN: Traceability code
- ARM: ARM logo

17. Ordering Information

Table 17-1. Ordering Information

Microchip Ordering Code	Package	Carrier Type	Package Type	Temperature Range
MPL360B-I/Y8X	48 TQFP	Tray	Pb-Free	Industrial (-40ºC to 85ºC)
MPL360BT-I/Y8X	48 TQFP	Tape and Reel	Pb-Free	Industrial (-40ºC to 85ºC)
MPL360B-I/SCB	48 QFN	Tray	Pb-Free	Industrial (-40ºC to 85ºC)
MPL360BT-I/SCB	48 QFN	Tape and Reel	Pb-Free	Industrial (-40ºC to 85ºC)



18. Revision History

18.1 Rev A - 06/2018

Document	First issue.

18.2 Rev B - 01/2019

8. Bootloader	Updated section 8.1 Description. Updated Figure in section 8.4 Functional Description. Updated 0xDE05 command in table of section 8.4 Functional Description. Added Figure in section 8.4.2 Bootloader Hardware Signature.

18.3 Rev C - 08/2019

3. Signal Description	Updated “function” field description in VDDCORE and VDDPLL signals.

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