PL904xxx

Revision 1.0

General Description

The PL904xxx series is a small form-factor, high performance, programmable device and a member of Micrel's JitterBlocker factory programmable jitter attenuators. The JitterBlocker product family cleans deterministic jitter by attenuating spurious components in the phase noise, thereby improving the phase jitter and the overall phase noise. The PL904xxx is capable of reducing multiple pico seconds of phase jitter in a clock to a level below 0.5ps$_{RMS}$ in most cases, making that clock usable for many more applications.

The PL904xxx operates on a single 2.5V or 3.3V supply and is housed in a small QFN package for a broad range of applications.

Input clock frequencies up to 250MHz can be filtered and frequency translation allows for output clock frequencies up to 850MHz. The input clock can be single-ended or differential.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Block Diagram



Features

- Input frequency up to 250MHz
- Output frequency up to 850MHz
- Programmable input type, differential or single-ended
- Up to two outputs with LVPECL, LVDS, HCSL, or LVCMOS logic types
- Output enable control for each output
- Jitter attenuation of 20db at 3MHz spur frequency
- Cleans up spurs to below 0.5ps$_{RMS}$ phase jitter
- Operating temperature range from –40°C to 85°C
- Available in 32-pin QFN GREEN/RoHS-compliant package
- Related devices:
  - PL902: LVCMOS, Period Jitter cleaning
  - PL903: Single ended input, one differential output, Phase Noise cleaning

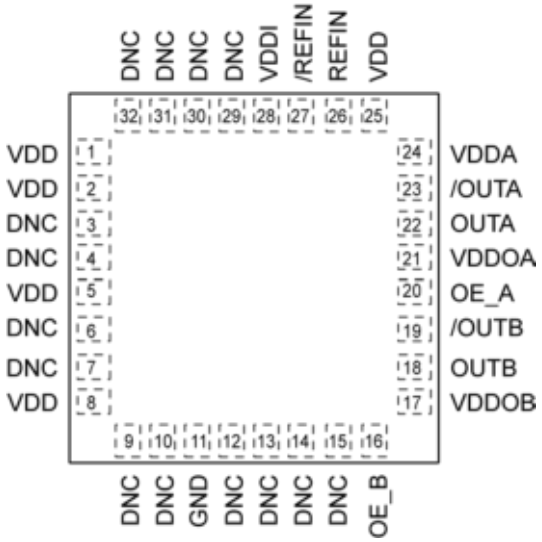
Applications

- 1/10/40/100 Gigabit Ethernet (GbE)
- SONET/SDH
- PCI Express
- CPRI/OBSAI wireless base stations
- Fibre Channel
- SAS/SATA
- DIMM

Ordering Information

Part Number	Marking	Shipping	Ambient Temp. Range	Package	Lead Finish
PL904xxxUMG	PL904 XXX	Tray	–40° to +85°C	QFN-32L	NiPdAu
PL904xxxUMG TR	PL904 XXX	Tape and Reel	–40° to +85°C	QFN-32L	NiPdAu

Pin Configuration



32-Pin QFN (5mm × 5mm)

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
18, 19 22, 23	OUTB, /OUTB OUTA, /OUTA	O	Various	Clock outputs. Can be programmed to one of the following logic types:(1) LVPECL, LVDS, HCSL, or LVCMOS.
26, 27	REFIN, /REFIN	I	Various	Reference clock input. Can be programmed to either differential or single-ended use.
20 16	OE_A OE_B	I	CMOS	Output Enable, Outputs disable to tri-state, 0 = Disabled, 1 = Enabled, on-chip 75kΩ pull-up
1, 2, 5, 8, 25	VDD	PWR		Core power supply.
28	VDDI	PWR		Input circuit power supply, +3.3V only.
24	VDDA	PWR		Analog circuit power supply.
21 17	VDDOA VDDOB	PWR		Output buffers power supply.
EPAD	VSS	PWR		Power supply ground and thermal relief.(2)
11	GND	I		This pin is not power supply ground, but must be tied to VSS for proper operation.
3, 4, 6, 7, 9, 10, 12, 13, 14, 15, 29, 30, 31, 32	DNC			Internally connected. Do not connect anything to these pins.

Note:

1. In case of LVCMOS, only the true output pin is enabled. The complementary output pin is disabled to a high impedance.
2. Exposed package pad is electrically active and must be connected to ground.

Functional Description

The PL904xxx series is a very flexible, advanced programmable jitter filter design for high performance, small form-factor applications. The PL904xxx accepts a reference clock input between 12MHz and 250MHz that can be either differential or single-ended. The PL904xxx is capable of producing up to 2 differential outputs up to 850MHz. The most common configuration will be with the same input and output frequency, but this flexible design also allows frequency translation from one frequency to another frequency, as long as both frequencies are within the specified ranges for input and output.

Jitter Attenuation

Typically, the jitter attenuation settings will be optimized for one particular input and output frequency.

The PL904xxx excels at attenuating deterministic jitter that presents itself as spurs in the phase noise plot above 1MHz.

Output Logic Programming

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS.

Each output can be programmed individually to one of the four logic types.

All logic types are differential, except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled and the complementary channel is disabled. With LVCMOS, there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength.

Unused outputs are disabled to high impedance.

Input Selection

The reference input for the device can be programmed to be either differential or single ended and requires only a small amplitude. See Figure 1 and Figure 2.

The single-ended signal can be LVCMOS and the differential signal can be any of the differential logic types. For the differential logic types, it is important to use the appropriate termination for the logic type.

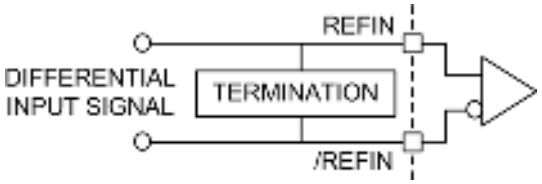


Figure 1. Differential Input Signal

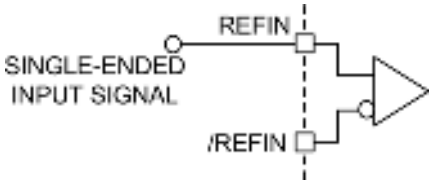


Figure 2. Single-Ended Input Signal

Absolute Maximum Ratings[3]

Supply Voltage (V_{DD}, V_{DDI}, V_{DDA}, $V_{DDOA/B}$).....+4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{DD} + 0.5V
Lead Temperature (soldering, 20s).....260°C
Case Temperature .....115°C
Storage Temperature (Ts).....–65°C to +150°C

Operating Ratings[4]

Supply Voltage
(V_{DD}, V_{DDA}, $V_{DDOA/B}$, V_{DDI})..... +2.375V to +3.465V
Ambient Temperature (T_A) .....–40°C to +85°C
Junction Thermal Resistance[5]
(θ_{JA}), Still-Air .....34°C/W

DC Electrical Characteristics[6]

V_{DD}, V_{DDA}, $V_{DDOA/B}$, V_{DDI} = 2.375V ~ 3.465V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD} V_{DDA} $V_{DDOA/B}$	Power supply voltage		2.375		3.465	V
V_{DDI}	Power supply voltage		3.135		3.465	V
I_{DD}	Total supply current, V_{DD} + V_{DDO}	2 × LVPECL, 156.25MHz Outputs open			220	mA
		2 × HCSL (PCIe), 100MHz Outputs terminated with 50Ω to V_{SS}			230	mA
		2 × LVCMOS, 125MHz Outputs open			210	mA

REFIN DC Electrical Characteristics[6]

V_{DDI} = 3.135V ~ 3.465V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CMR}	Input common mode voltage		0.3		V_{DDI} – 0.3	V
V_{SWING}	Input voltage swing	Peak to peak. Each side of the differential input.	0.2		V_{DDI}	V_{PP}

Notes:

3. Exceeding the absolute maximum ratings may damage the device.
4. The device is not guaranteed to function outside its operating ratings.
5. Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
6. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

LVDS Output DC Electrical Characteristics[6]

$V_{DDOA/B}$ = 2.375V ~ 3.465V, T_A = –40°C to +85°C, R_L = 100Ω across Q and /Q.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OD}	Differential output voltage		245	350	454	mV
V_{CM}	Common mode voltage		1.125	1.2	1.375	V
V_{OH}	Output high voltage		1.248	1.375	1.602	V
V_{OL}	Output low voltage		0.898	1.025	1.252	V

HCSL Output DC Electrical Characteristics[6]

$V_{DDOA/B}$ = 2.375V ~ 3.465V, T_A = –40°C to +85°C, R_L = 50Ω to V_{SS}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage		660	700	850	mV
V_{OL}	Output low voltage		–150	0	27	mV
V_{CROSS}	Crossing point voltage			350		mV

LVPECL Output DC Electrical Characteristics[6]

$V_{DDOA/B}$ = 2.375V ~ 3.465V, T_A = –40°C to +85°C, R_L = 50Ω to V_{DD} – 2V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage		V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.80	V
V_{OL}	Output low voltage		V_{DDO} – 2.00	V_{DDO} – 1.78	V_{DDO} – 1.60	V
V_{SWING}	Output voltage swing		0.65	0.77	0.95	V

LVCMOS Output DC Electrical Characteristics[6]

$V_{DDOA/B}$ = 2.375V ~ 3.465V, T_A = –40°C to +85°C, R_L = 50Ω to $V_{DD}/2$

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output high voltage		V_{DD} – 0.8			V
V_{OL}	Output low voltage				0.5	V

OE (LVCMOS) Input DC Electrical Characteristics[6]

V_{DD}, V_{DDA}, $V_{DDOA/B}$ = 2.375V ~ 3.465V; V_{DDI} = 3.135V ~ 3.465V, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage		V_{DD} – 0.7		V_{DD} + 0.3	V
V_{IL}	Input low voltage		V_{SS} – 0.3		0.3 × V_{DD}	V
I_{IH}	Input high current	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input low current	V_{DD} = 3.465V, V_{IN} = 0V	–150			µA

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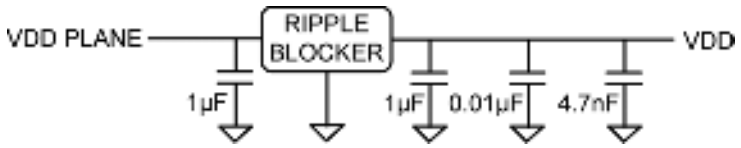
AC Electrical Characteristics

V_{DD}, V_{DDA}, $V_{DDOA/B}$, V_{DDI} = 2.375V ~ 3.465V; T_A = –40°C to +85°C.

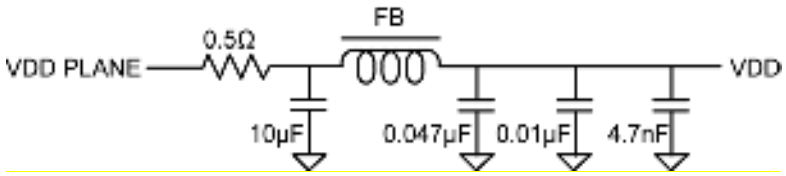
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
F_{IN}	Input frequency		12		250	MHz
F_{OUT}	Output frequency	LVPECL, LVDS, HCSL	12		850	MHz
		LVCMOS	12		250	MHz
T_R/T_F	Output rise/fall time See Figure 4	LVPECL output	85	135	350	ps
		LVDS output	85	140	300	ps
		HCSL output	175	340	700	ps
		LVCMOS output (default drive)	100	200	400	ps
ODC	Output duty cycle See Figure 3	All output frequencies	45	50	55	%
		<350MHz output frequencies	48	50	52	%
T_{LOCK}	PLL lock time			5	20	ms

Power Supply Filtering Recommendations

Preferred filter, using Micrel's MIC94300 or MIC94310 Ripple Blocker™:



Alternative, traditional filter, using a ferrite bead:



VDDO and VDD pins can be connected directly to the VDD power plane. For VDDA and VDDI it is recommended to use a power supply filter as described above.

Application Information

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF above) between the VDD and VSS pins, as close as possible to those pins and on the same side of the PCB as the IC. The shorter the physical path from VDD to the capacitor and back from the capacitor to VSS, the more effective the decoupling. Use one 4.7nF capacitor for each VDD pin on the PL904xxx.

The impedance value of the ferrite bead (FB) needs to be between 240Ω and 600Ω with a saturation current ≥150mA.

VDDO pins connect directly to the VDD plane. All VDD pins on the PL904xxx connect to VDD after the power supply filter.

A Ripple Blocker has advantages over using a ferrite bead. A Ripple Blocker filters much lower frequencies than a ferrite bead, at least two decades lower. Most ferrite beads cause peaking in the noise filter frequency response, so some noise frequencies are actually made worse. The Ripple Blocker is designed to not have any noise peaking.

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30Ω resistor in series with the output, as close as possible to the output pin, and start a 50Ω trace on the other side of the resistor.

For differential traces, you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

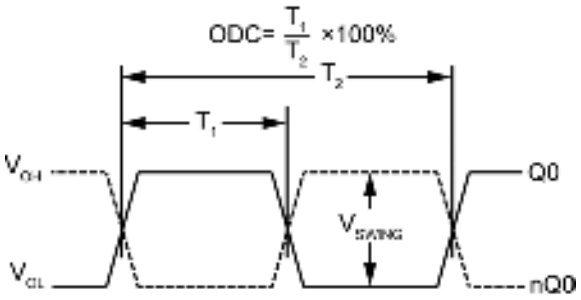


Figure 3. Duty Cycle Timing

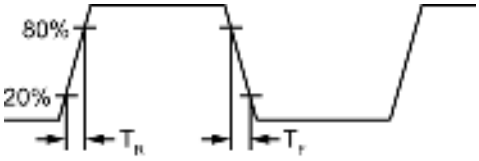


Figure 4. All Outputs Rise/Fall Time

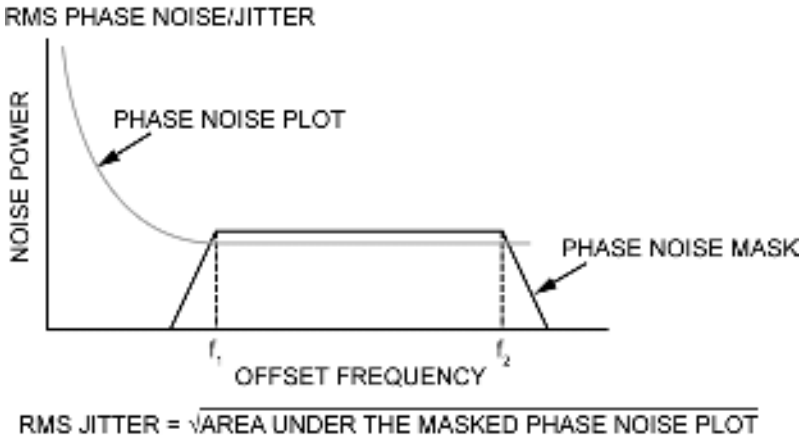


Figure 5. RMS Phase Noise Jitter

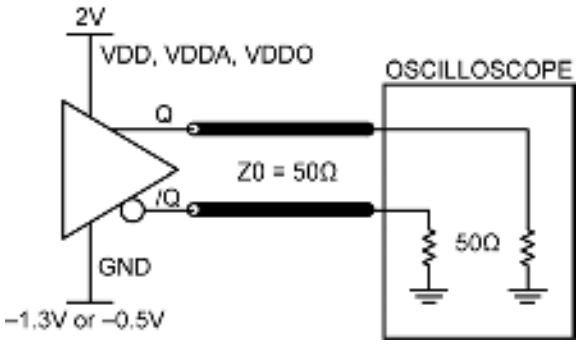


Figure 6. LVPECL Output Load and Test Circuit

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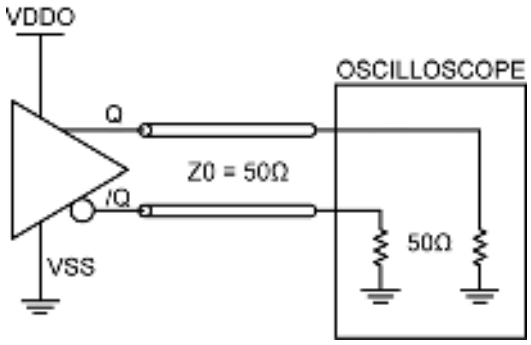


Figure 7. HCSL Output Load and Test Circuit

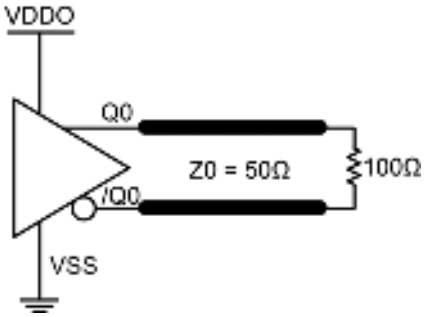


Figure 8. LVDS Output Load and Test Circuit

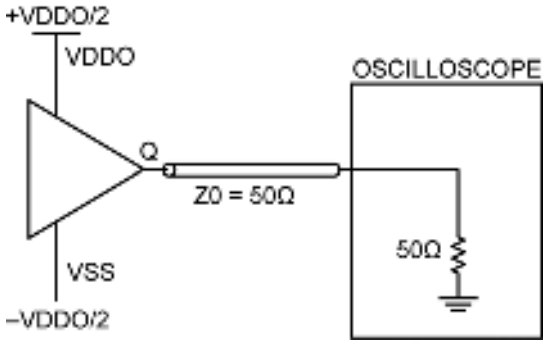
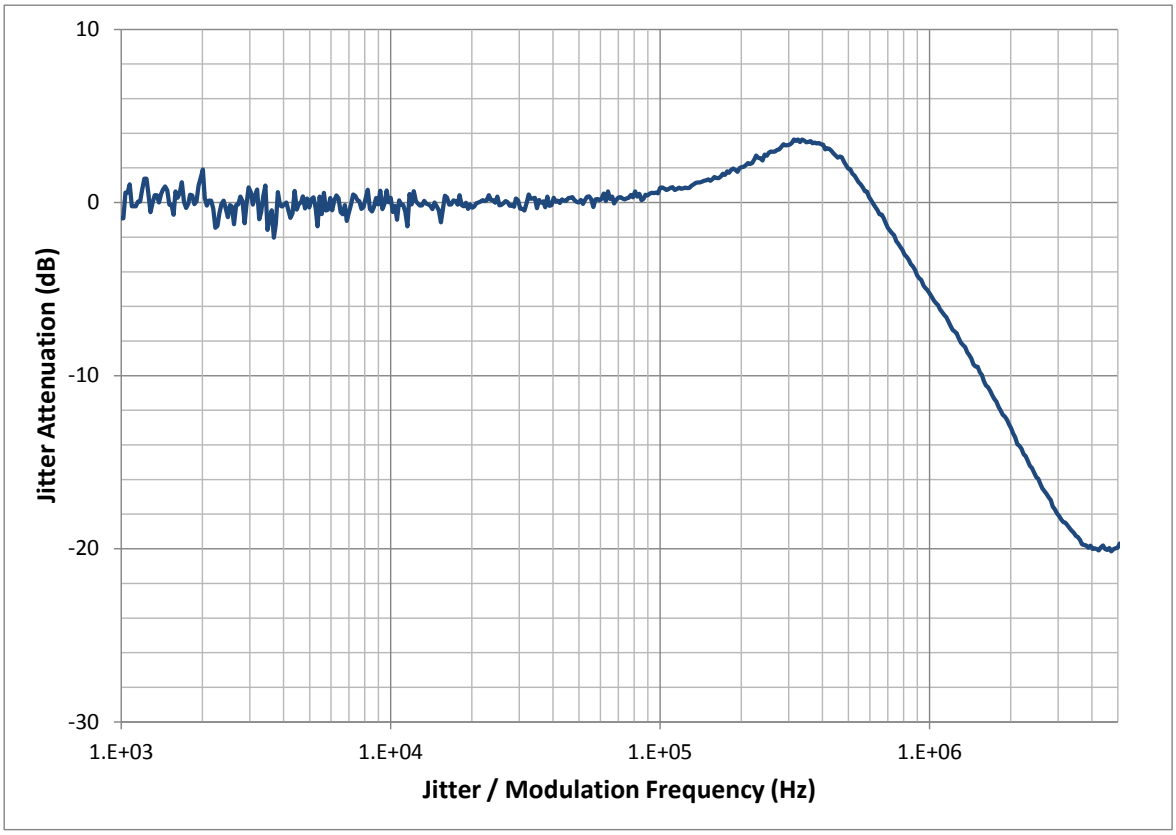


Figure 9. LVCMOS Output Load and Test Circuit

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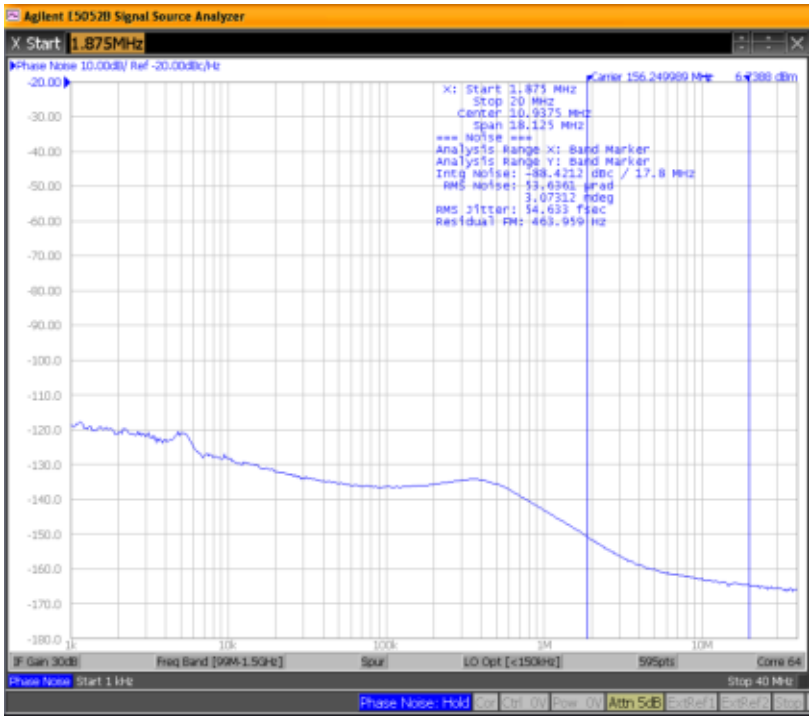
Jitter Attenuation Performance

The jitter attenuating frequency response was measured at 156.25MHz.

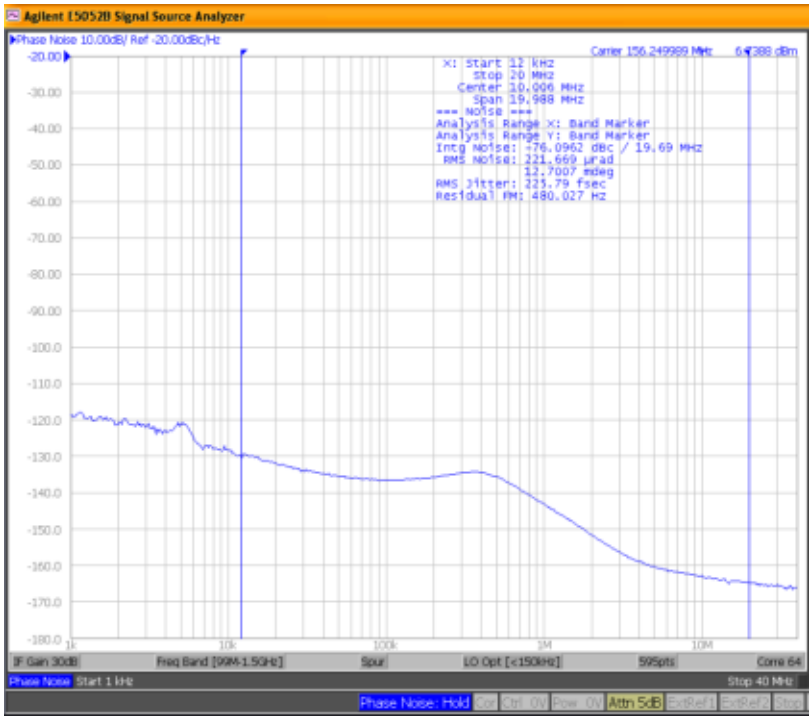


The jitter attenuation works like a low-pass filter for frequency modulated signals or noise. The bandwidth for this low-pass filter is 500kHz with a 12dB/octave slope above 500kHz. At about 5MHz the noise floor of this measurement is reached but in reality, the attenuation continues with the 12dB/octave slope.

Phase noise performance with a clean input clock.

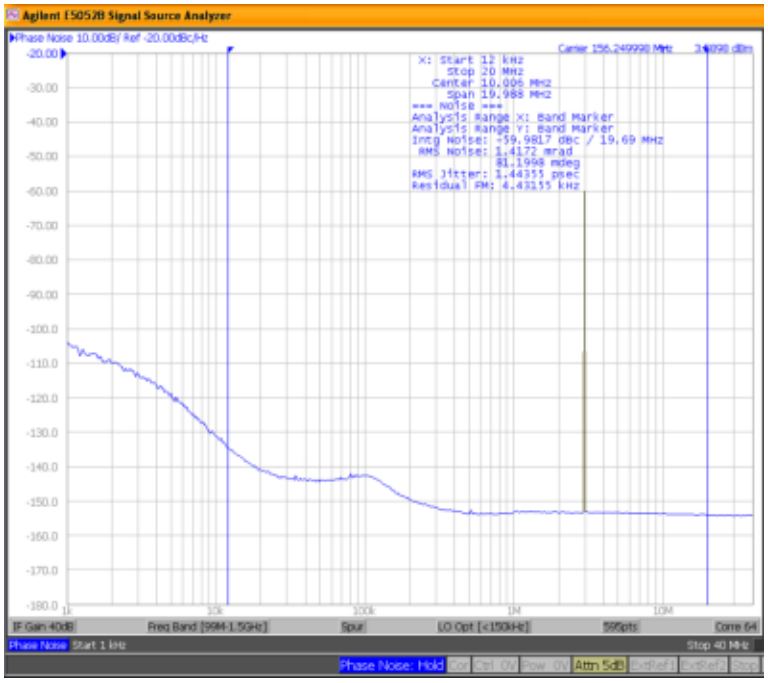


156.25MHz with 55fs$_{RMS}$ of phase jitter for 1.875MHz to 20MHz integration range



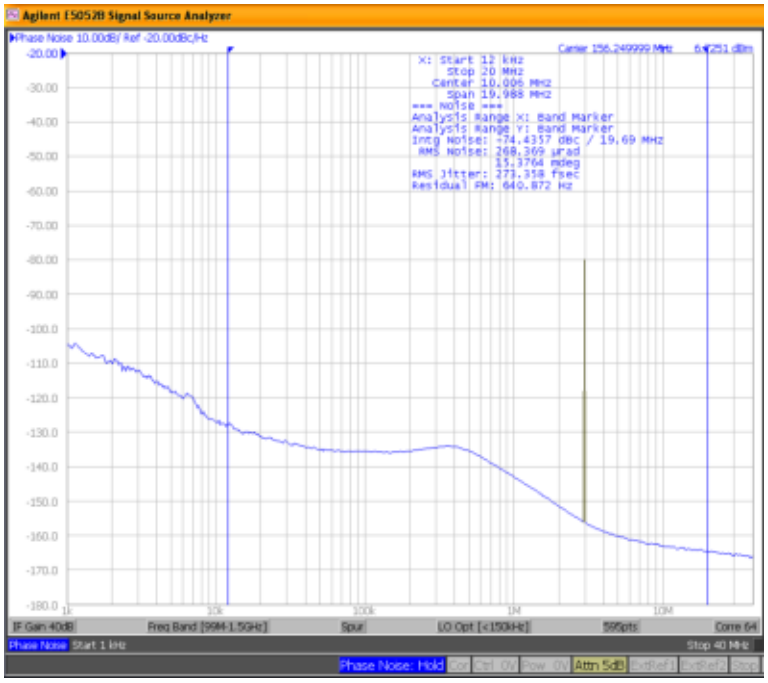
156.25MHz with 226fs$_{RMS}$ of phase jitter for 12kHz to 20MHz integration range

Example 156.25MHz input test clock with bad phase jitter cause by a 3MHz spur.



156.25MHz with 1.4ps$_{RMS}$ of phase jitter for 12kHz to 20MHz integration range

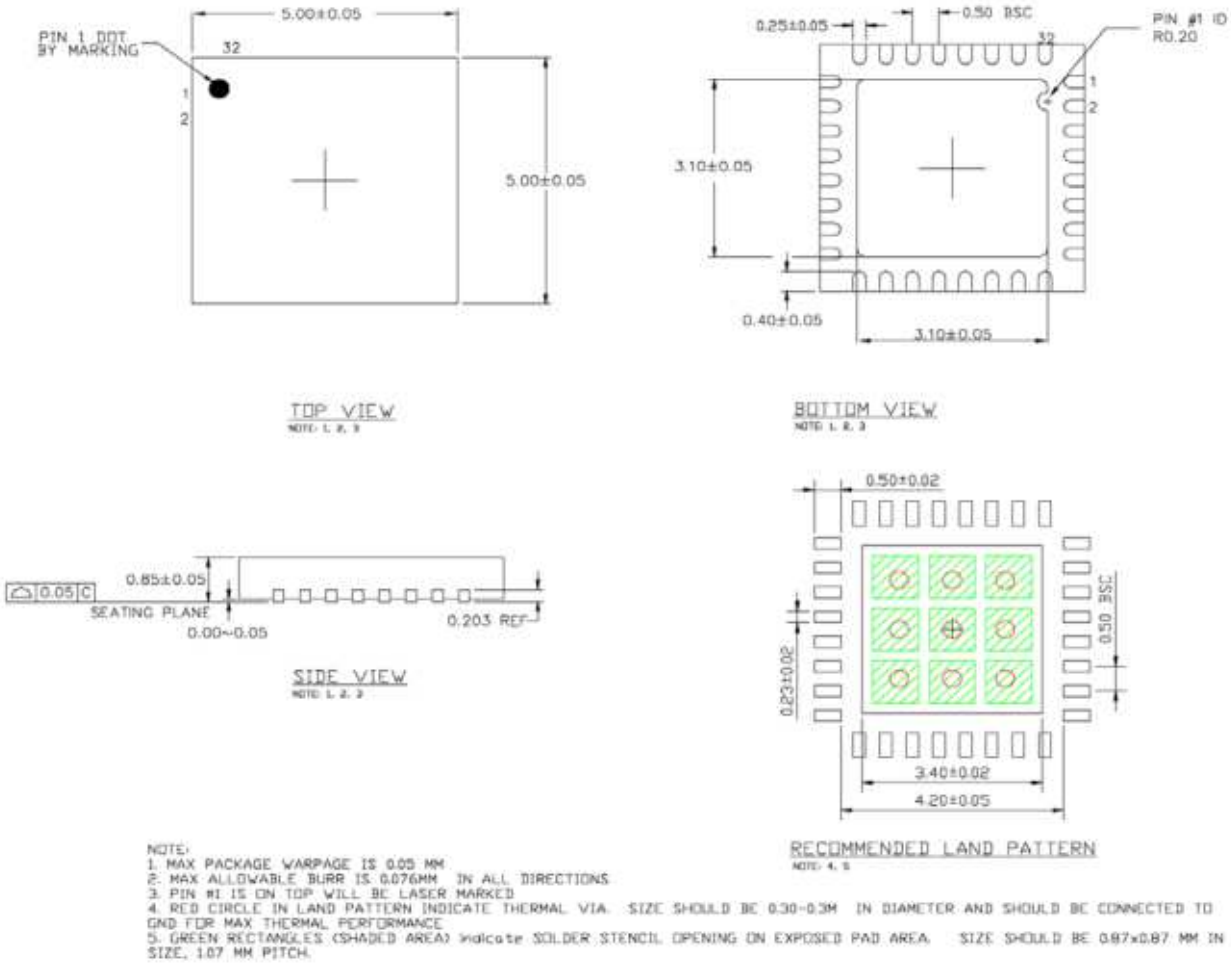
Output clock from PL904xxx.



156.25MHz with 273fs$_{RMS}$ of phase jitter for 12kHz to 20MHz integration range

The 3MHz spur is attenuated by 20dB, resulting in a phase jitter reduction from 1.4ps to 0.27ps.

Package Information and Recommended Landing Pattern[7]



32-Pin QFN

Note:

7. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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