**Important notice**

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

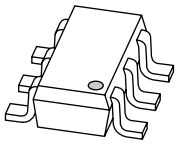
Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia



# PMD3001D

## MOSFET driver

Rev. 02 — 28 August 2009 Product data sheet

## 1. Product profile

### 1.1 General description

NPN/PNP transistor pair connected as push-pull driver in a SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package.

### 1.2 Features

- Low $V_{CEsat}$ Breakthrough In Small Signal (BISS) transistors in push-pull configuration
- Application-optimized pinout
- Space-saving solution
- Internal connections to minimize layout effort
- Reduces component count

### 1.3 Applications

- MOSFET driver
- Power bipolar transistor driver
- Output current booster for operational amplifier

### 1.4 Quick reference data

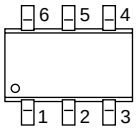
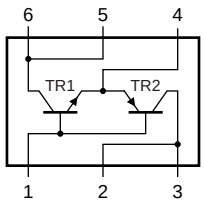
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| $V_{CEO}$ | collector-emitter voltage | open base | - | - | 40 | V |
| $I_C$ | collector current | | - | - | 1 | A |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | - | - | 2 | A |

NXP founded by Philips

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | base TR1, TR2 |  |  |
| 2 | collector TR2 | | |
| 3 | collector TR2 | | |
| 4 | emitter TR1, TR2 | | |
| 5 | collector TR1 | | |
| 6 | collector TR1 | | |



## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PMD3001D | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

## 4. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PMD3001D | 9F |



© NXP B.V. 2009. All rights reserved.

## 5. Limiting values

**Table 5. Limiting values**

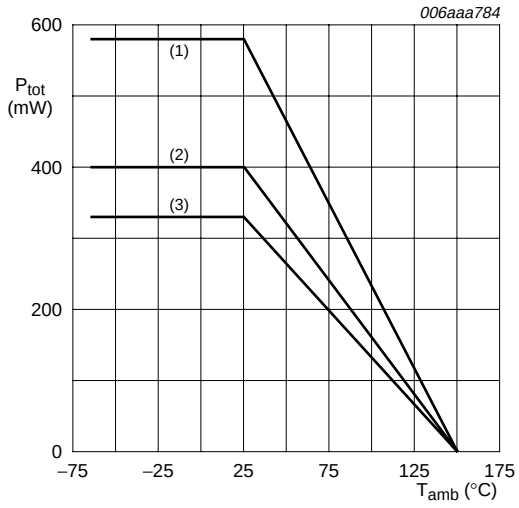
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Per transistor; for the PNP transistor with negative polarity** | | | | | | |
| $V_{CBO}$ | collector-base voltage | open emitter | | - | 40 | V |
| $V_{CEO}$ | collector-emitter voltage | open base | | - | 40 | V |
| $I_C$ | collector current | | | - | 1 | A |
| $I_{CM}$ | peak collector current | single pulse; $t_p \leq 1$ ms | | - | 2 | A |
| $I_{BM}$ | peak base current | | | - | 0.3 | A |
| | | single pulse; $t_p \leq 1$ ms | | - | 1 | A |
| **Per device** | | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb} \leq 25$ °C | [1] | - | 330 | mW |
| | | | [2] | - | 400 | mW |
| | | | [3] | - | 580 | mW |
| $T_j$ | junction temperature | | | - | 150 | °C |
| $T_{amb}$ | ambient temperature | | | –65 | +150 | °C |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm$^2$.

[3] Device mounted on a ceramic PCB, $Al_2O_3$, standard footprint.




(1) Ceramic PCB, $Al_2O_3$, standard footprint

(2) FR4 PCB, mounting pad for collector 1cm$^2$

(3) FR4 PCB, standard footprint

**Fig 1. Power derating curves**



© NXP B.V. 2009. All rights reserved.

## 6. Thermal characteristics

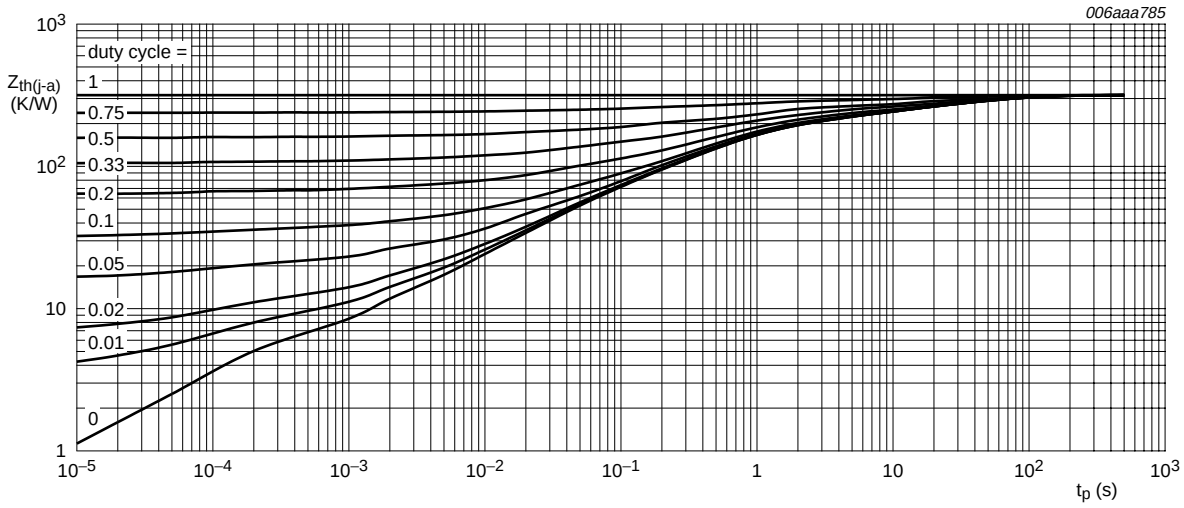
**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | - | 380 | K/W |
| | | | [2] | - | - | 315 | K/W |
| | | | [3] | - | - | 215 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1cm$^2$.

[3] Device mounted on a ceramic PCB, $Al_2O_3$, standard footprint.

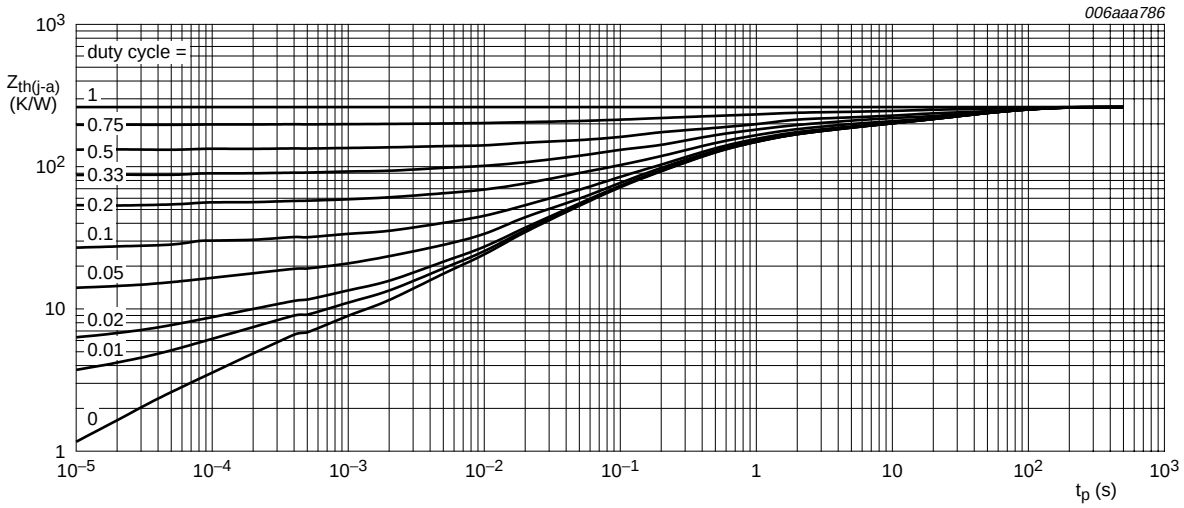



FR4 PCB, standard footprint

**Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

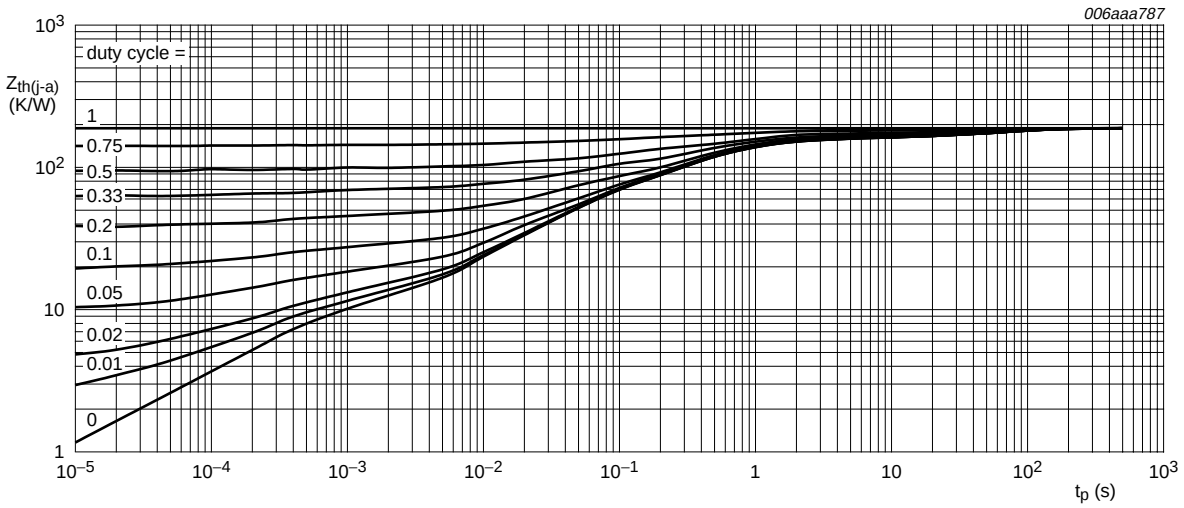


© NXP B.V. 2009. All rights reserved.




FR4 PCB, mounting pad for collector 1cm$^2$

**Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**




Ceramic PCB, $Al_2O_3$, standard footprint

**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



© NXP B.V. 2009. All rights reserved.

# 7. Characteristics

**Table 7. Characteristics**

*$T_{amb}$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Per NPN transistor** | | | | | | | |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = 40 V; $I_E$ = 0 A | | - | - | 100 | nA |
| | | $V_{CB}$ = 40 V; $I_E$ = 0 A; $T_j$ = 150 °C | | - | - | 50 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = 5 V; $I_C$ = 1 mA | | 300 | 450 | - | |
| | | $V_{CE}$ = 5 V; $I_C$ = 200 mA | | 300 | 450 | 830 | |
| | | $V_{CE}$ = 5 V; $I_C$ = 500 mA | [1] | 300 | 400 | - | |
| | | $V_{CE}$ = 5 V; $I_C$ = 1 A | [1] | 200 | 340 | - | |
| | | $V_{CE}$ = 5 V; $I_C$ = 2 A | [1] | 75 | 120 | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = 100 mA; $I_B$ = 5 mA | | - | 30 | 80 | mV |
| | | $I_C$ = 500 mA; $I_B$ = 50 mA | [1] | - | 100 | 120 | mV |
| | | $I_C$ = 1 A; $I_B$ = 100 mA | [1] | - | 180 | 230 | mV |
| | | $I_C$ = 2 A; $I_B$ = 200 mA | [1] | - | 360 | 440 | mV |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = 100 mA; $I_B$ = 5 mA | | - | 0.75 | 0.9 | V |
| | | $I_C$ = 500 mA; $I_B$ = 50 mA | [1] | - | 0.9 | 1.1 | V |
| | | $I_C$ = 1 A; $I_B$ = 100 mA | [1] | - | 1 | 1.2 | V |
| | | $I_C$ = 2 A; $I_B$ = 200 mA | [1] | - | 1.1 | 1.3 | V |
| $V_{BE}$ | base-emitter voltage | $V_{CE}$ = 5 V; $I_C$ = 1 A | | 700 | 800 | 1100 | mV |
| **Per PNP transistor** | | | | | | | |
| $I_{CBO}$ | collector-base cut-off current | $V_{CB}$ = –40 V; $I_E$ = 0 A | | - | - | –100 | nA |
| | | $V_{CB}$ = –40 V; $I_E$ = 0 A; $T_j$ = 150 °C | | - | - | –50 | µA |
| $h_{FE}$ | DC current gain | $V_{CE}$ = –5 V; $I_C$ = –1 mA | | 300 | 450 | - | |
| | | $V_{CE}$ = –5 V; $I_C$ = –200 mA | | 250 | 390 | 640 | |
| | | $V_{CE}$ = –5 V; $I_C$ = –500 mA | [1] | 215 | 290 | - | |
| | | $V_{CE}$ = –5 V; $I_C$ = –1 A | [1] | 150 | 200 | - | |
| | | $V_{CE}$ = –5 V; $I_C$ = –2 A | [1] | 50 | 85 | - | |
| $V_{CEsat}$ | collector-emitter saturation voltage | $I_C$ = –100 mA; $I_B$ = –5 mA | | - | –40 | –140 | mV |
| | | $I_C$ = –500 mA; $I_B$ = –50 mA | [1] | - | –110 | –170 | mV |
| | | $I_C$ = –1 A; $I_B$ = –100 mA | [1] | - | –200 | –310 | mV |
| | | $I_C$ = –2 A; $I_B$ = –200 mA | [1] | - | –400 | –500 | mV |
| $V_{BEsat}$ | base-emitter saturation voltage | $I_C$ = –100 mA; $I_B$ = –5 mA | | - | –0.75 | –0.9 | V |
| | | $I_C$ = –500 mA; $I_B$ = –50 mA | [1] | - | –0.88 | –1.1 | V |
| | | $I_C$ = –1 A; $I_B$ = –100 mA | [1] | - | –0.95 | –1.2 | V |
| | | $I_C$ = –2 A; $I_B$ = –200 mA | [1] | - | –1.1 | –1.3 | V |
| $V_{BE}$ | base-emitter voltage | $V_{CE}$ = –5 V; $I_C$ = –1 A | | –700 | –800 | –1100 | mV |



© NXP B.V. 2009. All rights reserved.

**Table 7. Characteristics** *...continued*

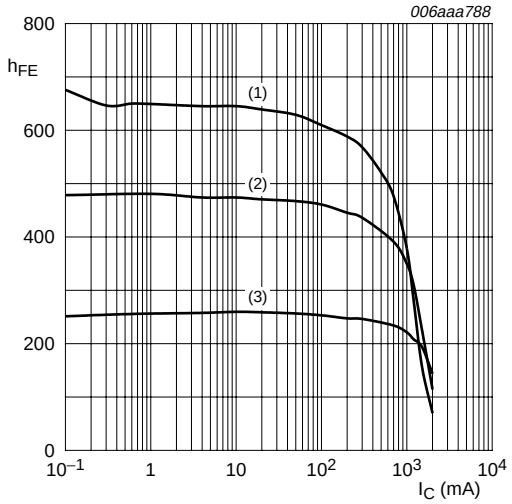
*$T_{amb}$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Per device** | | | | | | |
| $t_d$ | delay time | $I_C$ = 0.5 A; $V_I$ = 8 V | - | 3 | - | ns |
| $t_r$ | rise time | | - | 17 | - | ns |
| $t_{on}$ | turn-on time | | - | 20 | - | ns |
| $t_s$ | storage time | | - | 3 | - | ns |
| $t_f$ | fall time | | - | 6 | - | ns |
| $t_{off}$ | turn-off time | | - | 9 | - | ns |

[1] Pulse test: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$



© NXP B.V. 2009. All rights reserved.



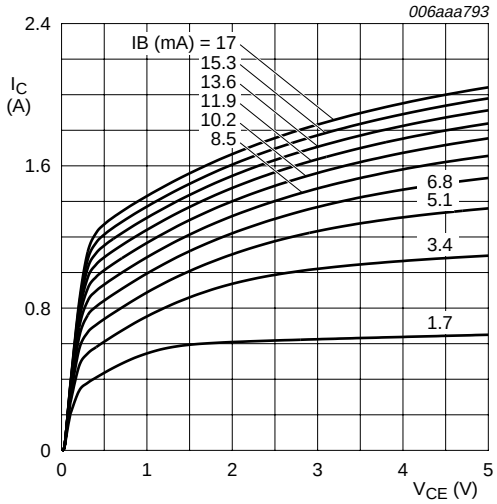

$V_{CE}$ = 5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

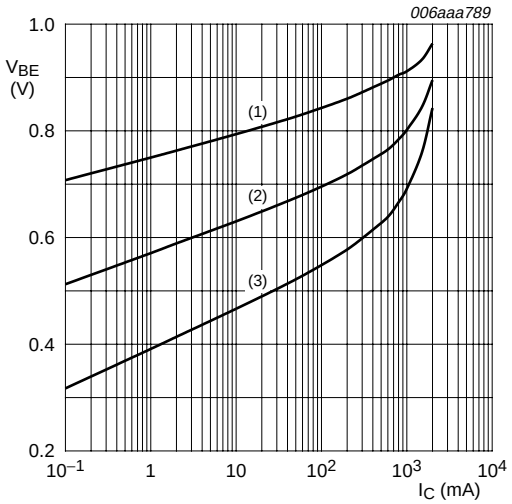
(3) $T_{amb}$ = –55 °C

**Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 6. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values**



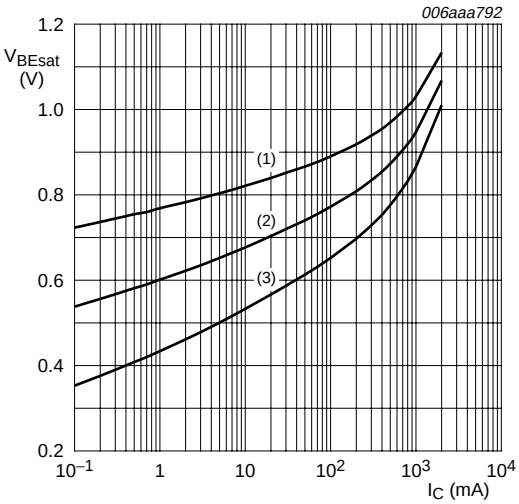

$V_{CE}$ = 5 V

(1) $T_{amb}$ = –55 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 7. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values**




$I_C/I_B$ = 20

(1) $T_{amb}$ = –55 °C

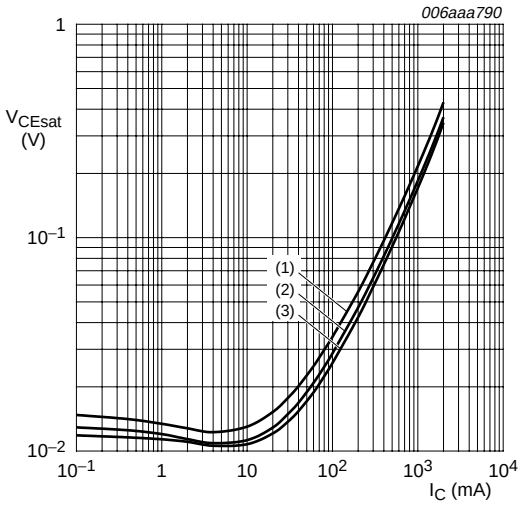
(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 8. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values**



© NXP B.V. 2009. All rights reserved.



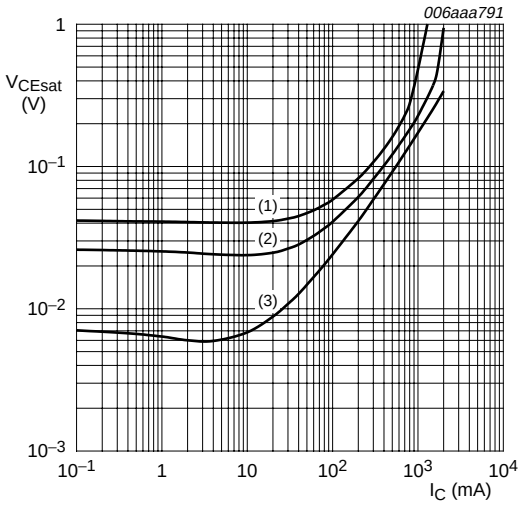

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**




$T_{amb}$ = 25 °C

(1) $I_C/I_B$ = 100

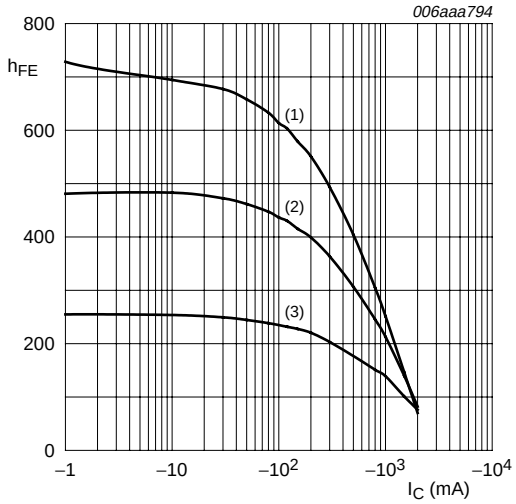
(2) $I_C/I_B$ = 50

(3) $I_C/I_B$ = 10

**Fig 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



© NXP B.V. 2009. All rights reserved.



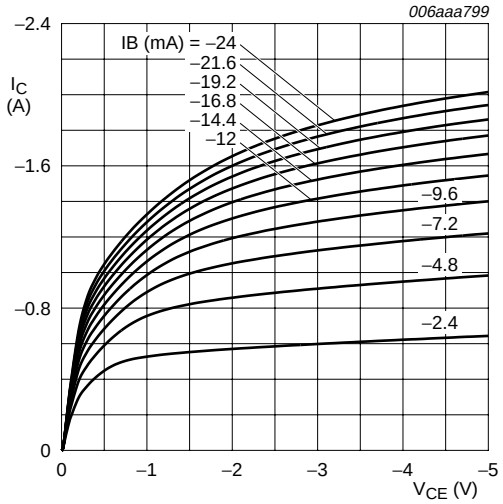

$V_{CE}$ = −5 V

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

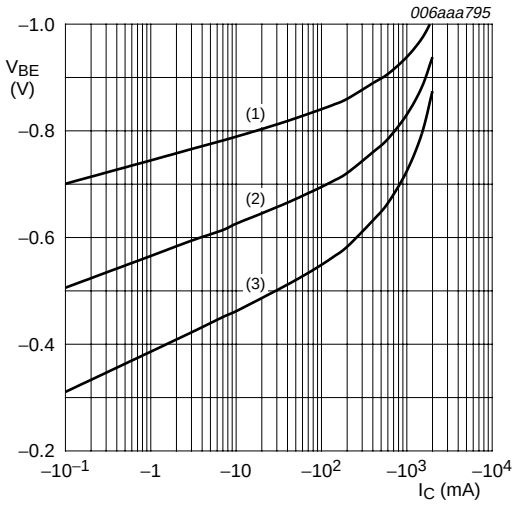
(3) $T_{amb}$ = −55 °C

**Fig 11. TR2 (PNP): DC current gain as a function of collector current; typical values**




$T_{amb}$ = 25 °C

**Fig 12. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values**



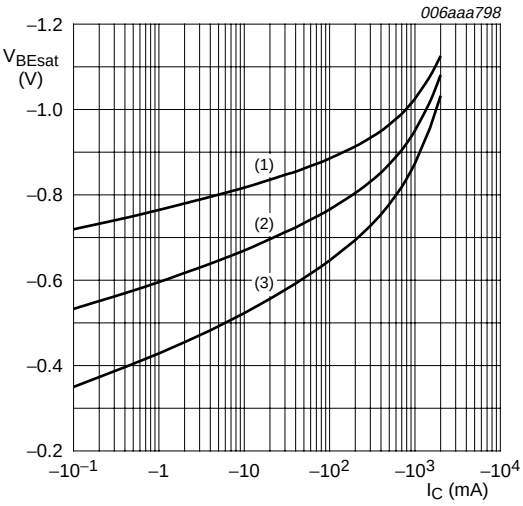

$V_{CE}$ = −5 V

(1) $T_{amb}$ = −55 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 13. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values**




$I_C/I_B$ = 20

(1) $T_{amb}$ = −55 °C

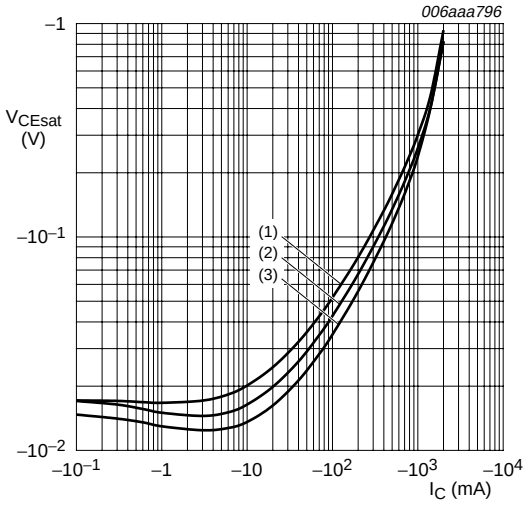
(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = 100 °C

**Fig 14. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values**



© NXP B.V. 2009. All rights reserved.



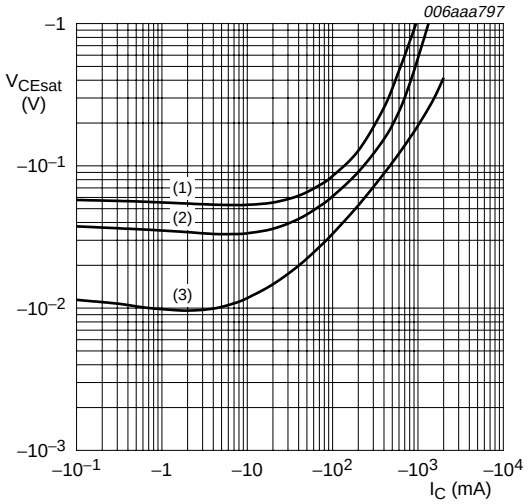

$I_C/I_B$ = 20

(1) $T_{amb}$ = 100 °C

(2) $T_{amb}$ = 25 °C

(3) $T_{amb}$ = −55 °C

**Fig 15. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**




$T_{amb}$ = 25 °C

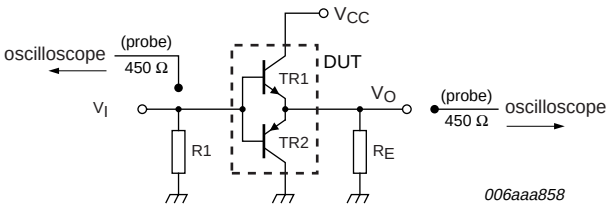
(1) $I_C/I_B$ = 100

(2) $I_C/I_B$ = 50

(3) $I_C/I_B$ = 10

**Fig 16. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**

## 8. Test information




$I_C$ = 0.5 A; $V_I$ = 8 V; R1 = 56 Ω; $R_E$ = 15 Ω

**Fig 17. Test circuit for switching times**



© NXP B.V. 2009. All rights reserved.

## 9. Package outline

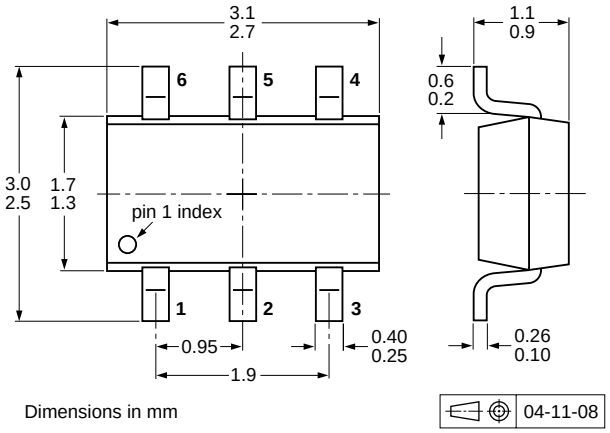



**Fig 18. Package outline SOT457 (SC-74)**

## 10. Packing information

**Table 8. Packing methods**

*The indicated -xxx are the last three digits of the 12NC ordering code.*[1]

| Type number | Package | Description | | Packing quantity | |
|---|---|---|---|---|---|
| | | | | 3000 | 10000 |
| PMD3001D | SOT457 | 4 mm pitch, 8 mm tape and reel; T1 | [2] | -115 | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 | [3] | -125 | -165 |

[1] For further information and the availability of packing methods, see Section 14.

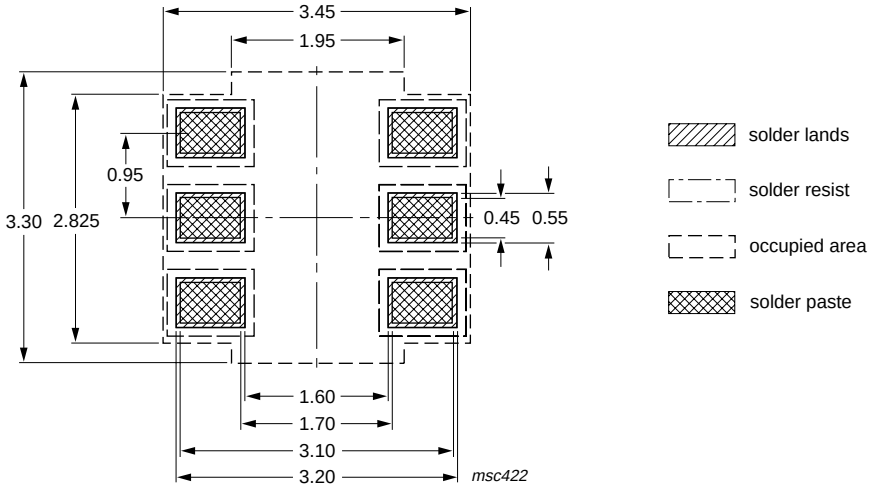
[2] T1: normal taping

[3] T2: reverse taping



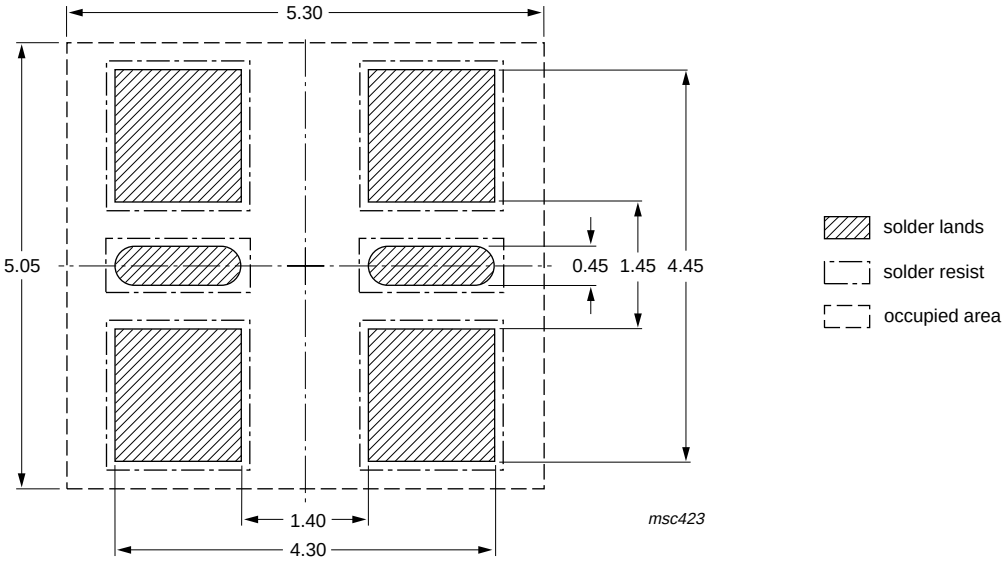
© NXP B.V. 2009. All rights reserved.

## 11. Soldering




Dimensions in mm

**Fig 19. Reflow soldering footprint SOT457 (SC-74)**




Dimensions in mm

**Fig 20. Wave soldering footprint SOT457 (SC-74)**



© NXP B.V. 2009. All rights reserved.

## 12. Revision history

**Table 9. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PMD3001D_2 | 20090828 | Product data sheet | - | PMD3001D_1 |
| Modifications: | • This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.<br>• Figure 20 “Wave soldering footprint SOT457 (SC-74)”: updated | | | |
| PMD3001D_1 | 20060926 | Product data sheet | - | - |


© NXP B.V. 2009. All rights reserved.

# 13. Legal information

## 13.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 13.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 13.3 Disclaimers

**General —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data —** The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

## 13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# 14. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**



© NXP B.V. 2009. All rights reserved.

## 15. Contents


| | | |
|---|---|---|
| **1** | **Product profile** | **1** |
| 1.1 | General description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| **2** | **Pinning information** | **2** |
| **3** | **Ordering information** | **2** |
| **4** | **Marking** | **2** |
| **5** | **Limiting values** | **3** |
| **6** | **Thermal characteristics** | **4** |
| **7** | **Characteristics** | **6** |
| **8** | **Test information** | **11** |
| **9** | **Package outline** | **12** |
| **10** | **Packing information** | **12** |
| **11** | **Soldering** | **13** |
| **12** | **Revision history** | **14** |
| **13** | **Legal information** | **15** |
| 13.1 | Data sheet status | 15 |
| 13.2 | Definitions | 15 |
| 13.3 | Disclaimers | 15 |
| 13.4 | Trademarks | 15 |
| **14** | **Contact information** | **15** |
| **15** | **Contents** | **16** |


Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

**© NXP B.V. 2009.** **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 28 August 2009**
**Document identifier: PMD3001D_2**

founded by

PHILIPS