PRM™ Regulator

PRM48AH480x200A00



High Efficiency Converter

Features

- 48.0 V input (36.0 V to 75.0 V), non-isolated ZVS buck-boost regulator
- 20.0 V to 55.0 V adjustable output range
- 200 W output power in 0.57 in^2 footprint
- 96.7% typical efficiency, at full load
- 1341 W/in^3 (82 W/cm^3) Power Density
- 5.29 MHrs MTBF (MIL-HDBK-217 Plus Parts Count)
- Pin selectable operating mode
  - Adaptive Loop
  - Remote Sense / Child Operation
- Half VI Chip® Package
  - 22.0mm x 16.5mm x 6.73mm

Typical Applications

- High Density Power Supply DC-DC rail outputs
- High Density ATE system DC-DC power
- Telecom NPU and ASIC core power
- Communications Systems
- Non-isolated and isolated power converters

Product Ratings	
V_{IN} = 36.0 V to 75.0 V	P_{OUT} = 200 W
V_{OUT} = 48.0 V (20.0 V to 55.0 V Trim)	I_{OUT} = 4.17 A

Product Description

The VI Chip® PRM™ Regulator is high efficiency converter, operating from a 36.0 to 75.0 Vdc input to generate a regulated 20.0 to 55.0 Vdc output. The ZVS buck-boost topology enables high switching frequency (~1.03 MHz) operation with high conversion efficiency. High switching frequency reduces the size of reactive components enabling power density up to 1341 W/in^3.

The Half VI Chip® package is compatible with standard pick-and-place and surface mount assembly processes with a planar thermal interface area and superior thermal conductivity.

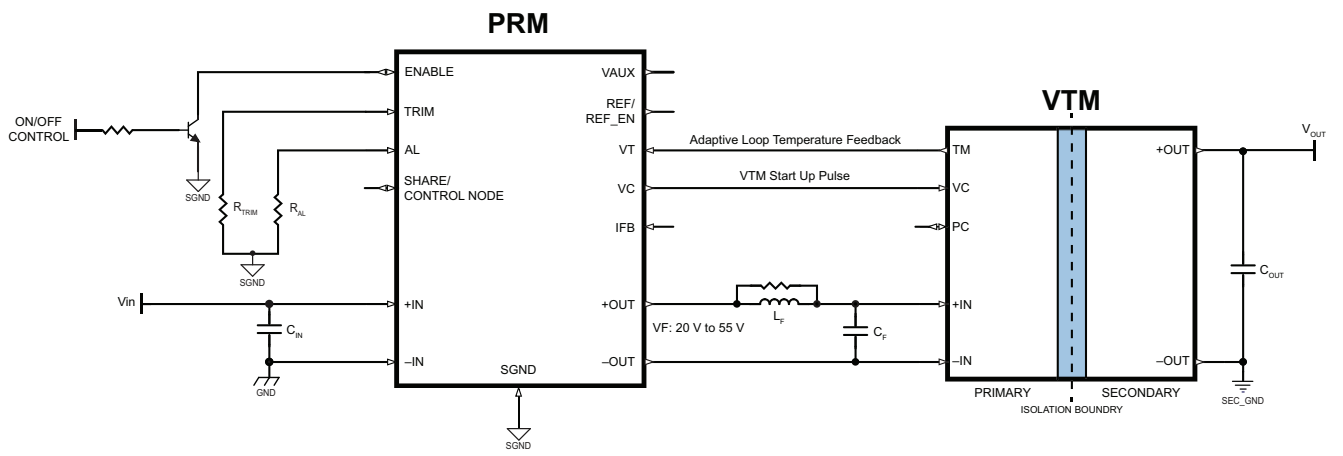
In a Factorized Power Architecture™ system, the PRM and downstream VTM™ current multiplier minimize distribution and conversion losses in a high power solution, providing an isolated, regulated output voltage.

The PRM48AH480**x**200A00 has two selectable modes of regulation depending on the application requirements.

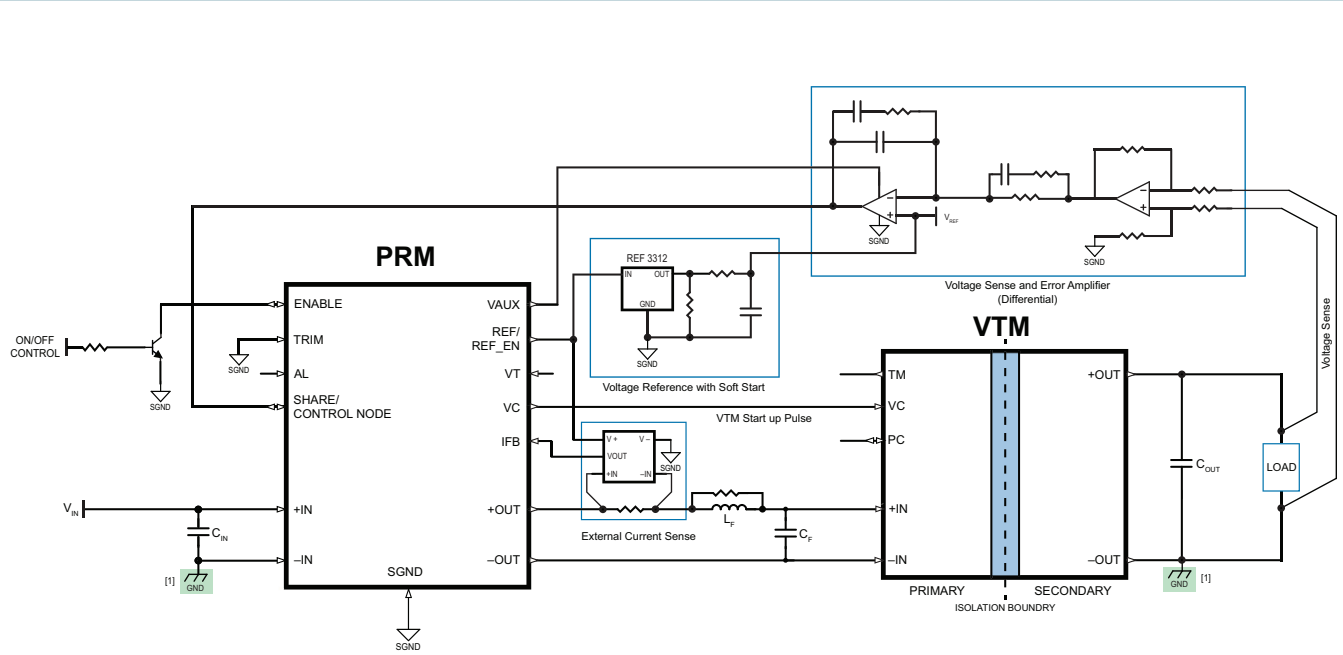
In Adaptive Loop Operation, the PRM48AH480**x**200A00 utilizes a unique feed-forward scheme that enables precise regulation of an isolated POL voltage without the need for remote sensing and voltage feedback.

In Remote Sense Operation, the internal regulation circuitry is disabled, and an external control loop and current sensor maintain regulation. This affords flexibility in the design of both voltage and current compensation loops to optimize performance in the end application.

Typical Applications



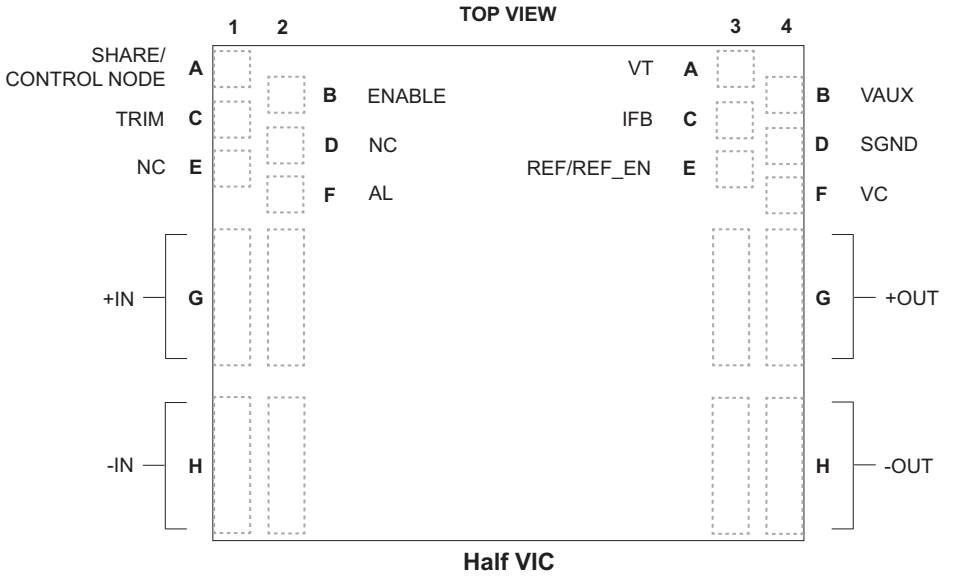
Typical Application: PRM48AH480x200A00 + VTM Adaptive Loop Configuration



Typical Application: PRM48AH480x200A00 + VTM, non-isolated Remote Sense Configuration

[1] Non-Isolated Configuration: –Out connected to -IN

Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
A1	SHARE (Adaptive Loop / Child Operation)	BIDIR	Parallel sharing control bus for parent-child configuration.
	CONTROL NODE (Remote Sense Operation)	INPUT	Modulator control node input. Driven by external error amplifier in Remote Sense Operation.
A3	VT (Adaptive Loop Operation)	INPUT	VTM TM input for temperature compensation. Leave disconnected for Remote Sense Operation.
B2	ENABLE	BIDIR	Enables power supply when allowed to float high. 5 V during normal operation.
B4	VAUX	OUTPUT	9 V auxiliary bias voltage.
C1	TRIM	INPUT	Selects operating mode. Adjusts output voltage in Adaptive Loop Operation.
C3	IFB (Remote Sense Operation)	INPUT	Current sense input for current limit and overcurrent protection in Remote Sense Operation. Leave disconnected for Adaptive Loop Operation.
D2	NC	n/a	Do not connect this pin.
D4	SGND	INPUT	Signal ground, reference for analog controls. Kelvin connected internally to –IN and –OUT.
E1	NC	n/a	Do not connect this pin.
E3	REF (Adaptive Loop Operation)	OUTPUT	Reference voltage for internal error amplifier in Adaptive Loop Operation.
	REF_EN (Remote Sense Operation)	OUTPUT	Powers and enables external control circuit voltage reference in Remote Sense Operation.
F2	AL (Adaptive Loop Operation)	INPUT	Adaptive loop gain control. Sets the magnitude of the Adaptive Loop load line in Adaptive Loop Operation. Leave disconnected for Remote Sense Operation.
F4	VC	OUTPUT	Bias voltage to power VTM module during start up
G1,G2	+IN	INPUT POWER	Positive input power terminal
G3,G4	+OUT	OUTPUT POWER	Positive output power terminal
H1,H2	-IN	INPUT POWER RETURN	Negative input power terminal. Connected internally to -OUT.
H3,H4	-OUT	OUTPUT POWER RETURN	Negative output power terminal. Connected internally to -IN.

Part Ordering Information

Device	Input Voltage Range	Package Type	Output Voltage x 10	Temperature Grade	Output Power	Revision	Version
PRM	48A	H	480	T	200	A	00
PRM = PRM	48A = 36.0 V - 75.0 V	H = Half VIC SMD	480 = 48.0 V	T = -40 to 125°C M = -55 to 125°C	200 = 200 W	A	00 = AL / RS

Standard Models

Part Number	V_{IN}	Package Type	V_{OUT}	Temperature	Power	Version
PRM48AH480T200A00	36.0 V - 75.0 V	Half VIC SMD	48.0 V (20.0 V to 55.0 V)	-40 to 125°C	200 W	AL / RS (Pin Selectable)
PRM48AH480M200A00				-55 to 125°C		

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for extended period of time may affect device reliability. All voltages are specified relative to SGND unless otherwise noted. Positive pin current represents current flowing out of the pin.

Parameter	Comments	Min	Max	Unit
SHARE / CONTROL NODE		-0.3	10.5	V
			+/-10	mA
ENABLE		-0.3	5.5	V
			+/-10	mA
+IN to –IN	Continuous, non-operating	-1	90	V
	100 ms, non-Operating		100	V
VAUX		-0.5	10.5	V
			+/-100	mA
SGND			+/-100	mA
IFB		-0.5	5.7	V
REF / REF _EN		-0.3	3.6	V
	Remote Sense Operation (REF _EN)		10	mA
	Adaptive Loop Operation (REF)		3.4	mA
TRIM		-0.3	3.6	V
AL		-0.3	3.6	V
VT		-0.3	4.8	V
VC to –OUT		-0.5	18	V
			+/-1.8	A
+OUT to –OUT		-1	62	V
Output Current			6.3	A
Internal Operating Temperature	T Grade	-40	125	°C
	M Grade	-55	125	°C
Storage Temperature	T Grade	-40	125	°C
	M Grade	-65	125	°C

Electrical Specifications

Specifications apply over all line and load conditions, and trim from 20.0 V to 55.0 V, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C < T_{INT} < 125°C; All Other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input Voltage Range	V_{IN}	Continuous, operating	**36.0**	48.0	**75.0**	V
V_{IN} Slew Rate	dV_{IN}/dt	0 ≤ V_{IN} ≤ 75.0 V	**0.001**		**1000**	V/ms
Initialization Voltage	V_{INIT}	Internal micro controller initialization voltage		10		V
Initialization Delay	t_{INIT}	From V_{IN} first crossing V_{INIT}	**5.0**	7.0	**9.0**	ms
No Load Power Dissipation	P_{NL}	ENABLE HIGH, V_{IN} = 48.0 V		2.4	**3.5**	W
Input Quiescent Current	I_{QC}	ENABLE LOW, V_{IN} = 48.0 V		14.5	**20.0**	mA
Input Current	I_{IN_DC}	I_{OUT} = 4.17 A, V_{IN} = 48.0 V, V_{OUT} = 48.0 V		4.3	**4.4**	A
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 48.0 V (see Fig. 13)		2		µF
Input Capacitance (Internal) ESR	R_{CIN}	Effective value, V_{IN} = 48.0 V		3.0		mΩ
Power Output Specification						
Rated Output Current	I_{OUT}	Standalone and Parent Operation, see Figure 1, SOA			**4.17**	A
Rated Output Power	P_{OUT}	Standalone and Parent Operation, see Figure 1, SOA			**200**	W
Switching Frequency	F_{SW}	V_{IN} = 48.0 V V_{OUT} = 48.0 V, I_{OUT} = 2.08 A, T_{INT} = 25°C	0.94	1.03	1.07	MHz
		Over line, load, trim and temperature, exclusive of burst mode	**0.70**		**1.07**	MHz
Output Turn-ON Delay	t_{ON}	From V_{IN} first crossing $V_{IN_UVLO+_SUPV}$ to ENABLE high; t_{INIT} expired		20		µs
		From ENABLE pin release to ENABLE high, V_{IN} applied, t_{OFF} expired		20		µs
Start up Sequence Timeout	$t_{STARTUP_SEQ}$	From ENABLE high to start up sequence complete		17		ms
Efficiency Ambient	η_{AMB}	V_{IN} = 48.0 V, V_{OUT} = 48.0 V, I_{OUT} = 4.17 A, T_{INT} = 25°C	95.25			%
		V_{IN} = 48.0 V, V_{OUT} = 48.0 V, I_{OUT} = 2.08 A, T_{INT} = 25°C	94.0	95.0		%
		V_{IN} = 36.0 V to 75.0 V, V_{OUT} = 48.0 V, I_{OUT} = 4.17 A, T_{INT} = 25°C	93.25			%
		V_{IN} = 36.0 V to 75.0 V, I_{OUT} = 4.17 A, T_{INT} = 25°C, over trim	90.0			%
Efficiency Hot	η_{HOT}	V_{IN} = 48.0 V, V_{OUT} = 48.0 V, I_{OUT} = 4.17 A, T_{INT} = 100°C	94.8	96.8		%
		V_{IN} = 48.0 V, V_{OUT} = 48.0 V, I_{OUT} = 2.08 A, T_{INT} = 100°C	94.0	96.0		%
		V_{IN} = 36.0 V to 75.0 V , V_{OUT} = 48.0 V, I_{OUT} = 4.17 A, T_{INT} = 100°C	93.5			%
		V_{IN} = 36.0 V to 75.0 V , I_{OUT} = 4.17 A, T_{INT} = 100°C, over trim	90.0			%
Efficiency Over Temperature	η	>50% load and V_{OUT} = 48.0 V; over temperature	**94.0**			%
		>50% load; over temperature and trim	**87.0**			%
Output Discharge current	I_{OD}	Average Value		0.5		mA
Output Voltage Ripple	V_{OUT_PP}	V_{IN} = 48.0 V, V_{OUT} = 48.0 V, I_{OUT} = 4.17 A, C_{OUT_EXT} = 0 F, 20 MHz BW		1000	**1500**	mV
Output Inductance (Parasitic)	L_{OUT_PAR}	Frequency @ 1.03 MHz, Simulated J-Lead model		2.5		nH
Output Capacitance (Internal)	C_{OUT_INT}	Effective value, V_{OUT} = 48.0 V (see Fig.13)		2		µF
Output Capacitance (Internal) ESR	R_{COUT}	Effective value, V_{OUT} = 48.0 V		3.0		mΩ

Electrical Specifications (cont.)

Specifications apply over all line and load conditions, and trim from 20.0 V to 55.0 V, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C < T_{INT} < 125°C; All Other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications: Adaptive Loop Operation						
Output Voltage Setpoint	V_{OUT_SET}	No load, trim Inactive, Adaptive Loop load line inactive	**47.00**	48.00	**49.00**	V
Output Voltage Trim Range	V_{OUT}		**20.0**		**55.0**	V
Output Voltage Rise Time	t_{RISE_VOUT}	From soft start initiated to output voltage settled	**1.7**	1.8	**1.9**	ms
Output Voltage Load Regulation	$V_{OUT_REG_LOAD}$	Adaptive loop load line inactive		0.02	**0.2**	%
Output Voltage Line Regulation	$V_{OUT_REG_LINE}$	Adaptive loop load line inactive		0.02	**0.2**	%
Total Regulation Error	$V_{OUT_REG_TOTAL}$	PRM output voltage, Adaptive Loop load line inactive			**0.2**	%
Total AL Regulation Error	$V_{OUT_REG_AL}$	VTM output voltage, total Adaptive Loop regulation, V_{OUT} = 48.0 V, trim inactive		1	**3**	%
		VTM output voltage, total Adaptive Loop regulation, trim active, exclusive of external resistor tolerances			**5**	%
Output Current Limit	I_{LIMIT}	V_{IN} = 48.0 V, V_{OUT} = 48.0 V, T_{INT} = 25°C, constant current limit after supervisory limit detection time t_{LIM_SUPV}	4.6	5.2	5.8	A
		Over line, load, trim and temperature	**4.2**		**6.3**	A
Load Capacitance (Electrolytic)	C_{LOAD_ALEL}	0.1 Ω ≤ ESR ≤ 1 Ω, See Figure 32, total capacitance (C_{LOAD_ALEL} + C_{LOAD_CER}) ≤ 47 µF			**47**	µF
Load Capacitance (Ceramic)	C_{LOAD_CER}	2 mΩ ≤ ESR ≤ 200 mΩ, See Figure 32			**25**	µF
Load Transient Voltage Deviation	V_{TRANS}	10% ↔ 100% load step, 10 A/µsec, 0 µF C_{OUT}, deviation from initial setpoint			**4.8**	V
Load Transient Recovery Time	t_{TRANS}	10% ↔ 100% load step, 10 A/µsec, 0 µF C_{OUT}, Recovery to 90% of final value, Adaptive Loop load line inactive		100		µs
		10% ↔ 100% load step, 10 A/µsec, 0 µF C_{OUT}, Recovery to 90% of final value, Adaptive Loop load line active, V_{AL} = 1.20 V		500		µs
Power Output Specifications: Child Operation with AL Parent						
Rated Current Within an Array	I_{OUT_ARRAY}	Child Operation within an array, up to 5°C case temperature differential, parent-child configuration			**3.3**	A
		Child Operation within an array, up to 30°C case temperature differential, parent-child configuration			**2.9**	A
Rated Power Within an Array	P_{OUT_ARRAY}	Child Operation within an array, up to 5°C case temperature differential, parent-child configuration			**160**	W
		Child Operation within an array, up to 30°C case temperature differential, parent-child configuration			**140**	W
Current Sharing Difference (Parent to Child)	$I_{OUT_SHARE_MS}$	Equal input, and output voltage at full load; V_{IN} = 48.0 V, V_{OUT} = 48.0 V			**15**	%
		Equal input and output voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 5°C part-part temp. mismatch			15	%
		Equal input, and output voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 30°C part-part temp. mismatch			20	%

Electrical Specifications (cont.)

Specifications apply over all line and load conditions, and trim from 20.0 V to 55.0 V, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C < T_{INT} < 125°C; All Other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications: Child Operations (cont.)						
Current Sharing Difference (Child to Child)	$I_{OUT_SHARE_SS}$	Equal input, output, and SHARE voltage at full load; V_{IN} = 48.0 V, V_{OUT} = 48.0 V			**5**	%
		Equal input, output and SHARE voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 5°C part-part temp. mismatch			10	%
		Equal input, output, and SHARE voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 30°C part-part temp. mismatch			15	%
Maximum Array Size	$N_{PRMS_PARALLEL}$	Maximum number of parallel devices, parent-child configuration			**5**	PRMs
Power Output Specifications: Remote Sense Operation						
Output Voltage Range	V_{OUT}		**20.0**		**55.0**	V
Rated Current Within an Array	I_{OUT_ARRAY}	Remote Sense Operation within an array, up to 5°C case temperature differential			**3.8**	A
		Remote Sense Operation within an array, up to 30°C case temperature differential			**3.3**	A
Rated Power Within an Array	P_{OUT_ARRAY}	Remote Sense Operation within an array, up to 5°C case temperature differential			**180**	W
		Remote Sense Operation within an array, up to 30°C case temperature differential			**160**	W
Current Sharing Difference	$I_{OUT_SHARE_RS}$	Equal input, output, and CONTROL NODE voltage at full load; V_{IN} = 48.0 V, V_{OUT} = 48.0 V			**5**	%
		Equal input, output and CONTROL NODE voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 5°C part-part temp. mismatch			10	%
		Equal input, output, and CONTROL NODE voltage at full load; Over line and trim, with 25°C ≤ T_C ≤ 100°C and ≤ 30°C part-part temp. mismatch (worst case)			15	%
Maximum Array Size	$N_{PRMS_PARALLEL}$	Maximum number of parallel devices, Remote Sense configuration, CONTROL NODE externally driven			**10**	PRMs

Electrical Specifications (cont.)

Specifications apply over all line and load conditions, and trim from 20.0 V to 55.0 V, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40ºC < T_{INT} < 125ºC; All Other specifications are at T_{INT} = 25ºC unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protections						
Input Undervoltage Turn-ON	V_{IN_UVLO+}			30.9	**33.0**	V
Input Undervoltage Turn-OFF	V_{IN_UVLO-}	Instantaneous powertrain shutdown, detected after t_{BLANK}	**26.0**	28.8		V
Input Undervoltage Hysteresis	V_{UVLO_HYST}	(V_{IN_UVLO+}) - (V_{IN_UVLO-})	**1.9**	2.2	**2.4**	V
Input Overvoltage Turn-ON	V_{IN_OVLO-}		**79.6**	82.9		V
Input Overvoltage Turn-OFF	V_{IN_OVLO+}	Instantaneous powertrain shutdown, detected after t_{BLANK}		84.6	**88.8**	V
Input Overvoltage Hysteresis	V_{OVLO_HYST}	(V_{IN_OVLO+}) - (V_{IN_OVLO-})	**1.4**	1.7	**2.1**	V
Output Overvoltage Threshold	V_{OUT_OVP+}	Instantaneous shutdown, detected after t_{PROT}	**56.0**	58.3	**60.1**	V
Minimum Current Limited Vout	V_{OUT_UVP}				**12**	V
Overtemperature Shutdown Setpoint	T_{INT_OTP}	Instantaneous shutdown, detected after t_{PROT}	**125**			ºC
Output Power Limit	P_{PROT}		**200**			W
Short Circuit V_{OUT} Threshold	V_{SC_VOUT}			8.8		V
Short Circuit V_{OUT} Recovery Threshold	V_{SC_VOUTR}			9.5		V
Short Circuit CONTROL NODE Threshold	V_{SC_VCN}			7.2		V
Short Circuit CONTROL NODE Recovery Threshold	V_{SC_VCNR}			6.9		V
Short Circuit Timeout	t_{SC}	Short circuit fault detected after V_{SC_VOUT} and V_{SC_VCN} thresholds persist for this time		5		ms
Short Circuit Recovery Time	t_{SCR}	Excludes t_{OFF}		75		ms
Overcurrent (IFB) and Input Over/Undervoltage Blanking Time	t_{BLANK}		**50**	120	**150**	µs
Overtemperature, Output Overvoltage and ENABLE Shutdown Response Time (Hardware)	t_{PROT}			2		µs
Powertrain Supervisory Limits						
Input Undervoltage Turn-ON (Supervisory)	$V_{IN_UVLO+_SUPV}$			33.8	**35.2**	V
Input Undervoltage Turn-OFF (Supervisory)	$V_{IN_UVLO-_SUPV}$	Powertrain shutdown, detected after t_{LIM_SUPV}	**30.5**	31.8		V
Input Undervoltage Hysteresis (Supervisory)	$V_{UVLO_HYST_SUPV}$	($V_{IN_UVLO+_SUPV}$) - ($V_{IN_UVLO-_SUPV}$)	**1.6**	2.0	**2.1**	V
Input Overvoltage Turn-ON (Supervisory)	$V_{IN_OVLO-_SUPV}$		**75.6**	78.8		V
Input Overvoltage Turn-OFF (Supervisory)	$V_{IN_OVLO+_SUPV}$	Powertrain shutdown, detected after t_{LIM_SUPV}		80.3	**82.7**	V
Input Overvoltage Hysteresis (Supervisory)	$V_{OVLO_HYST_SUPV}$	($V_{IN_UVLO+_SUPV}$) - ($V_{IN_UVLO-_SUPV}$)	**1.2**	1.5	**1.8**	V
Undertemperature Shutdown Setpoint (Supervisory)	T_{INT_UTP}	T Grade			-40	ºC
		M Grade			-55	ºC
Supervisory Limit Response Time	t_{LIM_SUPV}				**150**	µs

Signal Specifications

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

ENABLE

- The ENABLE pin enables and disables the PRM
- In PRM array configurations, ENABLE pins should be connected in order to synchronize start up
- ENABLE is 5 V with 1.8 mA source capability during normal operation

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Normal Operation	ENABLE Voltage	V_{ENABLE}		**4.7**	5.0	**5.3**	V
		ENABLE Current	I_{ENABLE_OP}				**1.8**	mA
	Start up	ENABLE Source Current	I_{ENABLE_EN}	After t_{OFF}		90		µA
		Minimum Time to Start	t_{OFF}		**13.0**	15.0	**17.0**	ms
Digital Input / Output	Start up	ENABLE Enable Threshold	V_{ENABLE_EN}			2.5	**3.2**	V
	Standby	ENABLE Disable Threshold	V_{ENABLE_DIS}		**0.97**	2.40		V
		ENABLE Resistance (External)	R_{ENABLE_EXT}	Resistance to SGND required to disable the PRM			**235**	Ω
Digital Output	Fault	ENABLE Sink Current to SGND	I_{ENABLE_FAULT}	ENABLE voltage 1 V or above			**4**	mA

VAUX: Auxillary Voltage Source

- Intended to power auxiliary circuits
- 9 V during normal operation with 5 mA source capability

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Normal Operation	VAUX Voltage	V_{VAUX}		**8.6**	9.0	**9.5**	V
		VAUX Current	I_{VAUX}				**5**	mA
		VAUX Voltage Ripple	V_{VAUX_PP}	I_{OUT} = 0A, C_{VAUX_EXT} = 0. Maximum specification includes powertrain operation in burst mode.		100	**400**	mV
	Transition	VAUX Capacitance (External)	C_{VAUX_EXT}				**0.04**	µF
		VAUX Fault Response Time	t_{FR_VAUX}	From fault recognition to VAUX = 1.5 V		30		µs

VC: VTM Control

- Pulsed voltage source used to power and synchronize downstream VTM during start up
- 14 V, 10 ms typical voltage pulse

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Start up	VC Voltage	V_{VC_START}	Connected to VTM VC or equivalent, I_{VC} = 115 mA, C_{VC} = 3.2 uF	**13**	14	**18**	V
		VC Available Current	I_{VC_START}	V_C = 14 V, V_{IN} > 20 V	**200**			mA
		VC Duration	t_{VC}		**7**	10	**16**	ms
		VC Slew Rate	dVC/dt	Connected to VTM or equivalent, I_{VC} = 115 mA, C_{VC} = 3.2 uF	**0.02**		**0.25**	V/µs
		ENABLE to VC Delay	$t_{ENABLE-VC}$			20		µs

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

SGND: Signal Ground								
• All control signals must be referenced to this pin, with the exception of VC • SGND is internally connected to -IN and -OUT								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input / Output	Any	Maximum Allowable Current	I_{SGND}		**-100**		**100**	mA

TRIM								
• TRIM is used to select operating mode and trim the output voltage in Adaptive Loop Operation • Internal pullup to V_{CC_INT} through 10 kΩ resistor • When pulled below 0.45 V during power up, Remote Sense / Child Operation is selected • When allowed to pull up above 0.55 V during power up, Adaptive Loop Operation is selected • Operating mode is detected during power up and cannot be changed unless input power is cycled								
Signal Type	**State**	**Attribute**	**Symbol**	**Conditions / Notes**	**Min**	**Typ**	**Max**	**Unit**
Analog Input	Normal Operation	Internally Generated VCC	V_{CC_INT}		**3.20**	3.28	**3.36**	V
		Internal Pullup Resistance to V_{CC_INT}	R_{TRIM_INT}	0.5% tolerance resistor	**9.83**	10.00	**10.18**	kΩ
	Mode Detect	Mode Detection Delay	t_{MODE_DETECT}	From ENABLE high to mode detected, after V_{IN} first applied	**100**	140	**200**	µs
		Remote Sense Enable Threshold	$V_{RS_MODE_EN}$	Pull **below** this value during first start up after application of power to enable Remote Sense / Child Operation	**0.45**			V
		Remote Sense Disable Threshold	$V_{RS_MODE_DIS}$	Pull **above** this value during first start up after application of power to enable Adaptive Loop Operation			**0.55**	V

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

TRIM (Adaptive Loop Operation Only)

- Provides dynamic trim control over the PRM output voltage in Adaptive Loop Operation
- Sampled prior to every start up to detect if trim is active or inactive
- Output voltage is equal to 20 times the voltage at the TRIM pin when applied TRIM voltage is within the active range
- Trim state is detected during normal operation and cannot be changed until start up is initiated

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Start up	Trim Enable Threshold	V_{TRIM_EN}	Pull **below** this value during start up to enable trim control	**3.10**			V
		Trim Disable Threshold	V_{TRIM_DIS}	Pull **above** this value during start up to disable trim control			**3.20**	V
		Minimum Trim Disable Resistance	$R_{TRIM_DIS_MIN}$	Minimum TRIM resistance required to disable trim	**10**			MΩ
		Trim Capacitance (External)	C_{TRIM_EXT}				**100**	pF
		Trim Sample Delay	t_{ENABLE_TRIM}	From ENABLE high to TRIM sampled	**100**	140	**200**	µs
	Normal Operation	TRIM Pin Analog Range	V_{TRIM_RANGE}	See Figure 26	**1.00**		**2.75**	V
		TRIM Gain	G_{TRIM}	V_{OUT} / V_{TRIM}, V_{TRIM} applied within active range		20		V / V
		Trim Accuracy	$\%_{ACC_TRIM}$	Vout accuracy, exclusive of external resistor tolerance		0.5	**2.0**	%
		V_{OUT} Referred Trim Resolution	V_{OUT_RES}			200		mV
		Trim Latency	t_{TRIM_LAT}		**60**	120	**240**	µs
		Trim Bandwidth	BW_{TRIM}	-3dB point		1.2		kHz

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

AL: Adaptive Loop (Adaptive Loop Operation Only)

- Provides Adaptive Loop load line programming in Adaptive Loop Operation
- Internal pullup to V_{CC_INT} through 10 kΩ resistor
- Sampled prior to every start up to detect if Adaptive Loop load line is active or inactive
- Leave open to disable Adaptive Loop load line
- Not used in Remote Sense Operation

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Start up	AL Enable Threshold	V_{AL_EN}	Pull **below** this value during start up to enable AL load line	**3.10**			V
		AL Disable Threshold	V_{AL_DIS}	Pull **above** this value during start up to disable AL load line			**3.20**	V
		Minimum AL Disable Resistance	$R_{AL_DIS_MIN}$	Minimum AL resistance required to disable AL load line	**10**			MΩ
		AL Capacitance (External)	C_{AL_EXT}				**100**	pF
		AL Sample Delay	t_{ENABLE_AL}	From ENABLE high to AL sampled	**100**	140	**200**	µs
	Normal Operation	Internally generated VCC	V_{CC_INT}		**3.20**	3.28	**3.36**	V
		Internal Pullup Resistance to V_{CC_INT}	R_{AL_INT}	0.5% tolerance resistor	**9.83**	10.00	**10.18**	kΩ
		AL Pin Analog Range	V_{AL_RANGE}		**0**		**3.10**	V
		AL Gain	G_{AL}	Positive correction slope, VT inactive		1.0		Ω/V
		AL Load Line Accuracy	$\%_{ACC_LL_AL}$	Full load slope accuracy exclusive of external resistor tolerance		0.5	**2.0**	%
		AL Load Line Resolution	LL_{AL_RES}			3		mΩ
		Maximum Output Referred Compensation	$V_{OUT_AL_MAX}$	Maximum increase from no load setpoint, $V_{OUT} \leq 55.0$ V			**5**	V
		AL Latency	t_{AL_LAT}		**60**	120	**240**	µs
		AL Bandwidth	BW_{AL}	-3dB point		1.2		kHz

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

VT: VTM Temperature (Adaptive Loop Operation Only)

- VTM temperature compensation for Adaptive Loop regulation
- Adjusts the slope of the Adaptive Loop load line to account for changes in VTM output resistance over temperature
- Connect to TM pin of compatible downstream VTM to enable temperature compensation
- Leave disconnected to disable temperature compensation

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Normal Operation	Internal Resistance to SGND	R_{VT_INT}			80.0		kΩ
		VT Enable Threshold	V_{VT_EN}				**2.1**	V
		VT Disable Threshold	V_{VT_DIS}	Pull below this value to disable VT temperature compensation	**1.9**			V
		VT Disable Default Temperature	T_{VT_DIS}	Default AL temperature setting when VT disabled		25		°C
		VT Analog Range	V_{VT_OP}		**2.18**		**3.98**	V
		VT Temperature Coefficient	TC_{VT}	VT within active range, referenced to 2.98 V		30		%/V
			TC_{VT}	VTM TM voltage applied, .01V/°K, referenced to 25°C		0.3		%/C
		VT Resolution	TC_{VT_RES}	VTM TM voltage applied, .01V/°K		0.4		°C
		VT Latency	t_{VT_LAT}		**60**	120	**240**	µs
		Bandwidth	BW_{VT}	-3dB point		1.5		kHz

REF: Reference (Adaptive Loop Operation Only)

- Functions as REF pin in Adaptive Loop Operation
- REF represents the internal voltage reference for the voltage control circuit
- V_{OUT} approximately equal to 20 times REF voltage

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Normal Operation	REF Voltage	V_{REF}	V_{OUT} = 48.0 V, trim inactive		2.4		V
		REF to V_{OUT} Scale Factor	G_{REF_VOUT}	V_{OUT} / V_{REF}		20		V / V
		REF Resistance (External)	R_{REF_EXT}		**10**			MΩ
		REF Capacitance (External)	C_{REF_EXT}				**200**	pF
		REF Voltage Ripple	V_{REF_PP}	Includes burst mode, 20 MHz BW		25		mV
	Transition	ENABLE to REF Delay	t_{ENABLE_REF}	ENABLE low to REF low		120		µs
		VAUX to REF Delay	t_{VAUX_REF}	VAUX = 8.1 V to REF soft start ramp initiated		1		ms

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

REF_EN: Reference Enable (Remote Sense and Child Operation Only)

- Functions as REF_EN pin in Remote Sense and Child Operation
- REF_EN signals successful start up and powertrain ready to operate
- Intended to power and enable the external feedback circuit reference in Remote Sense Operation
- 3.25 V, 4 mA regulated voltage source

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Normal Operation	REF_EN Voltage	V_{REF_EN}	REF_EN unloaded	**2.72**	3.25	**3.37**	V
		REF_EN Source Impedance	$R_{OUT_REF_EN}$			50	**100**	Ω
		REF_EN Current	I_{REF_EN}				**4**	mA
		REF_EN Capacitance (External)	$C_{REF_EN_EXT}$				**0.1**	µF
		REF_EN Voltage Ripple	$V_{REF_EN_PP}$	Includes burst mode, 20 MHz BW		25		mV
	Transition	ENABLE to REF_EN Delay	$t_{ENABLE_REF_EN}$	ENABLE low to REF_EN low		120		µs
		VAUX to REF_EN Delay	$t_{VAUX_REF_EN}$	VAUX = 8.1 V to REF_EN high		1		ms

Share (Adaptive Loop and Child Operation Only)

- Functions as SHARE pin in parent child array configuration
- Current share bus for array operation (parent/child scheme)
- Sources current and provides SHARE signal in parent operation
- Sinks constant current when externally driven in active range (Child Operation)

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Output	Standalone/ Parent Operation	SHARE Voltage Active Range	V_{SHARE}		**0.79**		**7.40**	V
		SHARE Available Current	I_{SHARE}	V_{SHARE} > 0.79 V	**2.5**			mA
		SHARE Resistance to SGND	R_{SHARE}			93.3		kΩ
Analog Input	Child Operation	SHARE Sink Current	I_{SHARE_SINK}	V_{SHARE} > 0.79 V	**0.25**	0.50	**0.75**	mA

Signal Specifications (cont.)

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

Control Node (Remote Sense Operation Only)

- Functions as CONTROL NODE pin in Remote Sense Operation
- Modulator control node voltage sets power train timing
- Driven by external error amplifier in Remote Sense Operation
- Sinks constant current when externally driven in active range
- Sources current, and clamps voltage to 0.79 V when pulled below active range

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Normal Operation	CONTROL NODE Voltage Active Range	V_{CN}		**0.79**		**7.40**	V
		CONTROL NODE Source Current	I_{CN_LOW}	V_{CN} < 0.79 V			**2.5**	mA
		CONTROL NODE Sink Current	I_{CN_SINK}	V_{CN} > 0.79 V	**0.25**	0.50	**0.75**	mA
		CONTROL NODE Resistance to SGND	R_{CN}			93.3		kΩ

IFB: Current Feedback (Remote Sense Operation Only)

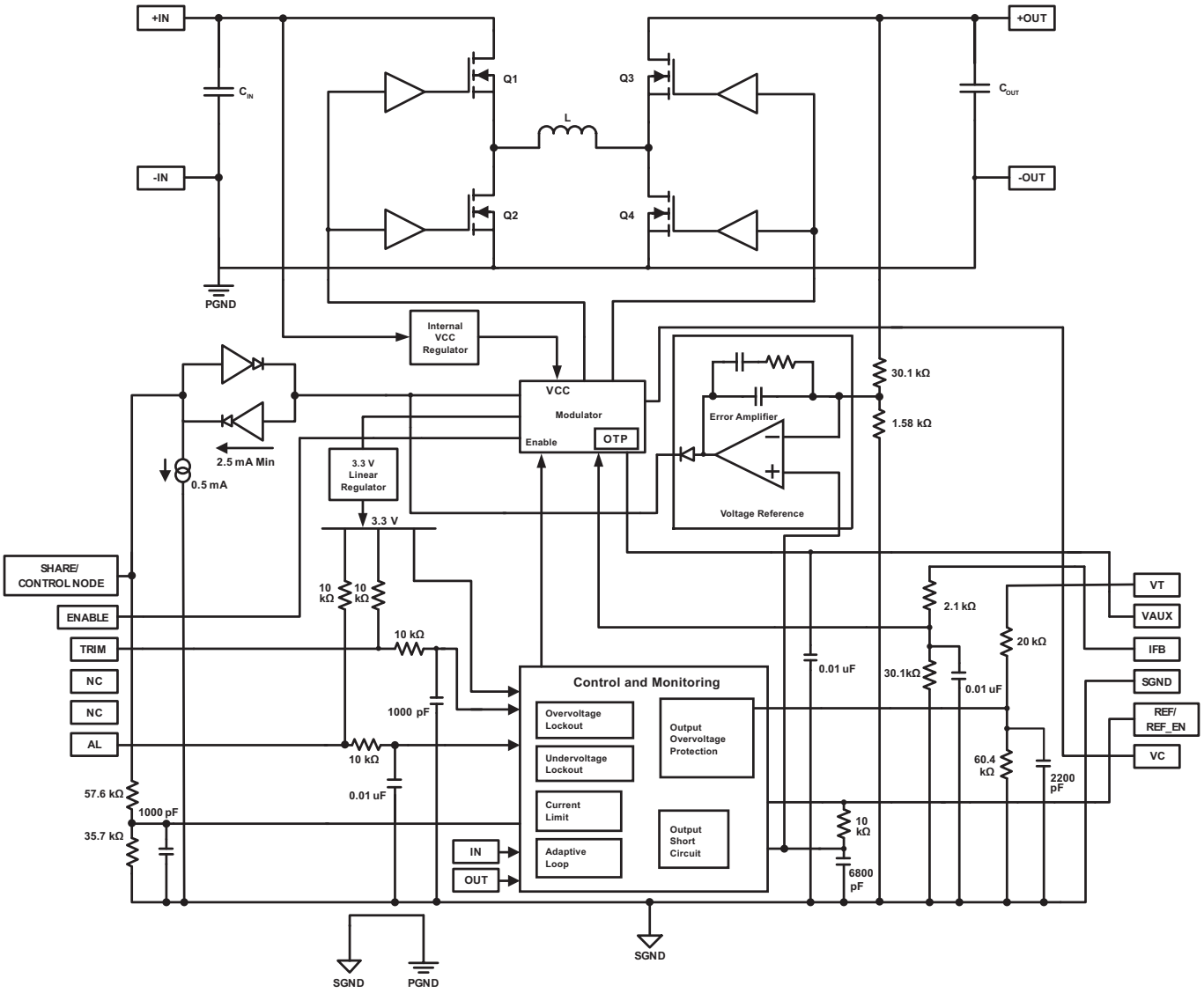
- Functions as IFB pin in Remote Sense Operation
- A voltage proportional to the PRM output current must be supplied externally to the IFB pin in order for the device to properly protect overcurrent events and to enable output current limit (clamp)
- Overcurrent protection trip will cause instantaneous powertrain disable, detected after t_{BLANK}
- Not used for Adaptive Loop Operation

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Normal Operation	Current Limit (Clamp) Threshold	V_{IFB_IL}	V_{IN} = 48.0 V; V_{OUT} = 48.0 V T_{INT} = 25°C	1.90	2.00	2.10	V
				Over line, trim, and temperature	**1.85**		**2.15**	V
		Overcurrent Protection Threshold	V_{IFB_OC}	Not production tested; guaranteed by design; T_{INT} = 25°C	**2.58**	2.69	**2.80**	V
				Not production tested; guaranteed by design; over line, trim, and temperature	**2.56**		**2.82**	V
		IFB Input Impedance	R_{IFB}		**2.09**	2.13	**2.17**	kΩ
		Current Limit Bandwidth	BW_{IL}			2.0		kHz

NC: No Connect

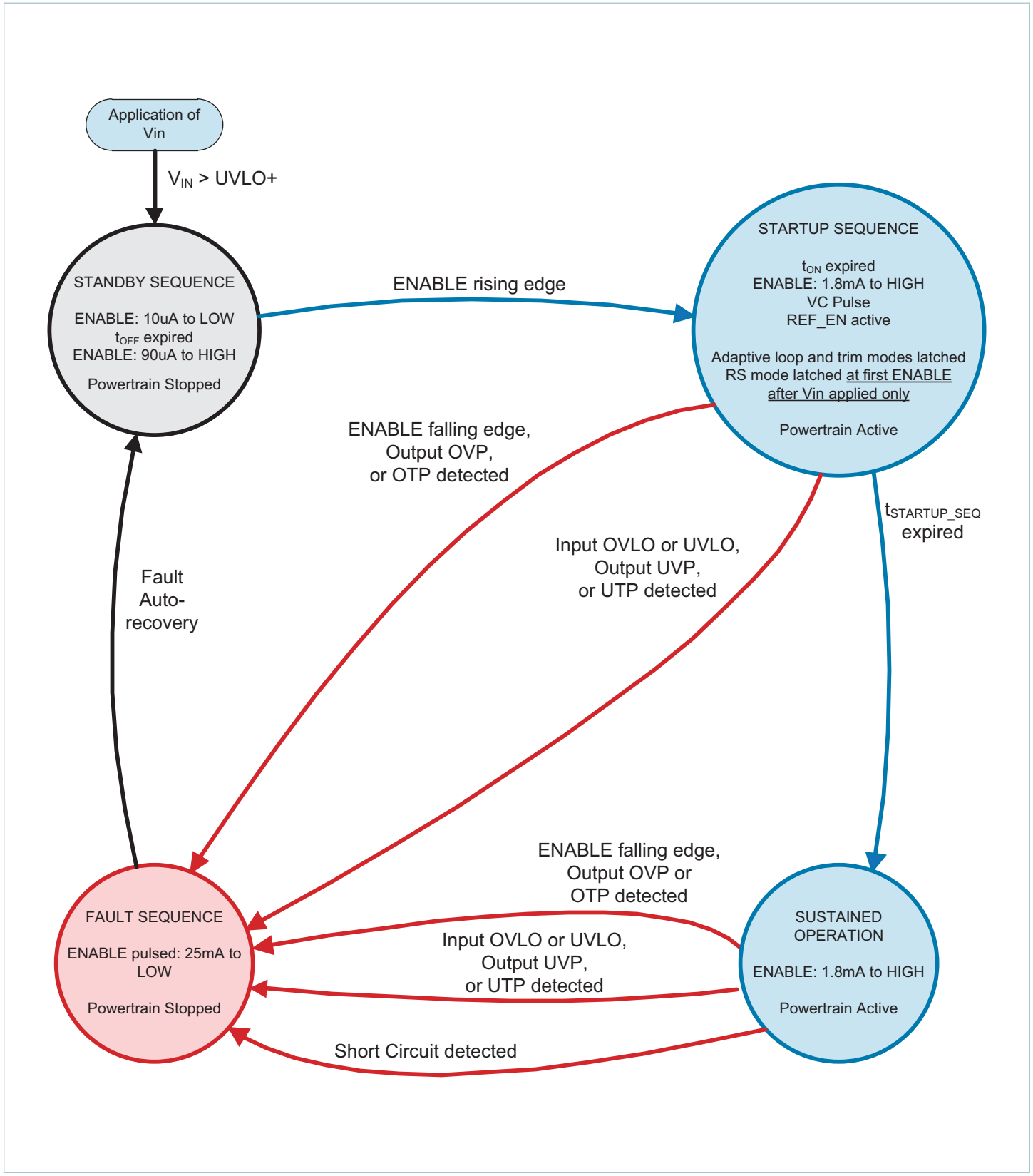
- Reserved for factory use only
- No connections should be made to these pins

Functional Block Diagram



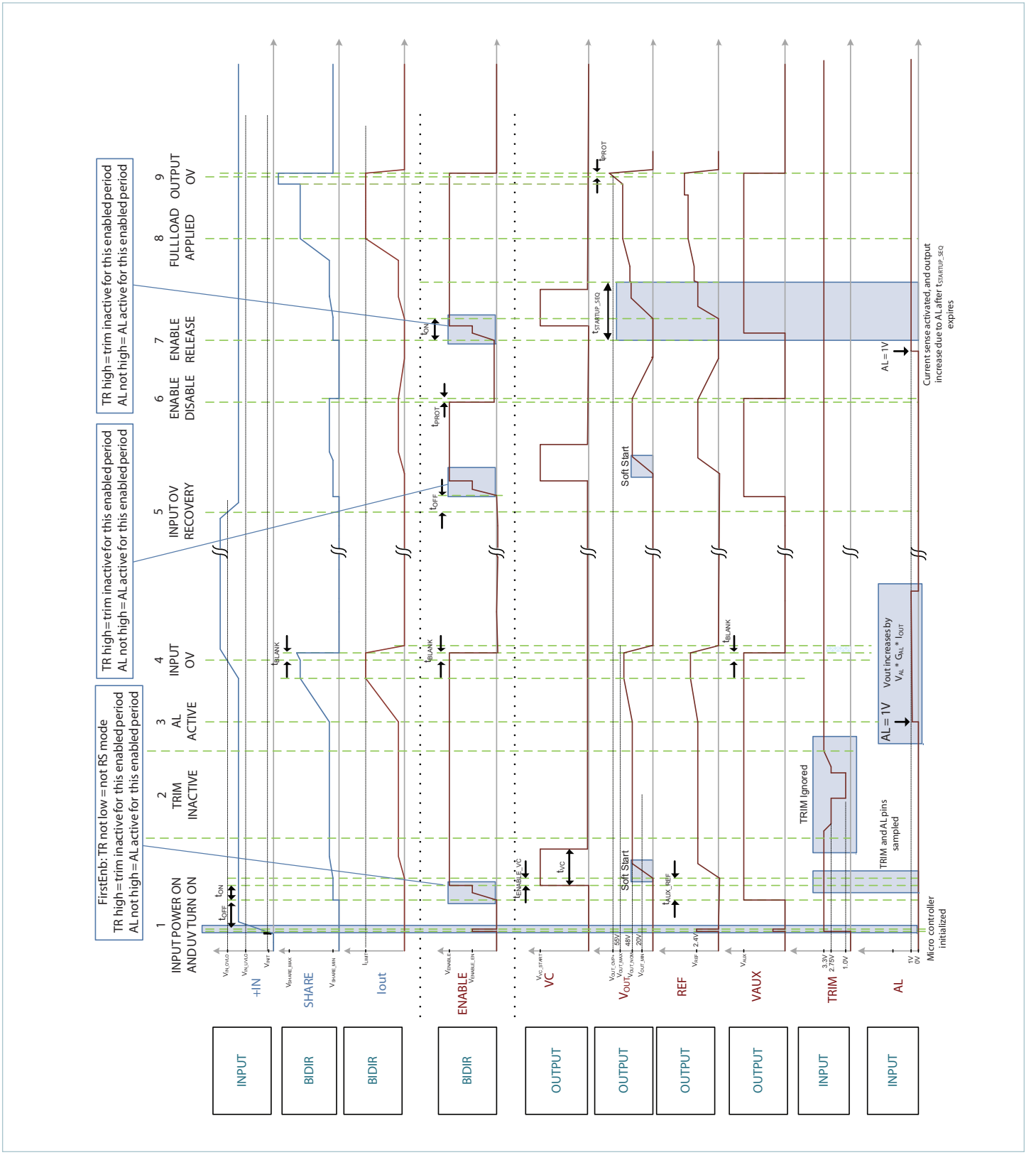
High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



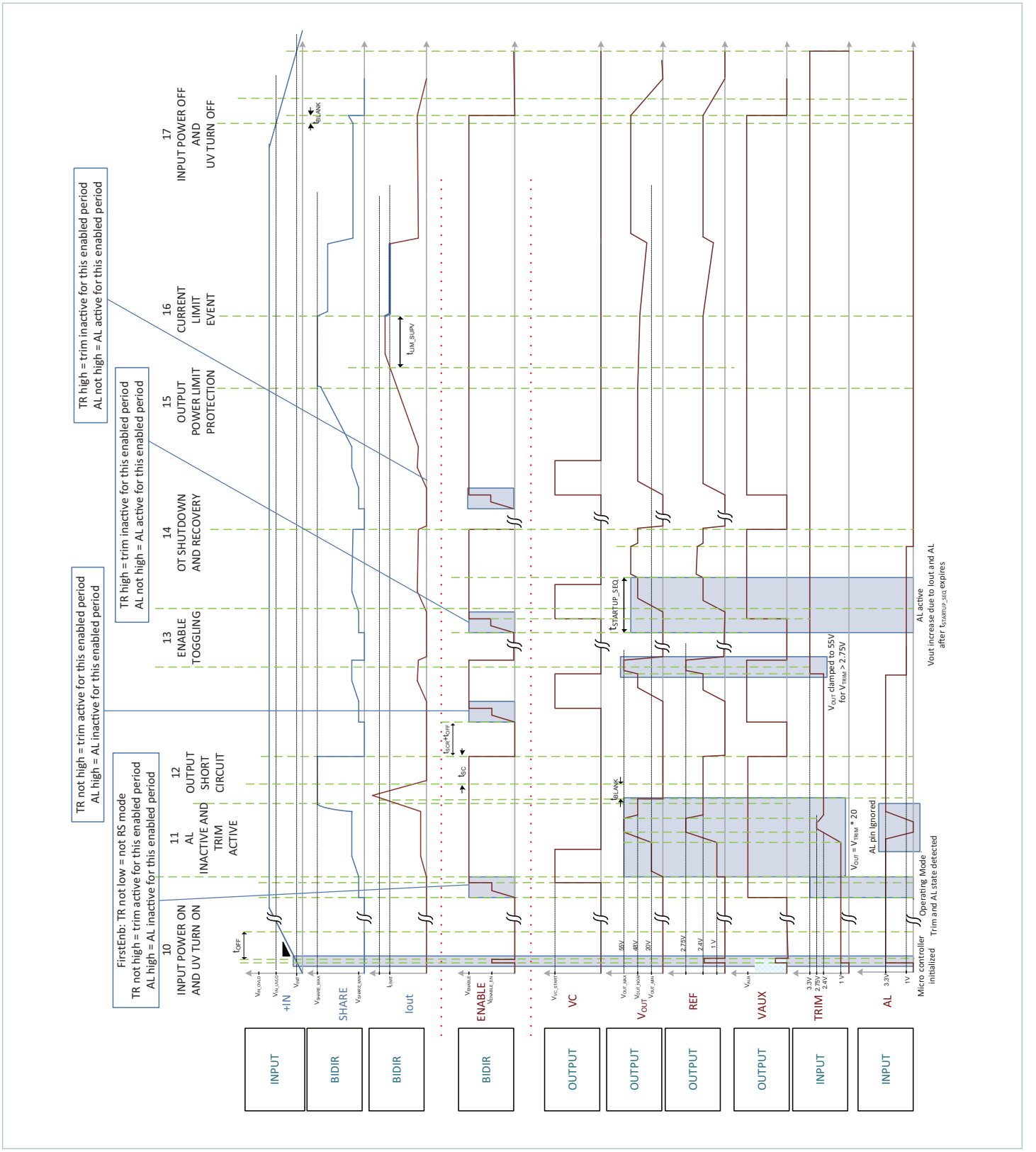
Timing Diagrams (Adaptive Loop Operation)

Module Inputs are shown in blue; Module Outputs are shown in brown.



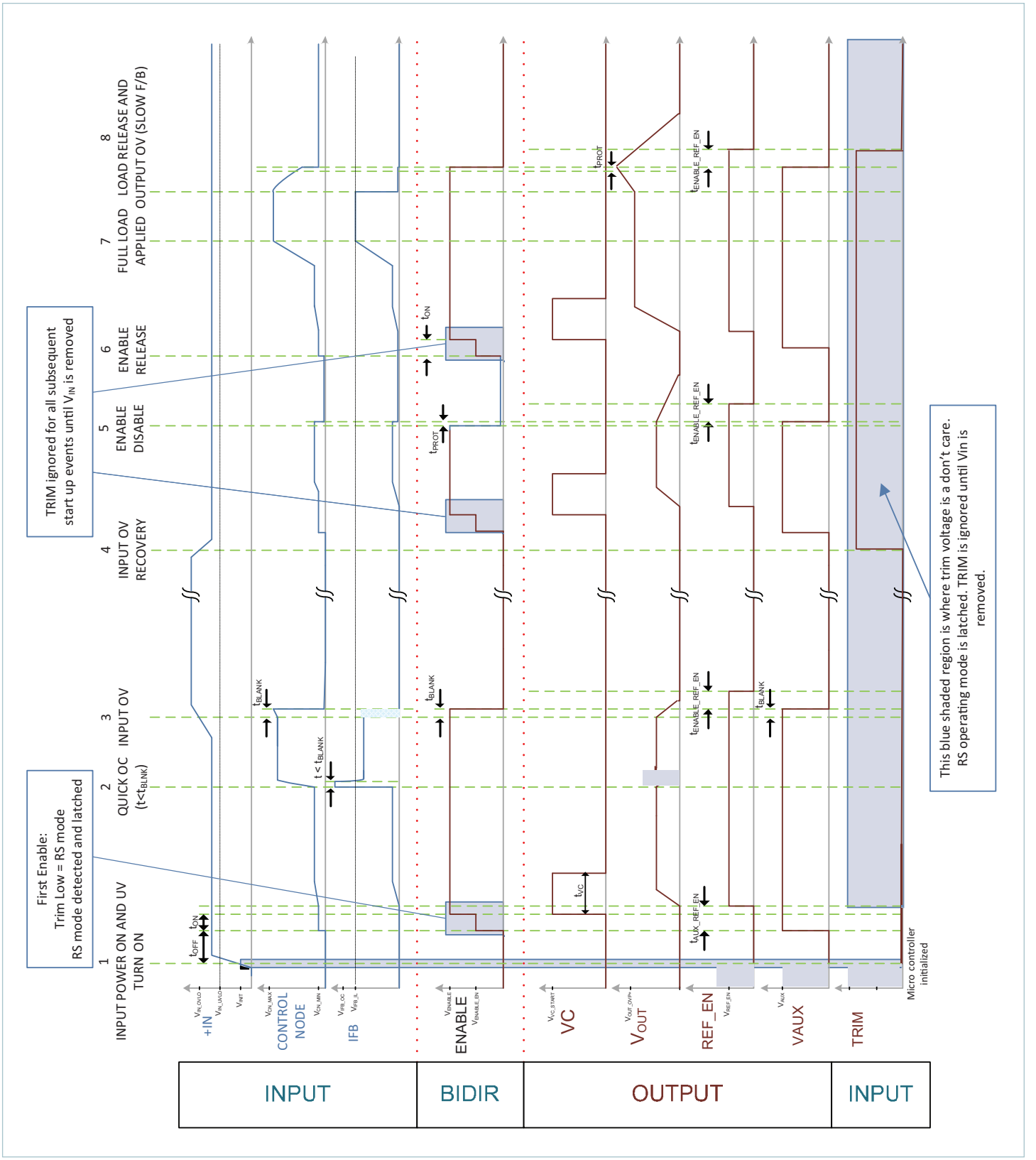
Timing Diagrams (Adaptive Loop Operation) (cont.)

Module Inputs are shown in blue; Module Outputs are shown in brown.



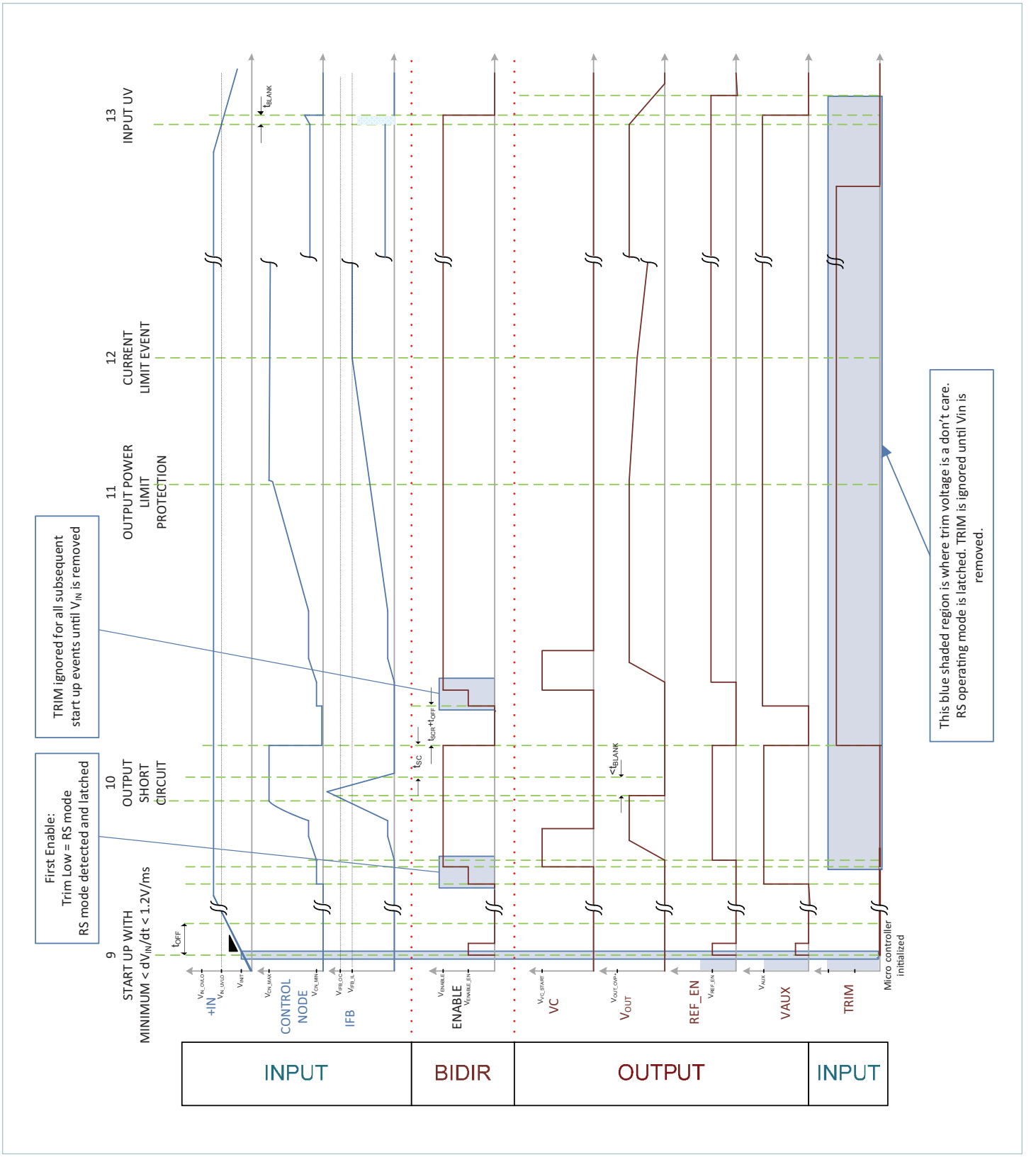
Timing Diagrams (Remote Sense Operation)

Module Inputs are shown in blue; Module Outputs are shown in brown.



Timing Diagrams (Remote Sense Operation) (cont.)

Module Inputs are shown in blue; Module Outputs are shown in brown.



Typical Performance Characteristics

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

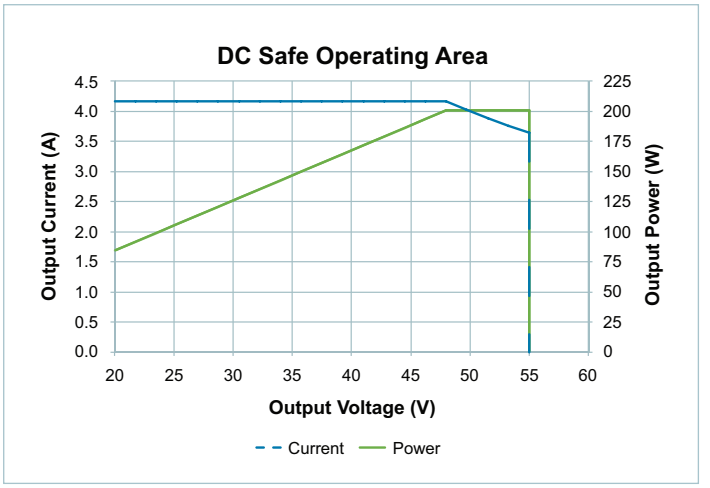


Figure 1 — *DC Safe Operating Area (SOA)*

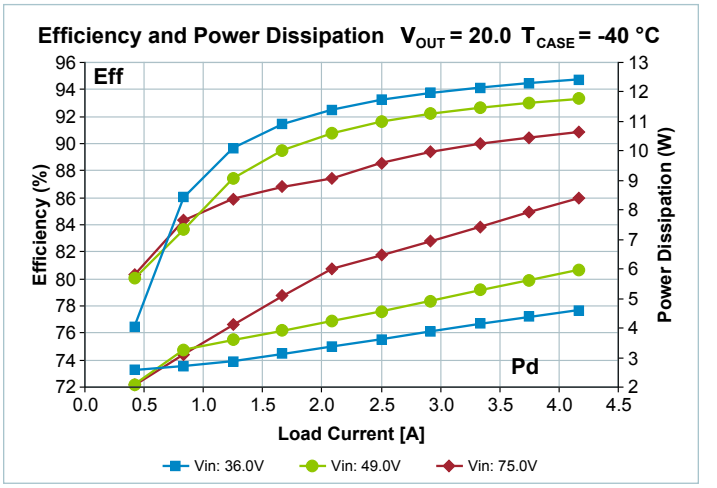


Figure 4 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 20.0 V, T_{CASE} = -40°C*

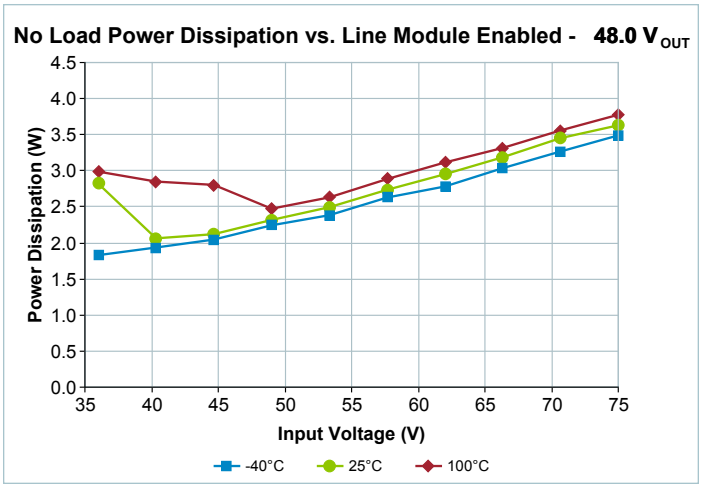


Figure 2 — *No Load Power Dissipation vs. V_{IN}, module enabled*

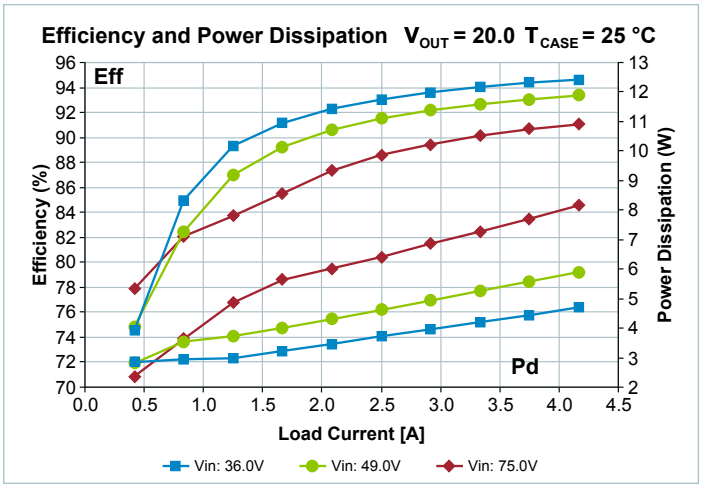


Figure 5 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 20.0 V, T_{CASE} = 25°C*

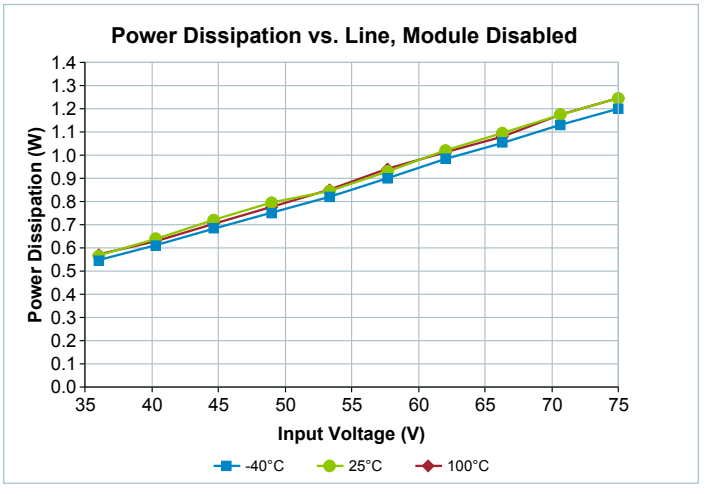


Figure 3 — *No Load Power Dissipation vs. V_{IN}, module disabled - Enable = Low*

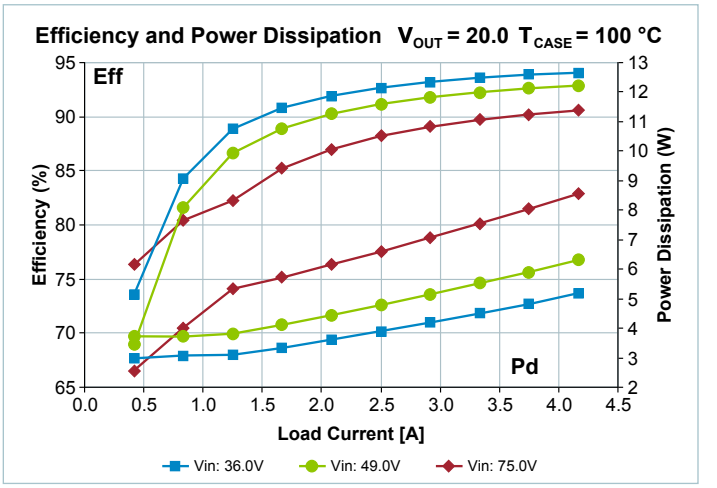


Figure 6 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 20.0 V, T_{CASE} = 100°C*

Typical Performance Characteristics (cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

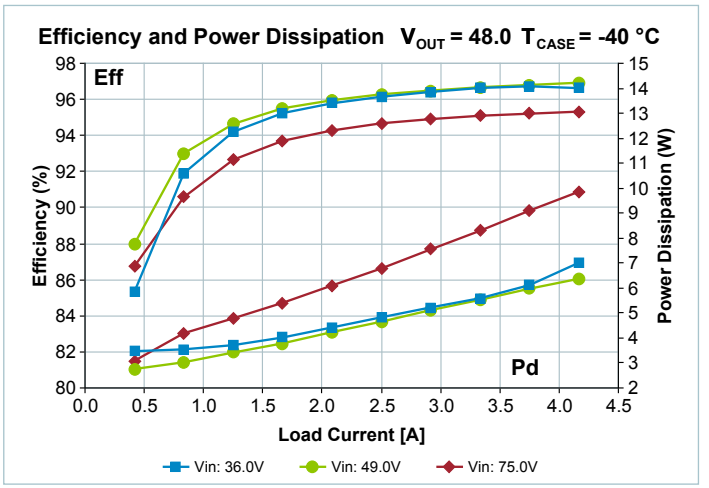


Figure 7 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 48.0 V, T_{CASE} = -40°C*

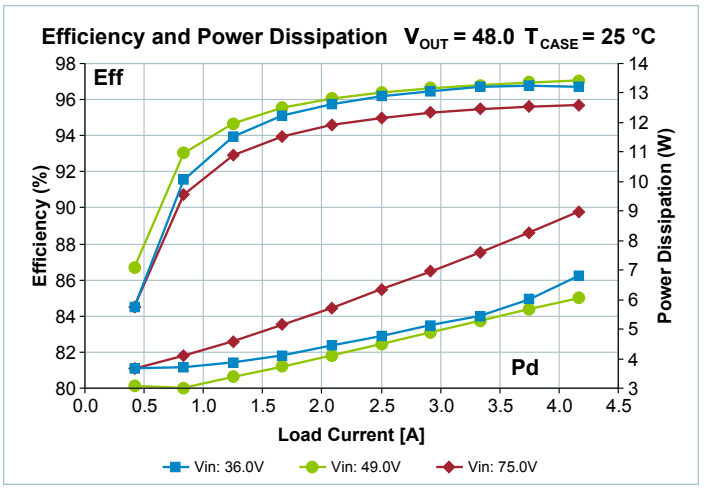


Figure 8 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 48.0 V, T_{CASE} = 25°C*

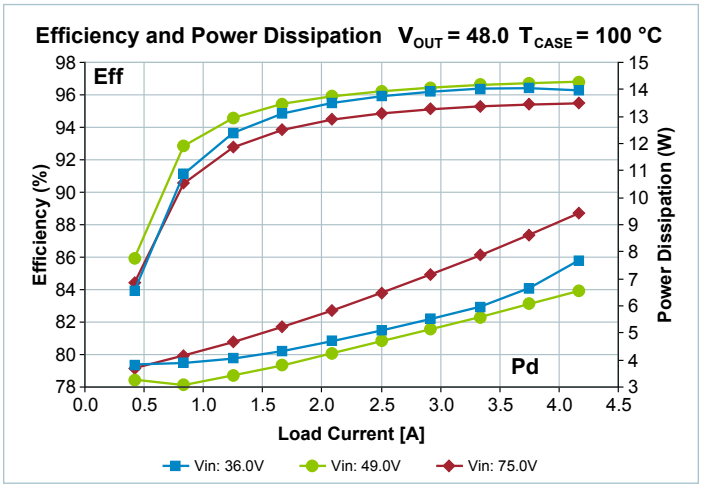


Figure 9 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 48.0 V, T_{CASE} = 100°C*

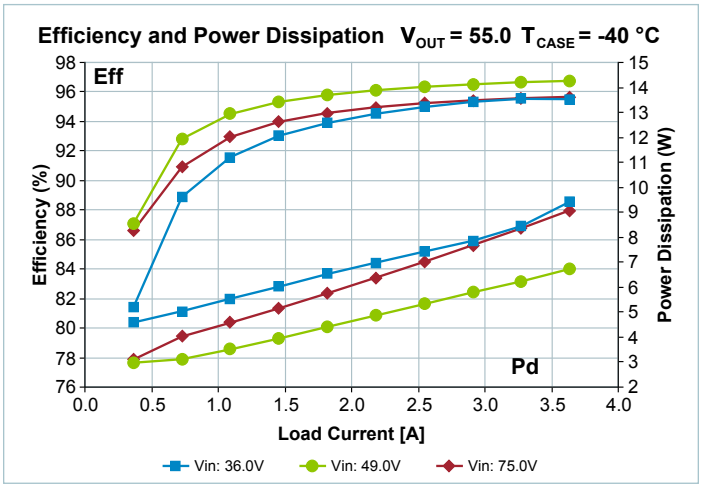


Figure 10 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 55.0 V, T_{CASE} = -40°C*

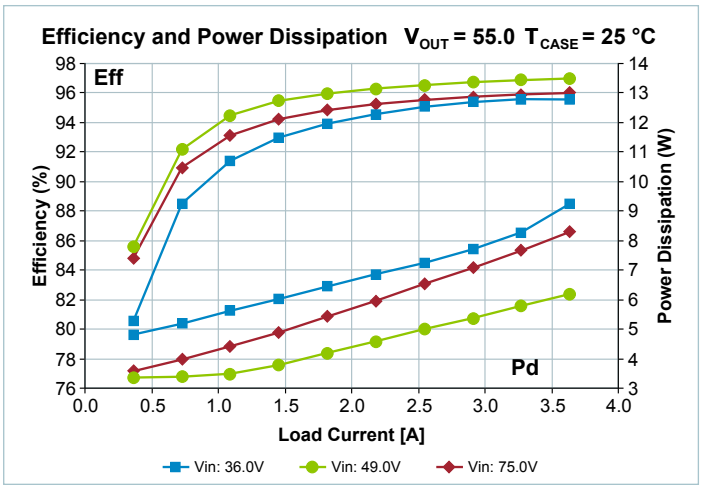


Figure 11 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 55.0 V, T_{CASE} = 25°C*

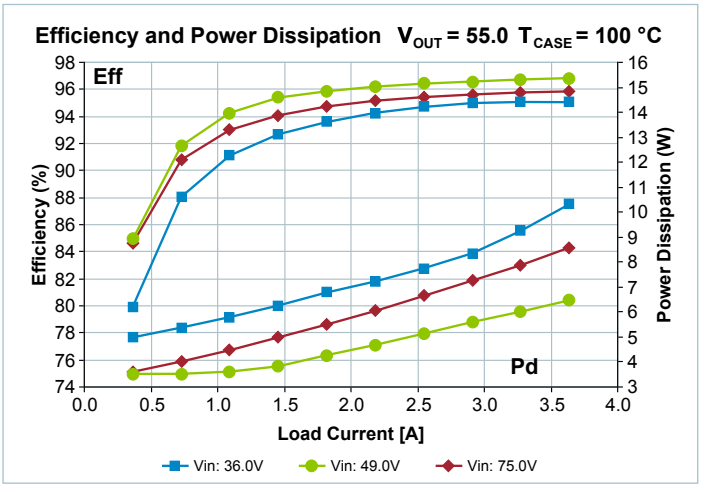


Figure 12 — *Total efficiency and power dissipation vs. V_{IN} and I_{OUT} V_{OUT} = 55.0 V, T_{CASE} = 100°C*

Typical Performance Characteristics (cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

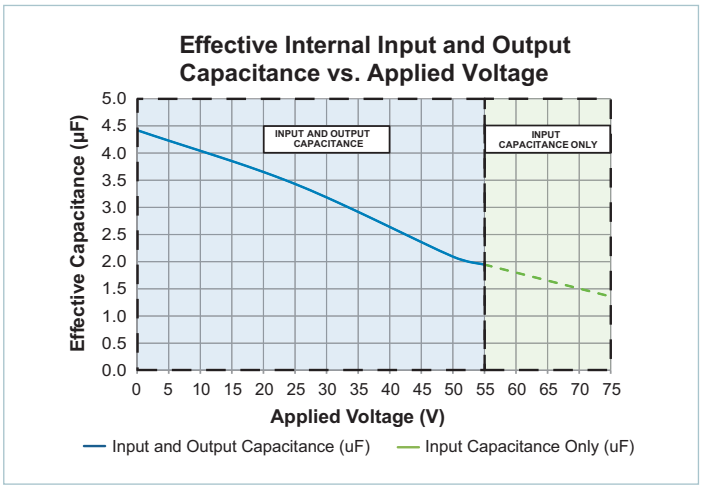


Figure 13 — *Effective Internal Input and Output Capacitance vs. Voltage – Ceramic Type*

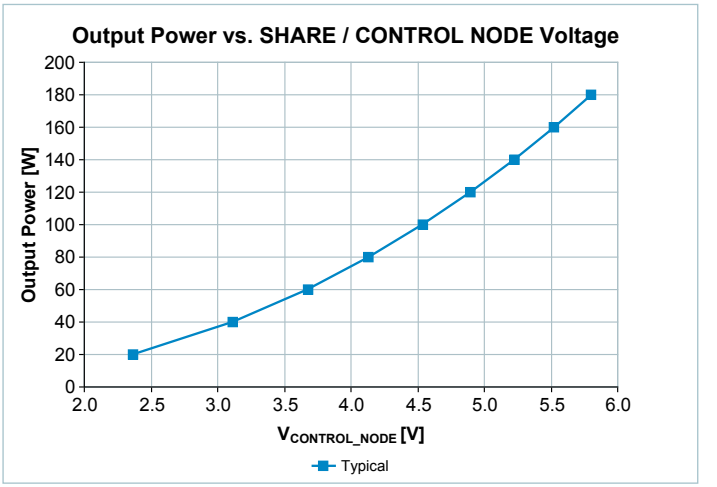


Figure 16 — *Output Power vs. SHARE / CONTROL NODE Voltage; V_{IN} = 48.0 V, V_{OUT} = 48.0 V, T_{CASE} = 25°C*

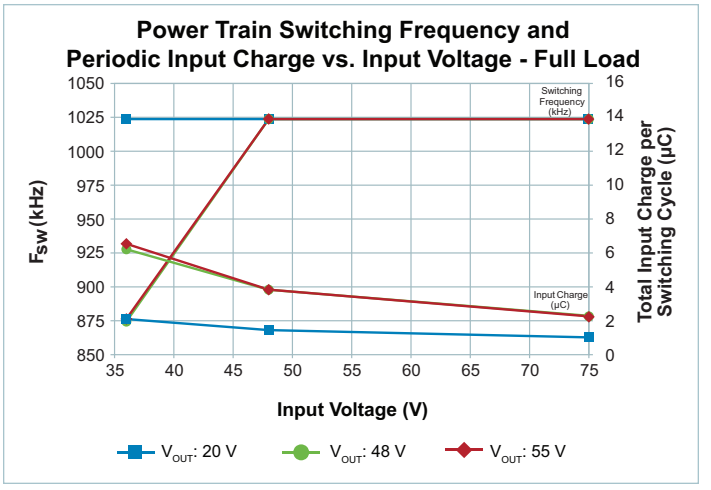


Figure 14 — *Typical Power Train Switching Frequency and Periodic Input Charge vs. V_{IN}, V_{OUT}; I_{OUT} = 4.17 A*

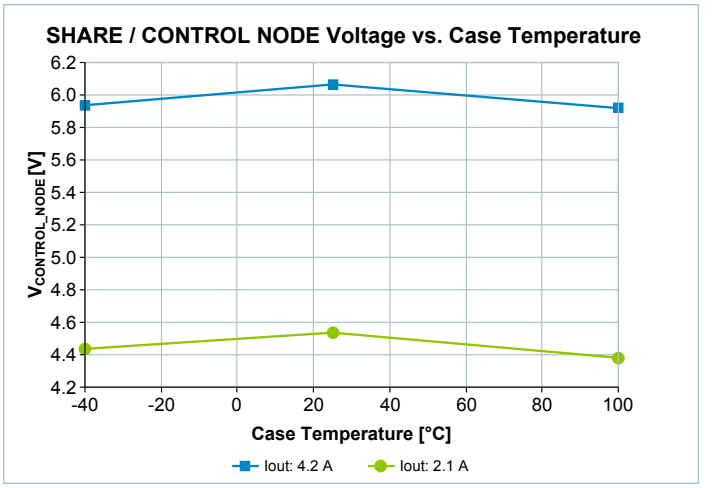


Figure 17 — *Typical SHARE / CONTROL NODE Voltage vs. T_{CASE} and I_{OUT}; V_{IN} = 48.0 V, V_{OUT} = 48.0 V*

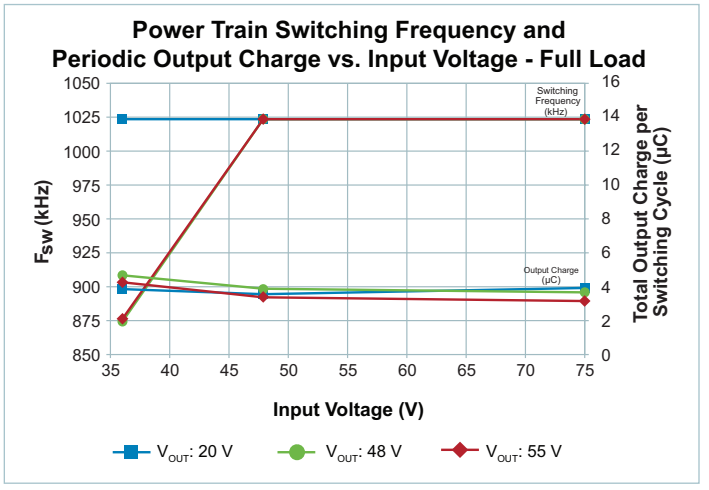


Figure 15 — *Typical Power Train Switching Frequency and Periodic Output Charge vs. V_{IN}, V_{OUT}; I_{OUT} = 4.17 A*

Typical Performance Characteristics (cont.)

The following figures present typical performance at T_C = 25ºC, unless otherwise noted. See associated figures for general trend data.

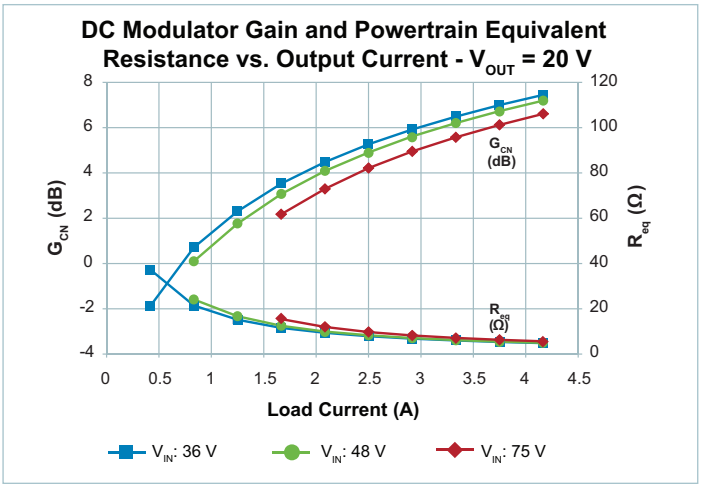


Figure 18 — *Powertrain Characteristics vs. I_{OUT}, V_{IN} Resistive Load, V_{OUT} = 20.0 V*

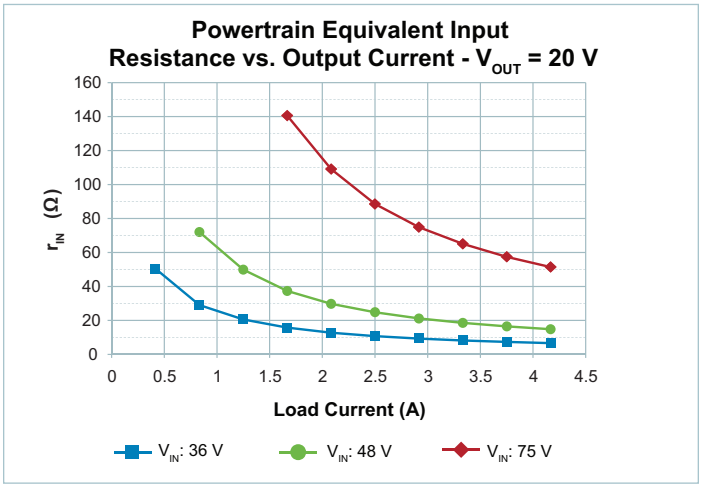


Figure 21 — *Magnitude of powertrain dynamic input impedance vs. I_{OUT}, V_{IN}; V_{OUT} = 20.0 V*

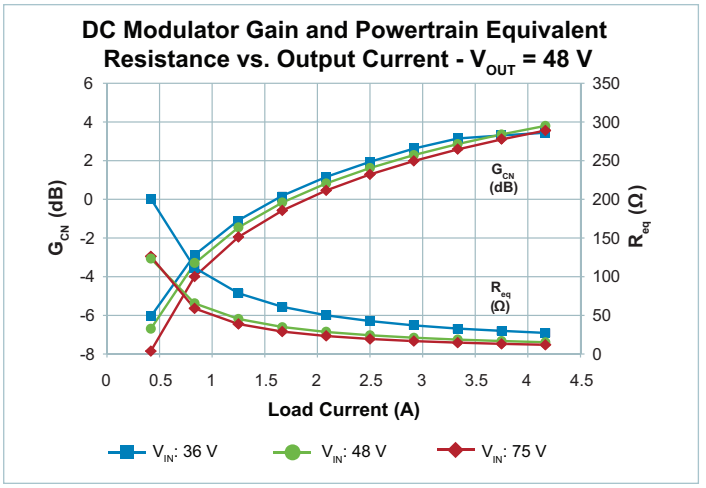


Figure 19 — *Powertrain Characteristics vs. I_{OUT}, V_{IN} Resistive Load, V_{OUT} = 48.0 V*

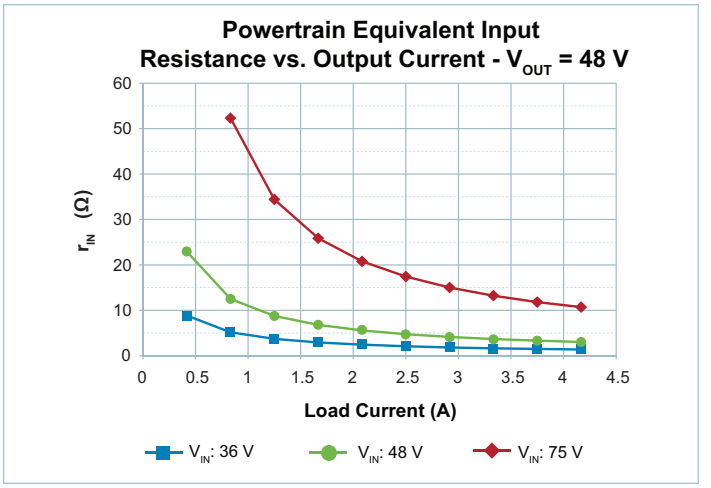


Figure 22 — *Magnitude of powertrain dynamic input impedance vs. I_{OUT}, V_{IN}; V_{OUT} = 48.0 V*

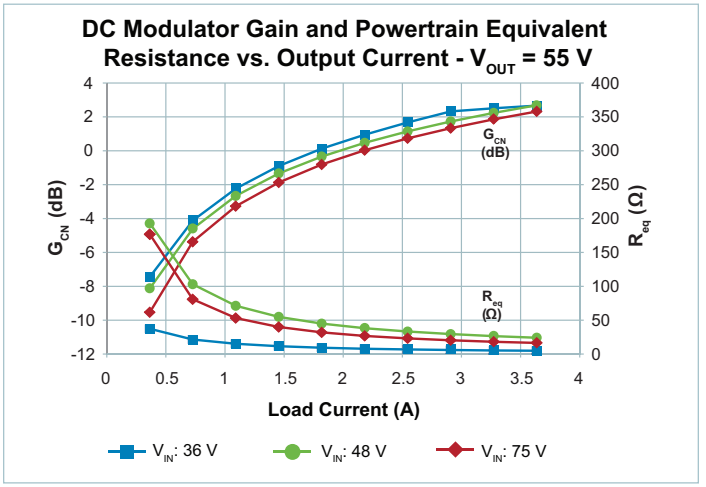


Figure 20 — *Powertrain Characteristics vs. I_{OUT}, V_{IN} Resistive Load, V_{OUT} = 55.0 V*

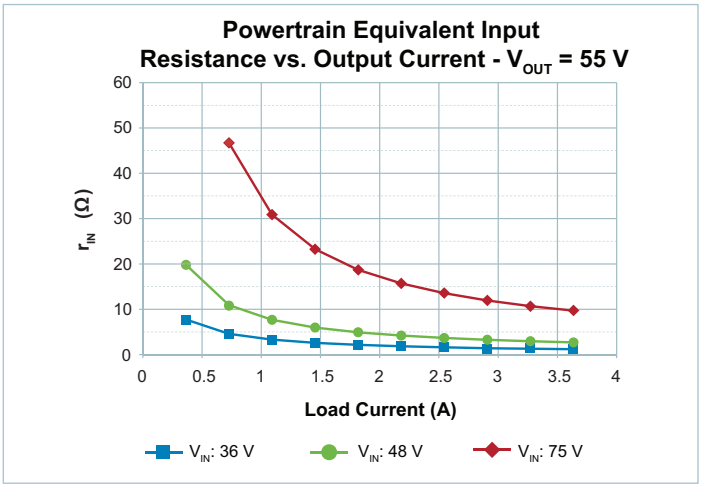


Figure 23 — *Magnitude of powertrain dynamic input impedance vs. I_{OUT}, V_{IN}; V_{OUT} = 55.0 V*

General Characteristics

Specifications apply over all line and load conditions, T_{INT} = 25°C and output voltage from 20.0 V to 55.0 V, unless otherwise noted.
Boldface specifications apply over the temperature range of -40°C < T_{INT} < 125°C (T-grade).

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		**21.8**	**22.0**	**22.3**	mm
			(0.86)	**(0.87)**	**(0.88)**	in
Width	W		**16.3**	**16.5**	**16.8**	mm
			(0.64)	**(0.65)**	**(0.66)**	in
Height	H		**6.48**	**6.73**	**6.98**	mm
			(0.255)	**(0.265)**	**(0.275)**	in
Volume	Vol	No Heatsink		**2.44**		cm^3
				(0.15)		in^3
Weight	W			**7**		g
Lead Finish		Nickel	**0.51**		**2.03**	µm
		Palladium	**0.02**		**0.15**	
		Gold	**0.003**		**0.050**	
Thermal						
Operating Internal Temperature	T_{INT}	T Grade	**-40**		**125**	°C
		M Grade	**-55**		**125**	°C
Thermal Impedance	$\theta_{INT-CASE}$			**2**		°C/W
	$\theta_{INT-LEAD}$			**9**		°C/W
Thermal Capacity				**5**		Ws / °C
Assembly						
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-Lead only			**3**	lbs
					5.3	lbs / in^2
Storage Temperature	T_{ST}	T Grade	**-40**		**125**	°C
		M Grade	**-65**		**125**	°C
ESD Rating	HBM	Method per Human Body Model Test ESDA/JEDEC JDS-001-2012	**CLASS 1C**			V
	CDM	Charged Device Model JESD22-C101E	**CLASS 2**			
Soldering						
Peak Temperature During Reflow		MSL 4 (Datecode 1528 and later)			**245**	°C
Maximum Time Above 217 °C				**60**	**90**	s
Peak Heating Rate During Reflow				**1.5**	**2.0**	°C / s
Peak Cooling Rate Post Reflow				**2.5**	**3.0**	°C / s
Reliability and General Agency Approvals						
MTBF		Telcordia Issue 2 - Method I Case 1; Ground Benign, Controlled		**5.28**		MHrs
		MIL-HDBK-217 Plus Parts Count - 25C Ground Benign, Stationary, Indoors / Computer Profile		**5.29**		MHrs
Agency Approvals / Standards		$_{C}TUV_{US}$				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Pin Functions

+IN, -IN
Input power pins

+OUT, -OUT
Output power pins. Module cannot sink current.

ENABLE
This pin turns the supply on and off. The pin is both an input and an output and can provide the following features:

- Delayed Start: upon application of voltage (>UVLO) to the module power input and after t_{off}, the ENABLE pin will source a constant 90 µA current.
- Output enable: When ENABLE is allowed to pull up above the enable threshold, the ENABLE pin will pull up to 5 V with 1.8 mA source capability, and the module will be enabled.
- Output disable: ENABLE may be pulled down externally in order to disable the module. Pull down resistance should be less than 235 Ω to SGND.
- Fault detection flag: The ENABLE 5 V voltage source is internally turned off when a fault condition is detected.

ENABLE control should be implemented using an open collector configuration. It is not recommended to drive this pin externally.

VAUX: Auxiliary Voltage Source
Use this pin to power external devices with a non-isolated 9 V supply, with up to 5 mA load capability, switched with ENABLE input. Do not place a capacitor over 0.04 µF on this pin.

SGND: Signal Ground
This is a low current pin which provides a Kelvin connection to the PRMs internal signal ground. Use this pin as the ground reference for external circuitry and signals to avoid voltage drops caused by high currents on power returns. In array configurations, SGND pins should be star connected at a single point. A series resistor (~1Ω) to the star location is recommended to decouple return currents.

VC: VTM Control
This output pin is used to temporarily provide VCC voltage to connected VTMs during start up. The pulse is nominally 14 V, 10 ms wide. A VTM can self-power once its input voltage reaches its minimum specified input voltage. The PRM output must be checked to make sure it reaches this threshold voltage before the VC pulse expires.

TRIM
The TRIM pin is used to select the operating mode and to trim the PRM output when Adaptive Loop operating mode is selected. The TRIM pin has an internal pull-up to V_{CC_INT} through a 10 kΩ resistor.

Operating Mode Select:
If TRIM is pulled below 0.45 V during the first startup after V_{IN} is applied, Remote Sense / Child operation is selected. Otherwise, Adaptive Loop operation is selected.
This selection persists until V_{IN} is removed from the part, and is not changed by fault or disable events.

Output Voltage Trim:
Sets the output voltage of the PRM in Adaptive Loop operation.

If TRIM is permitted to pull up to 3.20 V or higher during start up, trim is disabled, and the output is set to the nominal of 48.0 V.

If TRIM is held between 1.00 V to 2.75 V during start up, trim is enabled, and the output is scaled by a factor of 20 resulting in an output voltage range of 20.0 V to 55.0 V.

This selection persists until the PRM is restarted with the ENABLE pin, or due to fault auto-recovery.

AL: Adaptive Loop (Adaptive Loop Operation)
This input pin allows you to set the Adaptive Loop load line. Every volt on this pin represents 1.0 Ω of positive output slope. There is an internal 10 kΩ pullup resistor to V_{CC_INT}. If AL is permitted to pull up to 3.20 V or higher during start up, the Adaptive Loop load line is disabled.

This selection persists until the PRM is restarted with the ENABLE pin, or due to fault auto-recovery.

VT: VTM Temperature (Adaptive Loop Operation)
This pin is used in the Adaptive Loop compensation algorithm to account for the VTM output resistance variation as a function of temperature. The VTM TM pin provides this voltage, scaled as the temperature in K (Kelvin) divided by 100, so 25°C is 2.98 V. Leave disconnected or pull below 1.9 V to disable. The adjustment is fixed at 0.3%/°C relative to the value at 25°C

REF: Reference (Adaptive Loop Operation)
This output pin allows you to monitor the internal reference voltage in Adaptive Loop Operation. During normal operation it represents the output voltage scaled by a factor of 20.

In Adaptive Loop Operation this pin is for monitoring purposes only and should not be driven or loaded externally.

REF_EN: Reference Enable (Remote Sense Operation)
In Remote Sense Operation this pin outputs a regulated 3.25 V, 4 mA voltage source. It is enabled only after successful start up of the PRM powertrain. REF_EN is intended to power the output current transducer and also the voltage reference for the external control loop. Powering the reference generator with REF_EN helps provide a controlled start up, since the output voltage of the system is able to track the reference level as it comes up.

SHARE (Adaptive Loop and Child Operation)
This bus sets the output current level for all the PRM modules when operating in an array (parent-child configuration). Connect them together among the modules in the shared bus. One PRM should be configured as a parent by connecting TRIM for Adaptive Loop Operation. All other PRMs should be configured as children by pulling their respective TRIM pins low. This pin can be used to monitor the error voltage externally. 0 to 100% load is represented by a voltage between 0.79 V and 7.40 V.

CONTROL NODE (Remote Sense Operation)
In Remote Sense Operation, this is the input to the modulator which determines the powertrain timing and ultimately the module output power. An internal 0.5 mA current sink is always active. The bi-directional buffer between CONTROL NODE and the modulator has two states. In normal operation, CONTROL NODE will be above the 0.79 V switching threshold, and will drive the modulator through the buffer. An internal 7.40 V clamp determines the maximum output power that can be requested of the modulator.

When CONTROL NODE falls below 0.79 V, the converter will stop switching. An internal circuit clamps the modulator input to 7.40 V, and a buffer will source up to 2.5 mA out of the pin at that clamp level. For this reason, the output impedance of the amplifier driving CONTROL NODE must be taken into account. A rail-to-rail operational amplifier with low output impedance is always recommended.

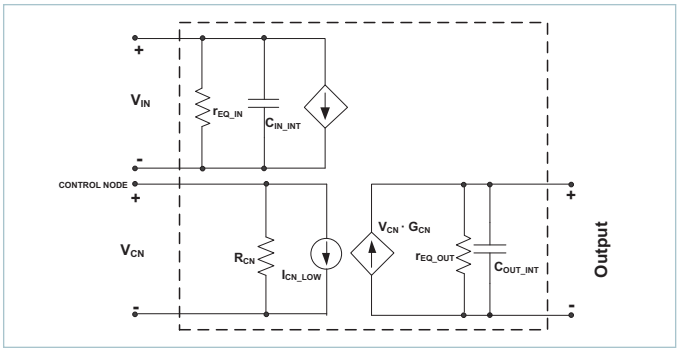


Figure 24 — *PRM48AH480x200A00 AC small signal model*

The powertrain small signal (plant) response consists of a single pole determined by the load resistance, the powertrain equivalent output resistance, and the total output capacitance (internal and external to the module). Both the modulator gain and the equivalent output resistance vary as a function of line, load and output voltage. As the load increases, the powertrain pole moves to higher frequency. As a result, the closed loop crossover frequency will be the highest at full load and lowest at minimum load. Figure 24 shows a reference AC small-signal model.

IFB: Current Feedback (Remote Sense Operation)

In Remote Sense Operation, IFB is the input for the module output overcurrent protection and current limit features. A voltage proportional to the powertrain output current must be applied to IFB in order for overcurrent protection to operate properly.
If the IFB voltage exceeds the IFB pin's overcurrent protection threshold, the powertrain will stop switching. If the IFB voltage falls below the overcurrent protection threshold within t_{BLANK} time, then the powertrain will immediately resume switching. Otherwise a fault is detected.

The current limit threshold for the IFB pin is set lower than the protection threshold. When the IFB pin average voltage exceeds the current limit threshold, an internal integrator will activate a clamp amplifier which overrides the modulator input maximum level. This causes the powertrain to maintain a constant output current.
The bandwidth of this current limit integrator is significantly slower than that of the CONTROL NODE input. Therefore this current limit cannot be used in lieu of properly compensating the (external) control loop to avoid exceeding maximum current or power ratings for the device.

Design Guidelines

The PRM48AH480x200A00 regulator is specifically designed to provide a controlled Factorized Bus distribution voltage for powering downstream VTM Transformer — fast, efficient, isolated, low noise Point-of-Load (POL) converters.

The PRM48AH480x200A00 can be configured for two operating modes depending on the type of regulation required.

In Adaptive Loop Operation the regulation circuitry is enabled within the device and regulates the voltage at the output terminals. The PRM48AH480x200A00 has a programmable Adaptive Loop load line which can be used to compensate for downstream VTM output resistance allowing for precise point of load regulation without the need for remote sensing.

In Remote Sense Operation, the internal regulation circuitry is disabled and the voltage regulation circuitry is provided externally allowing for remote sensing directly at the point of load. In certain applications Remote Sense Operation can improve regulation accuracy, and allow for operating with high amounts of load capacitance and optimizing load transient response.

Operating Mode Selection

The operating mode is selected through use of the TRIM pin.
When the part is first enabled after V_{IN} is applied, the TRIM voltage is sampled. The TRIM pin has an internal pull up resistor to V_{CC_INT}, so unless external circuitry pulls the pin voltage lower, it will float up to V_{CC_INT}.

If TRIM is pulled lower than 0.45 V during the first startup after V_{IN} is applied, the part will be configured for Remote Sense / Child Operation, where the internal voltage regulation circuitry is disabled. In this case, for all subsequent operation the part will output a voltage dependent on the SHARE / CONTROL NODE voltage provided externally (either from an external regulation circuit or parent PRM).

To configure the part for Remote Sense or Child Operation, connect the TRIM pin to SGND. It is recommended to make this connection through a 0 Ω jumper for troubleshooting purposes.

If the sampled TRIM voltage is higher than 0.55 V during the first startup after V_{IN} is applied, then the part will be configured for Adaptive Loop Operation, and the internal voltage regulation circuitry is enabled. The PRM will output a voltage dependent on the TRIM voltage, and will remain in this mode for as long as V_{IN} is applied.

To configure the part for Adaptive Loop Operation, leave the TRIM pin disconnected, or apply a voltage/resistance within the specified range.

The operating mode is detected during the first start up after V_{IN} is applied. This selection persists until V_{IN} is removed from the part, and is not changed by fault or disable events. Changing the operating mode can only be done by removing V_{IN}.

Design Guidelines (Adaptive Loop Operation)

In Adaptive Loop Operation, the internal voltage control circuitry is enabled and the voltage at the output terminals is regulated. The part is nominally set to provide a fixed 48.0 V output, and the TRIM pin can be used to adjust the output over the range of 20.0 V to 55.0 V.

When used with a VTM, the AL pin provides ability to program an Adaptive Loop load line to compensate for the output resistance (R_{OUT}) of a downstream VTM, while the VT pin provides temperature compensation to account for changes in the VTM R_{OUT} over temperature.

Trim Mode and Output Trim Control (Adaptive Loop Operation)

In Adaptive Loop Operation, during any start up and after ENABLE transitions high, the TRIM pin voltage is sampled to determine if trim is active or inactive. If the sampled TRIM voltage is higher than 3.20 V then the PRM will disable trim. In this case, for all subsequent operation the output voltage will be programmed to the nominal output of 48.0 V and the TRIM pin will be ignored during normal operation.

If the sampled TRIM voltage is between 1.00 V and 2.75 V then the PRM will activate trim mode and it will remain in this mode as long as the PRM is operating.

This selection persists until the PRM is restarted with the ENABLE pin, or due to fault auto-recovery.

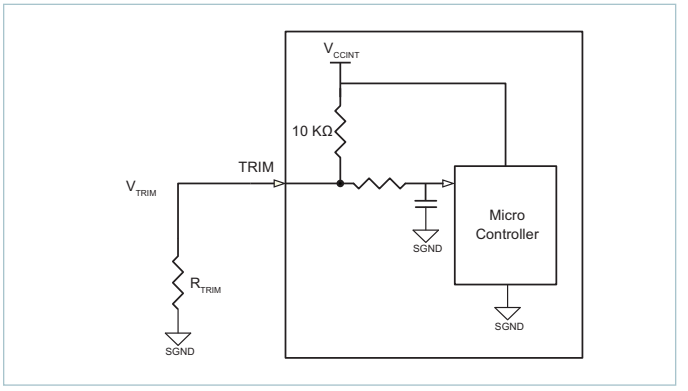


Figure 25 *— TRIM Connection*

The output as a function of V_{TRIM} is defined by equation (1) for 1.00 V ≤ V_{TRIM} ≤ 2.75 V, and allows for an output voltage ranging from 20.0 V to 55.0 V.

The TRIM pin is pulled up internally to V_{CC_INT} thorough a 10 kΩ resistor. V_{TRIM} can be actively set with a DAC that is ground referenced to SGND. V_{TRIM} can be passively set by connecting a resistor, R_{TRIM}, from TRIM to SGND such that the voltage divider made with V_{CC_INT} and the 10 kΩ pull up yields the desired V_{TRIM}. The formula for calculating this resistor is provided in Equation (1a).

$$V_{OUT} = V_{TRIM} \bullet 20 \qquad (1)$$

$$R_{TRIM} = \frac{10\,k\Omega \cdot V_{TRIM}}{V_{CC_INT} - V_{TRIM}} = \frac{10\,k\Omega \cdot V_{OUT_SET}}{20 \cdot V_{CC_INT} - V_{OUT_SET}} \qquad (1a)$$

For 1.00 V≤ V_{TRIM} ≤ 2.75 V where V_{OUT_SET} is the desired output voltage.

The output voltage transfer function saturates for applied TRIM voltages above approximately 2.75 V as illustrated in Figure 26 to prevent the output from being driven above its rated output voltage.

When TRIM is set lower than 1.00 V the output voltage is not specified and stable operation is not guaranteed.

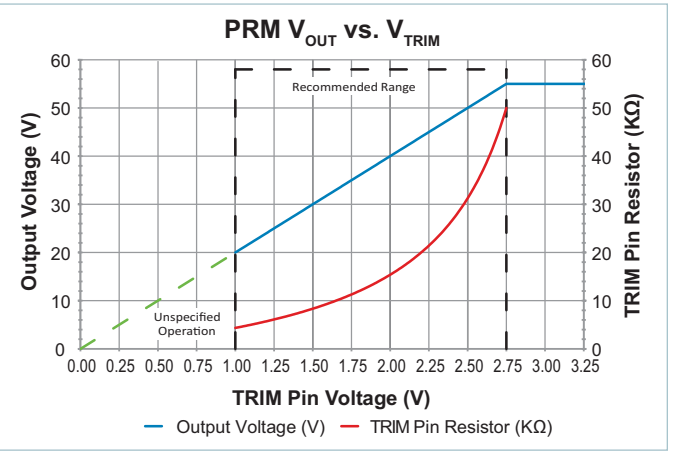


Figure 26 *— PRM V_{OUT} vs. V_{TRIM}*

When trim is enabled the voltage at this pin is sampled at 120 µs intervals to determine the trim level. The output can be dynamically trimmed during normal operation, however it is not recommended to use this pin in an external analog feedback loop.

Refer to Table 1 for a summary of the TRIM pin functionality and the recommended voltage/resistance that should be applied to this pin.

Trim Pin Function Summary				
Operating State		**V_{TRIM}**	**R_{TRIM}**	**Detected and Latched**
Remote Sense / Child Operation		<0.45 V	<1 kΩ	At application of V_{IN} when ENABLE first transitions high
Adaptive Loop Operation		>0.55 V [2]	>3 kΩ [2]	At application of V_{IN} when ENABLE first transitions high
Adaptive Loop Operation Trim Mode	Trim Active V_{OUT} = 20* V_{TRIM}	1.00 V to 2.75 V	4.32 kΩ to 49.9 kΩ	At every start up when ENABLE transitions high
	Trim Inactive V_{OUT} = 48.0 V	>3.20 V	>10 MΩ	

Table 1 *— TRIM Pin Function Summary*

[2] It is not recommended to configure TRIM with a voltage less than 1.00 V in Adaptive Loop Operation

Adaptive Loop Compensation (Adaptive Loop Operation)

A factorized power system naturally has a DC load line associated with it since the regulator stage (PRM) is positioned before the isolation and voltage transformation stage (VTM) Consider for a moment a factorized power system that has the following parameters:

- V_F = 40 V
- K_{VTM}=1/4
- R_{OUT_VTM} =10 mohm @ 25°C

At no load the output voltage at the load will be equal to 10 V ($V_F \bullet K_{VTM}$). With increasing load current, the output voltage at the load will drop at a rate proportional to the VTMs R_{OUT}. It should be noted that the R_{OUT} has a positive temperature coefficient and so the DC load line changes with temperature.

If the presence of this load line is acceptable for your application, then the PRM can be configured by way of the TRIM pin alone. Please refer to the Trimming the Output Voltage section for details. In this case both the AL and VT pins should be left open.

If the presence of this load line is undesirable, the load line can be eliminated by way of the PRMs Adaptive Loop (AL) engine. The AL engine measures the output current of the PRM and accordingly increases the output voltage of the PRM in order to regulate the PRMs output resistance to a fixed negative resistance, R_{LL_AL}, settable by way of the AL pin. R_{LL_AL} should be sized to exactly cancel the R_{OUT} of the VTM at 25°C. The AL engine is also able to account for the positive temperature coefficient of R_{OUT} by way of its VT pin which will be explained shortly.

Setting the Adaptive Loop Load Line (Adaptive Loop Operation)

To determine an appropriate value for the compensation slope (R_{LL_AL}) it helps to reflect the VTM's output resistance to the input side of the VTM. A resistance on the output side of the VTM is scaled by the VTMs transformer ratio (K_{VTM}) squared as defined by equation (2):

$$R_{LLAL} = R_{OUT_REFL} = R_{OUT_VTM_25C} \bullet \left(\frac{1}{K_{VTM}}\right)^2 \qquad (2)$$

Where
R_{OUT_VTM} is the VTM output resistance at 25°C
K_{VTM} is the VTM transformer ratio V_{IN}/V_{OUT}

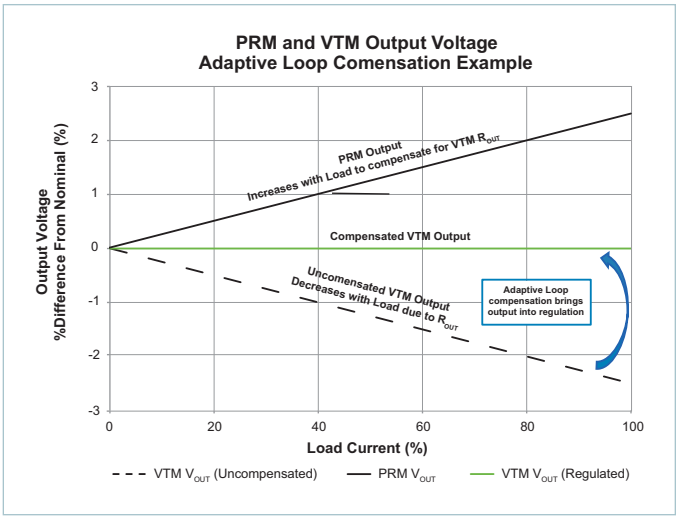


Figure 27 — *Adaptive Loop Compensation Illustration*

For our hypothetical VTM from above (with K_{VTM} = 1/4 and R_{OUT_VTM} = 10 mΩ) the output resistance reflected over to the input would be equal to 160 mΩ. For this example, R_{LL_AL} should be set to -160 mΩ to approximately cancel at 25°C the inherent load line from the VTM.

R_{LL_AL} is set by the voltage difference between the AL pin and SGND pin, V_{AL}, per the following formula:

$$R_{LL_AL} = V_{AL} \bullet (-1.0)\ \Omega/V \qquad (3)$$

$V_{AL} \leq 3.10\ V$
Where V_{AL} is the voltage on the AL pin

V_{AL} is sampled by a 10-bit ADC, whose input is connected to V_{CC_INT} through a 10 kΩ pull up resistor. This pull up disables the AL engine when the AL pin is left open. V_{AL} can be actively set with a DAC that is ground referenced to SGND. V_{AL} can be passively set by connecting a resistor, R_{AL}, from AL to SGND such that the voltage divider made with V_{CC_INT} and the 10 kΩ pull up yields the desired V_{AL}. The formula for calculating this resistor is provided in Equation (4).

$$R_{AL} = \frac{10\ k\Omega \cdot V_{AL}}{V_{CC_INT} - V_{AL}} \qquad (4)$$

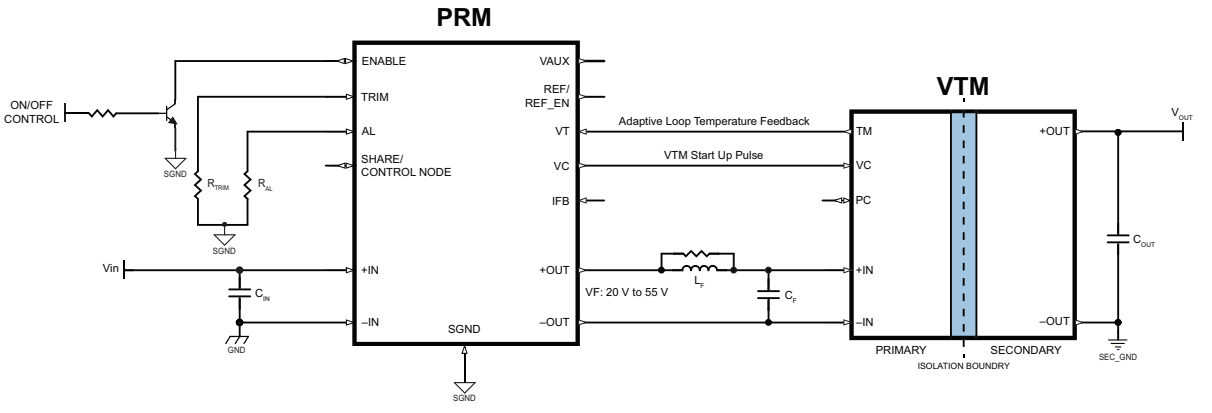


Figure 28 — *PRM-VTM Adaptive Loop Example*

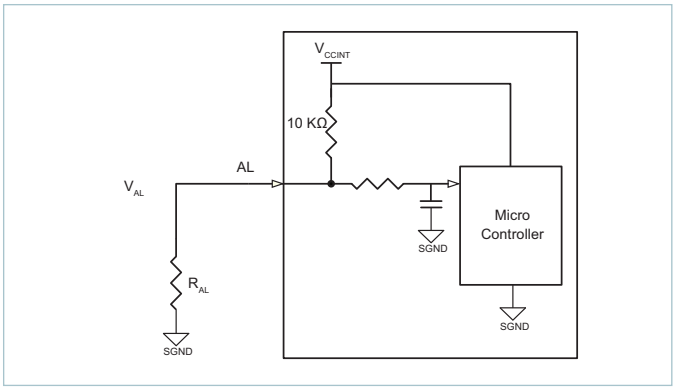


Figure 29 — *AL Connections*

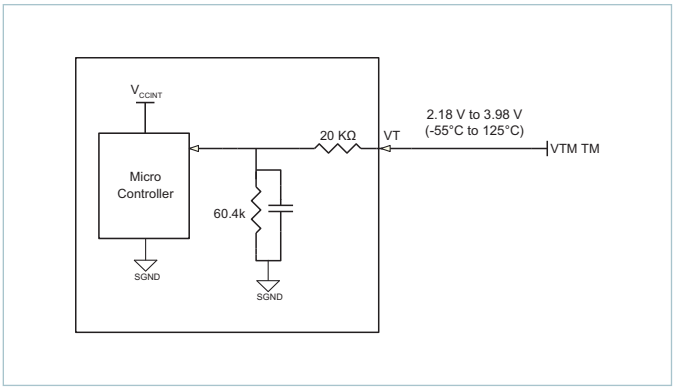


Figure 30 — *VT Connections*

Similar to TRIM, AL is sampled during every start up to determine if the Adaptive Loop load line is enabled or disabled. If the AL pin is allowed to pull up to 3.20 V or higher during start up, then the PRM will disable the Adaptive Loop load line as long as the PRM remains operating. In this case, for all subsequent operation the output voltage will be remain at the set voltage, and the AL pin will be ignored.

This selection persists until the PRM is restarted with the ENABLE pin, or due to fault auto-recovery. When AL is enabled, the voltage at this pin is sampled at 120 µs intervals to determine the load line. The load line can be adjusted during normal operation, however it is not recommended to use this pin in an external analog feedback loop.

Adaptive Loop Temperature Compensation (Adaptive Loop Operation)

By connecting the VT pin of the PRM to the VTM's TM pin, the PRM is able to monitor the internal temperature of the VTM. Knowing the VTM's internal temperature and the temperature coefficient of the VTM's R_{OUT}, which is preprogrammed into the PRMs microcontroller, the AL engine is able to scale the nominal value of R_{LL_AL} (set by the AL pin) to track the VTM's R_{OUT} over temperature. In this way the output resistance of the PRM can be tuned to cancel the output resistance of the VTM with the addition of a single resistor across the AL pin and a connection of the VTM's TM pin to the PRMs VT pin.

The VTM TM voltage is equal to the VTM internal sensed temperature in Kelvin divided by 100. For a temperature range of -55°C to 125°C the TM voltage will range from 2.18 V to 3.98 V. The Adaptive Loop temperature compensation is pre-programed into the internal microcontroller and is 0.3%/°C assuming the VT pin is connected to the TM pin of a compatible VTM.

The TM pin has an internal pull down to SGND, and temperature compensation is disabled for VT voltages less than 1.9 V. To disable temperature compensation, leave the VT pin unconnected and open circuit. When disabled, the temperature defaults 25°C.

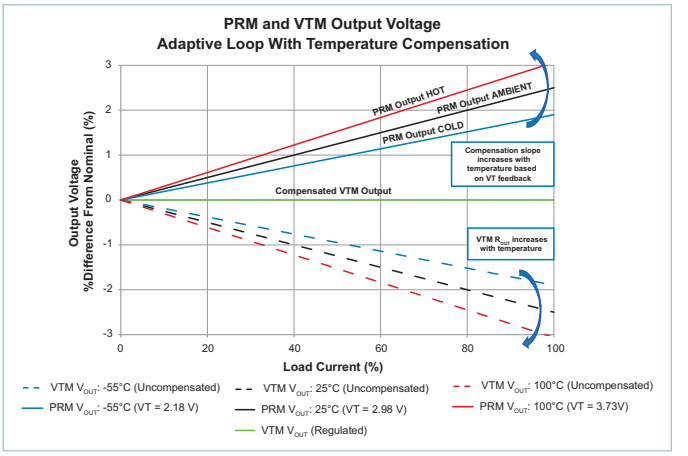


Figure 31 — *Adaptive Loop Temperature Compensation Illustration*

The discussion thus far only considered the case where the AL engine is used to compensate for the R_{OUT} of the VTM. The AL engine can be more generally used to account for distribution resistances in both the factorized bus and the VTM's output distribution bus. For more information on how to apply the AL engine towards this end please contact Vicor's Applications Engineering department.

Stability Considerations and External Capacitance (Adaptive Loop Operation)

In Adaptive Loop Operation, the internal voltage regulation is enabled which has a pre-determined, fixed compensation network. The compensation is designed to be stable over a fixed set of operating and load conditions including load capacitance.

Besides internal output capacitors, external output capacitors also contribute to the closed loop frequency response, thus should be identified and understood, in order to maintain the control loop stability. This includes capacitance placed directly on the PRM output, as well as capacitance on the output of any downstream VTM (if used) reflected to its input.

Figure 32 illustrates the requirements for external capacitors for both the capacitance and ESR value. As shown in Figure 32 (a), the maximum capacitance value of ceramic capacitor is 25 µF, and the capacitance of a combination of ceramic and electrotype capacitors needs to be less than 47 µF. As shown in Figure 32 (b) and (c), the ESR value of electrotype capacitors needs to be between 0.1 Ω and 1 Ω; the ESR value of ceramic capacitors needs to be between 2 mΩ and 200 mΩ.

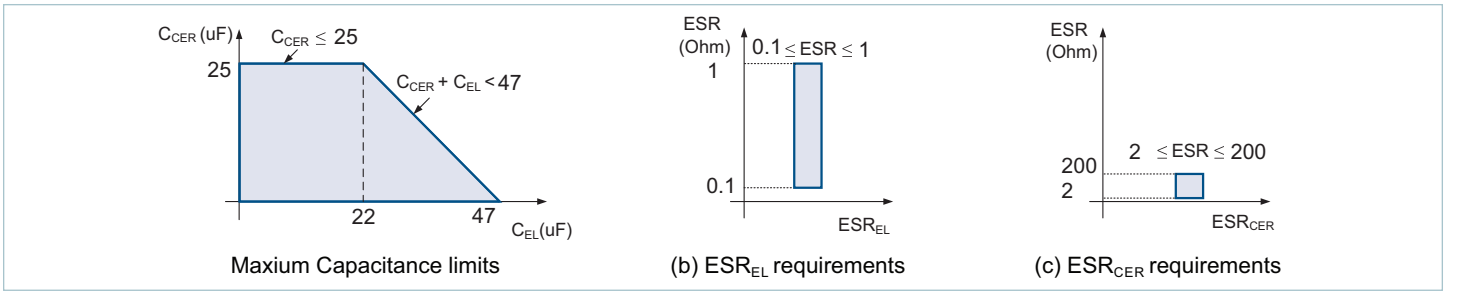


Figure 32 — *Output Capacitance Limits*

Current Limit (Adaptive Loop Operation)

In Adaptive Loop Operation, the current limit is controlled by the internal microcontroller. The current limit approximates a "brick-wall" limit where the output current is prevented from crossing the current limit threshold by reducing the output voltage. The current limit threshold is pre-programmed into the internal microcontroller and cannot be changed externally.

When the internal sensed current crosses the current limit threshold, the current limit will be activated after the detection time t_{LIM_SUPV}. Once activated, the microcontroller will reduce the error amplifier reference voltage(represented by REF) in order to maintain the output current at the limit value. Current limit is able to reduce the output down to V_{OUT_UVP}, below which the device will shut down do to output under voltage protection.

Soft Start Timing and Start up (Adaptive Loop Operation)

In Adaptive Loop Operation, the PRM has an internal soft start sequence which is initiated at every start up. This allows the PRM to start into fully discharged load capacitance. The soft start sequence ramps the output by modulating the error amplifier reference voltage (REF). The result is that the PRM output will rise at a controlled rate until the final voltage setpoint is reached. The total ramp time is typically 1.8 ms independent of the output trim level. This soft start ramp time is preprogrammed into the microcontroller and cannot be changed externally.

Load Transient Response (Adaptive Loop Operation)

In Adaptive Loop Operation, response time is dependent on the internal compensation. When the Adaptive Loop load line is disabled, the PRM output voltage will recover to the initial set value as illustrated in Figure 33 and Figure 34.

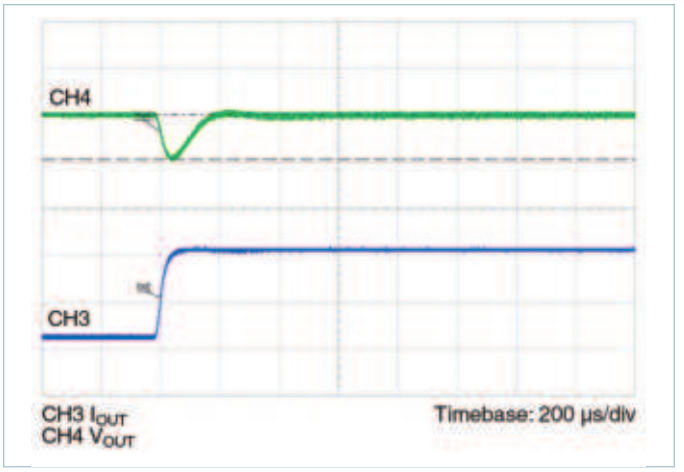


Figure 33 — *PRM Example 10% to 100% Load Transient Response, Adaptive Loop Load Line Disabled*

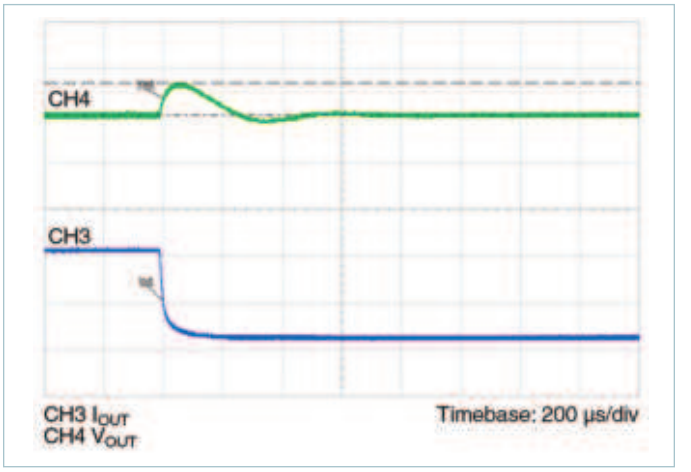


Figure 34 — *PRM Example 100% to 10% Load Transient Response, Adaptive Loop Load Line Disabled*

When the Adaptive Loop load line is enabled, the voltage will recover to the value determined by the set point and Adaptive Loop load line settings as illustrated in Figure 35.

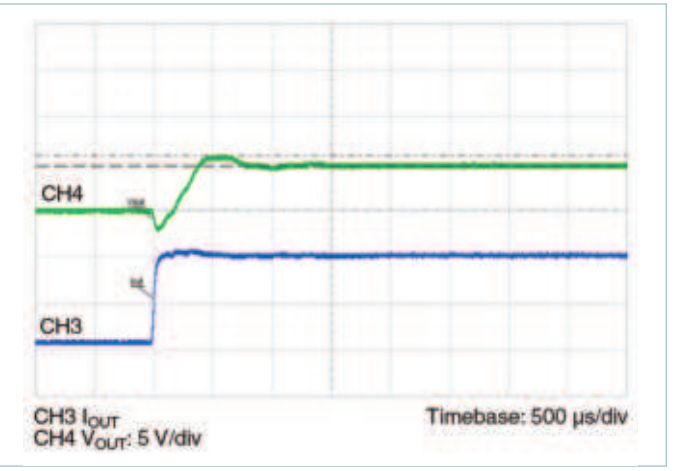


Figure 35 — *PRM Example 10% to 100% Load Transient Response, Adaptive Loop Load Line Enabled, V_{AL} = 1.20 V*

Actual response times are model dependent and will change based on the load step magnitude, load capacitance and operating conditions.

Because the compensation is fixed internally the load transient response cannot be altered for Adaptive Loop Operation.
In order to improve the load transient response performance, the part can be configured for Remote Sense Operation with an external voltage control loop optimized for the specific intended operating conditions. Remote Sense Operation is described in the next section.

Arrays (Adaptive Loop Operation)

In Adaptive Loop operation a parent-child configuration is used for arrays. Up to 5 PRMs of the same type may be placed in parallel to expand the power capacity of the system.

One PRM is designated as the parent and contains the active control loop which considers control pin inputs and drives SHARE. The other PRMs listen to SHARE and act as child powertrains only. The following high-level guidelines must be followed in order for the resultant system to start up and operate properly, and to avoid overstress or exceeding any absolute maximum ratings.

- One PRM must be designated as a parent through configuring the TRIM pin voltage within the recommended range.
- All other PRMs must be designated as child PRMs by tying TRIM pins to SGND. It is recommended to make this connection through a 0 Ω jumper for troubleshooting purposes.
- All PRMs in the array must be powered from a common power source so that the input voltage to each PRM is the same. The IN pins of all PRMs must be connected together.
- An independent fuse for each PRM +IN connection is required to maintain safety certifications (see Fusing section).
- An independent inductor for each PRM +IN connection is recommended when used in an array, to control circulating currents among the PRM inputs and reduce the impact of beat frequencies.
- Mismatches in both inductance, and resistance from the common power source to each PRM should be minimized.
- ENABLE pins must be connected together for start up synchronization and proper fault response of the array.
- SHARE pins must be connected together to enable sharing. The bandwidth requirements of SHARE are low enough that the bus can be considered a lumped element, rather than a transmission line, and so star connections to the parent PRM with stubs, as well as daisy chain connections are permitted.
- The resistances between child unit SHARE pins and the parent's should be well matched, to avoid introducing additional sharing mismatches. The SHARE bus should not be routed under any PRM. SHARE bus parasitic capacitance to +IN or +OUT should be minimized.
- SGND of the parent PRM is the reference for all control loop functions. The SGND pins of each child PRMs should be connected to the SGND reference node on the board through a 1 Ω resistor.
- When operating within an array, the parent PRM is rated for full power while the child PRMs are de-rated to the array rated power and current values provided for Child Operation (P_{OUT_ARRAY},I_{OUT_ARRAY}). The number of PRMs required to achieve a given array capacity must consider these de-ratings to avoid overstressing any PRM in the array.
- Adaptive Loop design procedures above will hold for an array, in general, although some parameters must be scaled against the number of PRMs in the system.

Arrays of more than 5 PRMs may be possible through use of external circuitry. Please contact Vicor Applications for assistance with array sizing above 5 units.

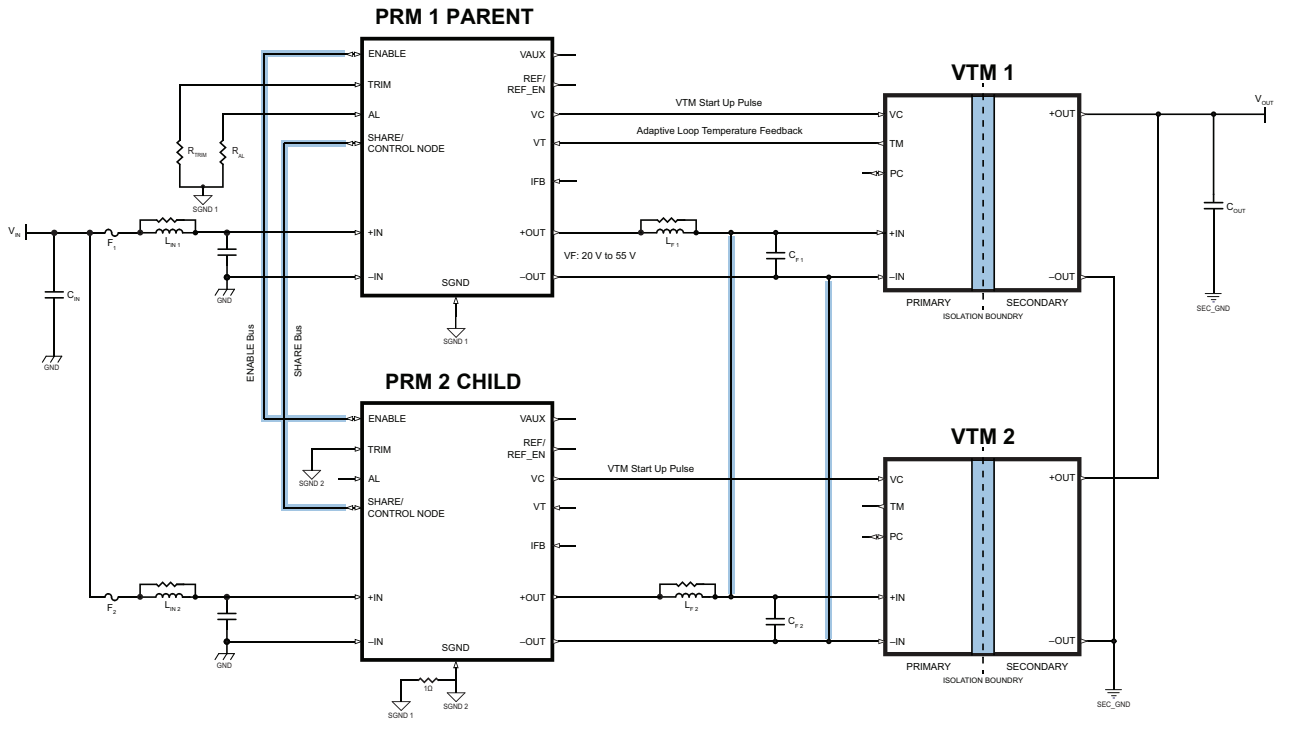


Figure 36 — *Adaptive Loop Array Example*

Design Guidelines (Remote Sense Operation)

In Remote Sense Operation, the PRM48AH480x200A00 is an intelligent powertrain module designed to fully exploit external output voltage feedback and current sensing sub-circuits. These two external circuits are illustrated in Figure 36, which shows an example of the PRM in a standalone application with local voltage feedback and high side current sensing.
In general, these circuits include a precision voltage reference, an operational amplifier which provides closed loop feedback compensation, and a high side current sense circuit which includes a shunt and current sense IC.

The following design procedures refer to the circuit shown in Figure 36.

Setting the Output Voltage Level (Remote Sense Operation)

The output voltage setpoint is a function of the voltage reference and the output voltage sense ratio. With reference to Figure 36, R1 and R2 form the output voltage sensing divider which provides the scaled output voltage to the negative input of the error amplifier; a dedicated reference IC provides the reference voltage to the positive input of the error amplifier. Under normal operation, the error amplifier will keep the voltages at the inverting and non-inverting inputs equal, and therefore the output voltage is defined by:

$$V_{OUT} = V_{REF} \cdot \frac{R1 + R2}{R2} \qquad (5)$$

Note that the component R1 will also factor into the compensation as described in a later section.

It is important to apply proper slew rate to the reference voltage rise when the control loop is initially enabled. The recommended range for reference rise time is 1 ms to 9 ms. The lower rise time limit will ensure optimized modulator timing performance during start up, and to allow the current limit feature (through IFB pin) to fully protect the device during power-up. The upper rise time limit is needed to guarantee a sufficient factorized bus voltage is provided to any downstream VTM input before the end of the VC pulse.

Setting the Output Current Limit and Overcurrent Protection Level (Remote Sense Operation)

In Remote Sense Operation, the internal current sensing is disabled, and an external current sense amplifier must be implemented to provide feedback to the IFB pin.

The current limit and overcurrent protection set points are linked, and scale together against the current sense shunt, and the gain of the current sense amplifier. The output of the current sense IC provides the IFB voltage which has V_{IFB_IL} and V_{IFB_OC} thresholds for the two functions respectively. The set points are therefore defined by:

$$I_{IL} = \frac{V_{IFB_IL}}{R_S \cdot G_{CS}} \qquad (6)$$

and

$$I_{OC} = \frac{V_{IFB_OC}}{R_S \cdot G_{CS}} \qquad (7)$$

where G_{CS} is the gain of the current sense amplifier.

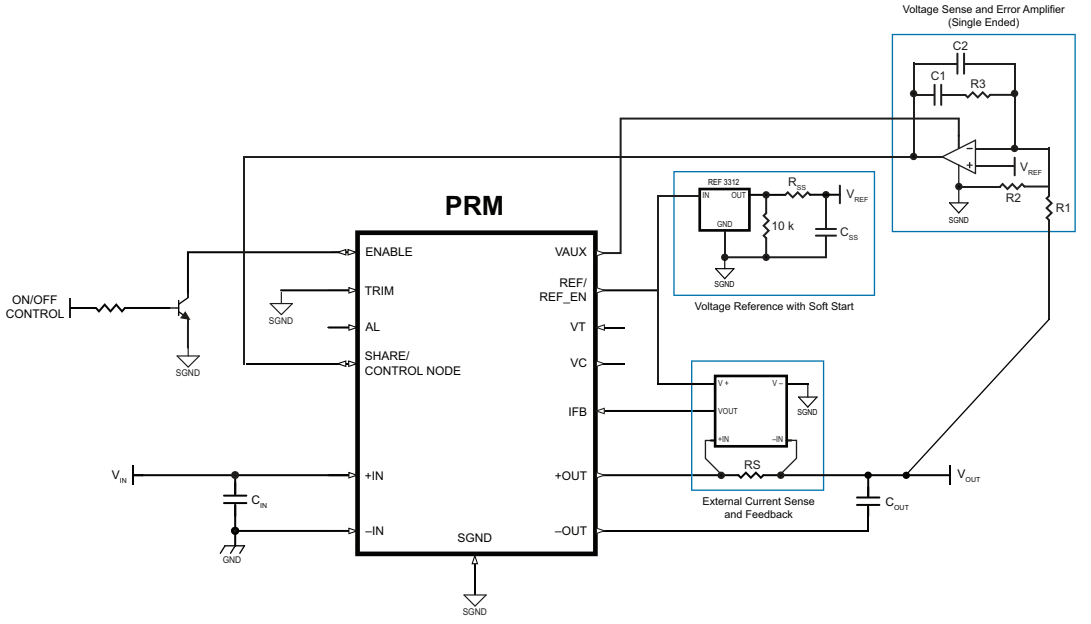


Figure 37 — *Remote Sense Example*

Control Loop Compensation Requirements (Remote Sense Operation)

In order to properly compensate the control loop, all components which contribute to the closed loop frequency response should be identified and understood. Figure 24 shows the AC small signal model for the module. Modulator DC gain G_{CN} and powertrain equivalent resistance r_{EQ_OUT} are shown. These modeling parameters will support a design cut-off frequency up to 50kHz.

Standard Bode analysis should be used for calculating the error amplifier compensation and analyzing the closed loop stability. The recommended stability criteria are as follows:

1) Phase Margin > 45º: for the closed loop response, the phase should be greater than 45º where the gain crosses 0 dB.

2) Gain Margin > 10dB : The closed loop gain should be lower than -10dB where the phase crosses 0º.

3) Gain Slope = -20dB/decade : The closed loop gain should have a slope of -20dB/decade at the crossover frequency.

The compensation characteristics must be selected to meet these stability criteria. Refer to Figure 37 for a local sense, voltage-mode control example based on the configuration in Figure 36. In this example, it is assumed that the maximum crossover frequency (F_{CMAX}) has been selected to occur between B and C. Type-2 compensation (Curve IJKL) is sufficient in this case.

The following data must be gathered in order to proceed:

- Modulator Gain G_{CN}: See Figures 18, 19, 20
- Powertrain equivalent resistance r_{EQ}: See Figures 18, 19, 20
- Internal output capacitance: see Figure 13
- External output capacitance value

In the case of ceramic capacitors, the ESR can be considered low enough to push the associated zero well above the frequency of interest. Applications with high ESR capacitor may require a different type of compensation, or cascade control.

The system poles and zeros of the closed loop can then be defined as follows:

- Powertrain pole, assuming the external capacitor ESR can be neglected:

$$R_{C_{OUT_EXT}} << \frac{r_{EQ_OUT} \cdot R_{LOAD}}{r_{EQ_OUT} + R_{LOAD}}$$

- Main pole frequency:

$$F_P \approx \frac{1}{2\pi \cdot \frac{r_{EQ_OUT} \cdot R_{LOAD}}{r_{EQ_OUT} + R_{LOAD}} \cdot (C_{OUT_INT} + C_{OUT_EXT})}$$

- Compensation Mid-Band Gain:

$$G_{MB} = 20 \log \frac{R_3}{R_1} \quad (8)$$

- Compensation Zero:

$$F_{Z1} = \frac{1}{2\pi \cdot R_3 \cdot C_1} \quad (9)$$

- Compensation Pole:

$$F_{P2} = \frac{1}{2\pi \cdot \frac{R_3 \cdot C_1 \cdot C_2}{C_1 + C_2}}$$

and for $F_{P2} >> F_{Z1}$ ($C_1 + C_2 \approx C_1$):

$$F_{P2} \approx \frac{1}{2\pi \cdot R_3 \cdot C_2} \quad (10)$$

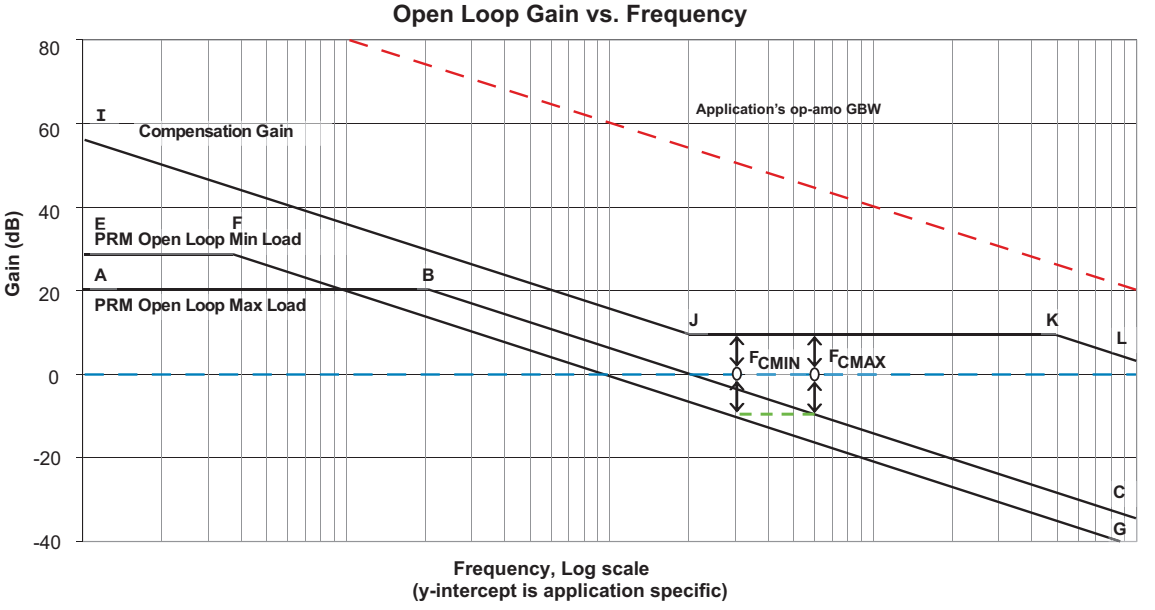


Figure 38 — *Reference asymptotic Bode plot for the considered system*

Midband Gain Design: R1, R3 (Remote Sense Operation)
With reference to Figure 37: curve ABC is the:

- minimum output voltage in the application
- maximum input voltage expected in the application
- maximum load

PRM open loop response, and is where the maximum crossover frequency occurs. In order for the maximum crossover frequency to occur at the design choice F_{CMAX}, the compensation gain must be equal and opposite of the powertrain gain at this frequency. For stability purposes, the compensation should be in the Mid-band (J-K) at the crossover. Using Equation (8), the mid-band gain can be selected appropriately.

Compensation Zero Design :C1 (Remote Sense Operation)
With reference to Figure 37: curve EFG is the:

- maximum output voltage in the application
- minimum input voltage expected in the application
- minimum load in the application

PRM open loop response, and is where the minimum crossover frequency F_{CMIN} occurs. Based on stability criteria, the compensation must be in the mid-band at the minimum crossover frequency, therefore F_{CMIN} will occur where EFG is equal and opposite of G_{MB}. C1 can be selected using Equation (9) so that F_{Z1} occurs prior to F_{CMIN}.

High Frequency Pole Design: C2 (Remote Sense Operation):
Using Equation (10), C2 should be selected so that F_{P2} is at least one decade above F_{CMAX} and prior to the gain bandwidth product of the operational amplifier (10MHz for this example). For applications with a higher desired crossover frequency the use of a high gain bandwidth product amplifier may be necessary to ensure that the real pole can be set at least one decade above the maximum crossover frequency.

Arrays (Remote Sense Operation)

In Remote Sense Operation up to 10 PRMs of the same type may be placed in parallel to expand the power capacity of the system. All PRMs within the array are configured for Remote Sense Operation and are driven by an external control circuit which considers the control inputs and drives the CONTROL NODE bus. The following high-level guidelines must be followed in order for the resultant system to start up and operate properly, and to avoid overstress or exceeding any absolute maximum ratings.

- All PRMs must be configured for Remote Sense Operation by tying TRIM pins to SGND. It is recommended to make this connection through a 0 Ω jumper for troubleshooting purposes.
- All PRMs in the array must be powered from a common power source so that the input voltage to each PRM is the same.
- An independent fuse for each PRM +IN connection is required to maintain safety certifications (see Fusing section).
- An independent inductor for each PRM +IN connection is recommended when used in an array, to control circulating currents among the PRM inputs and reduce the impact of beat frequencies.
- Mismatches in both inductance, and resistance from the common power source to each PRM should be minimized.
- ENABLE pins must be connected together for start up synchronization and proper fault response of the array.
- Reference supply to the control loop voltage reference and current sense circuitry must be enabled when all modules' R_{EF_EN} pins have reached their operational voltage levels.
- A single external control circuit must be implemented as described in the Remote Sense Operation design guidelines. The control circuit should drive the CONTROL NODE bus.
- CONTROL NODE pins must be connected together to enable sharing. The bandwidth requirements of CONTROL NODE are low enough that the bus can be considered a lumped element, rather than a transmission line, and so star connections as well as daisy chain connections are permitted.
- Each PRM must have its own local current shunt and current sense circuitry to drive its IFB pin.
- The resistances between CONTROL NODE pins should be well matched, to avoid introducing additional sharing mismatches. The CONTROL NODE bus should not be routed under any PRM. Parasitic capacitance to +IN or +OUT should be minimized.
- One PRM should be designated to provide the SGND reference, VAUX, and REF_EN voltages for the external circuitry.
- The SGND pins of each PRM should be connected to the SGND reference node on the board through a 1 Ω resistor.
- When operating within an array, the PRMs are de-rated to the array rated power and current values provided for Remote Sense Operation (P_{OUT_ARRAY}, I_{OUT_ARRAY}). The number of PRMs required to achieve a given array capacity must consider these de-ratings to avoid overstressing any PRM in the array.
- When using VAUX to power external circuitry, total current draw including CONTROL NODE sink currents must be taken into account to ensure the maximum VAUX current is not exceeded. Arrays of more than 5 PRMs may require additional circuitry to provide the required source current. Contact Vicor Applications Engineering for more information.

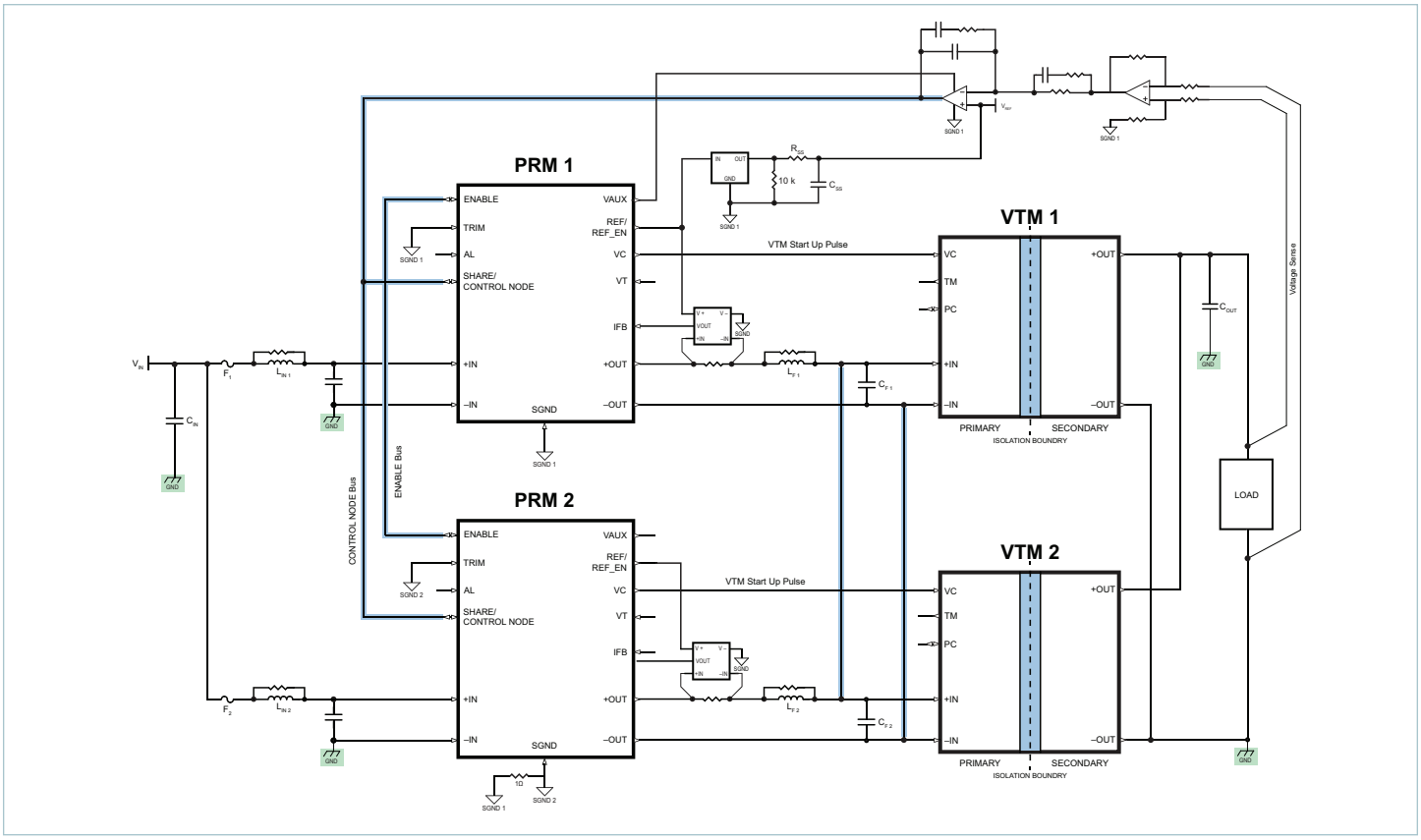


Figure 39 — *Non-Isolated Remote Sense Array Example*

[1] Non-Isolated Configuration: –Out connected to -IN

DESIGN GUIDELINES (General Operation)

The following guidelines are general guidelines that apply to any mode of operation.

FPA System Considerations

There are a few system level design considerations that should be carefully considered when using a PRM and VTM to implement a Factorized Power Architecture (FPA) system

The VC pin of the PRM should be directly connected to the VC pin of the VTM. The PRM and VTM coordinate the soft start sequence of the FPA system through this connection. If the VC pins are not connected the VTM will not start up. When the PRM is ready to start up, it applies a voltage on VC, which enables and powers the VTM's powertrain. The PRM then proceeds to ramp up its output voltage. After approximately 10 ms, VC returns to 0 V and the VTM can then derive power directly from the factorized bus provided that the factorized bus voltage is above the minimum specified VTM operating input voltage when the VC pulse expires.

All VTM faults latch the VTM powertrain off. Input power to the system as a whole must be recycled or the PRM should be disabled and enabled by way of its ENABLE pin in order to restart the system. It is recommended that the voltage on the factorized bus return to zero before the PRM is re-enabled. Otherwise the soft start of the system may be compromised.

A RL filter should be placed between the PRM and VTM to locally isolate switching ripple currents that can interfere with module operation. It is important that the inductance have an impedance that is much greater than that of the PRM output capacitance and VTM input capacitance at the switching frequencies of the devices. A resistor should be placed in shunt to this inductor to dampen the resultant LC tank. For most cases 100 nH in parallel with 1 Ω is sufficient to isolate the switching ripple currents.

Verifying Stability

A load step transient response can be used in order to estimate stability.

Figure 38 illustrates an example of a load step response. Equation (11) can be used to predict the phase margin based on the ratio of the "kick" to "droop" (as defined in Fig. 38).

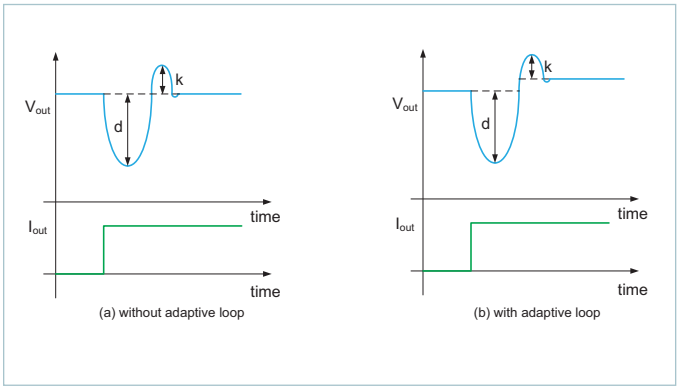


Figure 40 *— Load step response example and "droop" vs. "kick" (a) without Adaptive Loop; (b) with Adaptive Loop.*

$$\Phi_m \approx 100 \sqrt{\frac{\left(\ln\frac{k}{d}\right)^2}{\left(\ln\frac{k}{d}\right)^2 + \pi^2}} \qquad (11)$$

Burst Mode Operation

At light loads, the PRM will operate in a burst mode due to minimum timing constraints. An example burst operation waveform is illustrated in Figure 39.

For very light loads, and also for higher input voltages, the minimum time power switching cycle from the powertrain will exceed the power required by the load. In this case the error amplifier will periodically drive SHARE/CONROL NODE below the switching threshold in order to maintain regulation. Switching will cease momentarily until the error amplifier once again drives SHARE/CONTROL NODE voltage above the threshold.

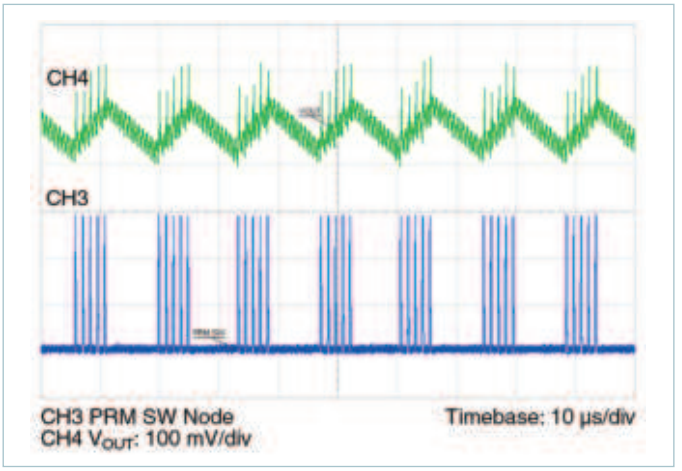


Figure 41 *— Light load burst mode of operation*

Note that during the bursts of switching, the powertrain frequency is constant, but the number of pulses as well as the time between bursts is variable. The variability depends on many factors including input voltage, output voltages, load impedance, and error amplifier output impedance.

In burst mode, the gain of the SHARE/CONTROL NODE input to the plant which is modeled in the previous sections is time varying. Therefore the small signal analysis cannot be directly applied to burst mode operation.

Input and Output filter design

Figures 14 and 15 provide the total input and output charge per cycle, as well as switching frequency, of the PRM at full load under various input and output voltages conditions.
Figure 13 provides the effective internal capacitance of the module.
A conservative estimate of input and output peak-peak voltage ripple at nominal line and trim is provided by equation (12):

$$\Delta V = \frac{Q_{TOT} - \frac{I_{FL} \cdot 0.4}{f_{SW}}}{C_{INT} + C_{EXT}} \qquad (12)$$

Q_{TOT} is the total input (Fig. 14) or output (Fig. 15) charge per switching cycle at full load, while C_{INT} is the module internal effective capacitance at the considered voltage (Fig. 13) and C_{EXT} is the external effective capacitance at the considered voltage.

Input Filter Stability

The PRM can provide very high dynamic transients. It is therefore very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate. For this purpose, the converter dynamic input impedance magnitude $|r_{EQ_IN}|$ is provided in Figures 21, 22, 23. It is recommended to provide adequate design margin with respect to the stability conditions illustrated in the previous sections.

Inductive source and local, external input decoupling capacitance with negligible ESR (i.e.: ceramic type)

The voltage source impedance can be modeled as a series R_{LINE} L_{LINE} circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(C_{IN_INT} + C_{IN_EXT}) \cdot |r_{EQ_IN}|} \qquad (13)$$

$$R_{line} << |r_{EQ_IN}| \qquad (14)$$

It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, 14. However, R_{LINE} cannot be made arbitrarily low otherwise equation 13 is violated and the system will show instability, due to under-damped RLC input network.

Inductive source and local, external input decoupling capacitance with significant R_{CIN_EXT} ESR (i.e.: electrolytic type)

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor L_{line}. Notice that the high performance ceramic capacitors C_{IN_INT} within the PRM, should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

$$|r_{EQ_IN}| > R_{C_{IN_EXT}} \qquad (15)$$

$$\frac{L_{line}}{C_{IN_EXT} \cdot R_{C_{IN_EXT}}} < |r_{EQ_IN}| \qquad (16)$$

Equation 16 shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. Again, an octave of design margin in satisfying 15 should be considered the minimum.

Layout Considerations

Application Note AN:005 details board layout recommendations using VI Chip® components, with details on good power connections, reducing EMI, and shielding of control signals and techniques to reference them to SGND.

Avoid routing control signals (ENABLE, TRIM, AL etc.) directly underneath the PRM. It is critical that all control signals (aside from VC and VT) are referenced to SGND, both for routing and for pull-down and bypassing purposes. VC and VT provide control and feedback from a VTM, and must be referenced to –OUT of the PRM (-IN of the VTM).

SGND is connected to –IN internally to the PRM. SGND should not be tied to any other ground in the system.

Input Fuse Recommendations

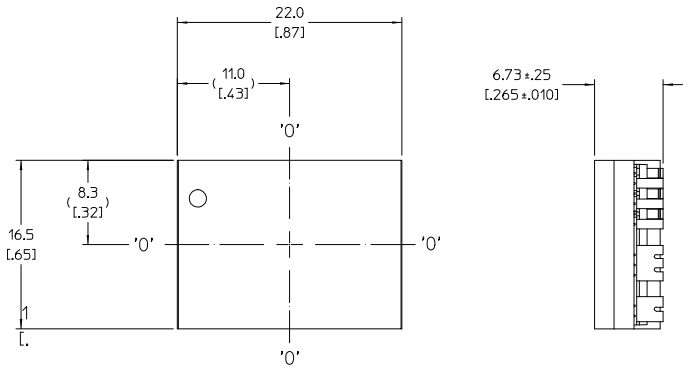
A fuse should be incorporated at the input to each PRM, in series with the +IN pin. A 10 A or smaller input fuse (Littelfuse® NANO2® 451/453 Series) is required to safety agency conditions of acceptability. Always ascertain and observe the safety, regulatory, or other agency specifications that apply to your specific application.

Thermal Considerations

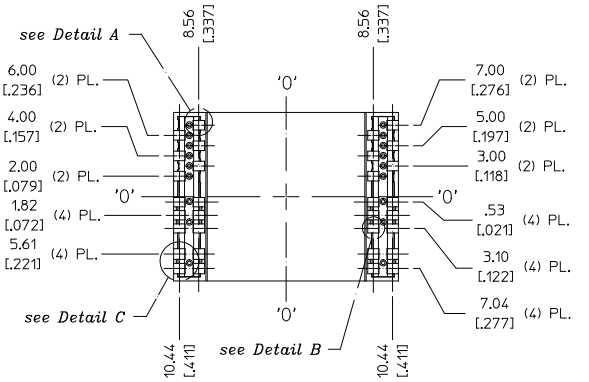
VIChip products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the PRM48AH480x200A00 case to less than 100ºC will keep all junctions within the VI Chip module below 125ºC for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

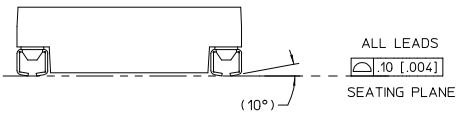
Product Outline Drawing and Recommended Land Pattern

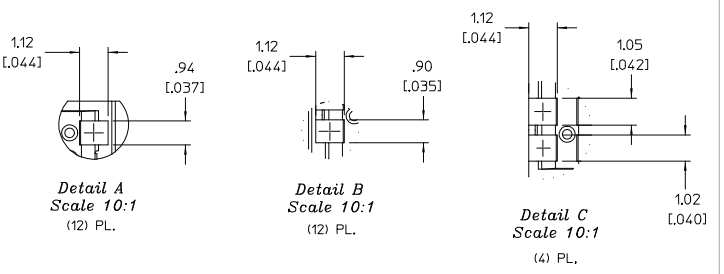


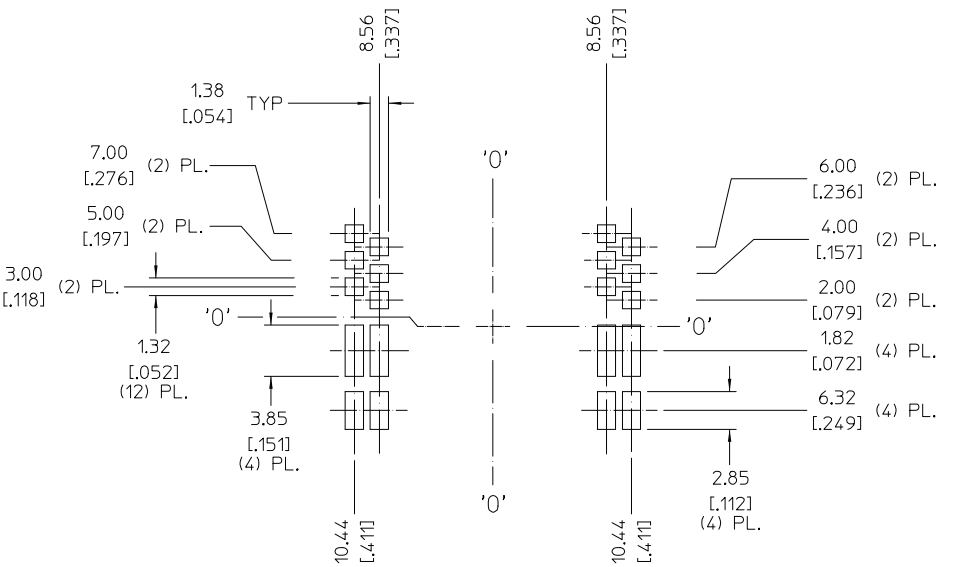
TOP VIEW (COMPONENT SIDE)



BOTTOM VIEW







RECOMMENDED LAND PATTERN
(COMPONENT SIDE SHOWN)

Revision History

Revision	Date	Description	Page Number(s)
1.1	11/12/12	Final approved data sheet for intital release	n/a
1.2	02/15/13	Updated format throughout	all
1.3	07/25/13	Updated Maximum Time Above 217°C Added Array Diagrams	26 33 & 37
1.4	09/30/15	Updated MSL Rating	26
1.5	11/16/15	Minor changes in efficiency specifications Corrections to schematic labels	5 16
1.6	09/08/20	Updated terminology	1, 4, 6, 7, 8, 9, 11, 15, 28, 29, 30, 34

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