Precision, Dual-Supply Analog Switches

Features

- Low On-Resistance (17ohms typ.) Minimizes Distortion and Error Voltages
- Low Glitching Reduces Step Errors in Sample-and-Holds
- Split-Supply Operation (±3V to ±8V)
- Improved Second Sources for MAX320/MAX321/MAX322
- On-Resistance Matching Between Channels, 0.2ohm typ.
- On-Resistance Flatness, <2ohm typ.
- Low Off-Channel Leakage, <5nA @ +85°C
- TTL/CMOS Logic Compatible
- Fast Switching Speed, t_{ON} <150ns
- Guaranteed Break-Before-Make action (PS322) eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Dynamic Range
- Low Power Consumption, <1.25mW
- Packaging (Pb-free & Green):
  — 8-pin MSOP (U)
  — 8-pin SOIC (W)

Applications

- Audio Switching and Routing
- Portable Instruments
- Data Acquisition Systems
- Sample-and-Holds
- Telecommunication Systems
- Battery-Powered Systems

Description

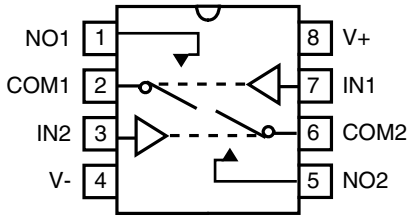
The PS320/PS321/PS322 are improved high-precision, medium voltage analog switches designed to operate with ±3V to ±8V power supplies. The PS320 is a dual, single-pole single-throw (SPST), normally open (NO) switch. The PS321 has the same pinout as the PS320 but it has two normally closed (NC) switches. The PS322 has one normally open (NO) and one normally closed (NC) switch per package. When on, each switch conducts current equally well in either direction. In the off state, each switch blocks voltages up to the power-supply rails.

With ±5V power supplies, the PS320/PS321/PS322 guarantee <35ohm ON-resistance. ON-resistance matching between channels is within 2ohm. ON-resistance flatness is less than 4ohm over the specified range. All three devices guarantee low leakage currents (<100pA @25°C, <10nA @+85°C) and fast switching speeds (t_{ON} <150ns). Break-before-make switching action protects against momentary crosstalk (PS322).

For single-supply operation the PS323/PS324/PS325 are recommended.

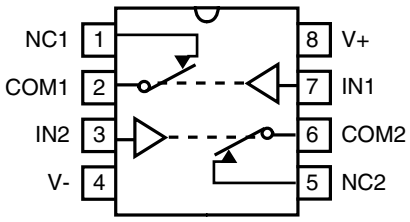
Functional Diagrams, Pin Configurations, and Truth Tables

PS320



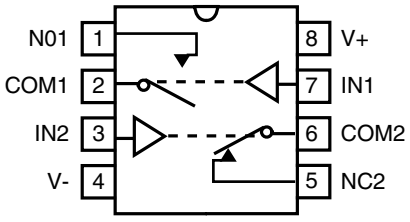
Top View

PS321



Top View

PS322



Top View

Switches shown for logic "0" input

PS320	
Logic	**Switch**
0	OFF
1	ON

PS321	
Logic	**Switch**
0	ON
1	OFF

PS322		
Logic	**Switch1**	**Switch2**
0	OFF	ON
1	ON	OFF

Absolute Maximum Ratings

Voltages Referenced to V–

V+ ..... -0.3V to +17V

V_{IN}, V_{COM}, V_{NC}, V_{NO}(1) ..... (V-) -2V to (V+) +2V

..... or 30mA, whichever occurs first

Current (any terminal) 30mA

Peak Current, COM, NO, NC

(pulsed at 1ms, 10% duty cycle) 100mA

ESD per Method 3015.7 ..... > 2000V

Note 1:
Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating

Thermal Information

Continuous Power Dissipation

Plastic DIP (derate 6mW/ºC above +70ºC) 500mW

Narrow SO (derate 6mW/ºC above +70ºC) 450mW

MSOP (derate 4mW/ºC above +70ºC) 330mW

Storage Temperature ..... -65ºC to +150ºC

Lead Temperature (soldering, 10s) ..... +300ºC

Caution:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Specifications - Dual Supplies ($V\pm = \pm 5V \pm 10\%$, $V_{INH} = 3.5V$, $V_{INL} = 1V$)

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Analog Switch							
Analog Signal Range (3)	V_{ANALOG}		Full	V–		V+	V
ON-Resistance	R_{ON}	V+ = 4.5V, V– = –4.5V, V_{NO} or V_{NC} = ±3.5V I_{COM} = 1mA,	25		16	35	ohm
			Full			45	
ON-Resistance Match Between Channels(4)	ΔR_{ON}	V+ = 5V, V– = –5V V_{NO} or V_{NC} = ±3V, I_{COM} = 1mA,	25		0.3	2	
			Full			4	
ON-Resistance Flatness(5)	$R_{FLAT(ON)}$	V+ = 5V, V– = –5V, I_{COM} = 1mA , V_{NO} or V_{NC} = ±3V	25		1	4	
			Full			6	
NO or NC Off Leakage Current(6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	25	–0.1	–0.01	0.1	nA
			Full	–5		5	
COM Off Leakage Current(6)	$I_{COM(OFF)}$	V+ = 5.5V, V– = –5.5V V_{COM} = ±4.5V, V_{NO} or V_{NC} = ±4.5V	25	–0.1	–0.01	0.1	
			Full	–5		5	
COM On Leakage Current(6)	$I_{COM(ON)}$	V+ = 5.5V , V– = –5.5V, V_{COM} = ±4.5V V_{NO} or V_{NC} = ±4.5V	25	–0.2	–0.04	0.2	
			Full	–10		10	

continued next page

Electrical Specifications - Dual Supplies ($V\pm = \pm 5V \pm 10\%$, $V_{INH} = 3.5V$, $V_{INL} = 1V$) continued

Parameter	Symbol	Conditions	Temp. (°C)	Min.(1)	Typ.(2)	Max.(1)	Units
Logic Input							
Input Current with Input Voltage High	I_{INH}	V_{IN} = 3.5V, all others = 0V	Full	– 0.5	0.005	0.5	mA
Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0V, all others = V+		– 0.5	0.005	0.5	
Logic High Input Voltage	V_{INH}	V+ = 5V ±10%, V– = – V+		3.5			V
		3V < V+ < 8V, V– = – V+			0.6V+		
Logic Low Input Voltage	V_{INL}	V+ = 5V ±10%, V– = – V+				1	
		3V < V+ < 8V, V– = – V+			0.3V+		
Dynamic							
Turn-On Time	t_{ON}	V_{COM} = ±3V, Figure 2	25		65	150	ns
			Full			175	
Turn-Off Time	t_{OFF}		25		35	100	
			Full			150	
Break-Before-Make Time Delay(3)	t_D	PS322 only, R_L = 300ohm, C_L= 35pF, Figure 3	25	2	5		
Charge Injection(3)	Q	C_L=1nF, V_{GEN} = 0V, R_{GEN} = 0ohm, Figure 4			8	12	pC
Off Isolation(7)	O_{IRR}	R_L = 50ohm, C_L= 5pF, f = 1MHz, Figure 5			–72		dB
Crosstalk	X_{TALK}	R_L = 50ohm, C_L= 5pF, f = 1MHz, Figure 6			–85		
NC or NO Off Capacitance	$C_{(OFF)}$	f = 1MHz, Figure 7			9		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, Figure 7			9		
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 8			22		
Supply							
Power-Supply Range	V+, V–			±2.7		±8	V
Positive Supply Current	I+	V+ = 5.5V, V- = – 5.5V, V_{IN} = 0V or V+, All channels on or off	25		80	125	µA
			Full			200	
Negative Supply Current	I–		25	– 125	– 80		
			Full	– 200			

Notes:
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = \Delta R_{ON}$ max. $-\Delta R_{ON}$ min.
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25ºC.
7. Off Isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})].

Test Circuits/Timing Diagrams

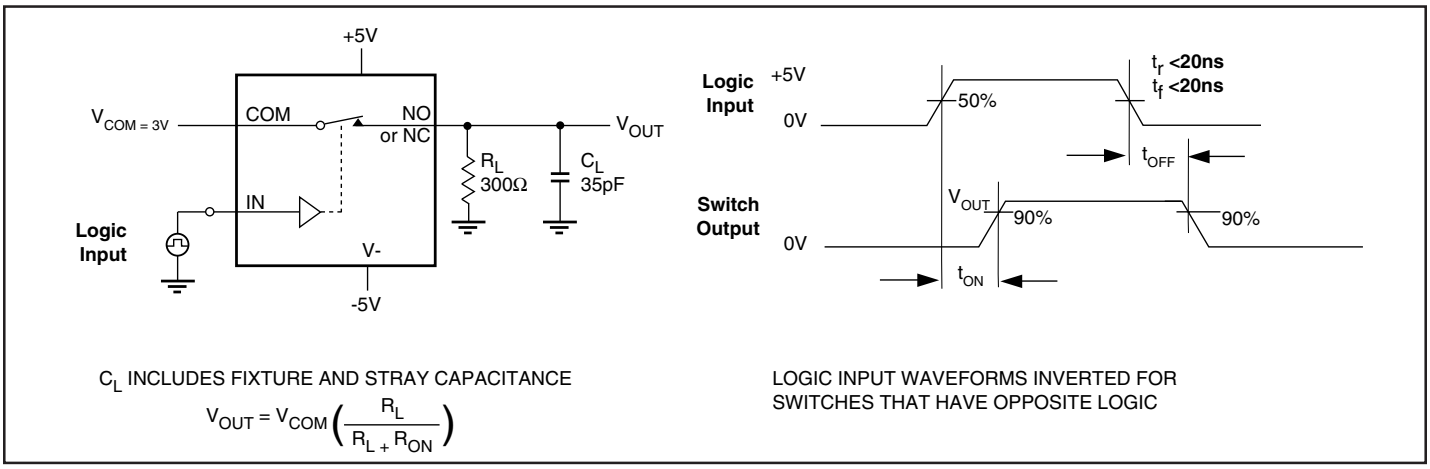


Figure 2. Switching Time

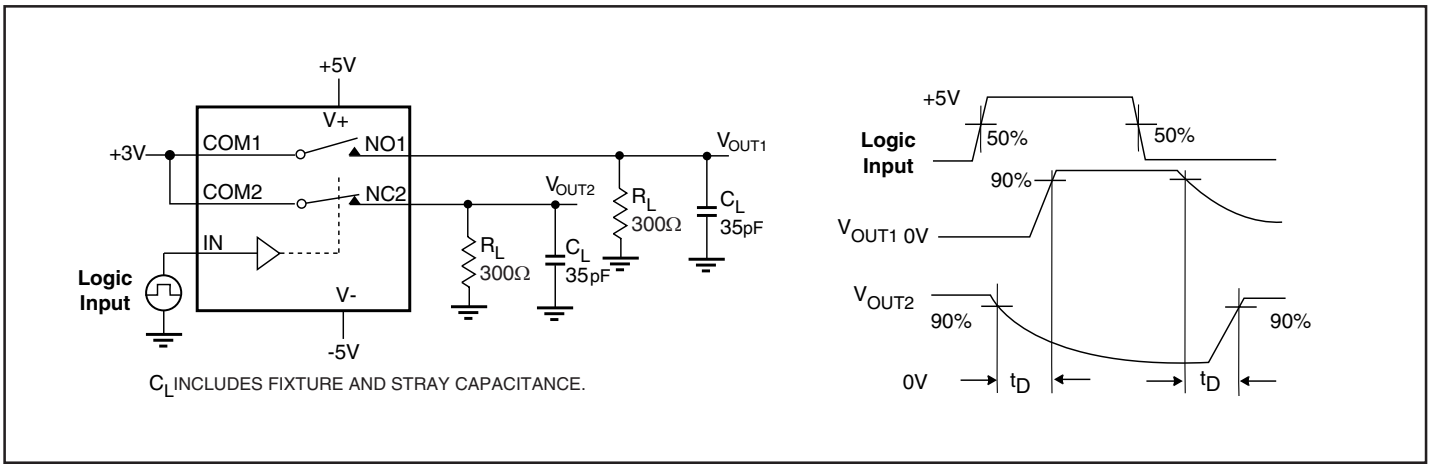


Figure 3. Break-Before-Make Interval (PS322 only)

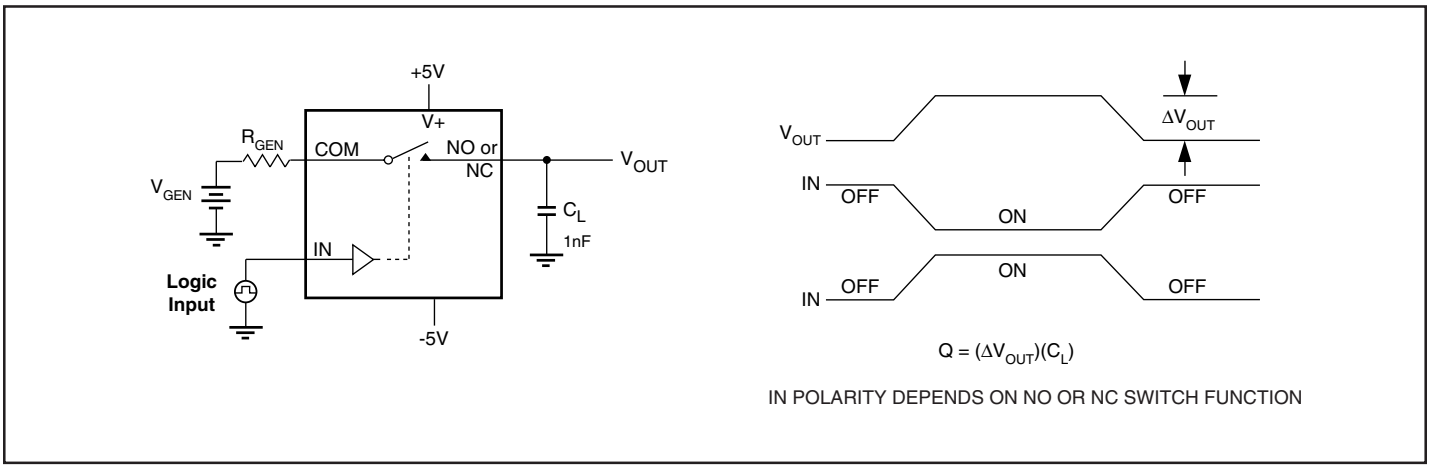


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

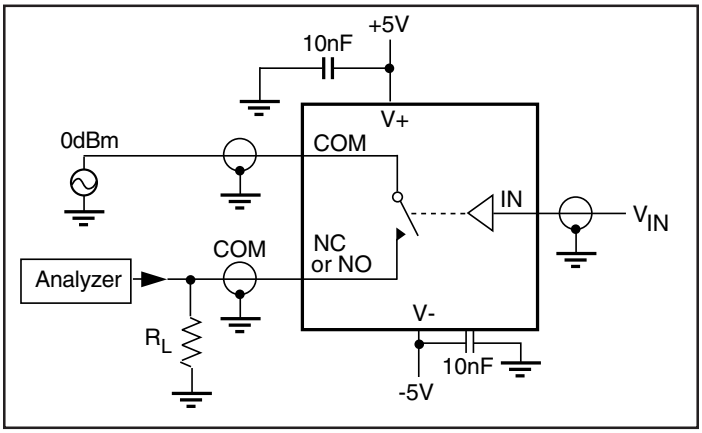


Figure 5. Off Isolation

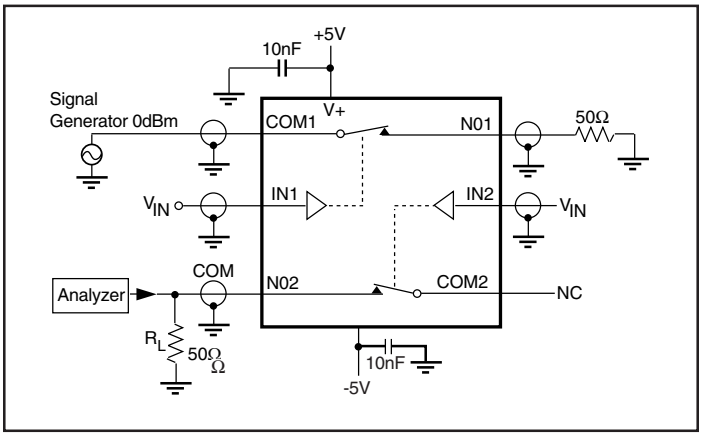


Figure 6. Crosstalk

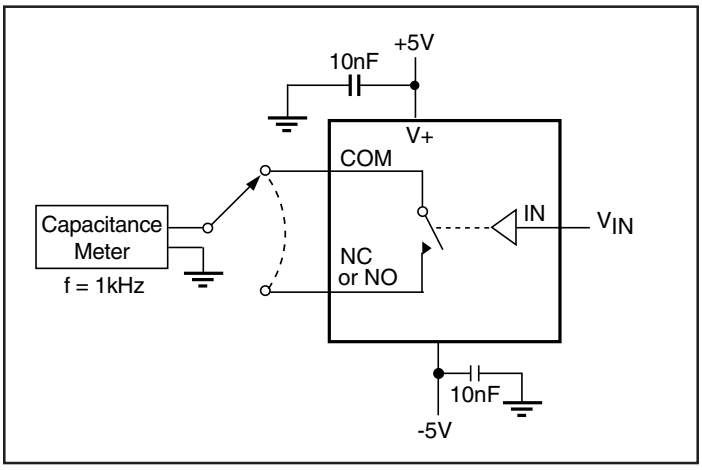


Figure 7. Channel-Off Capacitance

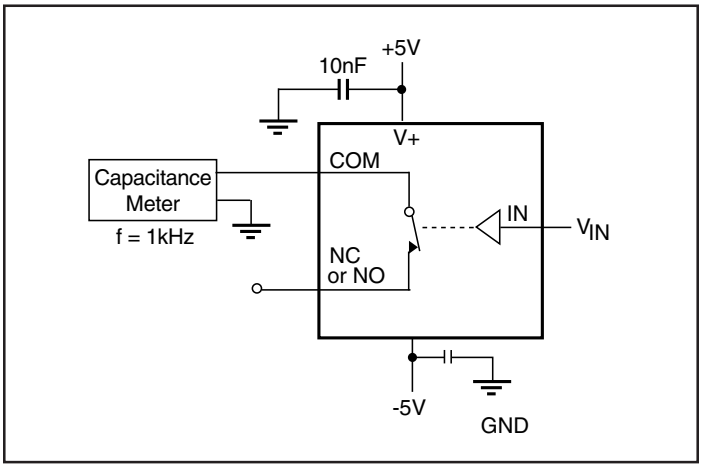
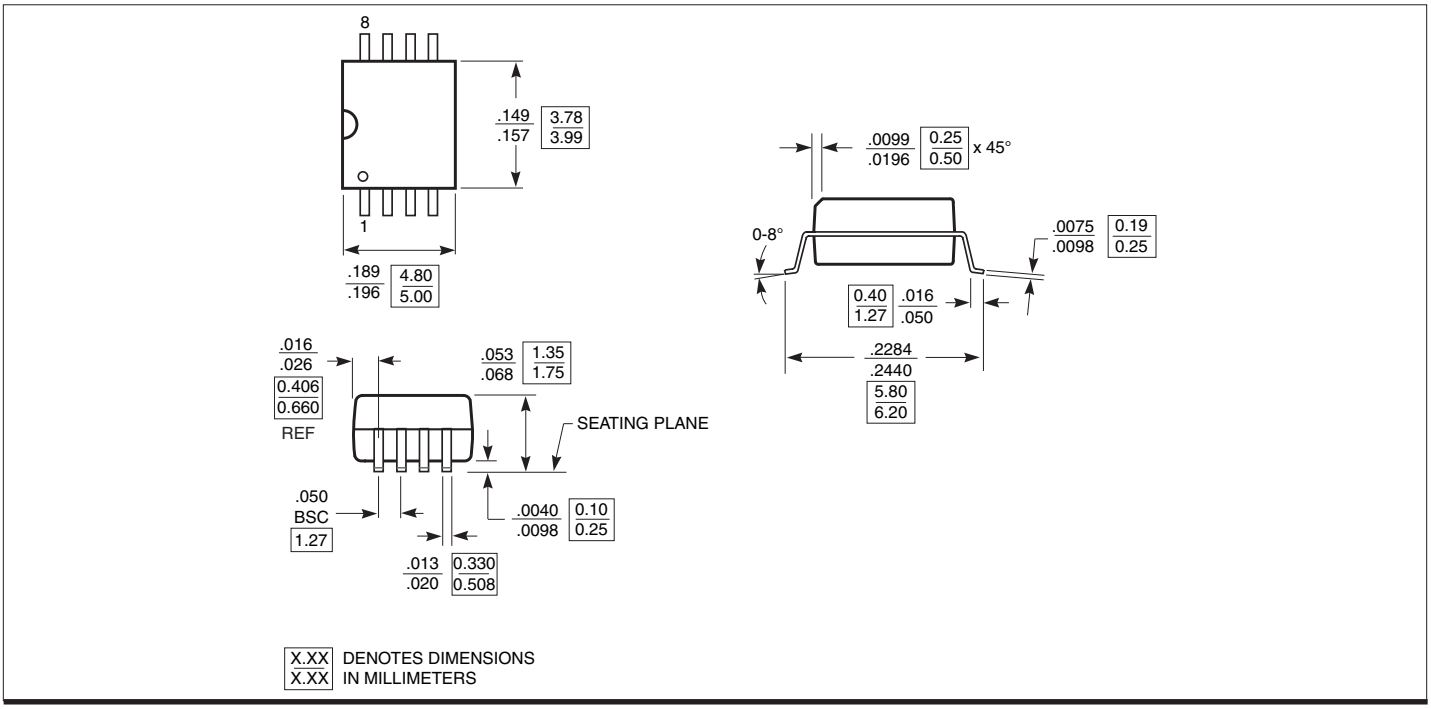
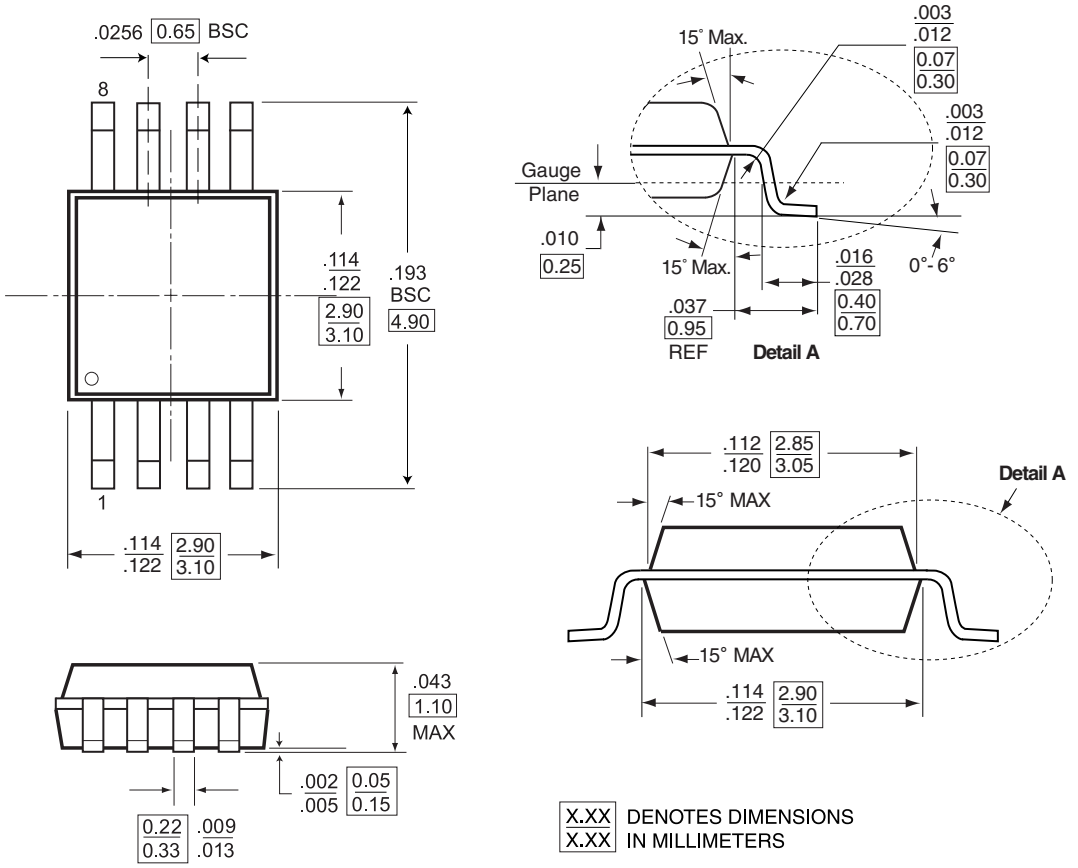


Figure 8. Channel-On Capacitance

Packaging Mechanical: 8-Pin SOIC (W) Package



Packaging Mechanical: 8-Pin MSOP (U) Package



Ordering Information

Part	Temp. Range	Package
PS320CUAX	0ºC to +70ºC	8 MSOP
PS320CUAEX		
PS320ESA	–40ºC to +85ºC	8 Narrow SO
PS320ESAE		