



PUMB3H

50 V, 100 mA PNP/PNP Resistor-Equipped double Transistor;
R1 = 4.7 kΩ, R2 = open

22 March 2021

Product data sheet

1. General description

PNP/PNP Resistor-Equipped double Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH7H

NPN/PNP complement: PUMD6H

2. Features and benefits

- 100 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- High-temperature applications up to 175 °C

3. Applications

- Digital applications
- Cost saving alternative for BC857 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

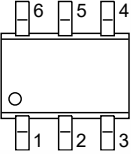
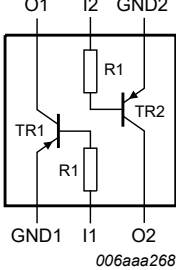
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1	T _{amb} = 25 °C	[1]	3.3	4.7	6.1 kΩ

[1] See section "Test information" for resistor calculation and test conditions

50 V, 100 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 4.7 kΩ, R2 = open

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 TSSOP6 (SOT363)	 006aaa268
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMB3H	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMB3H	2C%

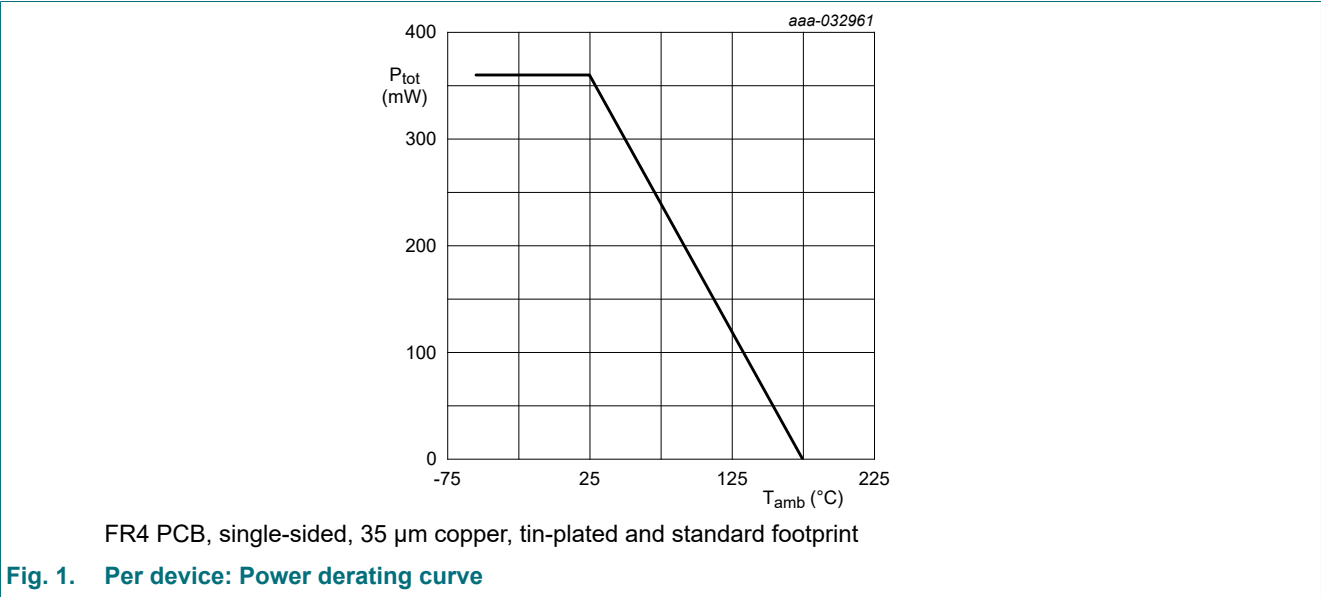
[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	-50	V
V _{CEO}	collector-emitter voltage	open base		-	-50	V
V _{EBO}	emitter-base voltage	open collector		-	-7	V
V _I	input voltage			-30	7	V
I _O	output current			-	-100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	240	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	360	mW
T _j	junction temperature			-	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.

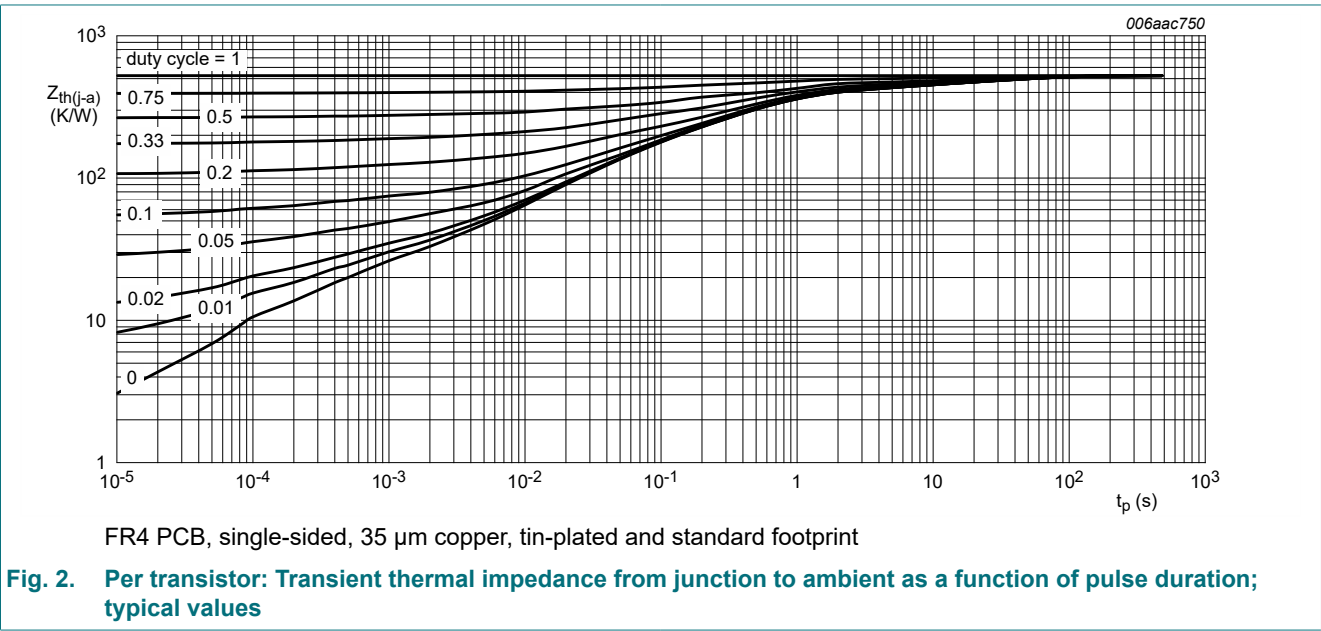


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	230	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.



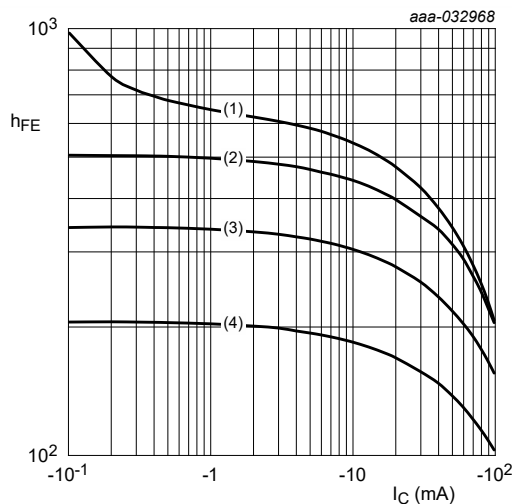
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100\ \mu\text{A}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2\ \text{mA}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\ \text{V}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\ \text{V}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	-100	nA
		$V_{CE} = -30\ \text{V}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 150\ ^\circ\text{C}$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -7\ \text{V}$; $I_C = 0\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -5\ \text{V}$; $I_C = -1\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	200	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\ \text{mA}$; $I_B = -0.5\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	-100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\ \text{V}$; $I_C = -100\ \mu\text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-585	-500	mV
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\ \text{V}$; $I_C = -10\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-1.3	-0.88	-	V
R1	bias resistor 1	$T_{\text{amb}} = 25\ ^\circ\text{C}$	[1]	3.3	4.7	6.1 kΩ
C_c	collector capacitance	$V_{CB} = -10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5\ \text{V}$; $I_C = -10\ \text{mA}$; $f = 100\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	[2]	-	180	MHz

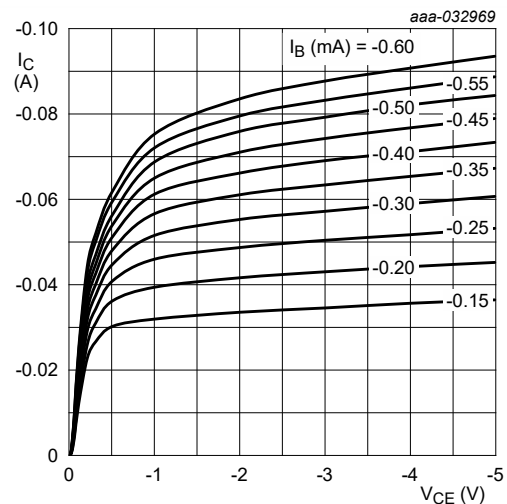
[1] See section "Test information" for resistor calculation and test conditions

[2] Characteristics of built-in transistor



$V_{CE} = -5\ \text{V}$
 (1) $T_{\text{amb}} = 175\ ^\circ\text{C}$
 (2) $T_{\text{amb}} = 100\ ^\circ\text{C}$
 (3) $T_{\text{amb}} = 25\ ^\circ\text{C}$
 (4) $T_{\text{amb}} = -40\ ^\circ\text{C}$

Fig. 3. DC current gain as a function of collector current; typical values



$T_{\text{amb}} = 25\ ^\circ\text{C}$

Fig. 4. Collector current as a function of collector-emitter voltage; typical values

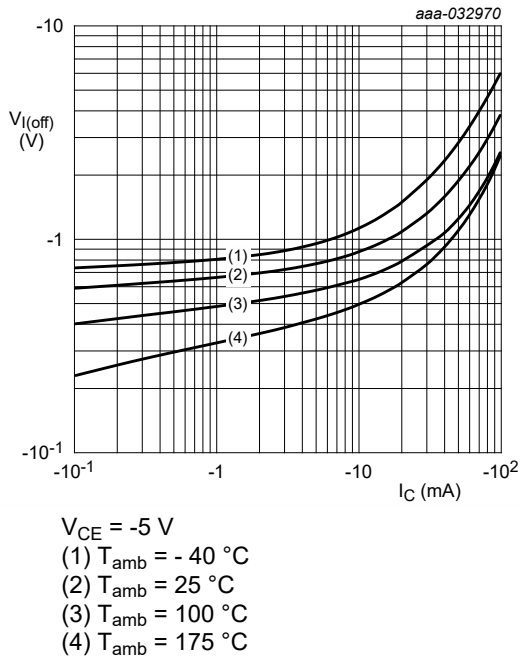


Fig. 5. Off-state input voltage as a function of collector current; typical values

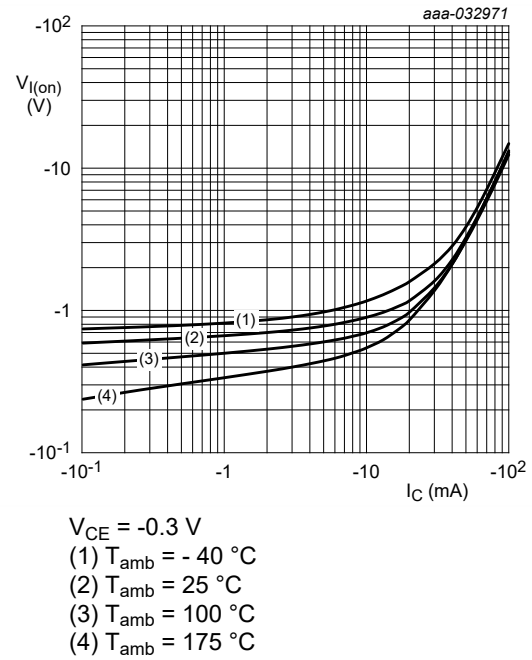


Fig. 6. On-state input voltage as a function of collector current; typical values

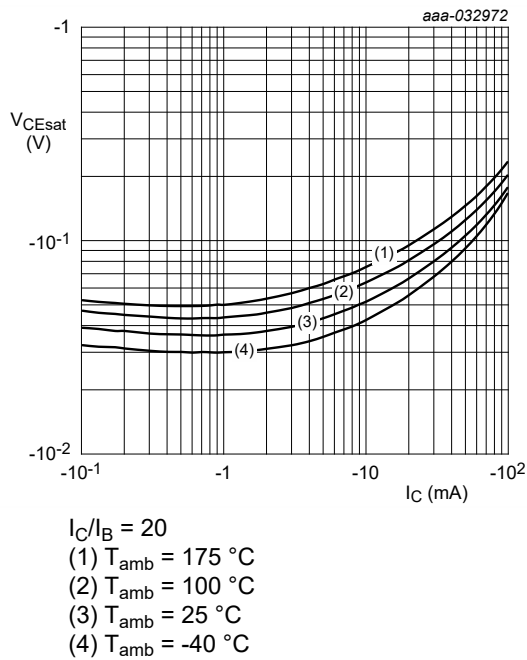


Fig. 7. Collector-emitter saturation voltage as a function of collector current; typical values

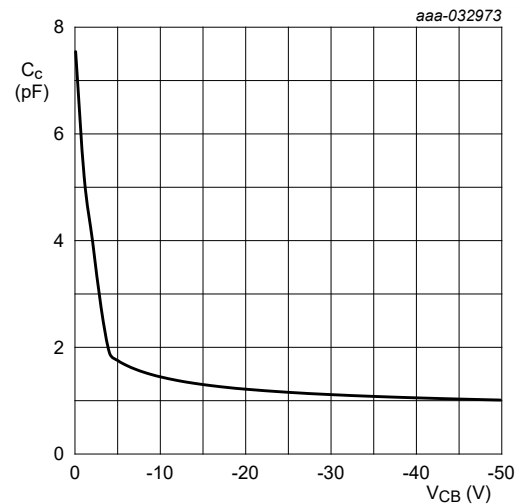
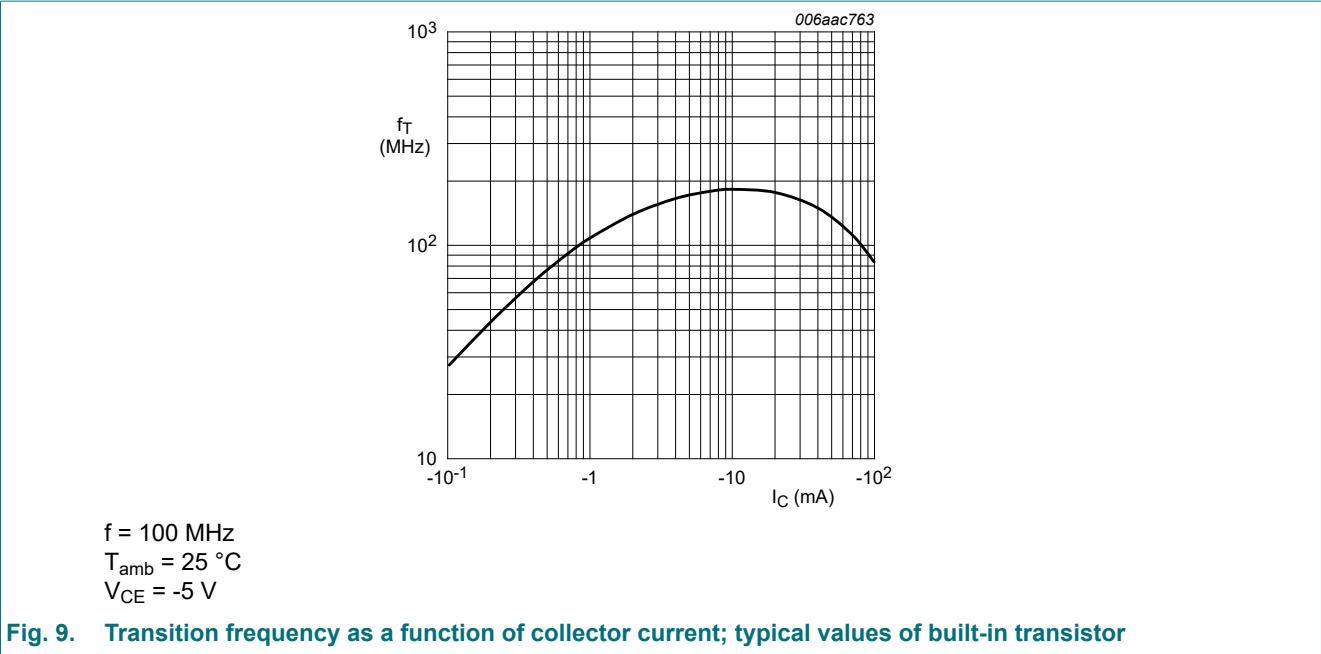


Fig. 8. Collector capacitance as a function of collector-base voltage; typical values

50 V, 100 mA PNP/PNP Resistor-Equipped double Transistor; R1 = 4.7 kΩ, R2 = open



11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)
- $$R_I = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

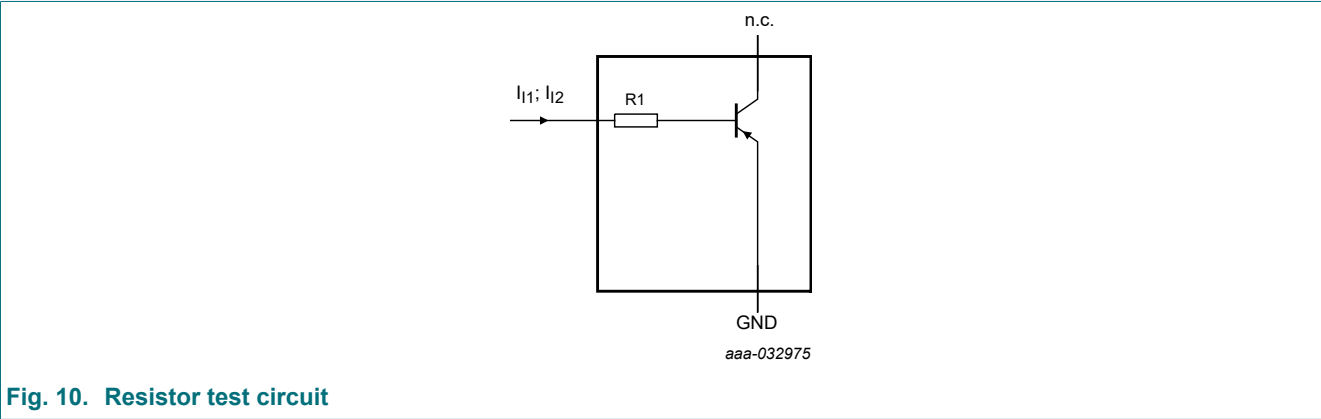


Fig. 10. Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions	
			I _{I1}	I _{I2}
Per transistor				
PUMB3H	4.7	open	-600 μA	-700 μA

12. Package outline

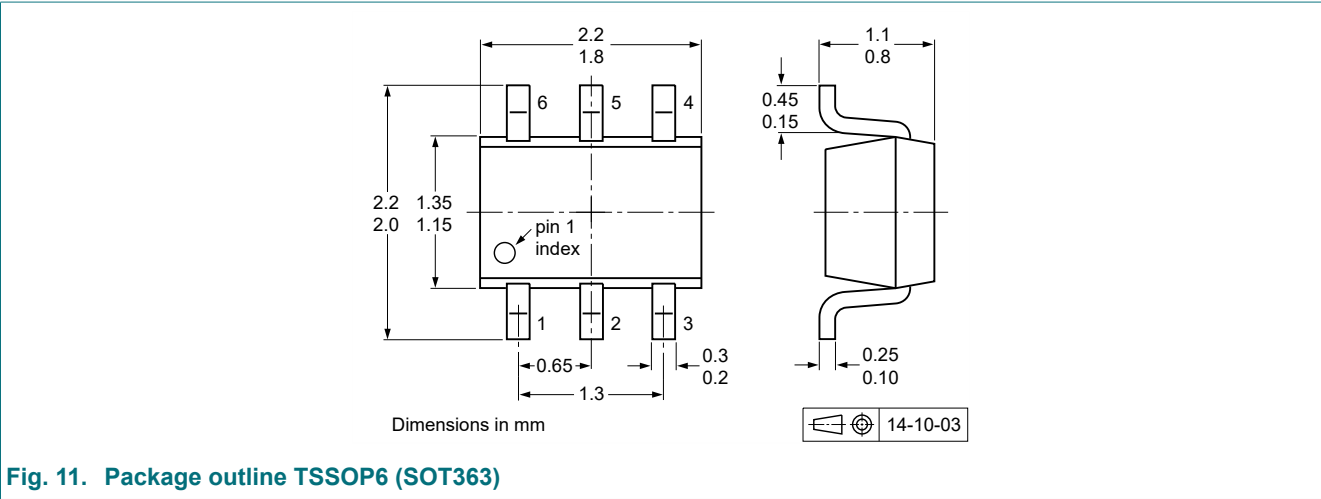


Fig. 11. Package outline TSSOP6 (SOT363)

13. Soldering

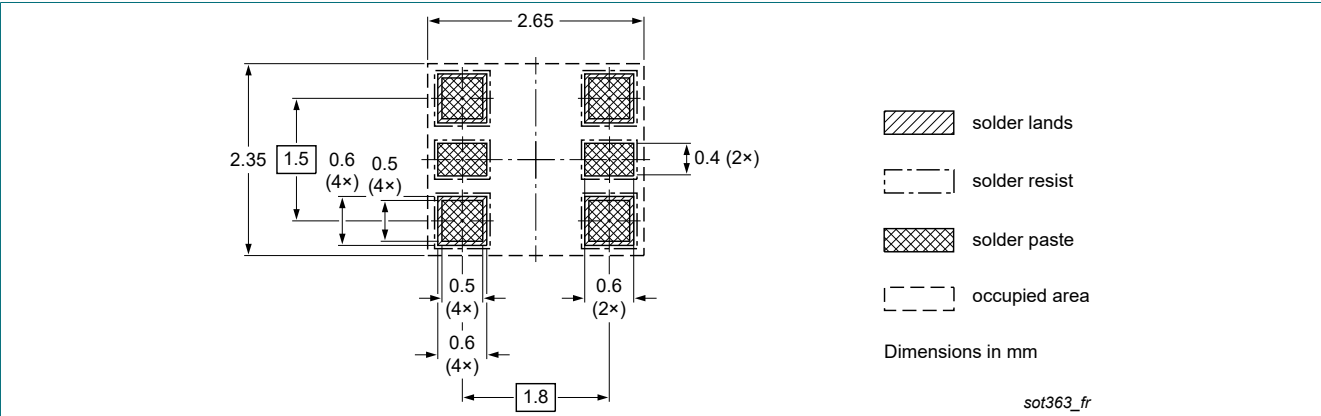


Fig. 12. Reflow soldering footprint for TSSOP6 (SOT363)

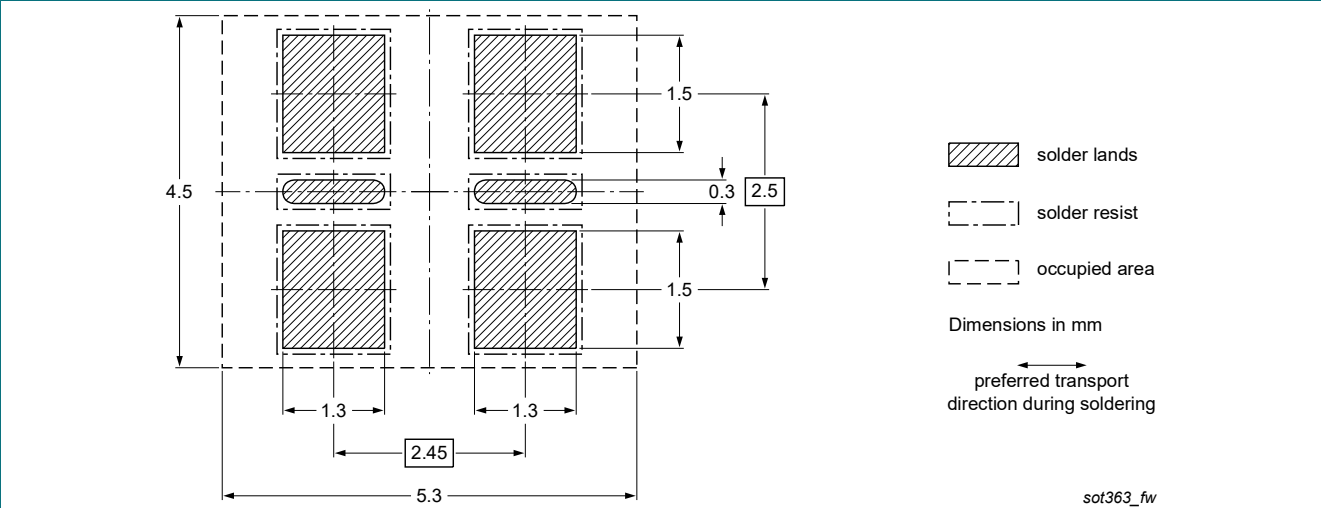


Fig. 13. Wave soldering footprint for TSSOP6 (SOT363)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMB3H v.1	20210322	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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