

PUMD10-Q

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 2.2 kΩ, R2 = 47 kΩ

20 July 2026 Product data sheet

1. General description

NPN/PNP double Resistor-Equipped Transistor (RET) in a very small SOT363-3 (SC-88) Surface-Mounted Device (SMD) plastic package.

PNP/PNP complement: PUMB10-Q

NPN/NPN complement: PUMH10-Q

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

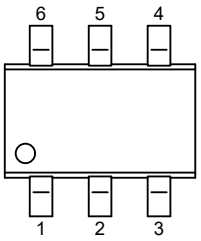
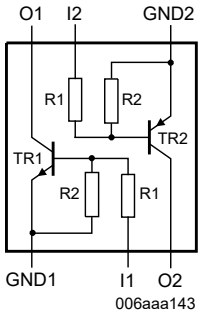
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity, where applicable							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	

[1] See section "Test information" for resistor calculation and test conditions.

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 Transparent top view **TSSOP6 (SOT363-3)**	
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMD10-Q	TSSOP6	Plastic surface-mounted package; 6 leads	SOT363-3

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD10-Q	D%0

[1] % = placeholder for manufacturing site code

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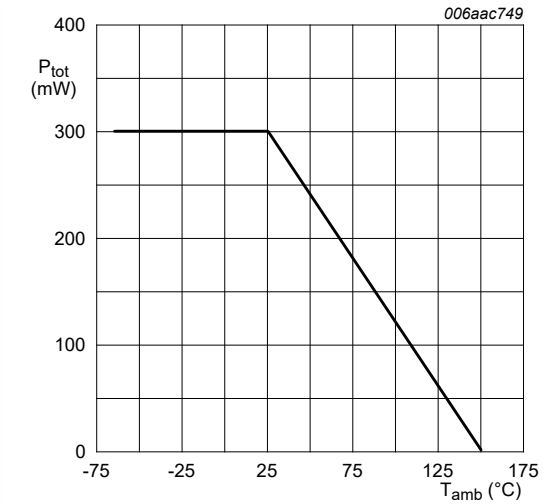
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity, where applicable						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	5	V
V_I	input voltage	positive (input voltage TR1)		-	12	V
		negative (Input voltage TR1)		-	-5	V
		positive (input voltage TR2)		-	5	V
		negative (Input voltage TR2)		-	-12	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 1. Per device: Power derating curve

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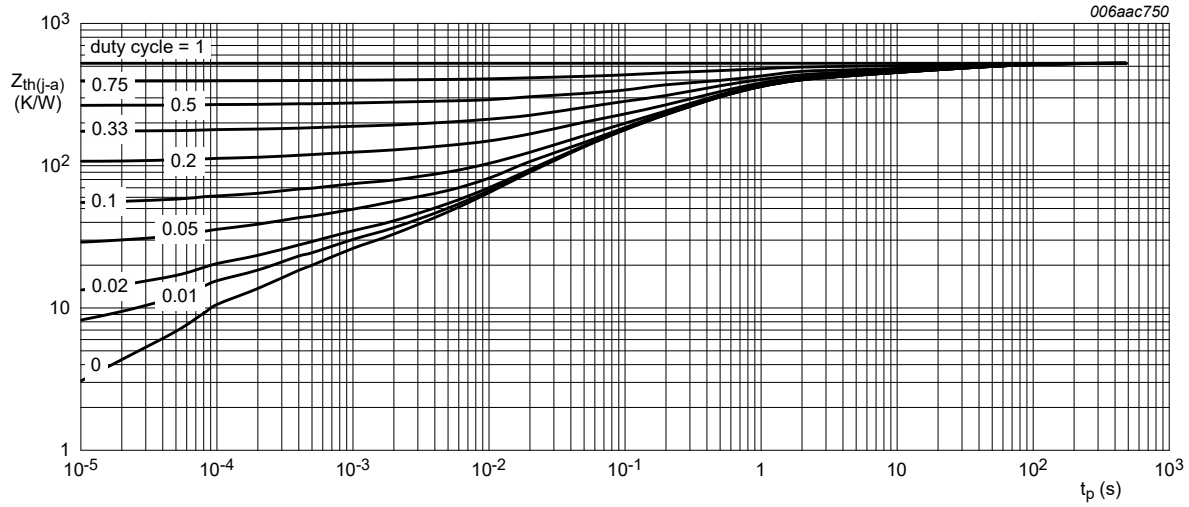
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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

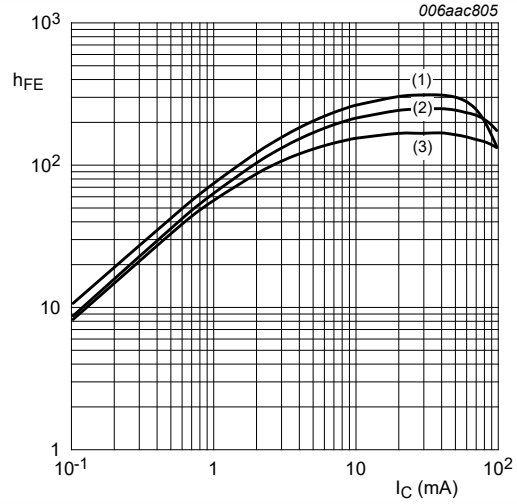
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor (TR2) with negative polarity, where applicable							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A		-	-	100	nA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A		-	-	180	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 10 mA		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 5 mA; I_B = 0.25 mA		-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA		-	0.6	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 5 mA		1.1	0.75	-	V
R1	bias resistor 1 (input)		[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	17	21	26	
TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz		-	-	2.5	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz	[2]	-	230	-	MHz
TR2 (PNP)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz		-	-	3	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz	[2]	-	180	-	MHz

[1] See section "Test information" for resistor calculation and test conditions.
[2] Characteristics of built-in transistor

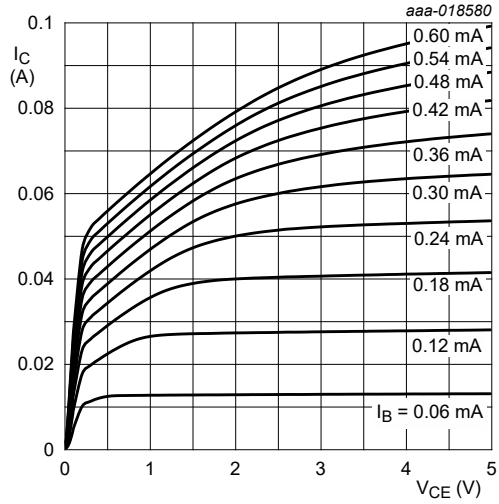
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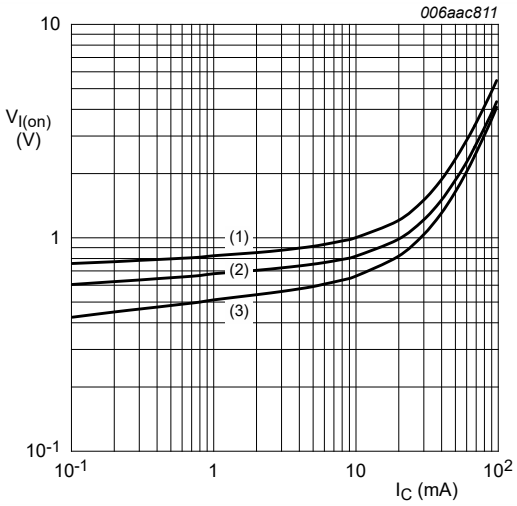
V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 3. NPN transistor: DC current gain as a function of collector current; typical values



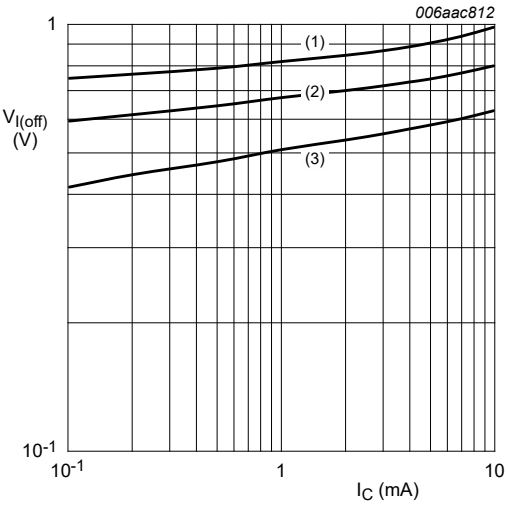
T_{amb} = 25 °C

Fig. 4. NPN transistor: Collector current as a function of collector-emitter voltage; typical values



V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

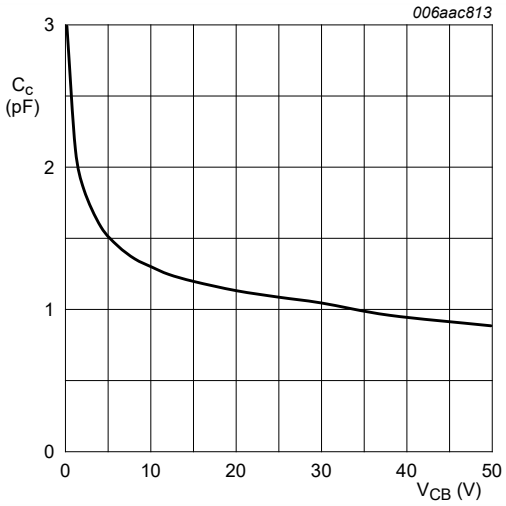
Fig. 5. NPN transistor: On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

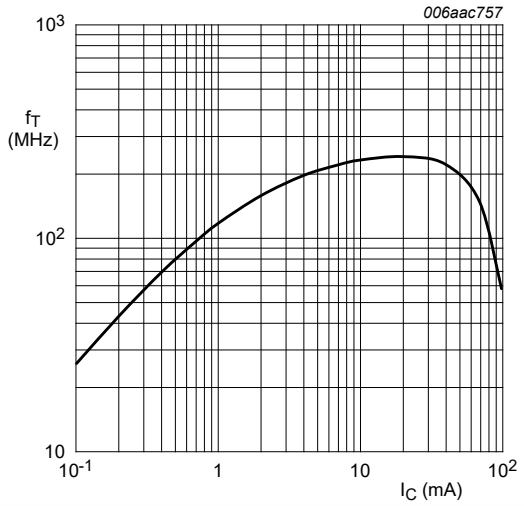
Fig. 6. NPN transistor: Off-state input voltage as a function of collector current; typical values

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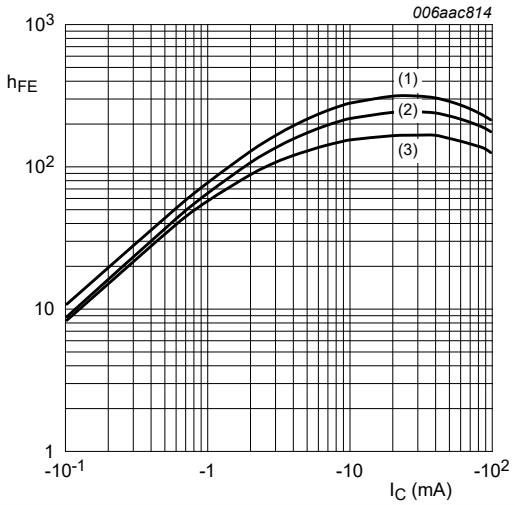
f = 1 MHz; T_{amb} = 25 °C

Fig. 7. NPN transistor: Collector capacitance as a function of collector-base voltage; typical values



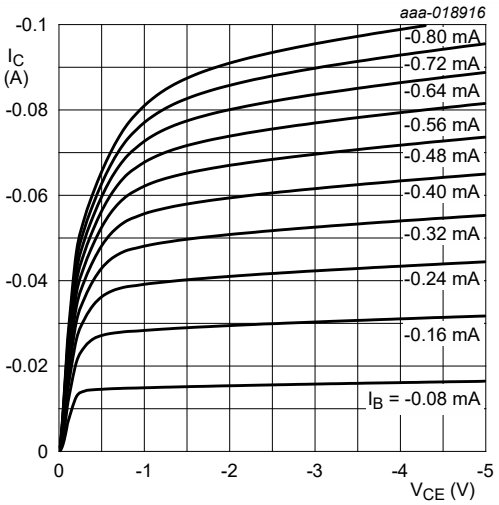
f = 100 MHz
T_{amb} = 25 °C
V_{CE} = 5 V

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor



V_{CE} = -5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

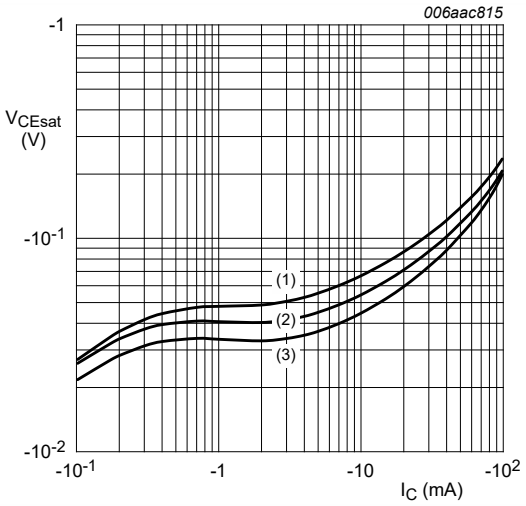
Fig. 9. PNP transistor: DC current gain as a function of collector current; typical values



T_{amb} = 25 °C

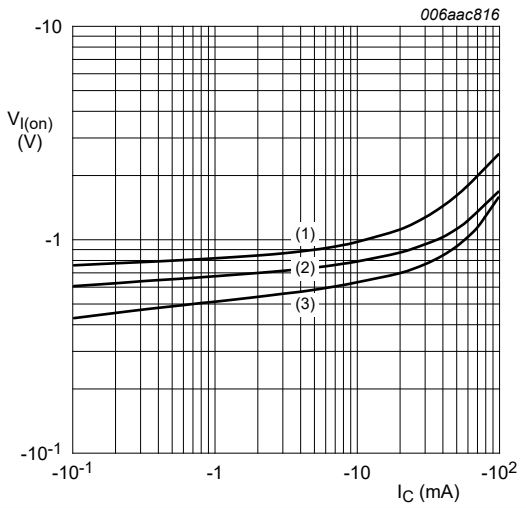
Fig. 10. PNP transistor: Collector current as a function of collector-emitter voltage; typical values

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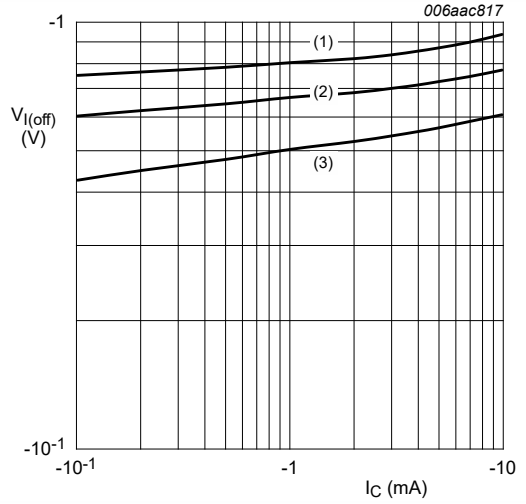
I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 11. PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values



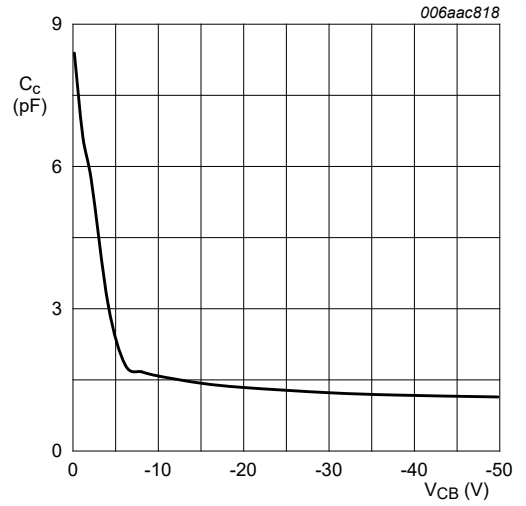
V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 12. PNP transistor: On-state input voltage as a function of collector current; typical values



V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

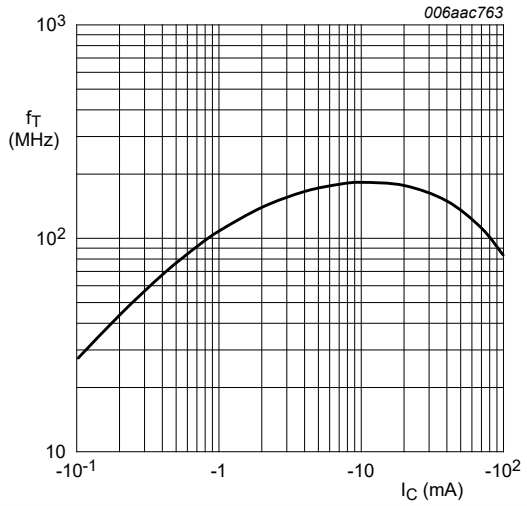
Fig. 13. PNP transistor: Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig. 14. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values

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V_{CE} = -5 V; T_{amb} = 25 °C

Fig. 15. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor

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11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_4) - V(I_3)}{R1 \cdot (I_4 - I_3)} - 1$$

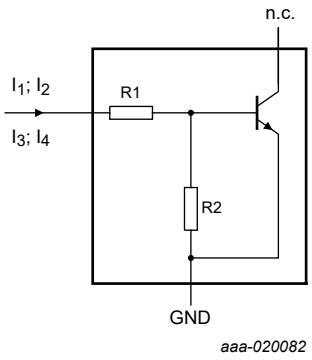


Fig. 16. NPN transistor: Resistor test circuit

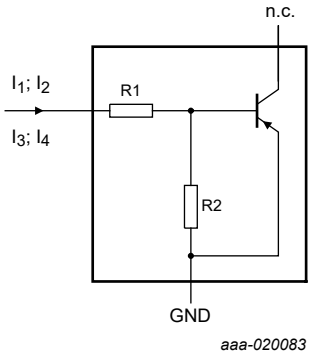


Fig. 17. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PUMD10-Q	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_1	I_2	I_3	I_4
TR1 (NPN)	2.2	47	90 µA	140 µA	-55 µA	-105 µA
TR2 (PNP)	2.2	47	-90 µA	-140 µA	55 µA	105 µA

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12. Package outline

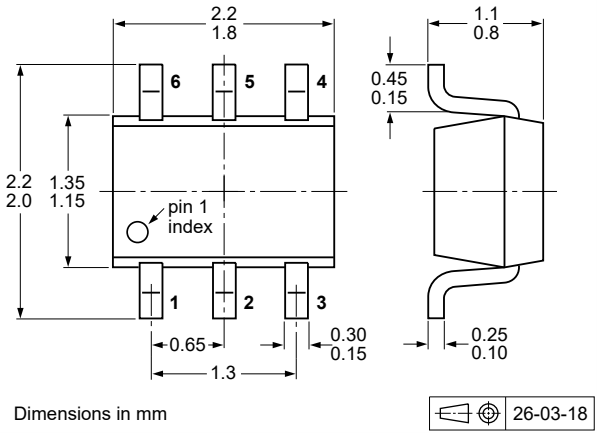


Fig. 18. Package outline TSSOP6 (SOT363-3)

13. Soldering

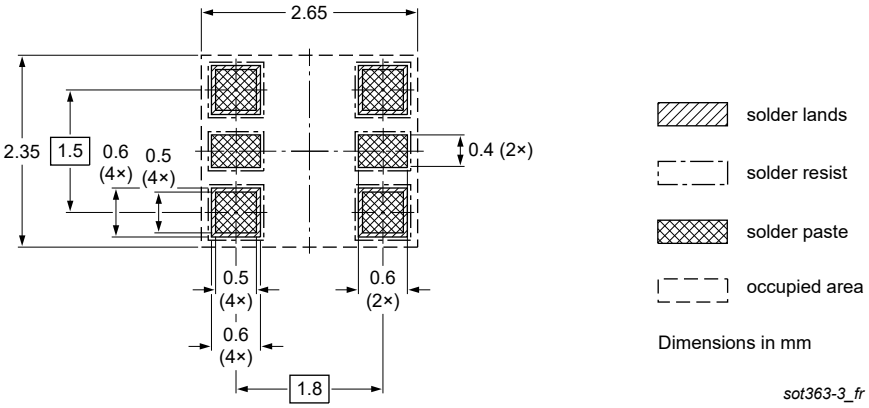


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363-3)

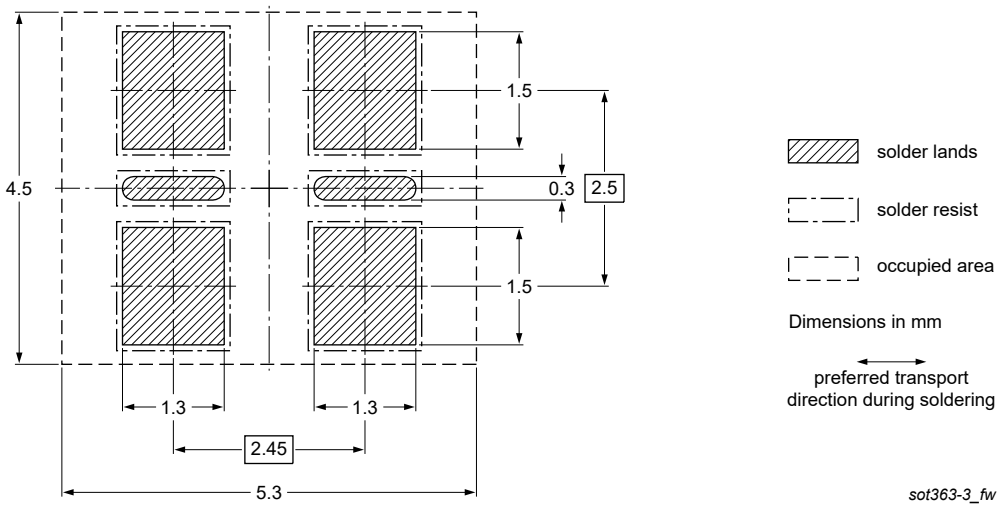


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363-3)

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14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD10-Q v.2	20260720	Product data sheet	-	PUMD10-Q v.1
Modifications:	• Package changed from SOT363 to SOT363-3			
PUMD10-Q v.1	20210914	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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