QT1081

8-KEY QTOUCH™ SENSOR IC

This datasheet is applicable to all revision 1 chips

The QT1081 is an improved, lower cost, simplified circuit version of the popular QT1080 sensor IC. The QT1081 is designed for low cost appliance, mobile, and consumer electronics applications.

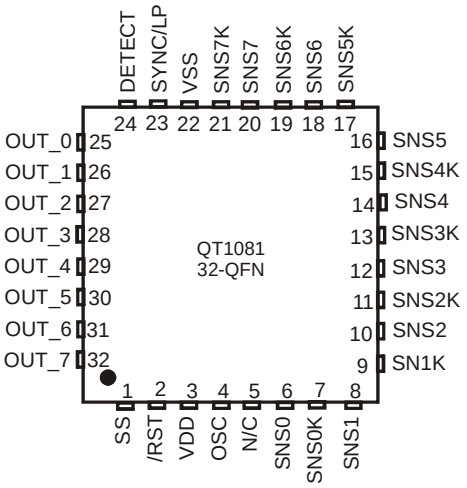
QTouch™ technology is a type of patented charge-transfer sensing method well known for its robust, stable, EMC-resistant characteristics. It is the only all-digital capacitive sensing technology in the market today. This technology has over a decade of applications experience spanning thousands of designs.

QTouch circuits are renowned for simplicity, reliability, ease of design, and cost effectiveness.

QTouch™ sensors employ a single reference capacitor tied to two pins of the chip for each sensing key; a signal trace leads from one of the pins to the sensing electrode which forms the key. The sensing electrode can be a simple solid shape such as a rectangle or circle. An LED can be placed near or inside the solid circle for illumination.

The key electrodes can be designed into a conventional printed circuit board (PCB) or flexible printed circuit board (FPCB) as a copper pattern, or as printed conductive ink.

The QT1081 is also compatible with clear films to make simple button-style touch screens over LCD displays.



AT A GLANCE

Number of keys:	1 to 8
Technology:	Patented spread-spectrum charge-transfer (one-per-key mode)
Key outline sizes:	5mm x 5mm or larger (panel thickness dependent); widely different sizes and shapes possible
Key spacings:	6mm or wider, center to center (panel thickness, human factors dependent)
Electrode design:	Single solid or ring shaped electrodes; wide variety of possible layouts
Layers required:	One layer substrate; electrodes and components can be on same side
Substrates:	FR-4, low cost CEM-1 or FR-2 PCB materials; polyamide FPCB; PET films, glass
Electrode materials:	Copper, silver, carbon, ITO, Orgacon† ink (virtually anything electrically conductive)
Panel materials:	Plastic, glass, composites, painted surfaces (low particle density metallic paints possible)
Adjacent Metal:	Compatible with grounded metal immediately next to keys
Panel thickness:	Up to 50mm glass, 20mm plastic (key size dependent)
Key sensitivity:	Settable via change in reference capacitor (Cs) value
Outputs:	Parallel discrete output, one-per-key, active-high
Moisture tolerance:	Good
Power:	2.8V ~ 5.0V, <15µA (8 keys at 2.8V, 340ms Low Power mode).
Package:	32-pin 5 x 5mm QFN RoHS compliant
Signal processing:	Self-calibration, auto drift compensation, noise filtering, patented Adjacent Key Suppression™
Applications:	Portable devices, domestic appliances and A/V gear, PC peripherals, office equipment
Patents:	**AKS™** (patented Adjacent Key Suppression)
	QTouch™ (patented Charge-transfer method)

†Orgacon is a registered trademark of Agfa-Gevaert N.V

AVAILABLE OPTION

T_A	32-QFN
-40ºC to +85ºC	QT1081-ISG

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Contents

1 Overview . . . 3
1.1 Differences With QT1080 . . . 3
1.2 Parameters . . . 3
1.2.1 Introduction . . . 3
1.2.2 Burst Operation . . . 3
1.2.3 Self-calibration . . . 3
1.2.4 Autorecalibration . . . 3
1.2.5 Drift Compensation . . . 3
1.2.6 Detection Integrator Confirmation . . . 3
1.2.7 Spread-spectrum Operation . . . 3
1.2.8 Sync Mode . . . 3
1.2.9 Low Power (LP) Mode . . . 3
1.2.10 Adjacent Key Suppression (AKS™) . . . 3
1.2.11 Outputs . . . 4
1.2.12 Simplified Mode . . . 4
1.3 Wiring . . . 5
2 Device Operation . . . 8
2.1 Start-up Time . . . 8
2.2 Option Resistors . . . 8
2.3 One-per-key Output Mode . . . 8
2.4 Binary Coded Output Mode . . . 8
2.5 DETECT Pin . . . 8
2.6 SYNC/LP Pin . . . 8
2.7 AKS™ Function Pins . . . 9
2.8 MOD_0, MOD_1 Inputs . . . 9
2.9 Fast Detect Mode . . . 9
2.10 Simplified Mode . . . 10
2.11 Unused Keys . . . 10
3 Design Notes . . . 11
3.1 Oscillator Frequency . . . 11
3.2 Spread-Spectrum Circuit . . . 11
3.3 Cs Sample Capacitors - Sensitivity . . . 11
3.4 Power Supply . . . 11
3.5 PCB Layout and Construction . . . 11
4 Specifications . . . 12
4.1 Absolute Maximum Specifications . . . 12
4.2 Recommended Operating Conditions . . . 12
4.3 AC Specifications . . . 12
4.4 DC Specifications . . . 12
4.5 Signal Processing . . . 13
4.6 Average Idd Curves . . . 14
4.7 LP Mode Typical Response Times . . . 15
4.8 Mechanical - 32-QFN Package . . . 16
4.9 Part Marking . . . 17
4.10 Moisture Sensitivity Level (MSL) . . . 17
5 Datasheet Control . . . 18
5.1 Changes . . . 18
5.2 Numbering Convention . . . 18

1 Overview

1.1 Differences With QT1080

The QT1081 is a general replacement device for the highly popular QT1080. It has all of the same features as the older device but differs in the following ways:

- Rs resistors on each channel eliminated
- Up to 4x more sensitive for a given value of Cs
- Shorter burst lengths, less power for a given value of Cs
- 'Burst B' only mode for lower key counts with less power

The QT1081 should be used over the QT1080 for new designs due to a simpler circuit, lower power and lower cost.

1.2 Parameters

1.2.1 Introduction

The QT1081 is an easy to use, eight-touch-key sensor IC based on Quantum's patented charge-transfer principles for robust operation and ease of design. This device has many advanced features which provide for reliable, trouble-free operation over the life of the product.

1.2.2 Burst Operation

The device operates in 'burst mode'. Each key is acquired using a burst of charge-transfer sensing pulses whose count varies depending on the value of the reference capacitor Cs and the load capacitance Cx. In LP mode, the device sleeps in an ultra-low current state between bursts to conserve power. The keys' signals are acquired using two successive bursts of pulses:

Burst A: Keys 0, 1, 4, 5
Burst B: Keys 2, 3, 6, 7

Bursts always operate in A-B sequence.

1.2.3 Self-calibration

On power-up, all eight keys are self- calibrated within 300 milliseconds (typical) to provide reliable operation under almost any conditions.

1.2.4 Autorecalibration

The device can time out and recalibrate each key independently after a fixed interval of continuous touch detection, so that the keys can never become 'stuck on' due to foreign objects or other sudden influences. After recalibration the key will continue to function normally. The delay is selectable to be either 10s, 60s, or infinite (disabled).

The device also autorecalibrates a key when its signal reflects a sufficient decrease in capacitance. In this case the device recalibrates after ~2 seconds so as to recover normal operation quickly.

1.2.5 Drift Compensation

Drift compensation operates to correct the reference level of each key slowly but automatically over time, to suppress false detections caused by changes in temperature, humidity, dirt and other environmental effects.

The drift compensation is asymmetric; in the increasing capacitive load direction the device drifts more slowly than in the decreasing direction. In the increasing direction, the rate of compensation is one count of signal per 2 seconds; in the opposing direction, it is one count every 500ms.

1.2.6 Detection Integrator Confirmation

Detection Integrator (DI) confirmation reduces the effects of noise on the QT1081. The 'detect integrator' mechanism requires consecutive detections over a number of measurement bursts for a touch to be confirmed and indicated on the outputs. In a like manner, the end of a touch (loss of signal) has to be confirmed over a number of measurement bursts. This process acts as a type of 'debounce' against noise.

A per-key counter is incremented each time the key has exceeded its threshold and stayed there for a number of measurement bursts. When this counter reaches a preset limit the key is finally declared to be touched.

For example, if the limit value is six, then the device has to exceed its threshold and stay there for six measurement bursts in succession without going below the threshold level, before the key is declared to be touched. If on any measurement burst the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

In normal operation, both the start and end of a touch must be confirmed for six measurement bursts. In a special 'Fast Detect' mode (available via jumper resistors), confirmation of the start of a touch requires only two sequential detections, but confirmation of the end of a touch is still six bursts.

Fast detect is only available when AKS is disabled.

1.2.7 Spread-spectrum Operation

The bursts operate over a spread of frequencies, so that external fields will have minimal effect on key operation and emissions are very weak. Spread-spectrum operation works with the DI mechanism to dramatically reduce the probability of false detection due to noise.

1.2.8 Sync Mode

The QT1081 features a Sync mode to allow the device to slave to an external signal source, such as a mains signal (50/60Hz), to limit interference effects. This is performed using the SYNC/LP pin. Sync mode operates by triggering two sequential acquire bursts, in sequence A-B from the Sync signal. Thus, each Sync pulse causes all eight keys to be acquired.

1.2.9 Low Power (LP) Mode

The device features an LP mode for microamp levels of current drain with a slower response time, to allow use in battery operated devices. On touch detection, the device automatically reverts to its normal mode and asserts the DETECT pin active to wake up a host controller. The device remains in normal, full acquire speed mode until requested to return to LP mode.

When four or fewer keys are required, current drain in LP mode can be further reduced by choosing appropriate channels on the QT1081.

1.2.10 Adjacent Key Suppression (AKS™)

AKS™ is a Quantum-patented feature that can be enabled via resistor strap option. AKS works to prevent multiple keys from responding to a single touch, a common complaint about capacitive touch panels. This can happen with closely spaced keys, or with control surfaces that have water films on them.

AKS operates by comparing signal strengths from keys within a group of keys to suppress touch detections from those that have a weaker signal change than the dominant one.

The QT1081 has two different AKS groupings of keys, selectable via option resistors. These groupings are:

- AKS operates in two groups of four keys.
- AKS operates over all eight keys.

These two modes allow the designer to provide AKS while also providing for shift or function operations.

If AKS is disabled, all keys can operate simultaneously.

1.2.11 Outputs

There are two output modes: one-per-key, and binary coded.

One-per-key output: In this mode there is one output pin per key. This mode has two output drive options, push-pull and open-drain. The outputs can also be made either active-high or active-low. These options are set via external configuration resistors.

Binary coded output: In this mode, three output lines encode for one possible key in detect. If more than one key is detecting, only the first one touched will be indicated.

1.2.12 Simplified Mode

To reduce the need for option resistors, the simplified operating mode places the part into fixed settings with only the AKS feature being selectable. LP mode is also possible in this configuration. Simplified mode is suitable for most applications.

1.3 Wiring

Table 1.1 Pinlist

32-QFN Pin	Name	Type	Function	Notes	If Unused
1	SS	OD	Spread spectrum	Spread spectrum drive	100K resistor to Vss
2	/RST	I	Reset input	Active low reset	Vdd
3	Vdd	Pwr	Power	+2.8 ~ +5.0V	-
4	OSC	I	Oscillator	Resistor to Vdd and optional spread spectrum RC network	-
5	n/c	-	-	Leave open	-
6	SNS0	I/O	Sense pin and option select	To Cs0 and/or option resistor	Option resistor
7	SNS0K	I/O	Sense pin	To Cs0 + Key	Open
8	SNS1	I/O	Sense pin and option select	To Cs1 and/or option resistor*	Open or option resistor*
9	SNS1K	I/O	Sense pin	To Cs1 + Key	Open
10	SNS2	I/O	Sense pin and option select	To Cs2 and/or option resistor*	Open or option resistor*
11	SNS2K	I/O	Sense pin	To Cs2 + Key	Open
12	SNS3	I/O	Sense pin and option select	To Cs3 and/or option resistor*	Open or option resistor*
13	SNS3K	I/O	Sense pin	To Cs3 + Key	Open
14	SNS4	I/O	Sense pin and option select	To Cs4 and/or option resistor*	Open or option resistor*
15	SNS4K	I/O	Sense pin	To Cs4 + Key	Open
16	SNS5	I/O	Sense pin and option select	To Cs5 and/or option resistor*	Open or option resistor*
17	SNS5K	I/O	Sense pin	To Cs5 + Key	Open
18	SNS6	I/O	Sense pin and option select	To Cs6 and/or option resistor*	Open or option resistor*
19	SNS6K	I/O	Sense pin and mode select	To Cs6 + Key and/or mode resistor†	Open or mode resistor†
20	SNS7	I/O	Sense pin and mode or option select	To Cs7 and/or mode resistor† or option resistor*	Open or mode resistor† or option resistor*
21	SN7K	I/O	Sense pin	To Cs7 + Key	Open
22	Vss	Pwr	Ground	0V	-
23	SYNC/LP‡	I	Sync In or LP In	Rising edge sync or LP pulse	Vdd or Vss
24	DETECT	O/OD	Detect Status	Active = any key in detect	Open
25	OUT_0	O/OD	Out 0	Also, binary coded output 0	Open
26	OUT_1	O/OD	Out 1	Also, binary coded output 1	Open
27	OUT_2	O/OD	Out 2	Also, binary coded output 2	Open
28	OUT_3	O/OD	Out 3	In binary coded mode, these pins are clamped internally to Vss	Open
29	OUT_4	O/OD	Out 4		Open
30	OUT_5	O/OD	Out 5		Open
31	OUT_6	O/OD	Out 6		Open
32	OUT_7	O/OD	Out 7		Open

Pin Type

I	CMOS input only
I/O	CMOS I/O
O	CMOS push-pull output
OD	CMOS open drain output
O/OD	CMOS push pull or open-drain output (option selected)
Pwr	Power / ground

Notes

† Mode resistor is required only in Simplified mode (see Figure 1.2)

* Option resistor is required only in Full Options mode (see Figure 1.1)

‡ Pin is either Sync or LP depending on options selected (functions SL_0, SL_1, see Figure 1.1)

Figure 1.1 Connection Diagram - Full Options

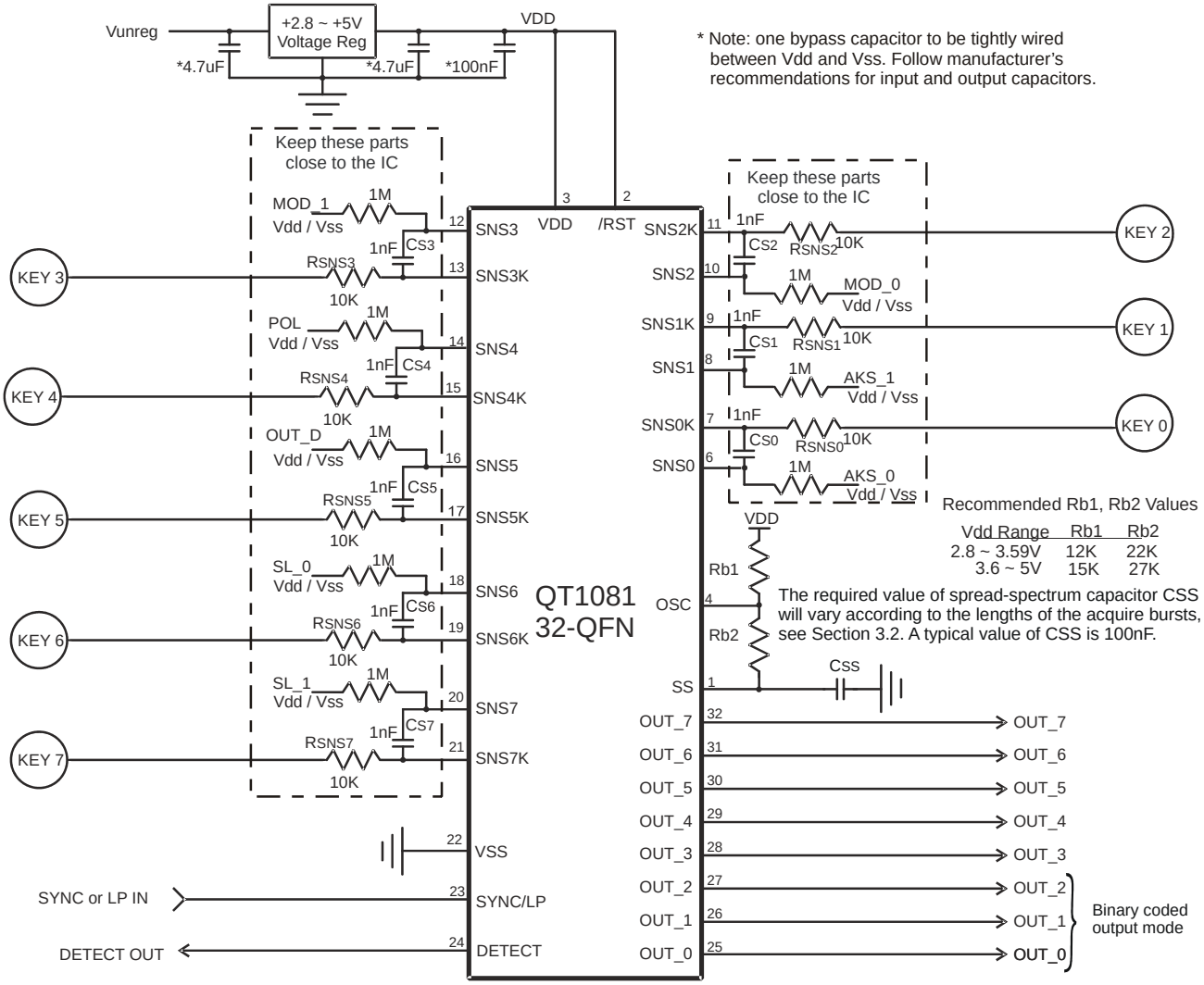


Table 1.2
AKS / Fast-Detect Options

AKS_1	AKS_0	AKS MODE	FAST-DETECT
Vss	Vss	Off	Off
Vss	Vdd	Off	Enabled
Vdd	Vss	On, in 2 groups	Off
Vdd	Vdd	On, global	Off

Table 1.3
Max On-Duration

MOD_1	MOD_0	MAX ON-DURATION MODE
Vss	Vss	10 seconds (nom) to recalibrate
Vss	Vdd	60 seconds (nom) to recalibrate
Vdd	Vss	Infinite (disabled)
Vdd	Vdd	(reserved)

Table 1.4
Polarity and Output

OUT_D	POL	OUT_n, DETECT PIN MODE
Vss	Vss	Binary coded, active high, push-pull
Vss	Vdd	One-per-key, active low, open-drain
Vdd	Vss	One-per-key, active high, push-pull
Vdd	Vdd	One-per-key, active low, push-pull

Table 1.5
SYNC/LP Function

SL_1	SL_0	SYNC/LP PIN MODE
Vss	Vss	Sync
Vss	Vdd	LP mode: 100ms nom response time
Vdd	Vss	LP mode: 180ms nom response time
Vdd	Vdd	LP mode: 340ms nom response time

Figure 1.2 Connection Diagram - Simplified Mode

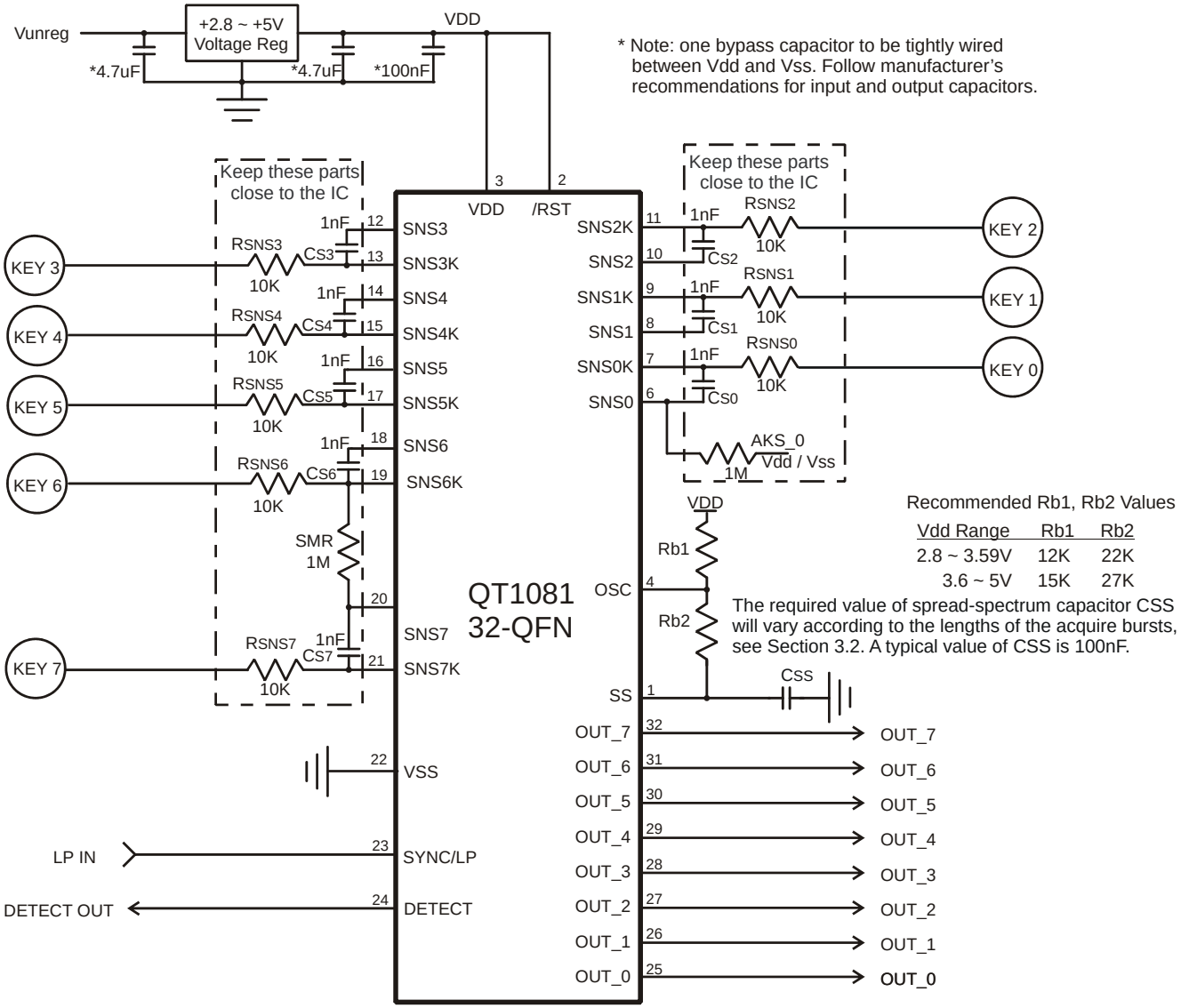


Table 1.6
AKS Resistor Options

AKS_0	AKS MODE	FAST-DETECT
Vss	Off	Enabled
Vdd	On, global	Off

Table 1.7
Functions in Simplified Mode

Function	Parameter
Output Drive, Polarity	One-per-key outputs, push-pull, active high
SYNC/LP pin	180ms nom LP function; sync not available
Max on-duration delay	60 seconds (nom)
Detect Pin	Active high on any detect

2 Device Operation

2.1 Start-up Time

After a reset or power-up event, the device requires 300ms to initialize, calibrate, and start operating normally. Keys will work properly once all keys have been calibrated after reset.

2.2 Option Resistors

The option resistors are read on power-up only; it is not possible to change the operating mode of the device once it has powered up. There are two primary option mode configurations: Full, and simplified.

Full options mode: Eight 1MΩ option resistors are required as shown in Figure 1.1. All eight resistors are mandatory.

Simplified mode: A 1MΩ resistor should be connected from SNS6K to SNS7. In simplified mode, only one additional 1MΩ option resistor is required for the AKS feature (Figure 1.2).

Note that the presence and connection of option resistors will affect the required values of Cs; this effect will be especially noticeable if the Cs values are under 22nF. Cs values should be adjusted for optimal sensitivity after the option resistors are connected.

2.3 One-per-key Output Mode

One-per-key output mode is selected via option resistors, as shown in Table 1.4.

In this mode, there is one output for each key; each is active when a touch is confirmed on the corresponding electrode. Unused OUT pins should be left open.

If AKS is off, it is possible for all OUT pins to be active at the same time.

Circuit of Figure 1.1: OUT polarity and drive are governed by the resistor connections to Vdd or Vss according to Table 1.4. The drive can be either push-pull or open-drain, active low or high.

Circuit of Figure 1.2: In this simplified circuit, the OUT pins are active high, push-pull only.

2.4 Binary Coded Output Mode

This mode is useful to reduce the number of connections to a host controller, at the expense of only being able to report one active key at a time. Note that in global AKS mode (Section 2.7), only one key can report active at a time anyway. Binary coded mode is selected via option resistors, as shown in Table 1.4.

In this mode, a key detection is registered as a binary code on pins OUT_2, OUT_1 and OUT_0, with possible values from 000 to 111. In practice, four lines are required to read the code, unless key 0 is not implemented; the output code 000 can mean either 'nothing detecting' or 'key 0 is detecting'. The fourth required line (if all eight keys are implemented) is the DETECT signal, which is active-high when any key is active.

The first key touched always wins and shows its output. Keys that come afterwards are hidden until the currently reported key has stopped detecting, in which case the code will change to a latent key.

Circuit of Figure 1.1: OUT polarity and drive can only be push-pull and active high.

Circuit of Figure 1.2: Binary coded not available.

2.5 DETECT Pin

DETECT represents the functional logical-OR of all eight keys. DETECT can be used to wake up a battery-operated product upon human touch.

DETECT is also required to indicate to a host when the binary coded output pins (in that mode) are showing an active key. While DETECT is active, the binary coded outputs should be read at least twice along with DETECT to make sure that the code was not transitioning between states, to prevent a false reading.

The output polarity and drive of DETECT are governed according to Table 1.4.

2.6 SYNC/LP Pin

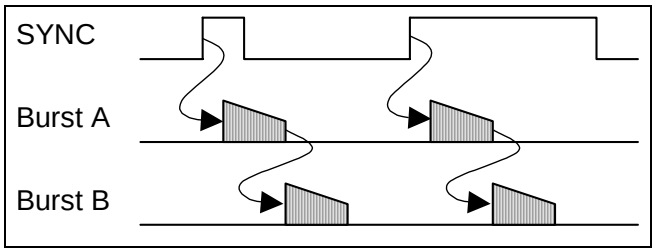
When full options are in use, the SYNC/LP pin function is selected according to the SL_0 and SL_1 resistor connections as given in Table 1.5. When the QT1081 is in sync mode the pin acts as a SYNC input; when the QT1081 is in LP mode the pin acts as an LP input.

When simplified options are in use, the QT1081 is always in LP mode and the SYNC/LP pin acts as an LP input.

Sync mode: Sync mode allows the designer to synchronize acquire bursts to an external signal source, such as mains frequency (50/60 Hz) to suppress interference. It can also be used to synchronize two QT parts which operate near each other, so that only one part generates acquire bursts at a time and hence they do not cross-interfere.

The SYNC input of the QT1081 is positive edge triggered. Following each rising edge the QT1081 will generate a pair of acquire bursts in A-B sequence; this operation is shown in Figure 2.1.

Figure 2.1 Acquire Bursts in A-B Sequence



If the SYNC input does not change level for ~150ms, the QT1081 will free-run, generating a continuous stream of acquire bursts A-B-A-B-A-... . While the QT1081 is in free-run operation, a rising edge on the SYNC input will return the QT1081 to synchronised operation.

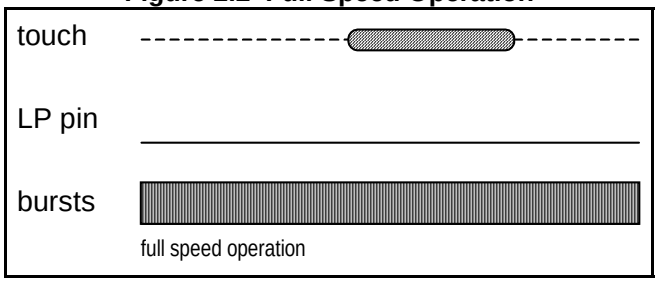
Note that the SYNC input must remain at one level (high or low) for >150µs to guarantee that the QT1081 will recognise that level.

Low Power LP Mode: LP mode allows the device to be switched between full speed operation (20ms typical response time and normal power consumption), and Low Power operation (low average power consumption but an increased maximum response time) according to the needs of the application. There are three maximum response time settings for low power operation: 100ms, 180ms, and 340ms nominal; the response time setting is determined by option resistors SL_1 and SL_0; see Table 1.5. Slower response times result in a lower average power drain.

Operation in low power mode is governed by the state of the LP input and whether at least one key has a confirmed touch.

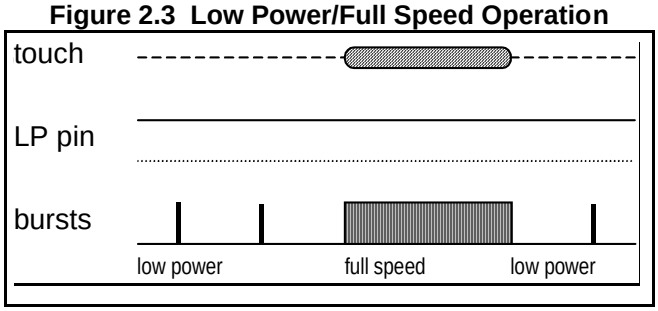
If the LP input is at a constant low level, then the QT1081 will remain in full speed operation (20ms typical response time and normal power consumption), as in Figure 2.2.

Figure 2.2 Full Speed Operation



If the LP input is at a constant high level, then the QT1081 will enter low power operation whenever it is not detecting a touch. It will switch automatically to full speed operation while there is a touch, and revert to low power operation at the end of the touch. This is shown in Figure 2.3.

Figure 2.3 Low Power/Full Speed Operation



While there is no touch, if the LP input is driven high then low, the QT1081 will enter low power operation, as described above, and remain in low power operation when LP is taken low. When there is a touch the QT1081 will switch automatically to full speed operation. At the end of the touch the choice of operation depends on the state of the LP input. This is shown in Figures 2.4 and 2.5 - the first with the LP pin being low at the end of the touch, and the second with the LP pin being high at the end of the touch.

Figure 2.4 LP Pin Low at End of Touch

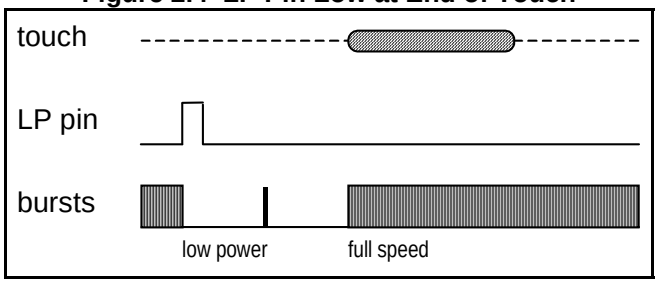
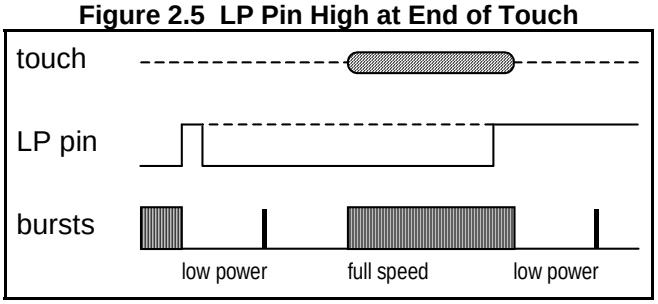


Figure 2.5 LP Pin High at End of Touch



Note that the LP input must remain at one level (high or low) for >150µs to guarantee that the QT1081 will recognise that level.

Optimization of LP Mode: For the lowest possible power consumption when up to four keys are required, all keys should be connected to QT1081 channels that are measured during acquire burst B (i.e. k2, k3, k6 and k7). If this is done the QT1081 automatically selects optimized LP operation, which gives a significantly lower power consumption than would be achieved if the burst A channels were used.

Optimized LP operation is identical to the standard LP operation in all other ways; it is controlled as described above.

2.7 AKS™ Function Pins

The QT1081 features an adjacent key suppression (AKS) function with two modes. Option resistors act to set this feature according to Tables 1.2 and 1.6. AKS can also be disabled, allowing any combination of keys to become active at the same time. When operating, the modes are:

Global: AKS functions operates across all eight keys. This means that only one key can be active at any one time.

Groups: AKS functions among two groups of four keys: 0-1-4-5 and 2-3-6-7. This means that up to two keys can be active at any one time.

In Group mode, keys in one group have no AKS interaction with keys in the other group.

Note that in Fast Detect mode, AKS can only be off.

2.8 MOD_0, MOD_1 Inputs

In full option mode, MOD_0 and MOD_1 resistors are used to set the 'Max On-Duration' recalibration timeouts. If a key becomes stuck on for a lengthy duration of time, this feature will cause an automatic recalibration event of that specific key once the specified on-time has been exceeded. Settings of 10s, 60s, and infinite are available.

The Max On-Duration feature operates on a key-by-key basis; when one key is stuck on, its recalibration has no effect on other keys.

The logic combination on the MOD option pins sets the timeout delay (see Table 1.3).

Simplified mode MOD timing: In simplified mode, the max on-duration is fixed at 60 seconds.

2.9 Fast Detect Mode

In many applications, it is desirable to sense touch at high speed. Examples include scrolling ‘slider’ strips or ‘Off’ buttons. It is possible to place the device into a ‘Fast Detect’ mode that usually requires under 10ms to respond. This is accomplished internally by setting the Detect Integrator to only two counts, i.e. only two successive detections are required to detect touch.

In LP mode, ‘Fast’ detection will not speed up the initial delay (which could be up to 340ms nominal depending on the option setting). However, once a key is detected the device is forced back into normal speed mode. It will remain in this faster mode until requested to return to LP mode.

When used in a ‘slider’ application, it is normally desirable to run the keys without AKS.

In both normal and ‘Fast’ modes, the time required to process a key release is the same. It takes six sequential confirmations of nondetection to turn a key off.

Fast Detect mode can be enabled as shown in Tables 1.2 and 1.6.

2.10 Simplified Mode

A simplified operating mode which does not require the majority of option resistors is available. This mode is set by connecting a resistor labelled SMR between pins SNS6K and SNS7 (see Figure 1.2).

In this mode there is only one option possible - AKS enable or disable. When AKS is disabled, Fast Detect mode is enabled; when AKS is enabled, Fast Detect mode is off.

AKS in this mode is Global only (i.e. operates across all functioning keys).

The other option features are fixed as follows:

OUT_n, DETECT Pins: Push-pull, active high, one-per-key outputs

SYNC/LP Function: LP mode, ~180ms response time

Max On-Duration: 60 seconds

See Tables 1.6 and 1.7.

2.11 Unused Keys

Unused keys should be disabled by removing the corresponding Cs, Rs, and Rsns components and connecting SNS pins as shown in the ‘Unused’ column of Table 1.1. Unused keys are ignored and do not factor into the AKS function (Section 2.7).

3 Design Notes

3.1 Oscillator Frequency

The QT1081's internal oscillator runs from an external resistor network connected to the OSC and SS pins, as shown in Figures 1.1 and 1.2, to achieve spread-spectrum operation. If spread-spectrum mode is not required, the OSC pin should be connected to Vdd with an 18KΩ one percent resistor.

Under different Vdd voltage conditions the resistor network (or the solitary 18KΩ resistor) might require minor adjustment to obtain the specified burst center frequency. The network should be adjusted slightly so that the positive pulses on any key are approximately 2.67µs wide in the 'solitary 18KΩ resistor' mode, or 2.87µs wide at the beginning of a burst with the recommended spread-spectrum circuit (see next section).

In practice, the pulse width has little effect on circuit performance if it varies in the range of 2µs to 3.3µs. The only effects seen will be proportional variations in Max On-Duration and non-LP mode response times.

3.2 Spread-Spectrum Circuit

The QT1081 offers the ability to spectrally spread its frequency of operation to heavily reduce susceptibility to external noise sources and to limit RF emissions. The SS pin is used to modulate an external passive RC network that modulates the OSC pin. OSC is the main oscillator current input. The circuit is shown in both Figures 1.1 and 1.2.

The resistors Rb1 and Rb2 should be changed depending on Vdd. As shown in Figures 1.1 and 1.2, two sets of values are recommended for these resistors depending on Vdd. The power curves in Section 4.6 also show the effect of these resistors.

The circuit can be eliminated, if it is not desired, by using an 18KΩ resistor from OSC to Vdd to drive the oscillator, and connecting SS to Vss with a 100KΩ resistor.

The spread-spectrum RC network will need to be adjusted according to the burst lengths. The sawtooth waveform observed on SS should reach a crest height as follows:

Vdd >= 3.6V: 17 percent of Vdd
Vdd < 3.6V: 20 percent of Vdd

The Css capacitor connected to the SS pin (Figures 1.1 and 1.2) should be adjusted so that the waveform approximates the above amplitude, ±10 percent, during normal operation in the target circuit. Where the bursts are of differing lengths, the adjustment should be done for the longer burst. If this is done, the circuit will give a spectral modulation of 12-15 percent.

Use of the spread-spectrum facility has the following effect on Idd:

- Full speed operation: Idd changes within ±10 percent.
- Idd increases by up to 15 percent.

In both cases the exact value depends on the precise circuit component values and timing. Vdd variations can shift the center frequency and spread slightly.

3.3 Cs Sample Capacitors - Sensitivity

The Cs sample capacitors accumulate the charge from the key electrodes and determine sensitivity. Higher values of Cs make the corresponding sensing channel more sensitive. The values of Cs can differ for each channel, permitting differences in sensitivity from key to key or to balance unequal sensitivities. Unequal sensitivities can occur due to key size and placement differences and stray wiring capacitances. More stray capacitance on a sense trace will desensitize the corresponding key; increasing the Cs for that key will compensate for the loss of sensitivity.

The Cs capacitors can be virtually any plastic film or low to medium-K ceramic capacitor. The normal Cs range is 1nF to 50nF depending on the sensitivity required; larger values of Cs require better quality to ensure reliable sensing. In certain circumstances the normal Cs range may be exceeded, hence the different values in Section 4.2. Acceptable capacitor types for most uses include PPS film, polypropylene film, and NP0 and X5R / X7R ceramics. Lower grades than X5R or X7R are not recommended.

The required values of Cs can be noticeably affected by the presence and connection of the option resistors (see Section 2.2). Cs values should be adjusted for optimal sensitivity after the option resistors are connected.

3.4 Power Supply

The power supply can range from 2.8 to 5.0 volts. If this fluctuates slowly with temperature, the device will track and compensate for these changes automatically with only minor changes in sensitivity. If the supply voltage drifts or shifts quickly, the drift compensation mechanism will not be able to keep up, causing sensitivity anomalies or false detections.

The power supply should be locally regulated, using a three-terminal device, to between 2.8V and 5.0V. If the supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags and surges which can cause adverse effects. It is not recommended to include a series inductor in the power supply to the QT1081.

For proper operation a 0.1µF or greater bypass capacitor must be used between Vdd and Vss; the bypass capacitor should be routed with very short tracks to the device's Vss and Vdd pins.

3.5 PCB Layout and Construction

Refer to Quantum application note AN-KD02 for information related to layout and construction matters.

4 Specifications

4.1 Absolute Maximum Specifications

Operating temperature, Ta. . . . . -40C to +85°C
Storage temp, Ts. . . . . -50°C to +125°C
Vdd. . . . . -0.3 to +6.0V
Max continuous pin current, any control or drive pin. . . . . ±20mA
Short circuit duration to ground or Vdd, any pin. . . . . infinite
Voltage forced onto any pin. . . . . -0.3V (Vdd + 0.3) Volts

4.2 Recommended Operating Conditions

Operating temperature, Ta. . . . . -40° to +85°C
V_{DD}. . . . . +2.8 to +5.0V
Short-term supply ripple+noise. . . . . ±5mV/s
Long-term supply stability. . . . . ±100mV
Cs range. . . . . 1nF to 100nF
Cx range. . . . . 0 to 50pF

4.3 AC Specifications

Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 1nF; circuit of Figure 1.1

Parameter	Description	Min	Typ	Max	Units	Notes
Trc	Recalibration time		150		ms	
Fc	Burst center frequency		132		kHz	
Fm	Burst modulation, percent		15		%	Total deviation
Tpc	Sample pulse duration		2		µs	Pulses appear 33 percent longer when viewed on an oscilloscope.
Tsu	Start-up time from cold start		300		ms	
Tbd	Burst duration		2.5		ms	Both bursts together
Tdf	Response time - Fast mode		6		ms	
Tdn	Response time - Normal mode		20		ms	
Tdl	Response time - LP mode		180		ms	180ms LP setting
Tdr	Release time - all modes		20		ms	End of touch

4.4 DC Specifications

Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 1nF; circuit of Figure 1.1 unless noted

Parameter	Description	Min	Typ	Max	Units	Notes
I_{DDN}	Average supply current, normal mode*		5.6 3.6 2.3 1.6	8	mA	@ Vdd = 5.0 @ Vdd = 4.0 @ Vdd = 3.3 @ Vdd = 2.8
I_{DDL}	Average supply current, LP mode*	22 15			µA	@ Vdd = 3.3V; 340ms LP mode @ Vdd = 2.8V; 340ms LP mode
	Average supply current, LP mode, keys on burst B only	15 10			µA	@ Vdd = 3.3V @ Vdd = 2.8V
V_{DDS}	Average supply turn-on slope	100			V/s	@ Vdd = 2.8V
V_{IL}	Low input logic level			0.7	V	
V_{HL}	High input logic level	3.5			V	
V_{OL}	Low output voltage			0.5	V	7mA sink
V_{OH}	High output voltage	Vdd-0.5			V	2.5mA source
I_{IL}	Input leakage current			±1	µA	
A_R	Acquisition resolution		8		bits	

***No spread spectrum circuit; Rosc = 18KΩ**

4.5 Signal Processing

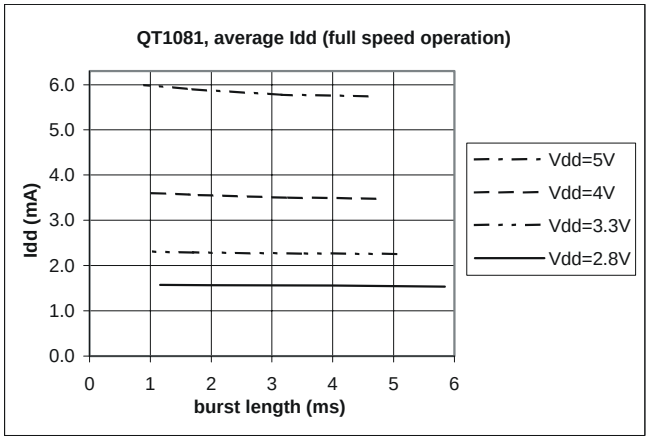
Vdd = 5.0, Ta = recommended, Cx = 5pF, Cs = 1nF

Description	Value	Units	Notes
Detection threshold	10	counts	Threshold for increase in Cx load
Detection hysteresis	2	counts	
Anti-detection threshold	6	counts	Threshold for decrease of Cx load
Anti-detection recalibration delay	2	secs	Time to recalibrate if Cx load has exceeded anti-detection threshold
Detect Integrator filter, normal mode	6	samples	Must be consecutive or detection fails
Detect Integrator filter, 'fast' mode	2	samples	Must be consecutive or detection fails
Max On-Duration	10, 60, ∞	secs	Option pin selected
Normal drift compensation rate	2,000	ms/level	Towards increasing Cx load
Anti-drift compensation rate	500	ms/level	Towards decreasing Cx load

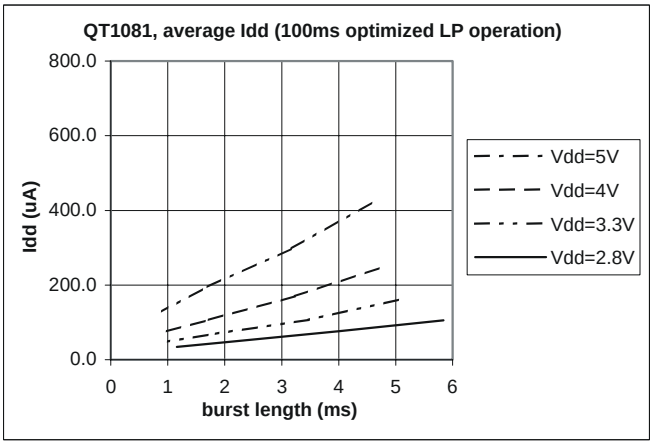
4.6 Average Idd Curves

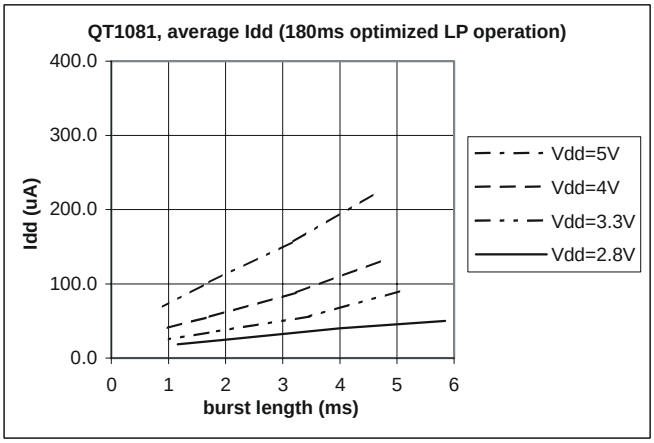
All Idd curves are average values, under the following conditions: Cx = 5pF, Ta = 20°C, Rosc = 18KΩ; no spread-spectrum circuit. Refer to page 9 for more information about optimization of LP modes.

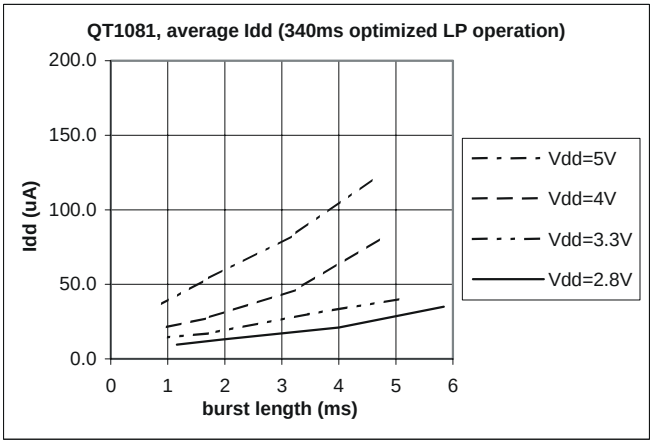
Full speed operation



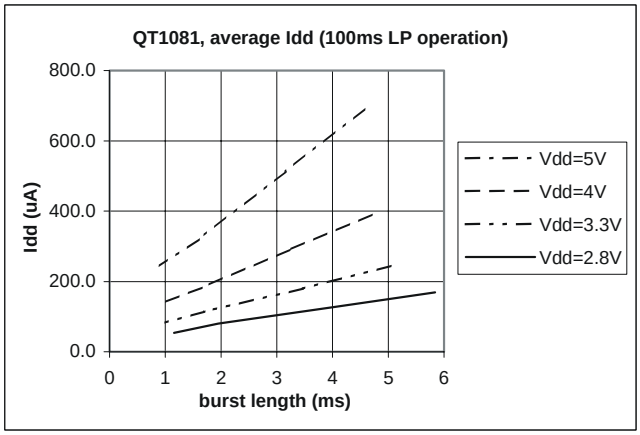
Low Power operation (optimized - only burst B in use)

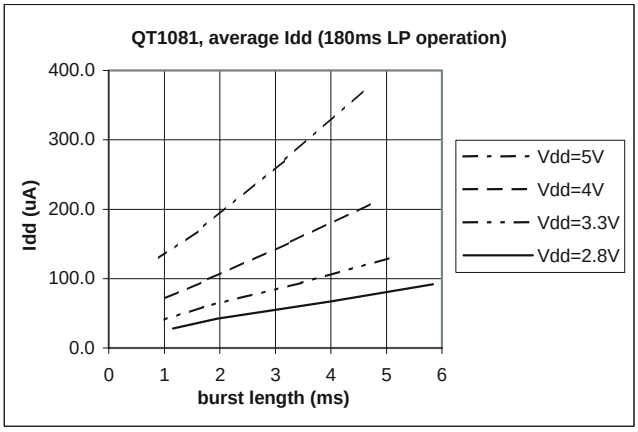


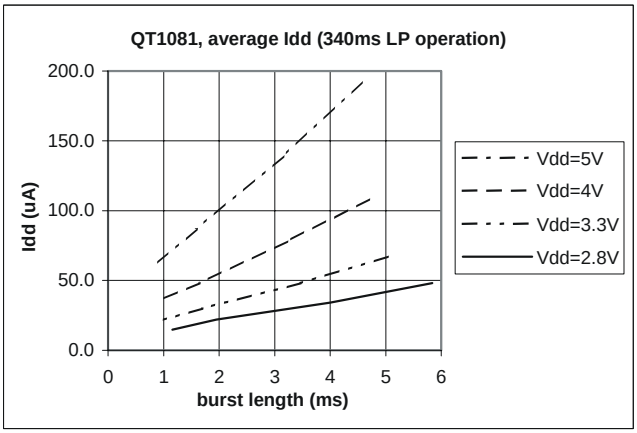




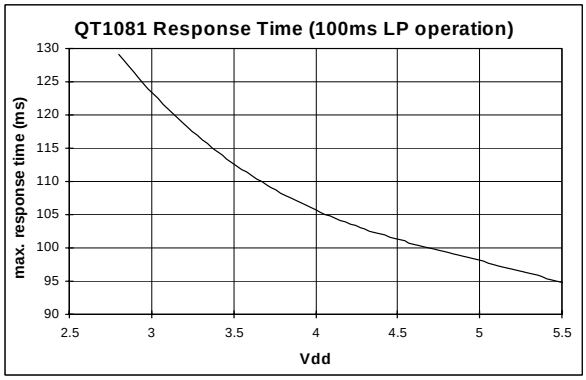
Low Power operation (non-optimized)

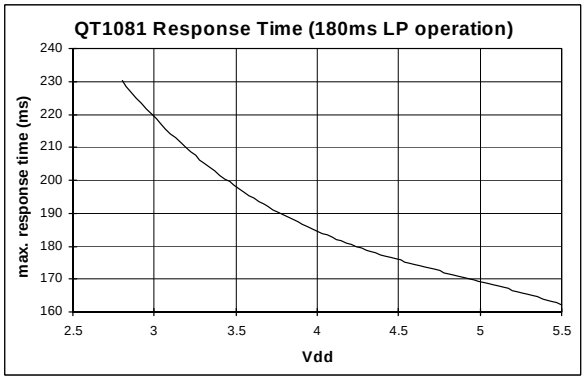


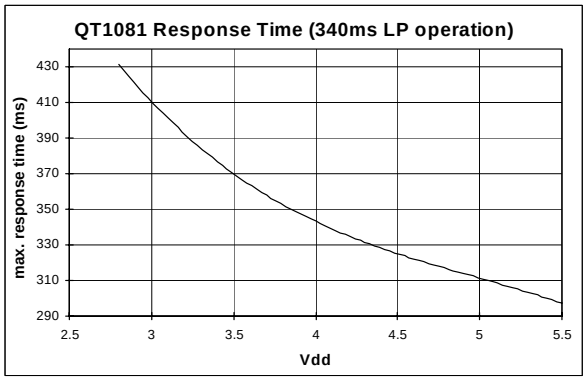




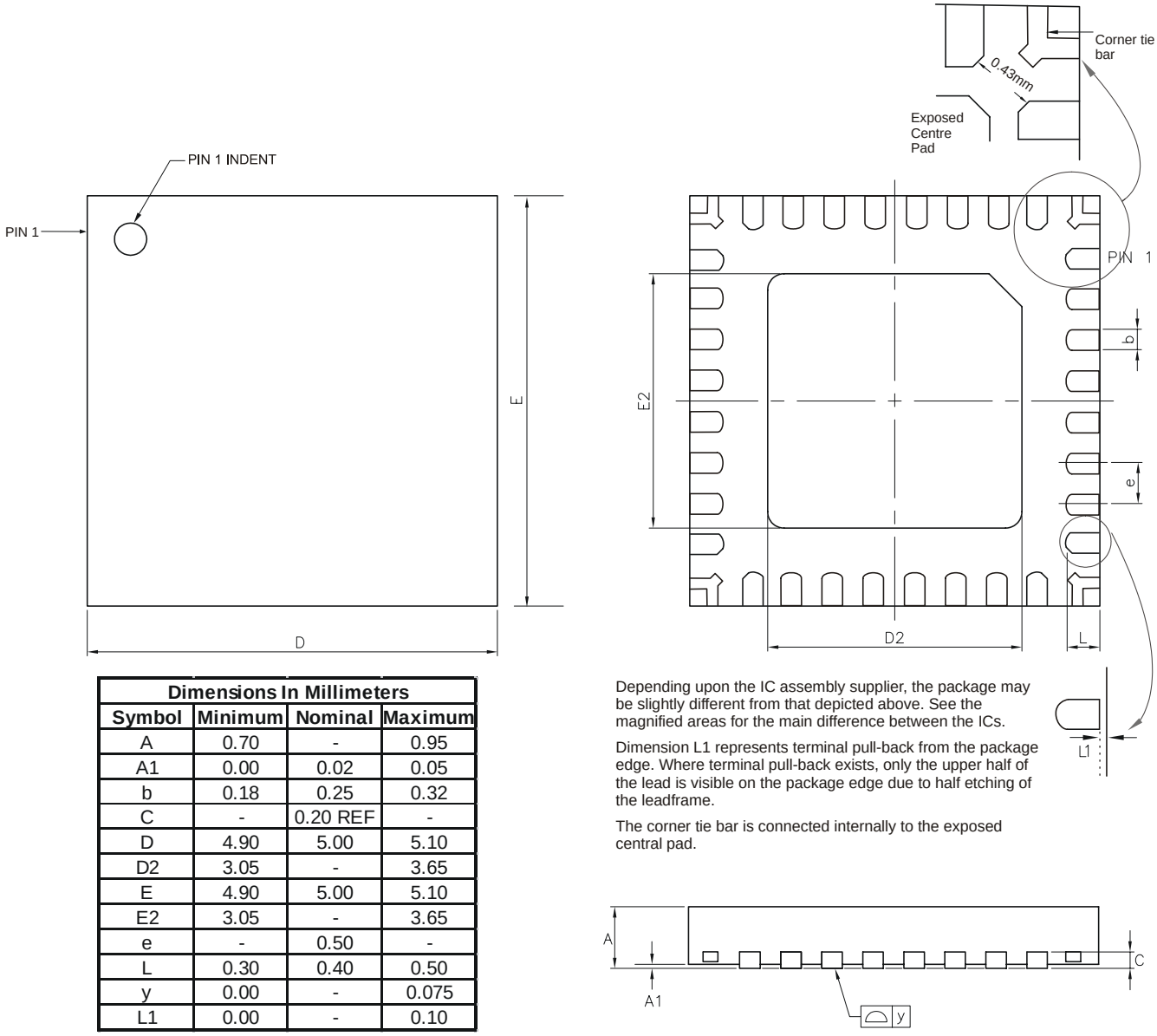
4.7 LP Mode Typical Response Times







4.8 Mechanical - 32-QFN Package



Dimensions In Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
A	0.70	-	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.32
C	-	0.20 REF	-
D	4.90	5.00	5.10
D2	3.05	-	3.65
E	4.90	5.00	5.10
E2	3.05	-	3.65
e	-	0.50	-
L	0.30	0.40	0.50
y	0.00	-	0.075
L1	0.00	-	0.10

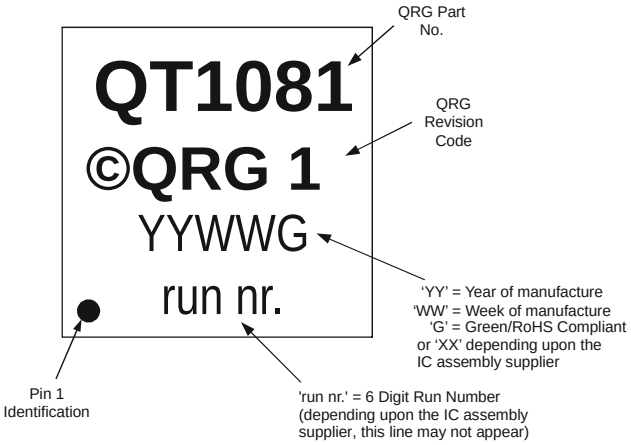
Depending upon the IC assembly supplier, the package may be slightly different from that depicted above. See the magnified areas for the main difference between the ICs.

Dimension L1 represents terminal pull-back from the package edge. Where terminal pull-back exists, only the upper half of the lead is visible on the package edge due to half etching of the leadframe.

The corner tie bar is connected internally to the exposed central pad.

Note that there is no functional requirement for the large pad on the underside of this package to be soldered. If the final application requires this area to be soldered for mechanical reasons, the pad to which it is soldered must be isolated and contained under the footprint only.

4.9 Part Marking



4.10 Moisture Sensitivity Level (MSL)

MSL Rating	Peak Body Temperature	Specifications
MSL3	260^{O}C	IPC/JEDEC J-STD-020C

5 Datasheet Control

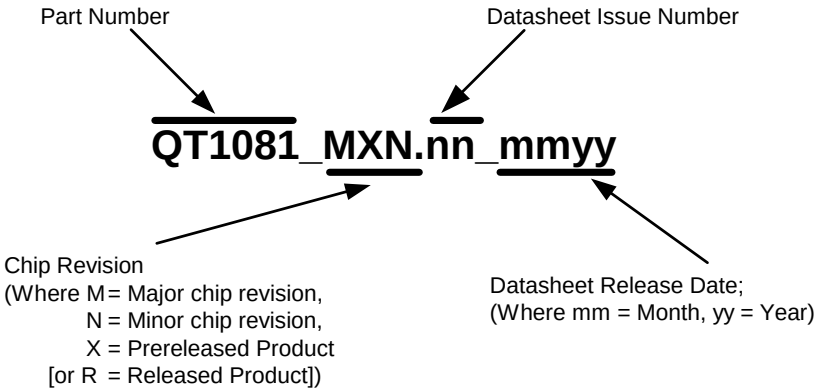
5.1 Changes

Changes this issue (datasheet rev 04)

Changes throughout to remove 48-SSOP package.

Section 5: new.

5.2 Numbering Convention



A minor chip revision (N) is defined as a revision change which does not affect product functionality or datasheet. The value of N is only stated for released parts (R).

NOTES:

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