

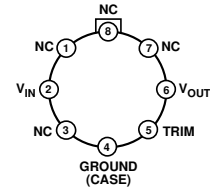
FEATURES

- 5 V output: $\pm 0.3\%$ maximum
- Temperature voltage output: $1.96 \text{ mV}/^\circ\text{C}$
- Adjustment range: $\pm 3\%$ minimum
- Excellent temperature stability: $8.5 \text{ ppm}/^\circ\text{C}$ maximum
- Low noise: $15 \text{ }\mu\text{V p-p}$ maximum
- Low supply current: 1.4 mA maximum
- Wide input voltage range: 7 V to 40 V
- High load-driving capability: 10 mA
- No external components
- Short-circuit proof

GENERAL DESCRIPTION

The REF02 precision voltage reference provides a stable 5 V output that can be adjusted over a $\pm 6\%$ range with minimal effect on temperature stability. Single-supply operation over an input voltage range of 7 V to 40 V , low current drain of 1 mA , and excellent temperature stability are achieved with an improved band gap design. Low cost, low noise, and low power make the REF02 an excellent choice whenever a stable voltage reference is required. Applications include DACs and ADCs, portable instrumentation, and digital voltmeters. The versatility of the REF02 is enhanced by its use as a monolithic temperature transducer. For new designs, refer to the ADR02.

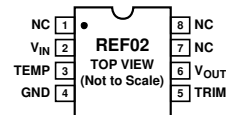
PIN CONFIGURATIONS



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00075-F-001

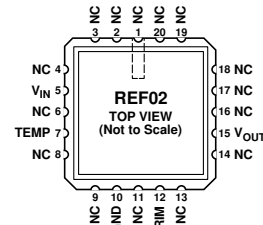
Figure 1. 8-Lead TO-99 (J-Suffix)



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00075-F-002

Figure 2. 8-Lead PDIP (P-Suffix), 8-Lead Cerdip (Z-Suffix) and 8-Lead SOIC (S-Suffix)



NC = NO CONNECT. DO NOT CONNECT ANYTHING ON THESE PINS. SOME OF THEM ARE RESERVED FOR FACTORY TESTING PURPOSES.

00075-F-003

Figure 3. 20-Terminal LCC (RC-Suffix)

OUTPUT RESISTORS			
REF02 OPTION	R9	R11	R12
883C PRODUCT	$18\text{k}\Omega$	$2\text{k}\Omega$	$6.1\text{k}\Omega$
P, S, J, Z PACKAGES	$18\text{k}\Omega$	$4.5\text{k}\Omega$	$15\text{k}\Omega$

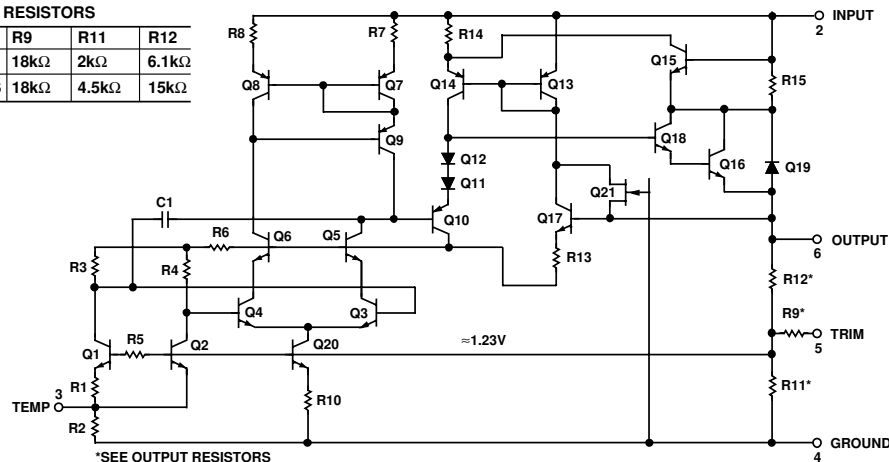


Figure 4. Simplified Schematic

Rev. I

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REVISION HISTORY

12/05—Rev. H to Rev. I

Changes to Figure 14.....	10
Changes to Ordering Guide	15

5/05—Rev. G to Rev. H

Updated Figure 4	1
Changes to Specifications	3
Updated Outline Dimensions	13
Changes to Ordering Guide	15

2/05—Rev. F to Rev. G

Changes to Specifications	3
Change to Outline Dimensions	13

7/04—Rev. E to Rev. F

Updated Format.....	Universal
Changes to Simplified Schematic	1
Changes to Specifications	3
Changes to Specifications	4
Changes to Specifications	5
Changes to Specifications	6
Changes to Figure 18.....	10
Changes to Ordering Guide	15

3/04—Rev. D to Rev. E

Changes to Features.....	1
Changes to Specifications	2
Changes to Ordering Guide	4
Replaced TPCs 3 and 4	5
Added Temperature Monitoring section	7
Updated Figure 5	7
Deleted Table I	7
Updated Figure 6	7

10/03—Rev. C to Rev. D

Updated TPCs.....	Universal
Changes to Features	1
Changes to Electrical Specifications	2
Change to Absolute Maximum Ratings	4
Changes to Ordering Guide	4
Deleted Typical Electrical Characteristics table	4
Deleted Wafer Test Limits	4
Deleted Figure 1	4

10/02—Rev. B to Rev. C

Changes to Features	1
Changes to General Description	1
Changes to Simplified Schematic	1
Changes to Specifications.....	2
Changes to Absolute Maximum Ratings	5
Changes to Package Type	5
Changes to Ordering Guide	5
Updated to Outline Dimensions	11

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

@ $V_{IN} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	REF02A/REF02E			REF02/REF02H			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	$I_L = 0\text{ mA}$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{TRIM}	$R_P = 10\text{ k}\Omega$	± 3	± 6		± 3	± 6		%
Output Voltage Noise ¹	e_n p-p	0.1 Hz to 10 Hz							
P, Z, and S Packages				15			15		$\mu\text{V p-p}$
J Package				20			20		$\mu\text{V p-p}$
883 Parts				10	15		10	15	$\mu\text{V p-p}$
Line Regulation ²		$V_{IN} = 8\text{ V to }40\text{ V}$		0.006	0.010		0.006	0.010	%/V
Load Regulation ²		$I_L = 0\text{ mA to }10\text{ mA}$		0.005	0.010		0.006	0.010	%/mA
Turn-On Settling Time ¹	t_{ON}	To $\pm 0.1\%$ of final value		5			5		μs
Quiescent Supply Current	I_{SY}	No load		1.0	1.4		1.0	1.4	mA
Load Current	I_L		10			10			mA
Sink Current ³	I_S		-0.3	-0.5		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	$V_O = 0$		30			30		mA
Temperature Voltage Output ⁴									
883C Product	V_T			630			630		mV
P, S, J, and Z Packages	V_T			550			550		mV

¹ Guaranteed by design.

² Line and load regulation specifications include the effect of self-heating.

³ During sink current test, the device meets the output voltage specified.

⁴ Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

REF02

@ $V_{IN} = 15\text{ V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for REF02A and REF02; $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for REF02E and REF02H; $I_L = 0\text{ mA}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	REF02A/REF02E			REF02/REF02H			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage Change with Temperature ^{1, 2}	ΔV_{OT}	$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		0.02	0.06		0.07	0.17	%
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient ³	TCV_O			3	8.5		10	25	ppm/ $^{\circ}\text{C}$
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10\text{ k}\Omega$		0.7			0.7		ppm/%
Line Regulation $V_{IN} = 8\text{ V to }40\text{ V}^4$		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		0.007	0.012		0.007	0.012	%/V
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.009	0.015		0.009	0.015	%/V
Load Regulation $I_L = 0\text{ mA to }8\text{ mA}^4$		$0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		0.006	0.010		0.007	0.012	%/mA
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		0.007	0.012		0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient ⁵ 883C Product	TCV_T			2.10			2.10		mV/ $^{\circ}\text{C}$
P, S, J, and Z Packages				1.96			1.96		mV/ $^{\circ}\text{C}$

¹ ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5 V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5\text{ V}} \right| \times 100$$

² ΔV_{OT} specification applies trimmed to 5,000 V or untrimmed.

³ TCV_O is defined as ΔV_{OT} divided by the temperature range.

$$TCV_O = \frac{\Delta V_{OT}}{70^{\circ}\text{C}}$$

⁴ Line and load regulation specifications include the effect of self-heating.

⁵ Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

@ $V_{IN} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	REF02C			REF02D			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O	$I_L = 0\text{ mA}$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{TRIM}	$R_P = 10\text{ k}\Omega$	± 2.7	± 6.0		± 2.0	± 6.0		%
Output Voltage Noise ¹ P, Z, and S Packages	e_n p-p	0.1 Hz to 10 Hz		15					$\mu\text{V p-p}$
J Package				20			15		$\mu\text{V p-p}$
883 Parts				12	18		20		$\mu\text{V p-p}$
Line Regulation ²		$V_{IN} = 8\text{ V to } 40\text{ V}$		0.009	0.015		0.010	0.04	%/V
Load Regulation ²		$I_L = 0\text{ mA to } 8\text{ mA}$		0.006	0.015				%/mA
		$I_L = 0\text{ mA to } 4\text{ mA}$					0.015	0.04	%/mA
Turn-On Settling Time ¹	t_{ON}	To $\pm 0.1\%$ of final value		5			5		μs
Quiescent Supply Current	I_{SY}	No load		1.0	1.6		1.0	2.0	mA
Load Current	I_L		8			8			mA
Sink Current ³	I_S		-0.3	-0.5		-0.3	-0.5		mA
Short-Circuit Current	I_{SC}	$V_O = 0$		30			30		mA
Temperature Voltage Output ⁴ 883C Product	V_T			630			630		mV
P, S, J, and Z Packages	V_T			550			550		mV

¹ Guaranteed by design.

² Line and load regulation specifications include the effect of self-heating.

³ During sink current test, the device meets the output voltage specified.

⁴ Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

REF02

@ $V_{IN} = 15\text{ V}$, $I_L = 0\text{ mA}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for REF02CJ, REF02CZ, and REF02DP; and $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for REF02CP and REF02CS, unless otherwise noted.

Table 4.

Parameter	Symbol	Conditions	REF02C			REF02D			Unit
			Min	Typ	Max	Min	Typ	Max	
Output Voltage Change with Temperature ^{1,2}	ΔV_{OT}			0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient ³	TCV_O	$R_P = 10\text{ k}\Omega$		20	65		70	250	ppm/ $^\circ\text{C}$
Change in V_O Temperature Coefficient with Output Adjustment				0.7			0.7		ppm/%
Line Regulation ⁴		$V_{IN} = 8\text{ V to }40\text{ V}$		0.011	0.018		0.012	0.05	%/V
Load Regulation ⁴		$I_L = 0\text{ mA to }5\text{ mA}$		0.008	0.018		0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient ⁵	TCV_T								
883C Product				2.10			2.10		mV/ $^\circ\text{C}$
P, S, J, and Z Packages				1.96			1.96		mV/ $^\circ\text{C}$

¹ ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5 V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5\text{ V}} \right| \times 100$$

² ΔV_{OT} specification applies trimmed to 5,000 V or untrimmed.

³ TCV_O is defined as ΔV_{OT} divided by the temperature range.

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ\text{C}}$$

⁴ Line and load regulation specifications include the effect of self-heating.

⁵ Limit current in or out of Pin 3 to 50 nA and capacitance on Pin 3 to 30 pF.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating ¹
Input Voltage	40 V
Output Short-Circuit Duration to Ground or V_{IN}	Indefinite
Storage Temperature Range	
J, RC, and Z Packages	–65°C to +150°C
P Package	–65°C to +125°C
Operating Temperature Range	
REF02A, REF02J, REF02RC	–55°C to +125°C
REF02CJ, REF02CZ	0°C to 70°C
REF02CP, REF02CS, REF02E, and REF02H	–40°C to +85°C
Lead Temperature Range (Soldering 10 sec)	300°C

¹ Absolute maximum ratings apply to both DICE packaged parts, unless otherwise noted.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA} ¹	θ_{JC}	Unit
TO-99 (J)	170	24	°C/W
8-Lead CERDIP (Z)	162	26	°C/W
8-Lead PDIP (P)	110	50	°C/W
20-Terminal Ceramic LCC (RC)	120	40	°C/W
8-Lead SOIC (S)	160	44	°C/W

¹ θ_{JA} is specified for worst-case mounting conditions; device in socket for TO, CERDIP, PDIP, and LCC packages; and device soldered to printed circuit board for SOIC package.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

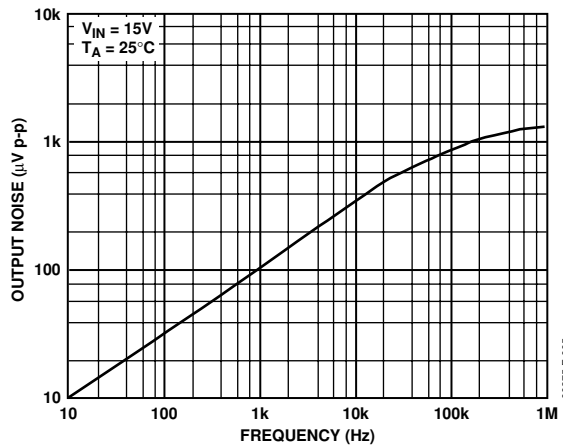


Figure 5. Output Wideband Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)

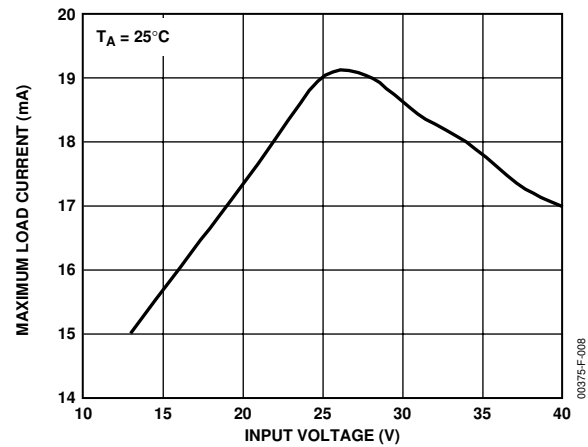


Figure 8. Maximum Load Current vs. Input Voltage

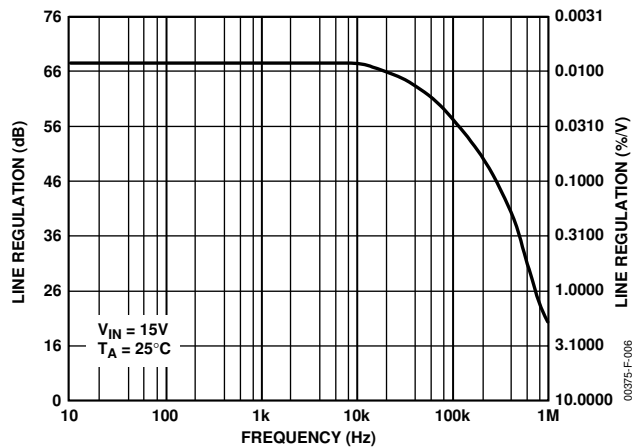


Figure 6. Line Regulation vs. Frequency

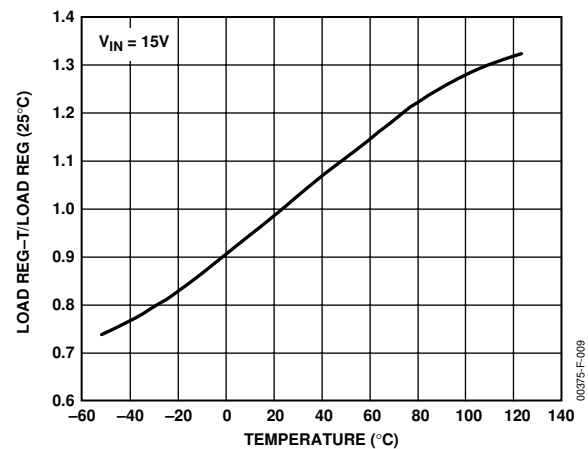


Figure 9. Normalized Load Regulation ($\Delta I_L = 10\text{ mA}$) vs. Temperature

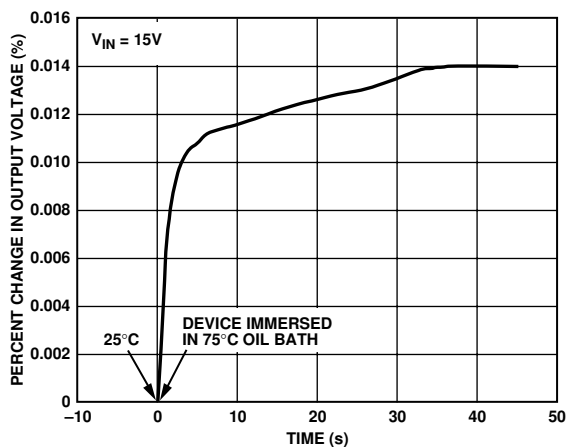


Figure 7. Output Change Due to Thermal Shock

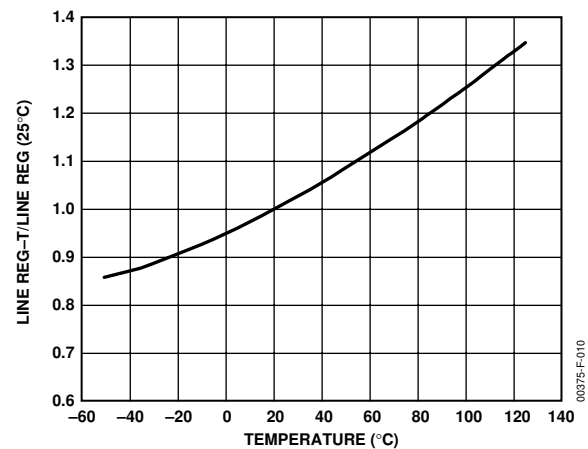


Figure 10. Normalized Line Regulation vs. Temperature

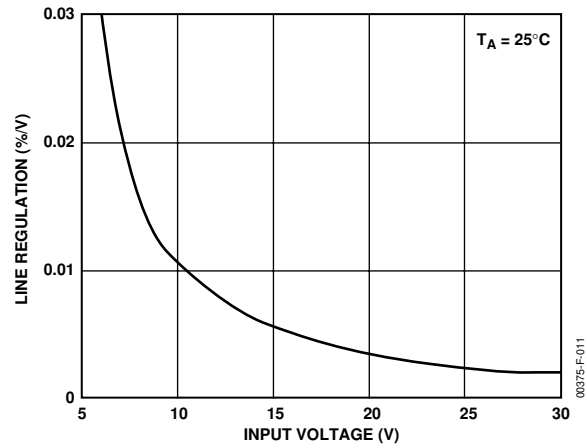


Figure 11. Line Regulation vs. Input Voltage

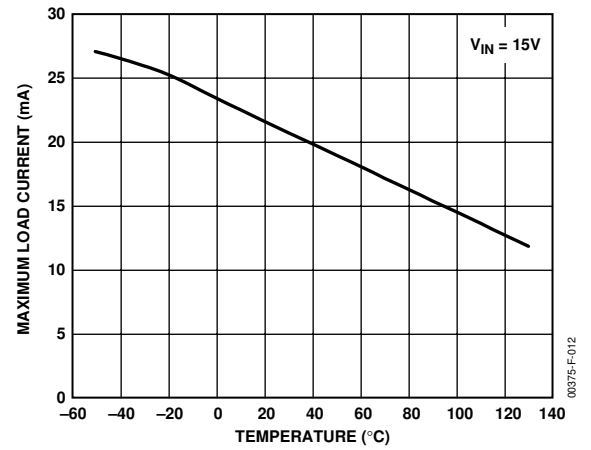


Figure 13. Maximum Load Current vs. Temperature

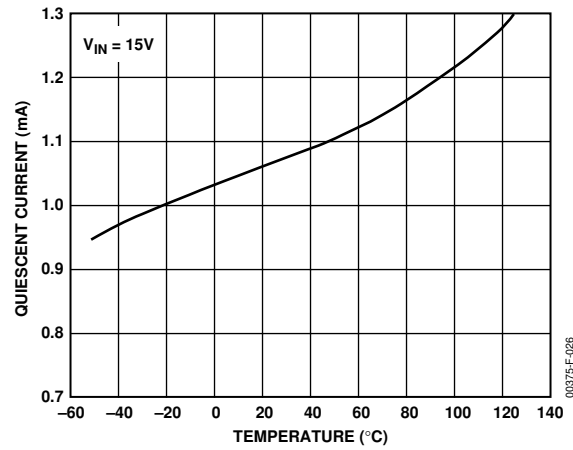


Figure 12. Quiescent Current vs. Temperature

REF02

OUTPUT ADJUSTMENT

The REF02 trim terminal can be used to adjust the output voltage over a $5\text{ V} \pm 300\text{ mV}$ range. This feature lets the system designer trim system errors by setting the reference to a voltage other than 5 V. The output also can be set to exactly 5.00 V or to 5.12 V for binary applications.

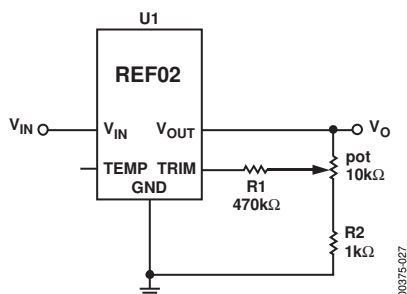


Figure 14. Output Adjustment Circuit

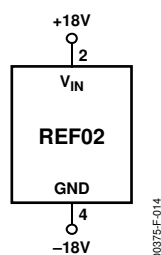


Figure 15. Burn-In Circuit

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately $0.7\text{ ppm}/^{\circ}\text{C}$ for 100 mV of output adjustment.

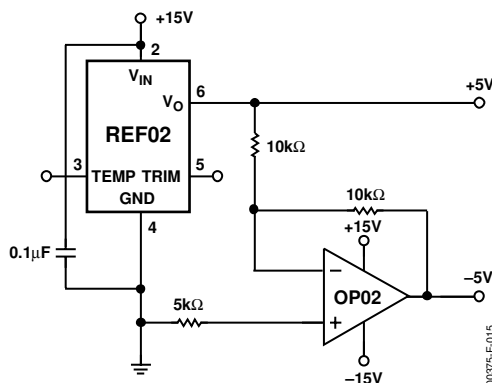


Figure 16. $\pm 5\text{ V}$ Reference

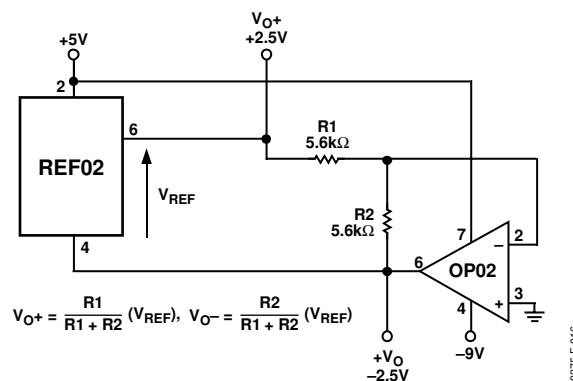


Figure 17. $\pm 2.5\text{ V}$ Reference

TEMPERATURE MONITORING

The REF02 provides a TEMP output (Pin 3) that varies linearly with temperature. This output can be used to monitor the temperature change in the system. The voltage at V_{TEMP} is approximately 550 mV at 25°C, and the temperature coefficient is approximately 1.96 mV/°C (see Figure 18).

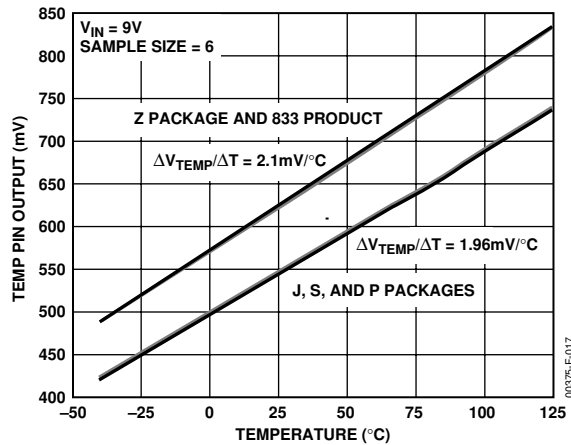


Figure 18. Voltage at TEMP Pin vs. Temperature

A voltage change of 39.2 mV at the TEMP pin corresponds to a 20°C change in temperature.

The TEMP function is provided as a convenience rather than a precise feature. Since the voltage at the TEMP node is acquired from the band gap core, current pulling from this pin has a significant effect on V_{OUT} . Care must be taken to buffer the TEMP output with a suitable low bias current op amp, such as the AD8601, AD820, or OP1177. Using any of these three op amps results in less than a 100 μ V change in ΔV_{OUT} (see Figure 19). Without buffering, even tens of microamps drawn from the TEMP pin can cause V_{OUT} to fall out of specification.

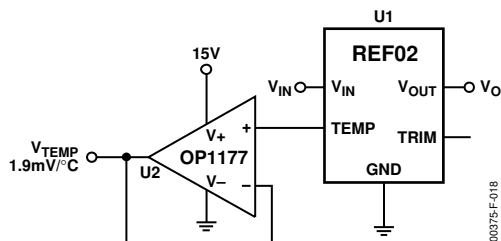


Figure 19. Temperature Monitoring

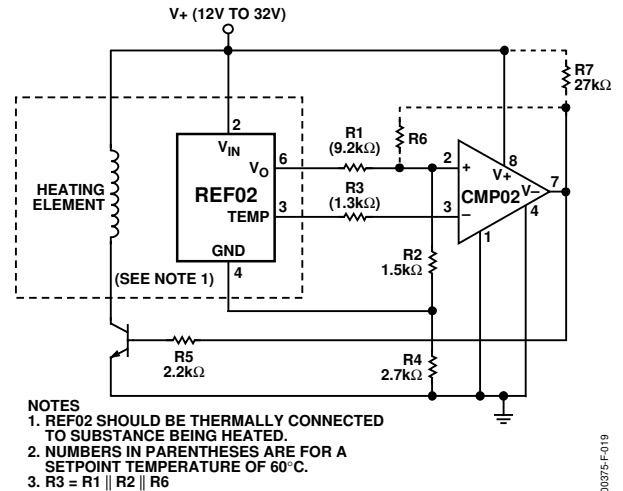


Figure 20. Temperature Controller

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF01s and one REF02 can be stacked to yield 5.00 V, 15.00 V, and 25.00 V outputs. An additional advantage is near-perfect line regulation of the 5.0 V and 15.0 V output. A 27 V to 55 V input change produces an output change that is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SV}) of the 15.00 V regulator.

In general, any number of REF01s and REF02s can be stacked this way. For example, 10 devices yield 10 outputs in 5 V or 10 V steps. The line voltage can change from 100 V to 130 V. Care must be taken, however, to ensure that the total load currents do not exceed the maximum usable current (typically 21 mA).

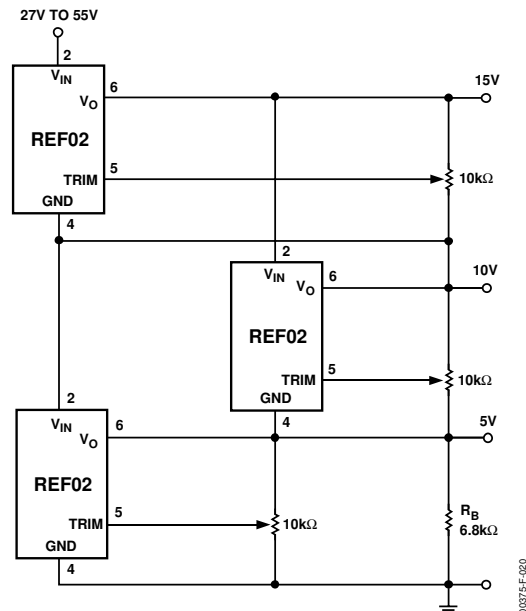


Figure 21. Reference Stack

REF02

PRECISION CURRENT SOURCE

A current source with 35 V output compliance and excellent output impedance can be obtained using this circuit. REF02 keeps the line voltage and power dissipation constant in the device; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3 \mu\text{V/V}$ PSRR of the OP02E creates a 20 ppm change ($3 \mu\text{V/V} \times 35 \text{ V/5 V}$) in output current over a 25 V range. For example, a 5 mA current source can be built ($R = 1 \text{ k}\Omega$) with $350 \text{ M}\Omega$ output impedance.

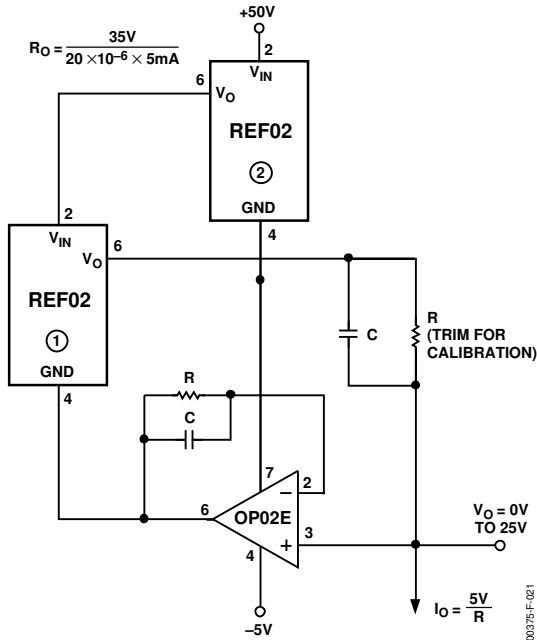


Figure 22. Precision Current Source

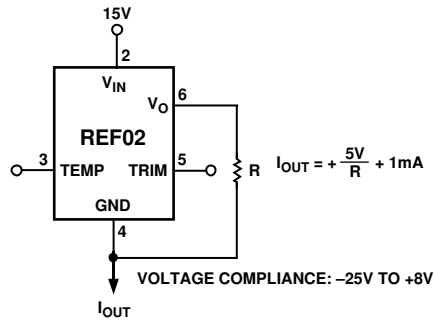


Figure 23. Current Source

SUPPLY BYPASSING

For best results, it is recommended that the power supply pin be bypassed with a $0.1 \mu\text{F}$ disc ceramic capacitor.

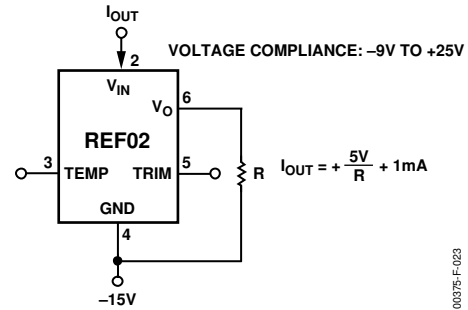


Figure 24. Current Sink

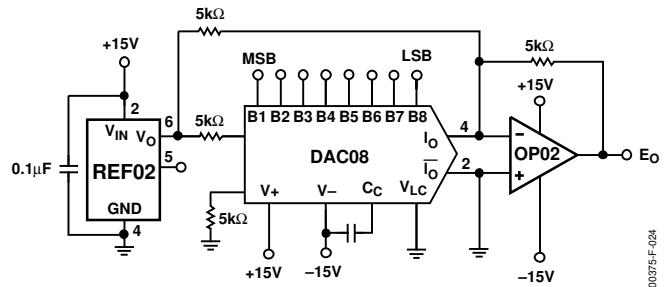


Figure 25. DAC Reference

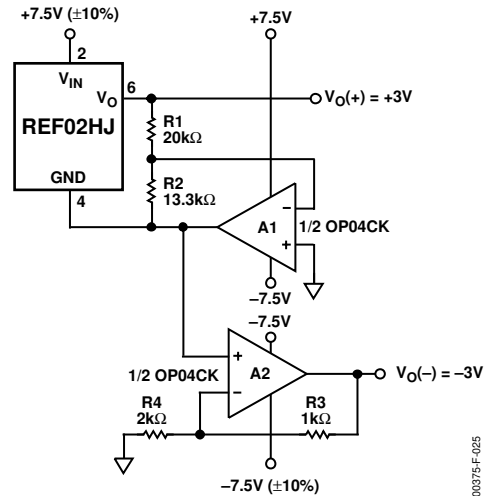
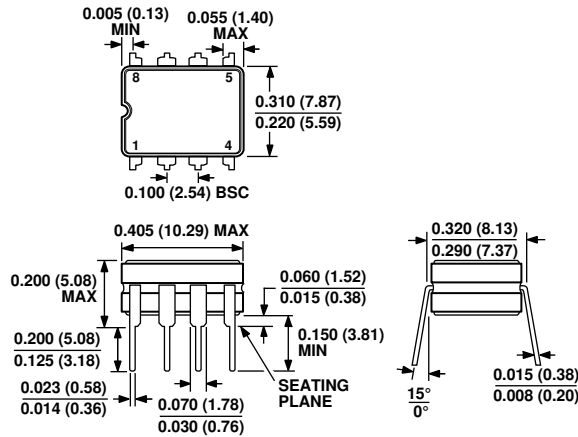


Figure 26. $\pm 3 \text{ V}$ Reference

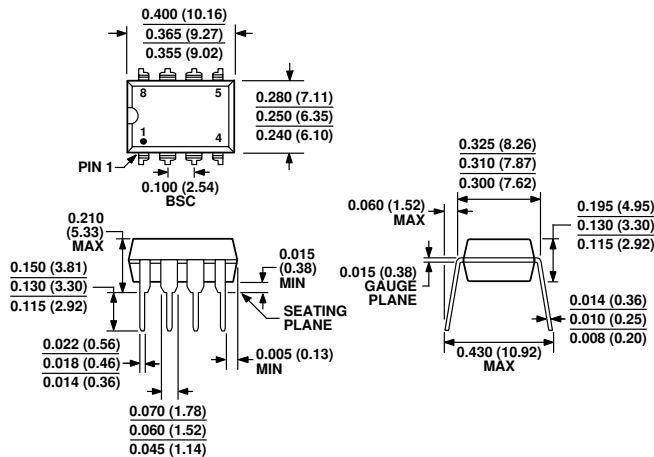
OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 27. 8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix
(Q-8)

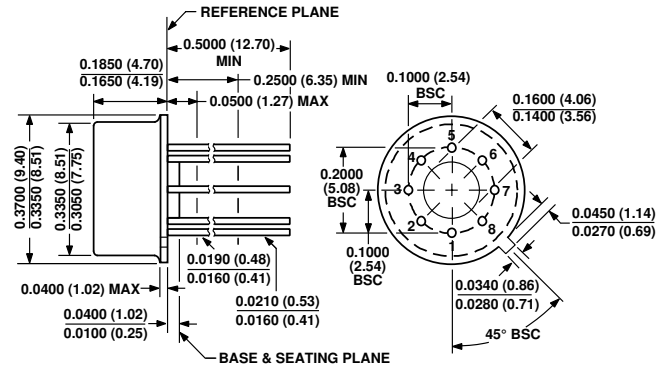
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001-BA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 28. 8-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
P-Suffix
(N-8)

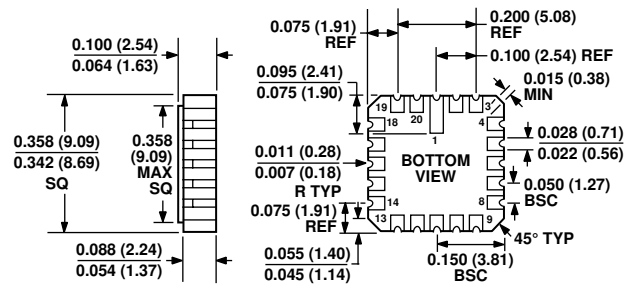
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002-AK
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 29. 8-Lead Metal Header Package [TO-99]
J-Suffix
(H-08)

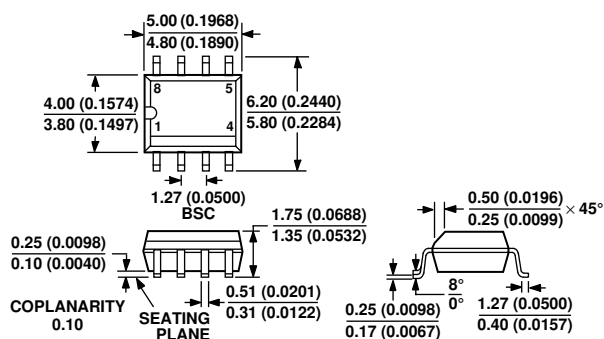
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 30. 20-Terminal Ceramic Leadless Chip Carrier [LCC]
RC-Suffix
(E-20A)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 31. 8-Lead Standard Small Outline Package [SOIC]

Narrow Body

S-Suffix

(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	$T_A = 25^\circ\text{C}$ $\Delta V_{OS} \text{ Max (mV)}$	Temperature Range	Package Description	Package Option
REF02AJ/883C ¹	±15	–55°C to +125°C	8-Lead TO-99	J-Suffix (H-08)
REF02AZ	±15	–55°C to +125°C	8-Lead Cerdip	Z-Suffix (Q-8)
REF02AZ/883C ¹	±15	–55°C to +125°C	8-Lead Cerdip	Z-Suffix (Q-8)
REF02CJ	±50	0°C to 70°C	8-Lead TO-99	J-Suffix (H-08)
REF02CP	±50	–40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02CPZ ²	±50	–40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02CS	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CS-REEL	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CS-REEL7	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ ²	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ-REEL ²	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CSZ-REEL7 ²	±50	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02CZ	±50	0°C to 70°C	8-Lead Cerdip	Z-Suffix (Q-8)
REF02DP	±100	0°C to 70°C	8-Lead PDIP	P-Suffix (N-8)
REF02DPZ ²	±100	0°C to 70°C	8-Lead PDIP	P-Suffix (N-8)
REF02EJ	±15	–40°C to +85°C	8-Lead TO-99	J-Suffix (H-08)
REF02EZ	±15	–40°C to +85°C	8-Lead Cerdip	Z-Suffix (Q-8)
REF02J	±25	–55°C to +125°C	8-Lead TO-99	J-Suffix (H-08)
REF02HJ	±25	–40°C to +85°C	8-Lead TO-99	J-Suffix (H-08)
REF02HZ	±25	–40°C to +85°C	8-Lead Cerdip	Z-Suffix (Q-8)
REF02HP	±25	–40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02HPZ ²	±25	–40°C to +85°C	8-Lead PDIP	P-Suffix (N-8)
REF02HS	±25	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02HSZ ²	±25	–40°C to +85°C	8-Lead SOIC	S-Suffix (R-8)
REF02RC/883 ¹	±25	–55°C to +125°C	20-Lead LCC	RC-Suffix (E-20A)
REF02Z	±25	–55°C to +125°C	8-Lead Cerdip	Z-Suffix (Q-8)

¹ Consult sales for 883 data sheet.² Z = Pb-free part.

REF02

NOTES