User's Manual

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RL78/G1E

User's Manual: Hardware

16-Bit Microcontrollers with Smart Analog IC

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the RL78/G1E and design and develop application systems and programs for these devices.
The target products are as follows.

- 64-pin: R5F10FLx (x = C, D, E)
- 80-pin: R5F10FMx (x = C, D, E)

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The RL78/G1E manual is separated into three parts: this manual, RL78/G1A user's manual, and the RL78 family software user's manual.

RL78/G1E User's Manual (This Manual)	**RL78/G1A Hardware User's Manual**	**RL78 family Software User's Manual**
• Pin functions • Internal block functions • On-chip peripheral functions • Electrical specifications	• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**. The mark "<R>" shows major revised points. The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the assembler, and is defined as an sfr variable using the #pragma sfr directive in the compiler.

- To know details of the microcontroller block:
  →Refer to the separate document **RL78/G1A Hardware User's Manual (R01UH0305E)**.

- To know details of the RL78 microcontroller instructions:
  → Refer to the separate document **RL78 family User's Manual Software (R01US0015E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
RL78/G1E User's Manual Hardware	This manual
RL78/G1A User's Manual Hardware	R01UH0305E
RL78 family User's Manual Software	R01US0015E

Documents Related to Flash Memory Programming

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	R02UT0008E

Other Documents

Document Name	Document No.
Renesas MPUs & MCUs RL78 Family	R01CS0003E
Semiconductor Package Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
NEC Semiconductor Device Reliability/Quality Control System	R51ZZ0001E

Note See the "Semiconductor Device Mount Manual" website (http://www.renesas.com/products/package/manual/index.jsp).

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CHAPTER 1 OUTLINE

<R> 1. 1 Features

The RL78/G1E is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package. The chip of analog block features a range of front-end analog circuits for small sensor signal processing such as a configurable gain amplifier, gain adjustment amplifier, filter circuit, D/A converter, and temperature sensor. The chip of 16-bit microcontroller block corresponds to the RL78/G1A (64-pin products).

1. 1. 1 Microcontroller block

Low power consumption technology by standby function

- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from 0.03125 μs (32 MHz operation with high-speed on-chip oscillator) to 0.05 μs (20 MHz operation with high-speed system clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 2 to 4 KB

Code flash memory

- Code flash memory: 32 to 64 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 4 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy ±1.0 % (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)

Power supply voltage

- V_{DD} (Power supply for microcontroller block) = 1.6 to 5.5 V
- AV_{DD} (Power supply for A/D converter in microcontroller block) = 1.6 to 3.6 V
- AV_{DDn} (Power supply for analog block) = 3.0 to 5.5 V
- DV_{DD} (Power supply for SPI in analog block) = 3.0 to 5.5 V

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 3 levels)

DMA (Direct Memory Access) controller

- 2 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

Multiplier and divider/multiply-accumulator

- 16 bits × 16 bits = 32 bits (Unsigned or signed)
- 32 bits ÷ 32 bits = 32 bits (Unsigned)
- 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)

Serial interface

- CSI : 2 channels (64-pin products), 6 channels (80-pin products)
- UART / UART (LIN-bus supported) : 2 channels / 1channel
- I^2C/Simplified I^2C communication : 1 channel (64-pin products), 3 channels (80-pin products)

Timer

- 16-bit timer : 8 channels
- 12-bit interval timer : 1 channel
- Watchdog timer : 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/12-bit resolution A/D converter
- Analog input: 13 channels (64-pin products), 17 channels (80-pin products)
- Internal reference voltage (1.45 V) and temperature sensor[Note]

Note Can be selected only in HS (high-speed main) mode

Remarks 1. n = 1 to 3

2. The functions mounted depend on the product. See **1.6 Outline of Functions**.

I/O port

- I/O port : 24 (64-pin products), 30 (80-pin products)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

ROM, RAM capacities

Flash ROM	Data Flash	RAM	RL78/G1E	
			64 pins	80 pins
32 KB	4 KB	2 KB	R5F10FLC	R5F10FMC
48 KB	4 KB	3 KB	R5F10FLD	R5F10FMD
64 KB	4 KB	4 KB	R5F10FLE	R5F10FME

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

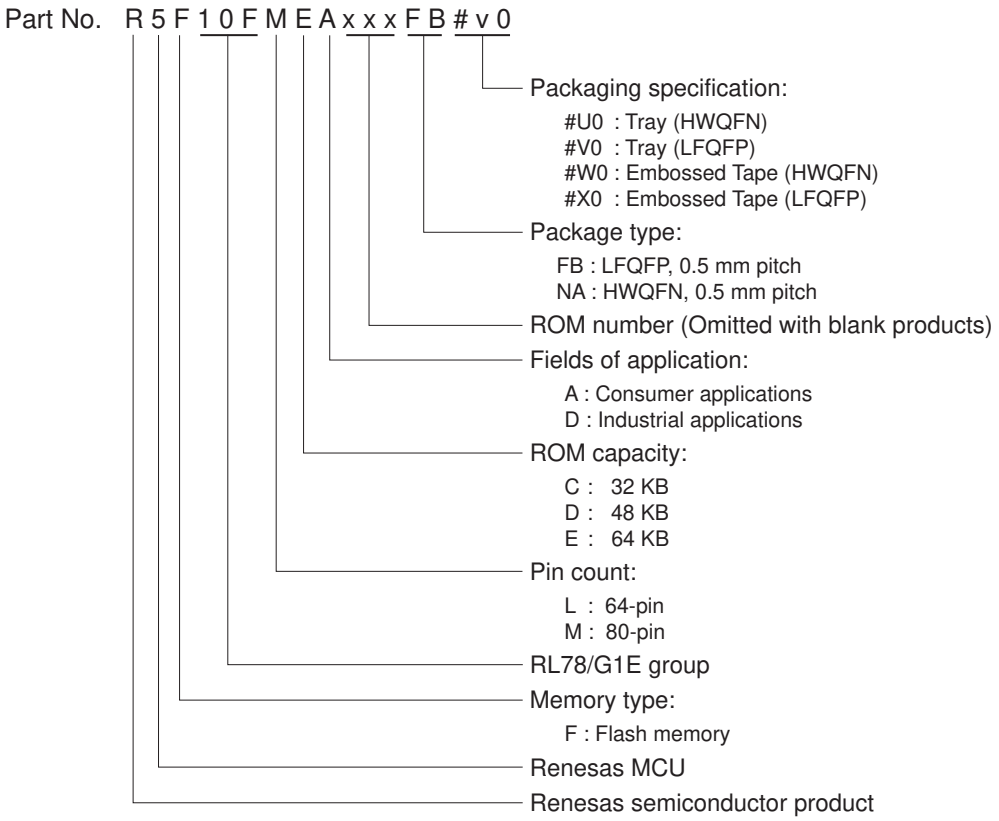
1. 1. 2 Analog block

- Configurable amplifier: 3 channels
- Gain adjustment amplifier: 1 channel
- High-pass filter: 1 channel **Note**
- Low-pass filter: 1 channel
- D/A converter: 4 channels
- Variable output voltage regulator: 1 channel
- Reference voltage generator: 1 channel
- Temperature sensor: 1 channel
- SPI (for analog block): 1 channel

Note 80-pin products only.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1. 2 List of Part Numbers



<R>

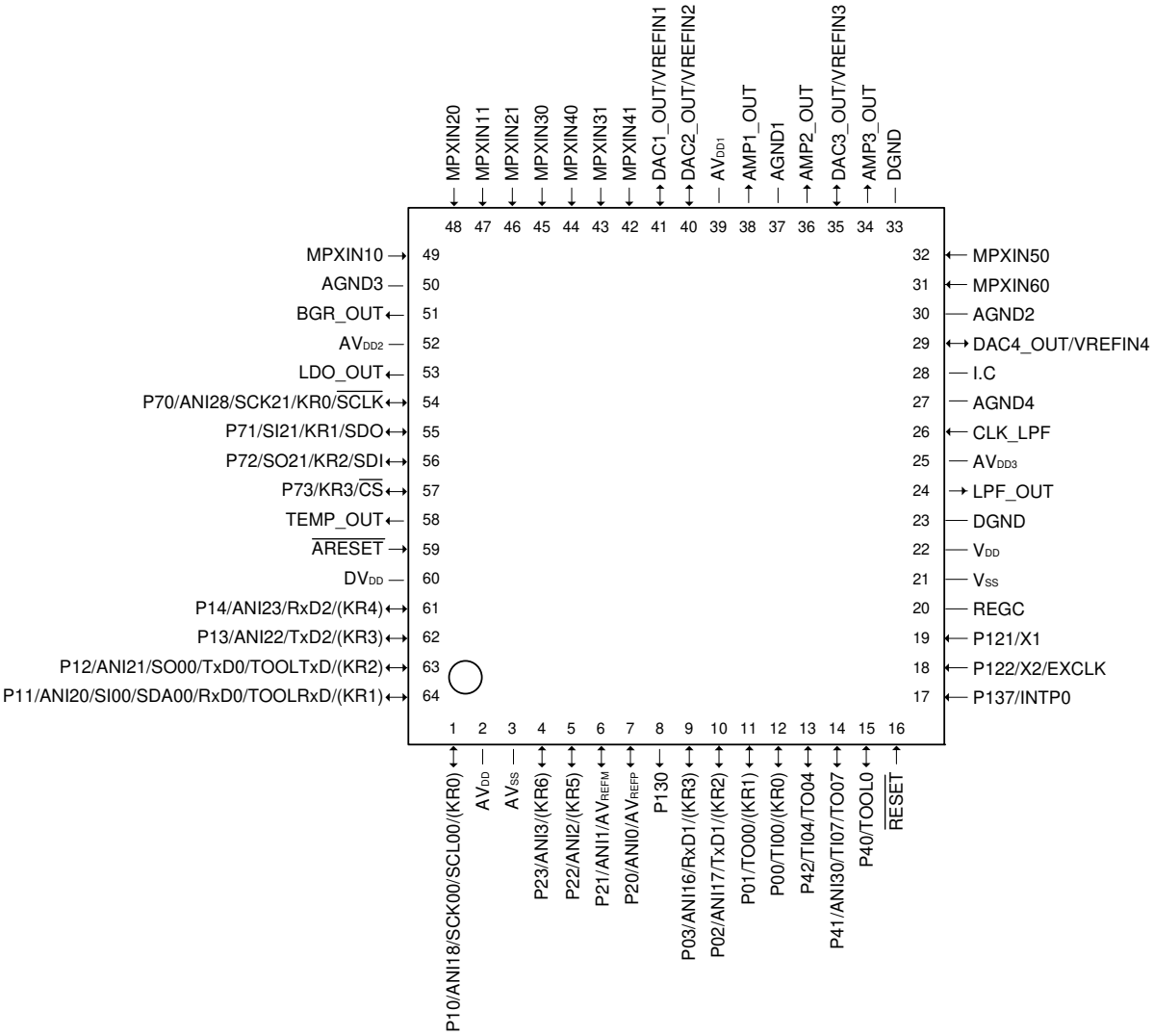
Pin count	Package	Data Flash	Part Number
64 pins	64-pin plastic HWQFN (fine pitch) (9 × 9)	Mounted	R5F10FLCANA#U0, R5F10FLCANA#W0, R5F10FLDANA#U0, R5F10FLDANA#W0, R5F10FLEANA#U0, R5F10FLEANA#W0, R5F10FLCDNA#U0, R5F10FLCDNA#W0, R5F10FLDDNA#U0, R5F10FLDDNA#W0, R5F10FLEDNA#U0, R5F10FLEDNA#W0
80 pins	80-pin plastic LFQFP (12 × 12)	Mounted	R5F10FMCAFB#V0, R5F10FMCAFB#X0, R5F10FMDAFB#V0, R5F10FMDAFB#X0, R5F10FMEAFB#V0, R5F10FMEAFB#X0, R5F10FMCDFB#V0, R5F10FMCDFB#X0, R5F10FMDDFB#V0, R5F10FMDDFB#X0, R5F10FMEDFB#V0, R5F10FMEDFB#X0

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

<R> 1. 3 Pin Configuration (Top View)

1. 3. 1 64-pin products

64-pin plastic WQFN (fine pitch) (9 × 9)



Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

2. Make the potential of VDD, AVDD1, AVDD2, AVDD3, and DVDD the same.

3. Make the potential of VSS, AGND1, AGND2, AGND3, AGND4, and DGND the same.

4. Leave I.C open.

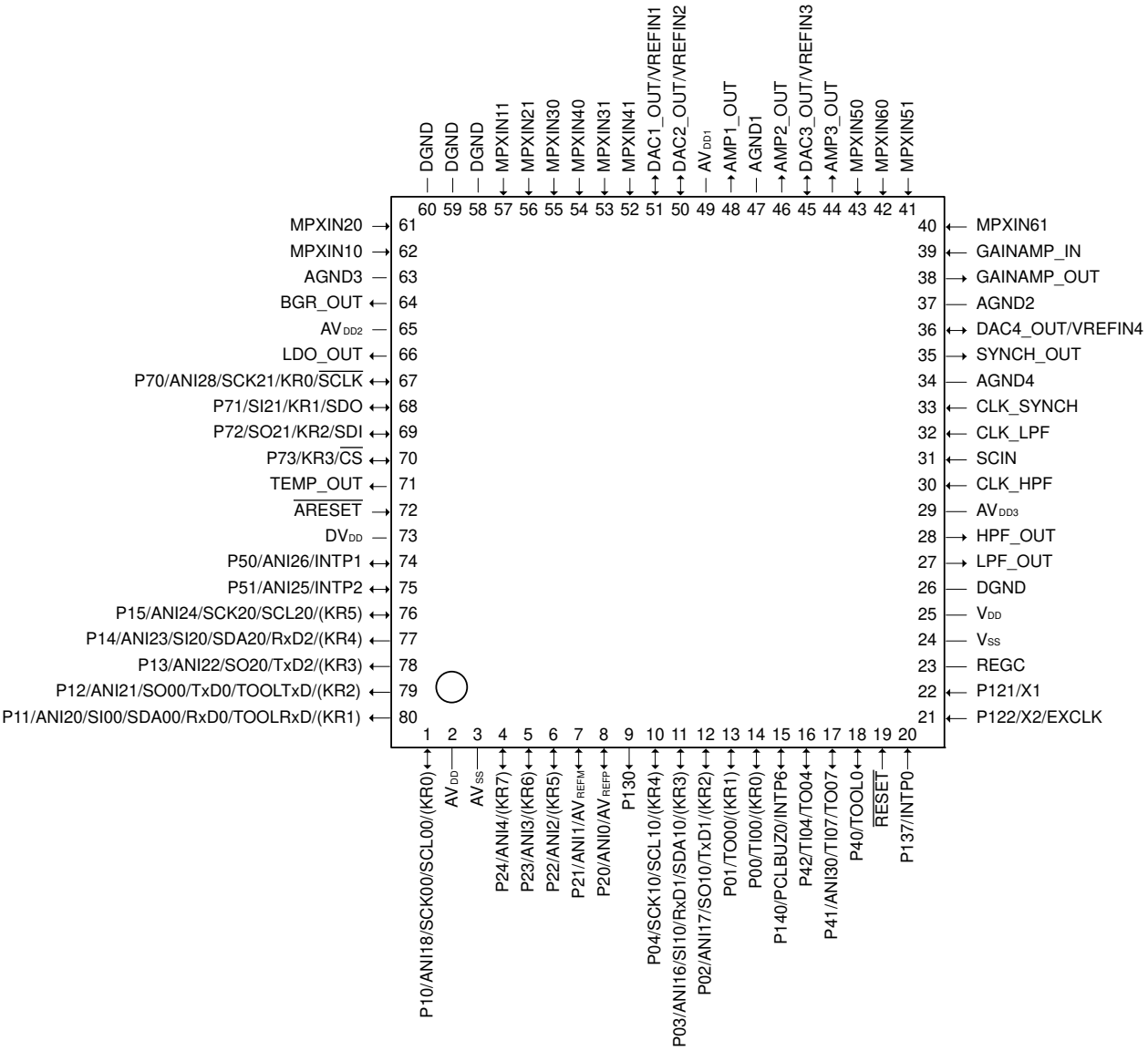
5. Connect the LDO_OUT pin to AGND3 via a capacitor (4.7 μF: recommended).

6. Connect the BGR_OUT pin to AGND3 via a capacitor (0.1 μF: recommended).

7. When using Low-pass filter or High-pass filter,
connect the DAC4_OUT/VREFIN4 pin to AGND1 via a capacitor (470 pF: recommended).

<R> **1. 3. 2 80-pin products**

80-pin plastic LQFP (fine pitch) (12 × 12)



Cautions 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

2. Make the potential of VDD, AVDD1, AVDD2, AVDD3, and DVDD the same.

3. Make the potential of VSS, AGND1, AGND2, AGND3, AGND4, and DGND the same.

4. Connect the LDO_OUT pin to AGND3 via a capacitor (4.7 μF: recommended).

5. Connect the BGR_OUT pin to AGND3 via a capacitor (0.1 μF: recommended).

6. When using Low-pass filter or High-pass filter,
connect the DAC4_OUT/VREFIN4 pin to AGND1 via a capacitor (470 pF: recommended).

<R> 1. 4 Pin Identification

○ Microcontroller Block

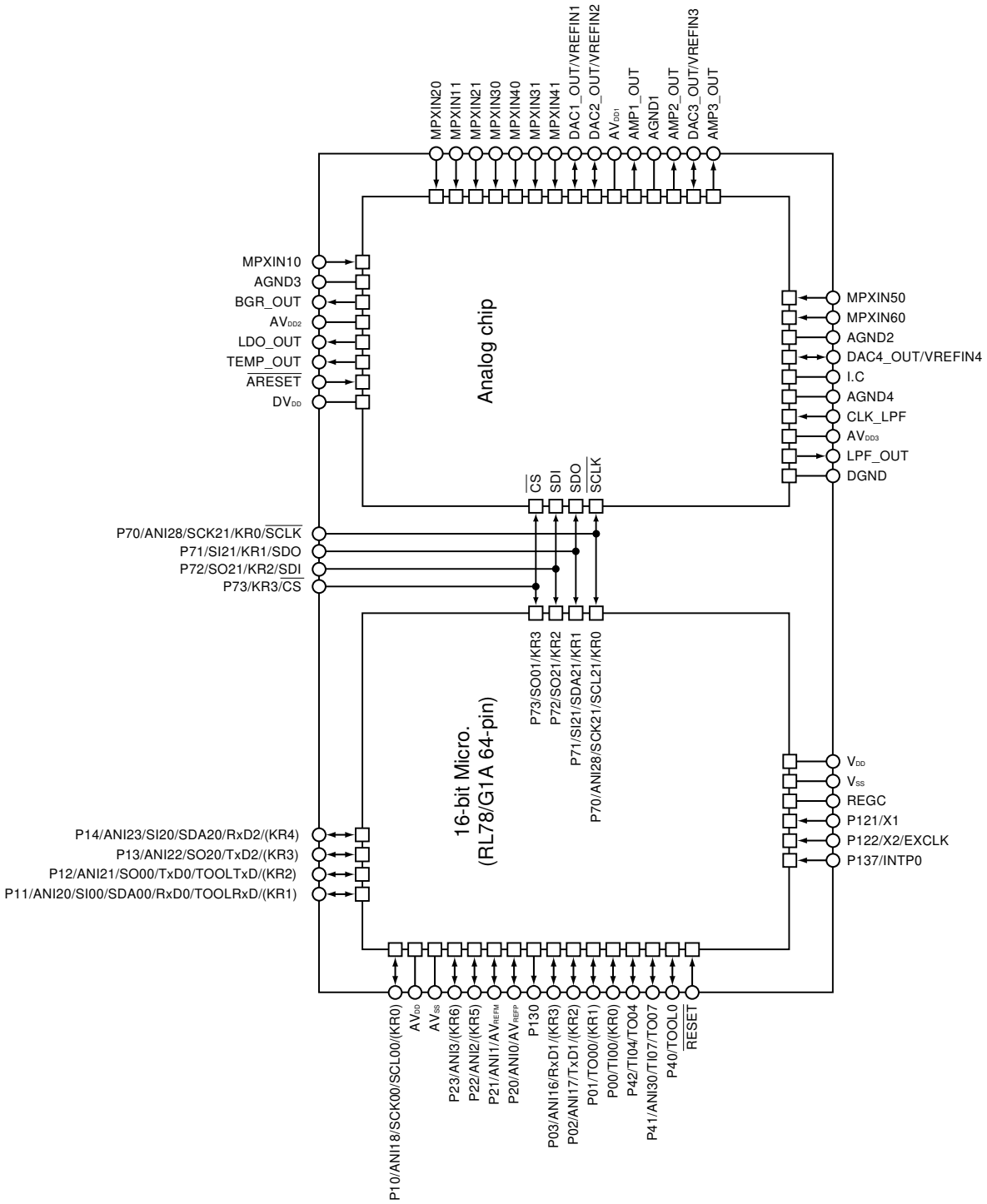
ANI0-ANI4,	Analog Input	RxD0-RxD2	Receive Data
ANI16-ANI18,		SCK00, SCK10,	Serial Clock Input/Output
ANI20-ANI26,		SCK20, SCK21	
ANI28, ANI30		SCL00, SCL10,	Serial Clock Input/Output
AV_{REFM}	Analog Reference Voltage	SCL20	
	Minus	SDA00, SDA10,	Serial Data Input/Output
AV_{REFP}	Analog Reference Voltage	SDA20	
	Plus	SI00, SI10,	Serial Data Input
EXCLK	External Clock Input	SI20, SI21	
	(Main System Clock)	SO00, SO10	Serial Data Output
INTP0-INTP2	External Interrupt Input	SO20, SO21	
INTP6		TI00, TI04,	Timer Input
KR0-KR7	Key Return	TI07	
P00-P04	Port 0	TO00, TO04,	Timer Output
P10-P15	Port 1	TO07	
P20-P24	Port 2	TOOL0	Data Input/Output for Tool
P40-P42	Port 4	TOOLRxD,	Data Input/Output for External
P50, P51	Port 5		Device
P70-P73	Port 7	TOOLTxD	
P121, P122	Port 12	TxD0-TxD2	Transmit Data
P130, P137	Port 13	V_{DD}	Power Supply
P140	Port 14	V_{SS}	Ground
PCLBUZ0	Programmable Clock Output/	X1, X2	Crystal Oscillator
	Buzzer Output		(Main System Clock)
REGC	Regulator Capacitance	AV_{DD}	Analog Power Supply
$\overline{\text{RESET}}$	Reset	AV_{SS}	Analog Ground

○ Analog Block

AV_{DD1}	Power supply for configurable amplifiers	AMP1_OUT, AMP2_OUT, AMP3_OUT	Configurable amplifier output
AV_{DD2}	Power supply for variable output voltage regulator and reference voltage generator	DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT	D/A converter output
AV_{DD3}	Power supply for low-pass filter and high-pass filter	VREFIN1, VREFIN2, VREFIN3	Reference voltage input for configurable amplifier
AGND1	Ground for configurable amplifiers	VREFIN4	Reference voltage input for Gain adjustment amplifier, low-pass filter, and high-pass filter
AGND2	Ground for gain adjustment amplifier		
AGND3	Ground for variable output voltage regulator and reference voltage generator		
AGND4	Ground for low-pass filter and high-pass filter		
MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61	Multiplexer input	$\overline{SCLK}$	Serial clock input
		SDO	Serial data output
		SDI	Serial data input
		$\overline{CS}$	Chip select input
		TEMP_OUT	Temperature sensor output
		$\overline{ARESET}$	Reset for analog block
		DV_{DD}	Power supply for SPI
		DGND	Ground for SPI
		HPF_OUT	High-pass filter output
		CLK_HPF	Pin for inputting high-pass filter control clock
		CLK_LPF	Pin for inputting low-pass filter control clock
SC_IN	Input for filter signal processing		
CLK_SYNCH	Synchronous detector control clock input	LPF_OUT	Low-pass filter output
		BGR_OUT	Reference voltage generator output
SYNCH_OUT	Synchronous detector output	LDO_OUT	Variable output voltage regulator
GAINAMP_IN	Gain adjustment amplifier input	I.C	Internal connect
GAINAMP_OUT	Gain adjustment amplifier output		

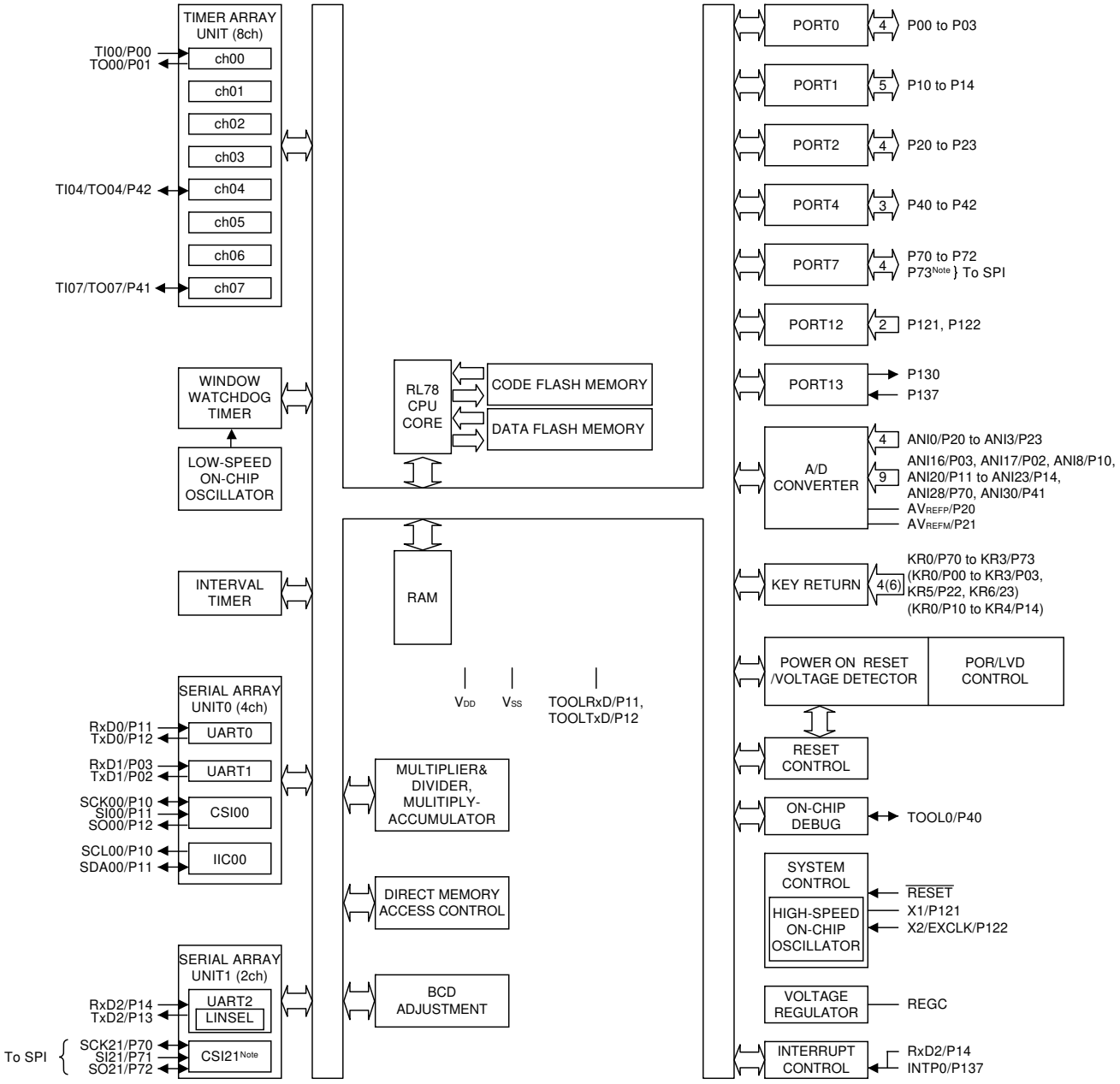
<R> 1. 5 Block Diagram

1. 5. 1 64-pin products



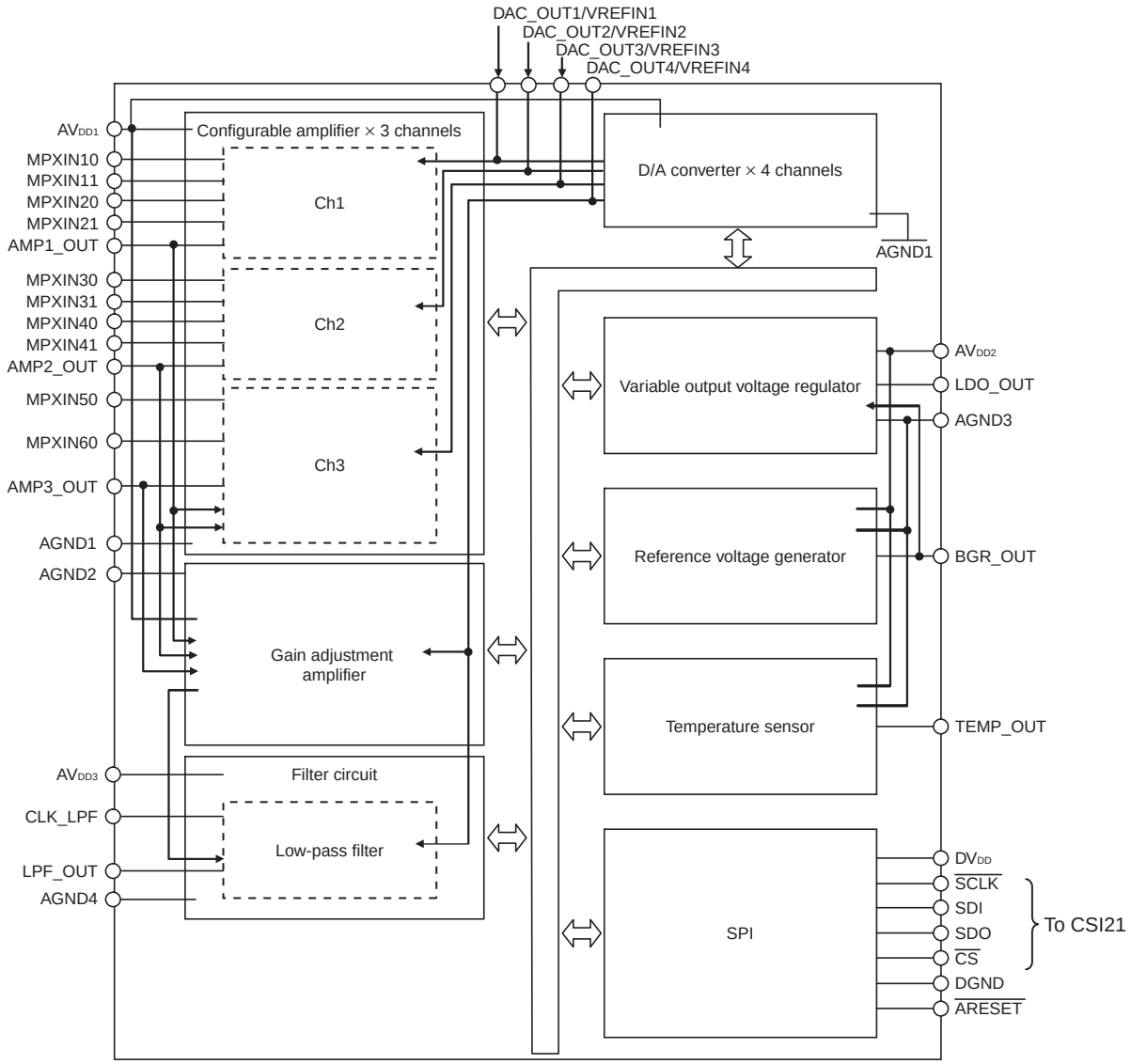
Remark The RL78/G1E (64-pin products) is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package.

<R> **(1) Block diagram in microcontroller block (64-pin products)**

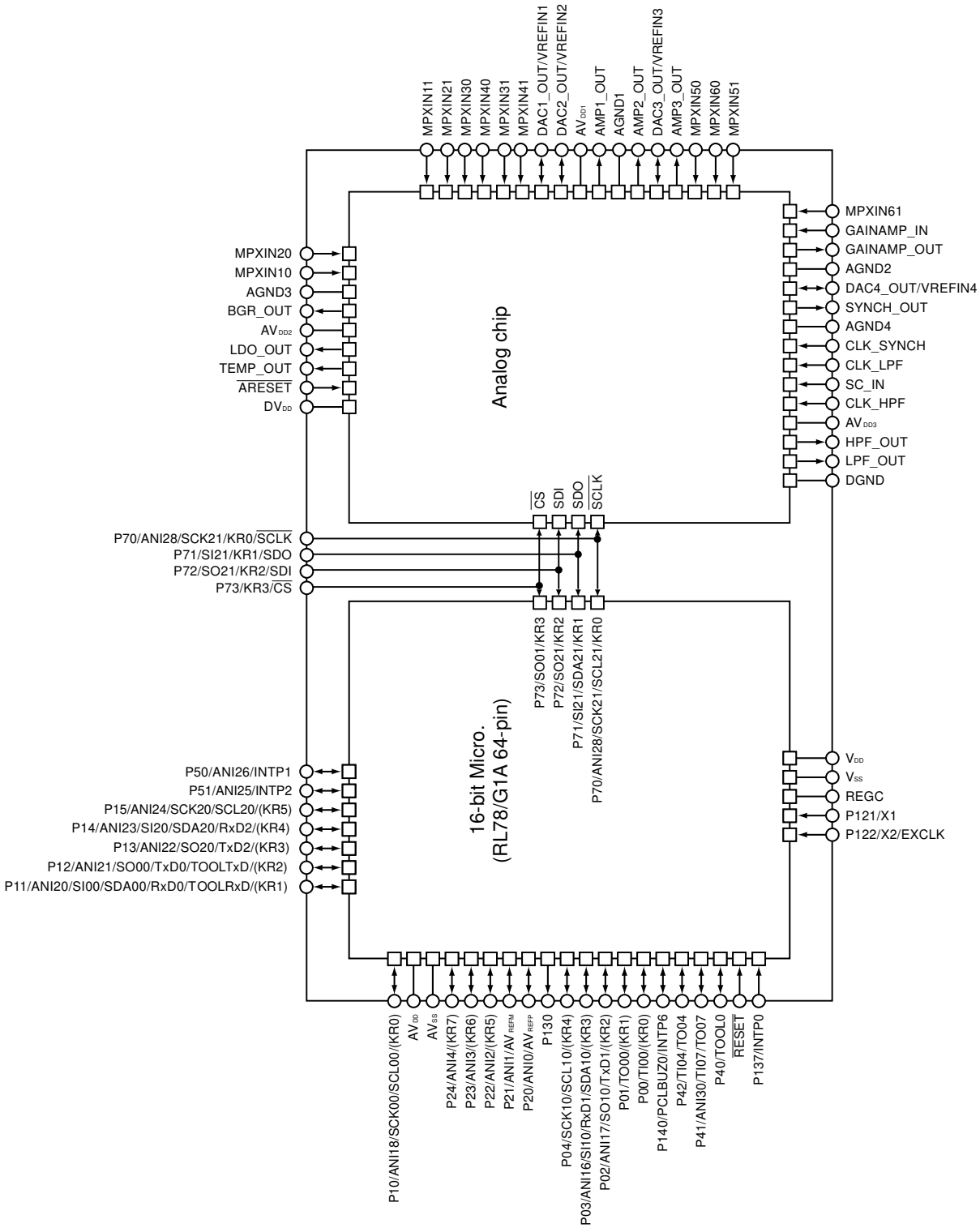


Note Connected inside the package.

(2) Block diagram in analog block (64-pin products)

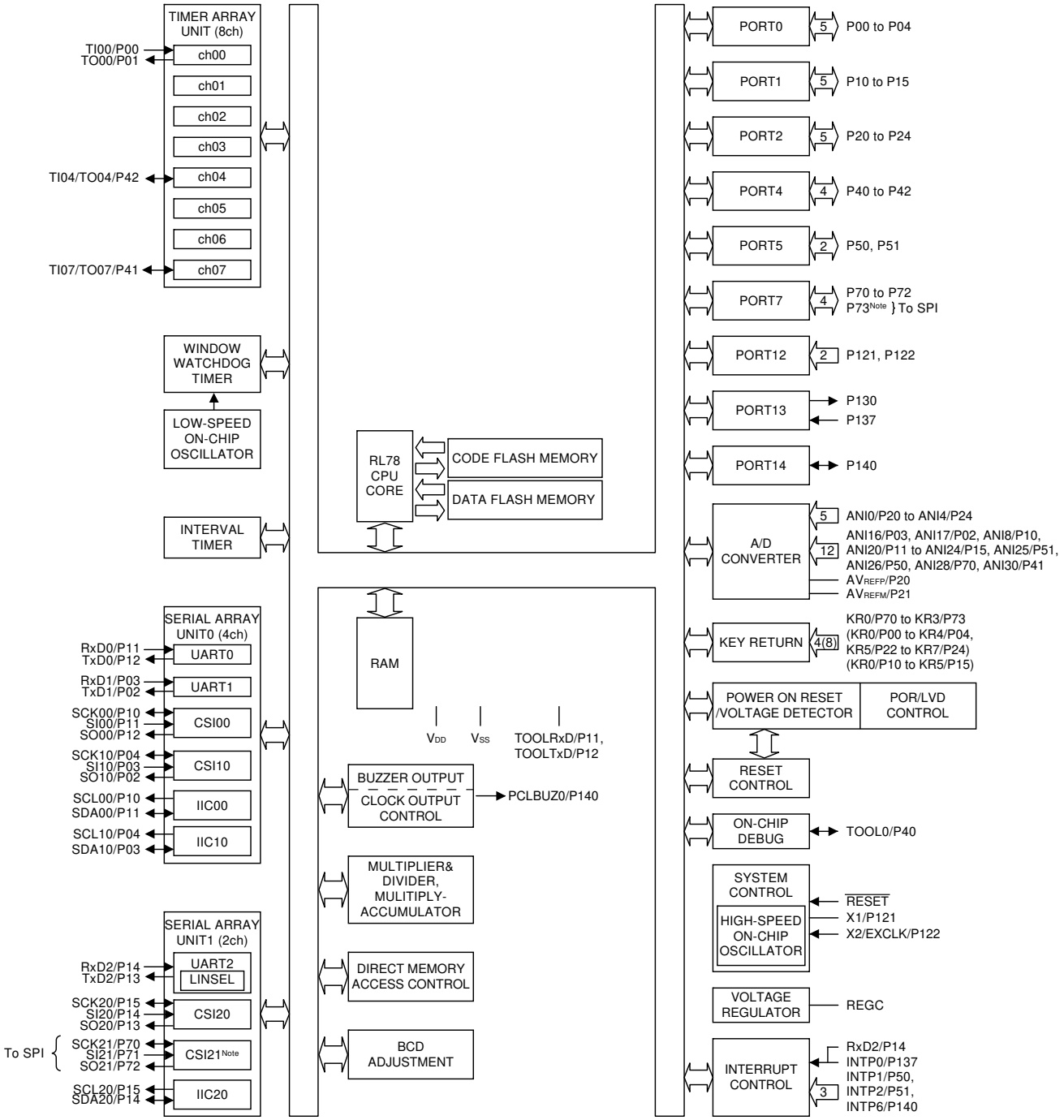


<R> **1. 5. 2 80-pin products**



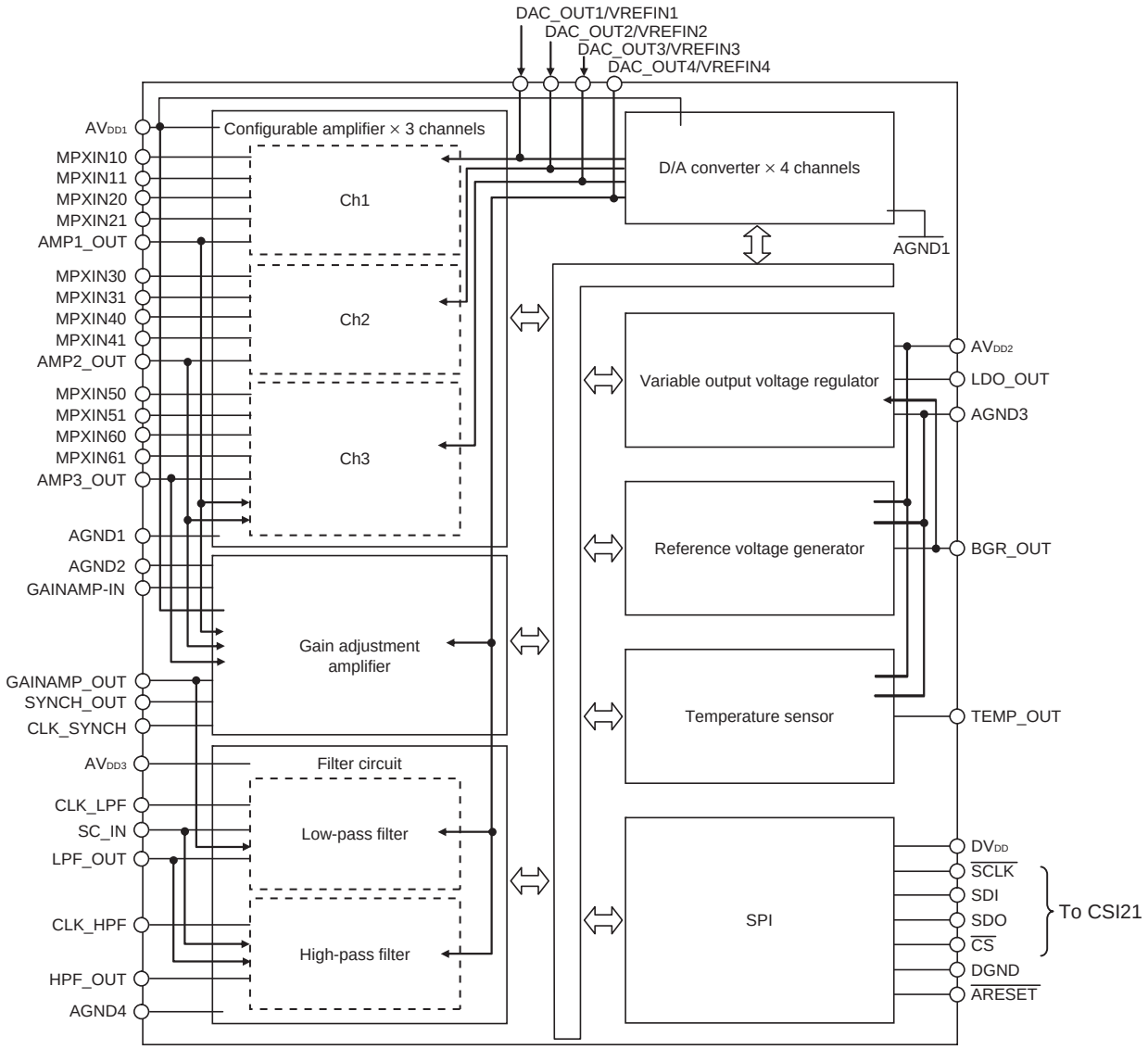
Remark The RL78/G1E (80-pin products) is a multi-chip package (MCP) device that integrates a chip of an analog block and a chip of 16-bit microcontroller block in a single package.

<R> (1) Block diagram in microcontroller block (80-pin products)



Note Connected inside the package.

(2) Block diagram in analog block (80-pin products)



<R> 1. 6 Outline of Functions

Table 1-1 Outline of Functions (Microcontroller Block) (1/2)

Item		64-pin products	80-pin products
		R5F10FLx	R5F10FMx
Code flash memory (KB)		32 to 64	32 to 64
Data flash memory (KB)		4	4
RAM (KB)		2 to 4 Note1	2 to 4 Note1
Memory space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V	
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)	
Subsystem clock		–	
Low-speed on-chip oscillator		15 kHz (TYP.)	
General-purpose register		(8-bit register × 8) × 4 banks	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor / logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	
I/O port	Total	24	30
	CMOS I/O	20	26
	CMOS input	3	3
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	–	–
Timer	16-bit timer	8 channels	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	–	
	12-bit Interval timer (IT)	1 channel	
	Timer output	3 channels (PWM outputs: 2 channels Note2)	
	RTC output	–	
Clock output / buzzer output		–	1 channel • 2.44 kHz, 4.88 kHz,9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)
8/12-bit resolution A/D converter		13 channels	17 channels

Notes 1. In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used. (For details, see **3. 3 CPU Architecture**)

2. The number of PWM outputs varies depending on the setting of channels in use. (For details, see **3. 6 Timer Array Unit)**

Table 1-1 Outline of Functions (Microcontroller Block) (2/2)

Item		64-pin products	80-pin products
		R5F10FLx	R5F10FMx
Serial interface		• 64-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel UART: 1 channel CSI: 1 channel / UART (LIN-bus supported): 1 channel • 80-pin products CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 1 channel / simplified I^2C: 1 channel / UART: 1 channel CSI: 2 channels / simplified I^2C: 1 channel / UART (LIN-bus supported): 1 channel	
	I^2C bus	–	
Multiplier and divider / multiply accumulator		Multiplier: 16 bits × 16 bits (Unsigned or signed) Divider: 32 bits ÷ 32 bits (Unsigned) Multiply accumulator: 16 bits × 16 bits + 32 bits (Unsigned or signed)	
DMA controller		2 channels	
Vectored interrupt sources	Internal	25	
	External	2	5
Key interrupt		4 ch (7) Note 1	4 ch (8) Note 1
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access	
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V	
Voltage detector		Detection level: 3 stages	
On-chip debug function		Provided	

<R>

Notes 1. The number in parentheses is the channels of key interrupt when using the peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed. Rest by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Table 1-2 Outline of Functions (Analog Block)

Item	64-pin products	80-pin products
	R5F10FLx	R5F10FMx
Sensor interface amplifier	Configurable amplifiers: 3 channels	
Gain adjustment amplifier	1 channel	1 channel (with synchronous detector)
Low-pass filter	1 channel	
High-pass filter	–	1 channel
8-bit D/A converter	4 channels	
Variable output voltage regulator	1 channel	
Reference voltage generator	1 channel	
<R> Temperature sensor circuit	1 channel	
Power supply voltage	V_{DD} = 1.6 to 5.5 V, AV_{DD} = 1.6 to 3.6 V, AV_{DDn} = 3.0 to 5.5 V, DV_{DD} = 3.0 to 5.5 V	
Operating ambient temperature	T_A = −40°C to +85°C	

Remark n = 1 to 3

CHAPTER 2 PIN FUNCTIONS

2. 1 Pin Functions in Microcontroller Block

The microcontroller block in the RL78/G1E is the RL78/G1A (64-pin products), but a part of pin functions of them are different from each other. The microcontroller function pins in the RL78/G1E (64-pin and 80-pin products) that differ from those in the RL78/G1A (64-pin products) are shown in the table below.

<R> **(1) Comparison of port functions (64-pin products)**

(1/2)

RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P00	Same as RL78/G1A (64-pin products)	P00	TI00/(KR0)
P01	Same as RL78/G1A (64-pin products)	P01	TO00/(KR1)
P02	ANI17/TxD1/(KR2)	P02	ANI17/SO10/TxD1/(KR2)
P03	P03/ANI6/RxD1/(KR3)	P03	ANI16/SI10/SDA10/RxD1/(KR3)
		P04	SCK10/SCL10/(KR4)
		P05	TI05/TO05/KR8
		P06	TI06/TO06/KR9
P10	Same as RL78/G1A (64-pin products)	P10	ANI18/SCK00/SCL00/(KR0)
P11	Same as RL78/G1A (64-pin products)	P11	ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12	Same as RL78/G1A (64-pin products)	P12	ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13	ANI22/TxD2/(KR3)	P13	ANI22/SO20/TxD2/(KR3)
P14	ANI23/RxD2/(KR4)	P14	ANI23/SI20/SDA20/RxD2/(KR4)
		P15	ANI24/SCK20/SCL20/(KR5)
		P16	TI01/TO01/INTP5
P20	Same as RL78/G1A (64-pin products)	P20	ANI0/AV_{REFP}
P21	Same as RL78/G1A (64-pin products)	P21	ANI1/AV_{REFM}
P22	Same as RL78/G1A (64-pin products)	P22	ANI2/(KR5)
P23	Same as RL78/G1A (64-pin products)	P23	ANI3/(KR6)
		P24	ANI4/(KR7)
		P25	ANI5/(KR8)
		P26	ANI6/(KR9)
		P27	ANI7
		P30	ANI27/SCK11/SCL11/INTP3/RTC1HZ
		P31	ANI29/TI03/TO03/INTP4
P40	Same as RL78/G1A (64-pin products)	P40	TOOL0
P41	Same as RL78/G1A (64-pin products)	P41	ANI30/TI07/TO07
P42	Same as RL78/G1A (64-pin products)	P42	TI04/TO04
		P43	–
		P50	ANI26/SI11/SDA11/INTP1
		P51	ANI25/SO11/INTP2
		P60	SCLA0
		P61	SDAA0
		P62	–
		P63	–

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

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<R>

RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P70	ANI28/SCK21/KR0/SCLK Note	P70	ANI28/SCK21/SCL21/KR0
P71	SI21/KR1/SDO Note	P71	SI21/SDA21/KR1
P72	SO21/KR2/SDI Note	P72	SO21/KR2
P73	KR3/$\overline{CS}$ Note	P73	SO01/KR3
		P74	SI01/SDA01/INTP8/KR4
		P75	SCK01/SCL01/INTP9/KR5
		P76	INTP10/KR6
		P77	INTP11/KR7
		P120	ANI19
P121	Same as RL78/G1A (64-pin products)	P121	X1
P122	Same as RL78/G1A (64-pin products)	P122	X2/EXCLK
		P123	XT1
		P124	XT2/EXCLKS
P130	Same as RL78/G1A (64-pin products)	P130	–
P137	Same as RL78/G1A (64-pin products)	P137	INTP0
		P140	PCLBUZ0/INTP6
		P141	PCLBUZ1/INTP7
		P150	ANI8
		P151	ANI9/(KR6)
		P152	ANI10/(KR7)
		P153	ANI11/(KR8)
		P154	ANI12/(KR9)

Note $\overline{SCLK}$, SDO, SDI, $\overline{CS}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

<R> **(2) Comparison of port functions (80-pin products)**

(1/2)

RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P00	Same as RL78/G1A (64-pin products)	P00	TI00/(KR0)
P01	Same as RL78/G1A (64-pin products)	P01	TO00/(KR1)
P02	Same as RL78/G1A (64-pin products)	P02	ANI17/SO10/TxD1/(KR2)
P03	Same as RL78/G1A (64-pin products)	P03	ANI16/SI10/SDA10/RxD1/(KR3)
P04	Same as RL78/G1A (64-pin products)	P04	SCK10/SCL10/(KR4)
		P05	TI05/TO05/KR8
		P06	TI06/TO06/KR9
P10	Same as RL78/G1A (64-pin products)	P10	ANI18/SCK00/SCL00/(KR0)
P11	Same as RL78/G1A (64-pin products)	P11	ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)
P12	Same as RL78/G1A (64-pin products)	P12	ANI21/SO00/TxD0/TOOLTxD/(KR2)
P13	Same as RL78/G1A (64-pin products)	P13	ANI22/SO20/TxD2/(KR3)
P14	Same as RL78/G1A (64-pin products)	P14	ANI23/SI20/SDA20/RxD2/(KR4)
P15	Same as RL78/G1A (64-pin products)	P15	ANI24/SCK20/SCL20/(KR5)
		P16	TI01/TO01/INTP5
P20	Same as RL78/G1A (64-pin products)	P20	ANI0/AV_{REFP}
P21	Same as RL78/G1A (64-pin products)	P21	ANI1/AV_{REFM}
P22	Same as RL78/G1A (64-pin products)	P22	ANI2/(KR5)
P23	Same as RL78/G1A (64-pin products)	P23	ANI3/(KR6)
P24	Same as RL78/G1A (64-pin products)	P24	ANI4/(KR7)
		P25	ANI5/(KR8)
		P26	ANI6/(KR9)
		P27	ANI7
		P30	ANI27/SCK11/SCL11/INTP3/RTC1HZ
		P31	ANI29/TI03/TO03/INTP4
P40	Same as RL78/G1A (64-pin products)	P40	TOOL0
P41	Same as RL78/G1A (64-pin products)	P41	ANI30/TI07/TO07
P42	Same as RL78/G1A (64-pin products)	P42	TI04/TO04
		P43	–
P50	ANI26/INTP1	P50	ANI26/SI11/SDA11/INTP1
P51	ANI25/INTP2	P51	ANI25/SO11/INTP2
		P60	SCLA0
		P61	SDAA0
		P62	–
		P63	–

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

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<R>

RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
Function Name	Alternate Function	Function Name	Alternate Function
P70	ANI28/SCK21/KR0/$\overline{\text{SCLK}}$ Note	P70	ANI28/SCK21/SCL21/KR0
P71	SI21/KR1/SDO Note	P71	SI21/SDA21/KR1
P72	SO21/KR2/SDI Note	P72	SO21/KR2
P73	KR3/$\overline{\text{CS}}$ Note	P73	SO01/KR3
		P74	SI01/SDA01/INTP8/KR4
		P75	SCK01/SCL01/INTP9/KR5
		P76	INTP10/KR6
		P77	INTP11/KR7
		P120	ANI19
P121	Same as RL78/G1A (64-pin products)	P121	X1
P122	Same as RL78/G1A (64-pin products)	P122	X2/EXCLK
		P123	XT1
		P124	XT2/EXCLKS
P130	Same as RL78/G1A (64-pin products)	P130	–
P137	Same as RL78/G1A (64-pin products)	P137	INTP0
P140	Same as RL78/G1A (64-pin products)	P140	PCLBUZ0/INTP6
		P141	PCLBUZ1/INTP7
		P150	ANI8
		P151	ANI9/(KR6)
		P152	ANI10/(KR7)
		P153	ANI11/(KR8)
		P154	ANI12/(KR9)

Note $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

(3) Comparison of functions other than port functions (60-pin products and 80-pin products)

About the comparison of functions other than port pins, See **2. 1. 2. 1 Functions available for each product**.

2. 1. 1 Port functions

The relationship between pin I/O buffer power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

(1) 64-pin products

Power Supply	Corresponding Pins
V_{DD}	• Port pins other than P20 to P23 • $\overline{RESET}$, REGC
AV_{DD}	• P20 to P23

(2) 80-pin products

Power Supply	Corresponding Pins
V_{DD}	• Port pins other than P20 to P24 • $\overline{RESET}$, REGC
AV_{DD}	• P20 to P24

<R> 2. 1. 1. 1 64-pin products

(1/2)

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P00	8-1-1	I/O	Input port	TI00/(KR0)	Port 0. 4-bit I/O port. Input of P00, P01, and P03 can be set to TTL input buffer. Output of P02 and P03 can be set to N-ch open-drain output (V_{DD} tolerance). P02 and P03 can be set to analog input. Note1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P01				TO00/(KR1)	
P02	7-3-2		Analog input port	ANI17/TxD1/(KR2)	
P03	8-3-2			ANI16/RxD1/(KR3)	
P10	8-3-2	I/O	Analog input port	ANI18/SCK00/SCL00/(KR0)	Port 1. 5-bit I/O port. Input of P10, P11, and P14 can be set to TTL input buffer. Output of P10 to P14 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P14 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P11				ANI20/SI00/RxD0/TOOLRxD/SDA00/(KR1)	
P12	7-3-2			ANI21/SO00/TxD0/TOOLTxD/(KR2)	
P13				ANI22/TxD2/(KR3)	
P14	8-3-2			ANI23/RxD2/(KR4)	
P20	4-3-1	I/O	Analog input port	ANI0/AV_{REFP}	Port 2. 4-bit I/O port. Can be set to analog input. Note 2 Input/output can be specified in 1-bit units.
P21				ANI1/AV_{REFM}	
P22				ANI2/(KR5)	
P23				ANI3/(KR6)	
P40	7-1-1	I/O	Input port	TOOL0	Port 4. 3-bit I/O port. P41 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41	7-3-1		Analog input port	ANI30/TI07/TO07	
P42	7-1-1		Input port	TI04/TO04	
P70	7-3-1	I/O	Analog input port	ANI28/KR0/SCK21/$\overline{SCLK}$ Note3	Port 7. 4-bit I/O port. P70 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P71	7-1-2		Input port	KR1/SI21/SDO Note3	
P72	7-1-1			KR2/SO21/SDI Note3	
P73				KR3/$\overline{CS}$ Note3	

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

2. Digital or analog for each pin can be selected with the A/D port configuration register (ADPC).

3. $\overline{SCLK}$, SDO, SDI, $\overline{CS}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

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<R>

P121	2-2-1	Input	Input port	X1	Port 12. 2-bit input port.
P122				X2/EXCLK	
P130	1-1-1	Output	Output port	–	Port 13. 1-bit output port and 1-bit input port.
P137	2-1-2	Input	Input port	INTP0	
RESET	2-1-1	Input	–	–	Input only pin for external reset. When external reset is not used, connect this pin to V_{DD} directly or via a resistor.

2. 1. 1. 2 80-pin products

(1/2)

<R>

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P00	8-1-1	I/O	Input port	TI00/(KR0)	Port 0. 5-bit I/O port. Input of P00, P01, P03, and P04 can be set to TTL input buffer. Output of P02 to P04 can be set to N-ch open-drain output (V_{DD} tolerance). P02 and P03 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P01				TO00/(KR1)	
P02	7-3-2		Analog input port	ANI17/SO10/TxD1/(KR2)	
P03	8-3-2			ANI16/SI10/RxD1/ SDA10/(KR3)	
P04	8-1-2		Input port	SCK10/SCL10/(KR4)	
P10	8-3-2	I/O	Analog input port	ANI18/SCK00/ SCL00/(KR0)	Port 1. 6-bit I/O port. Input of P10, P11, P14, and P15 can be set to TTL input buffer. Output of P10 to P15 can be set to N-ch open-drain output (V_{DD} tolerance). P10 to P15 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P11				ANI20/SI00/RxD0/ TOOLRxD/SDA00/(KR1)	
P12	7-3-2			ANI21/SO00/TxD0/ TOOLTxD/(KR2)	
P13				ANI22/TxD2/SO20/(KR3)	
P14	8-3-2			ANI23/RxD2/SI20/ SDA20/(KR4)	
P15				ANI24/SCK20/ SCL20/(KR5)	
P20	4-3-1	I/O	Analog input port	ANI0/AV_{REFP}	Port 2. 5-bit I/O port. Can be set to analog input. Note 2 Input/output can be specified in 1-bit units.
P21				ANI1/AV_{REFM}	
P22				ANI2/(KR5)	
P23				ANI3/(KR6)	
P24				ANI4/(KR7)	
P40	7-1-1	I/O	Input port	TOOL0	Port 4. 3-bit I/O port. P41 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P41	7-3-1		Analog input port	ANI30/TI07/TO07	
P42	7-1-1		Input port	TI04/TO04	

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

2. Digital or analog for each pin can be selected with the A/D port configuration register (ADPC).

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). About format, see Figure in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**.

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<R>

Function Name	Pin Type	I/O	After Reset	Alternate Function	Function
P50	7-3-2	I/O	Analog input port	ANI26/INTP1	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V_{DD} tolerance). P50 and P51 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port.
P51	7-3-1			ANI25/INTP2	
P70	7-3-1	I/O	Analog input port	ANI28/KR0/ SCK21/$\overline{\text{SCLK}}$ Note2	Port 7. 4-bit I/O port. P70 can be set to analog input. Note 1 Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software setting at input port.
P71	7-1-2		Input port	KR1/SI21/SDO Note2	
P72	7-1-1			KR2/SO21/SDI Note2	
P73				KR3/$\overline{\text{CS}}$ Note2	
P121	2-2-1	Input	Input port	X1	Port 12. 2-bit input port.
P122				X2/EXCLK	
P130	1-1-1	Output	Output port	–	Port 13. 1-bit output port and 1-bit input port.
P137	2-1-2	Input	Input port	INTP0	
P140	7-1-1	I/O	Input port	PCLBUZ0/INTP6	Port 14. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
RESET	2-1-1	Input	–	–	Input only pin for external reset. When external reset is not used, connect this pin to V_{DD} directly or via a resistor.

<R> **Notes 1.** Digital or analog for each pin can be selected with the port mode control register x (PMCx) (can be set in 1-bit units).

2. $\overline{\text{SCLK}}$, SDO, SDI, $\overline{\text{CS}}$ represent the pin functions of analog block. P70 to P73 which are connected to the pins of the chip of analog block inside the package have some alternate functions for analog block.

2. 1. 2 Functions other than port functions

2. 1. 2. 1 Functions available for each product

(1/3)

Function Name	RL78/G1E (64-pin)	RL78/G1E (80-pin)	RL78/G1A (64-pin)
ANI0	√	√	√
ANI1	√	√	√
ANI2	√	√	√
ANI3	√	√	√
ANI4	–	√	√
ANI5	–	–	√
ANI6	–	–	√
ANI7	–	–	√
ANI8	–	–	√
ANI9	–	–	√
ANI10	–	–	√
ANI11	–	–	√
ANI12	–	–	√
ANI16	√	√	√
ANI17	√	√	√
ANI18	√	√	√
ANI19	–	–	√
ANI20	√	√	√
ANI21	√	√	√
ANI22	√	√	√
ANI23	√	√	√
ANI24	–	√	√
ANI25	–	√	√
ANI26	–	√	√
ANI27	–	–	√
ANI28	√	√	√
ANI29	–	–	√
ANI30	√	√	√
INTP0	√	√	√
INTP1	–	√	√
INTP2	–	√	√
INTP3	–	–	√
INTP4	–	–	√
INTP5	–	–	√
INTP6	–	√	√
INTP7	–	–	√
INTP8	–	–	√
INTP9	–	–	√
INTP10	–	–	√
INTP11	–	–	√

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<R>

Function Name	RL78/G1E (64-pin)	RL78/G1E (80-pin)	RL78/G1A (64-pin)
KR0	√	√	√
KR1	√	√	√
KR2	√	√	√
KR3	√	√	√
KR4	(√)	(√)	√
KR5	(√)	(√)	√
KR6	(√)	(√)	√
KR7	–	(√)	√
KR8	–	–	√
KR9	–	–	√
PCLBUZ0	–	√	√
PCLBUZ1	–	–	√
REGC	√	√	√
RTC1HZ	–	–	√
$\overline{\text{RESET}}$	√	√	√
RXD0	√	√	√
RXD1	√	√	√
RXD2	√	√	√
SCK00	√	√	√
SCK01	–	–	√
SCK10	–	√	√
SCK11	–	–	√
SCK20	–	√	√
SCK21	√	√	√
SCLA0	–	–	√
SCL00	√	√	√
SCL01	–	–	√
SCL10	–	√	√
SCL11	–	–	√
SCL20	–	√	√
SCL21	–	–	√
SDAA0	–	–	√
SDA00	√	√	√
SDA01	–	–	√
SDA10	–	√	√
SDA11	–	–	√
SDA20	–	√	√
SDA21	–	–	√
SI00	√	√	√
SI01	–	–	√
SI10	–	√	√
SI11	–	–	√
SI20	–	√	√
SI21	√	√	√

<R> **Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(3/3)

Function Name	RL78/G1E (64-pin)	RL78/G1E (80-pin)	RL78/G1A (64-pin)
SO00	√	√	√
SO01	–	–	√
SO10	–	√	√
SO11	–	–	√
SO20	–	√	√
SO21	√	√	√
TI00	√	√	√
TI01	–	–	√
TI03	–	–	√
TI04	√	√	√
TI05	–	–	√
TI06	–	–	√
TI07	√	√	√
TO00	√	√	√
TO01	–	–	√
TO03	–	–	√
TO04	√	√	√
TO05	–	–	√
TO06	–	–	√
TO07	√	√	√
TxD0	√	√	√
TxD1	√	√	√
TxD2	√	√	√
X1	√	√	√
X2	√	√	√
EXCLK	√	√	√
EXCLKS	–	–	√
XT1	–	–	√
XT2	–	–	√
V_{DD}	√	√	√
EV_{DD0}	_Note	_Note	√
AV_{DD}	√	√	√
AV_{REFP}	√	√	√
AV_{REFM}	√	√	√
V_{SS}	√	√	√
EV_{SS0}	_Note	_Note	√
AV_{SS}	√	√	√
TOOLRxD	√	√	√
TOOLTxD	√	√	√
TOOL0	√	√	√

Note EV_{DD0} is connected to V_{DD}, and EV_{SS0} is connected to V_{SS} inside the package.

2. 1. 2. 2 Description of each function

The functions of RL78/G1E (64-pin products and 80-pin products) are described below.

(1/2)

Function Name	I/O	Function
ANI0- ANI4, ANI16- ANI18, ANI20- ANI26, ANI28, ANI30	Input	A/D converter analog input
INTP0- INTP2, INTP6	Input	External interrupt request input
KR0- KR7	Input	Key interrupt input
PCLBUZ0	Output	Clock output / buzzer output
REGC	–	Pin for connecting to regulator output stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
$\overline{\text{RESET}}$	Input	External reset signal input for the functions of microcontroller block
RxD0- RxD2	Input	Serial data input pins of serial interface UART0 to UART2
TxD0-TxD2	Output	Serial data output pins of serial interface UART0 to UART2
<R> SCK00, SCK10, SCK20, SCK21	I/O	Serial clock I/O pins of serial interface CSI00, CSI10, CSI20 and CSI21
SCL00, SCL10, SCL20	Output	Serial clock output pins of serial interface IIC00, IIC10 and IIC20
SDA00, SDA10, SDA20	I/O	Serial data I/O pins of serial interface IIC00, IIC10 and IIC20
SI00, SI10, SI20, SI21	Input	Serial data input pins of serial interface CSI00, CSI10, CSI20 and CSI21
SO00, SO10, SO20, SO21	Output	Serial data output pins of serial interface CSI00, CSI10, CSI20 and CSI21
TI00, TI04, TI07	Input	The pins for inputting an external count clock/capture trigger to 16-bit timers 00, 04 and 07
TO00, TO04, TO07	Output	Timer output pins of 16-bit timers 00, 04 and 07
X1, X2	–	Resonator connection for main system clock
EXCLK	Input	External clock input for main system clock

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Function Name	I/O	Function
V_{DD}	–	< 64-pin products > Positive power supply for port pins other than P20 to P23 and also for $\overline{RESET}$, REGC pin. < 80-pin products > Positive power supply for port pins other than P20 to P24 and also for $\overline{RESET}$, REGC pin.
AV_{DD}	–	Positive power supply for P20 to P24 and A/D converter
AV_{REFP}	Input	A/D converter reference potential (+ side) input
AV_{REFM}	Input	A/D converter reference potential (− side) input Make the potential of AV_{REFM} pin the same as AV_{SS} pin and V_{SS} pin.
V_{SS}	–	< 64-pin products > Ground potential for port pins other than P20 to P23 and also for $\overline{RESET}$, REGC pin. < 80-pin products > Ground potential for port pins other than P20 to P24 and also for $\overline{RESET}$, REGC pin.
AV_{SS}	–	Ground potential for P20 to P24 and A/D converter Make the potential of AV_{SS} pin the same as V_{SS} pin.
TOOLRxD	Input	UART reception pin for the external device connection used during flash memory programming
TOOLTxD	Output	UART transmission pin for the external device connection used during flash memory programming
TOOL0	I/O	Data I/O for flash memory programmer / debugger

<R> **Caution After reset release, the relationships between P40/TOOL0 and the operating mode are as follows.**

Table 2-2. Relationship Between P40/TOOL0 and Operation Mode After Reset Release

P40/TOOL0	Operating Mode
V_{DD}	Normal operation mode
0 V	Flash memory programming mode

For details, see **3. 25. 4 Serial programming method**.

<R> **Remark** Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} line.

2. 2 Pin Functions in Analog Block

<R> About I/O circuit type, see **2. 4 Block Diagrams of Pins**.

<R> 2. 2. 1 64-pin products

Function Name	I/O Circuit Type	I/O	Function
AV_{DD3}	–	–	Power supply pin for filter
AGND2	–	–	GND pin for gain adjustment amplifier
MPXIN60	ANALOG6	Input	Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin 0 (+))
MPXIN50	ANALOG6		Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin 0 (-))
AMP3_OUT	ANALOG10	Output	Configurable amplifier Ch3 output pin
DAC3_OUT/ VREFIN3	ANALOG2	I/O	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
AMP2_OUT	ANALOG11	Output	Configurable amplifier Ch2 output pin
AGND1	–	–	GND pin for configurable amplifiers Ch1 to Ch3.
AMP1_OUT	ANALOG11	Output	Configurable amplifier Ch1 output pin
AV_{DD1}	–	–	Power supply pin for configurable amplifiers Ch1 to Ch3
DAC2_OUT/ VREFIN2	ANALOG2	I/O	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
DAC1_OUT/ VREFIN1	ANALOG2		D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
MPXIN41	ANALOG6	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
MPXIN31	ANALOG6		Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (-))
MPXIN40	ANALOG6		Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
MPXIN30	ANALOG6		Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (-))
MPXIN21	ANALOG6		Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
MPXIN11	ANALOG6		Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (-))
MPXIN20	ANALOG6		Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
MPXIN10	ANALOG6		Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (-))
AGND3	–	–	GND pin for variable output voltage regulator and reference voltage generator
BGR_OUT	ANALOG9	Output	Reference voltage generator output pin
AV_{DD2}	–	–	Power supply pin for variable output voltage regulator and reference voltage generator
LDO_OUT	ANALOG3	Output	Variable output voltage regulator output pin
TEMP_OUT	ANALOG4	Output	Temperature sensor output pin
$\overline{ARESET}$	ANALOG5	Input	External reset signal input for the functions of analog block
DV_{DD}	–	–	Power supply pin for SPI
$\overline{SCLK}$	ANALOG8	Input	Serial clock input pin for SPI
SDO	ANALOG12	Output	Serial data output pin for SPI
SDI	ANALOG8	Input	Serial data input pin for SPI
$\overline{CS}$	ANALOG8	Input	Chip select input pin for SPI
DGND	–	–	GND pin for SPI
DAC4_OUT/ VREFIN4	ANALOG13	I/O	D/A converter Ch4 output pin/gain adjustment amplifier, filter reference voltage input pin
CLK_LPF	ANALOG7	Input	Pin for inputting low-pass filter control clock
AGND4	–	–	GND pin for filter
LPF_OUT	ANALOG1	Output	Low-pass filter output pin

<R> **2. 2. 2 80-pin products**

Function Name	I/O Circuit Type	I/O	Function
AV_{DD3}	–	–	Power supply pin for filter
SC_IN	ANALOG6	Input	Input pin for filter signal processing
CLK_SYNCH	ANALOG7	Input	Pin for inputting synchronous detector control clock
SYNCH_OUT	ANALOG11	Output	Synchronous detector output pin
AGND2	–	–	GND pin for gain adjustment amplifier
GAINAMP_OUT	ANALOG10	Output	Output pin for gain adjustment amplifier
GAINAMP_IN	ANALOG6	Input	Input pin for gain adjustment amplifier
MPXIN61	ANALOG6	Input	Multiplexer 6 input pin 1 (Configurable amplifier Ch3 input pin 1 (+))
MPXIN51	ANALOG6		Multiplexer 5 input pin 1 (Configurable amplifier Ch3 input pin 1 (-))
MPXIN60	ANALOG6		Multiplexer 6 input pin 0 (Configurable amplifier Ch3 input pin 0 (+))
MPXIN50	ANALOG6		Multiplexer 5 input pin 0 (Configurable amplifier Ch3 input pin 0 (-))
AMP3_OUT	ANALOG10	Output	Configurable amplifier Ch3 output pin
DAC3_OUT/ VREFIN3	ANALOG2	I/O	D/A converter Ch3 output pin/configurable amplifier Ch3 reference voltage input pin
AMP2_OUT	ANALOG11	Output	Configurable amplifier Ch2 output pin
AGND1	–	–	GND pin for configurable amplifiers Ch1 to Ch3
AMP1_OUT	ANALOG11	Output	Configurable amplifier Ch1 output pin
AV_{DD1}	–	–	Power supply pin for configurable amplifiers Ch1 to Ch3
DAC2_OUT/ VREFIN2	ANALOG2	I/O	D/A converter Ch2 output pin/configurable amplifier Ch2 reference voltage input pin
DAC1_OUT/ VREFIN1	ANALOG2		D/A converter Ch1 output pin/configurable amplifier Ch1 reference voltage input pin
MPXIN41	ANALOG6	Input	Multiplexer 4 input pin 1 (Configurable amplifier Ch2 input pin 1 (+))
MPXIN31	ANALOG6		Multiplexer 3 input pin 1 (Configurable amplifier Ch2 input pin 1 (-))
MPXIN40	ANALOG6		Multiplexer 4 input pin 0 (Configurable amplifier Ch2 input pin 0 (+))
MPXIN30	ANALOG6		Multiplexer 3 input pin 0 (Configurable amplifier Ch2 input pin 0 (-))
MPXIN21	ANALOG6		Multiplexer 2 input pin 1 (Configurable amplifier Ch1 input pin 1 (+))
MPXIN11	ANALOG6		Multiplexer 1 input pin 1 (Configurable amplifier Ch1 input pin 1 (-))
MPXIN20	ANALOG6		Multiplexer 2 input pin 0 (Configurable amplifier Ch1 input pin 0 (+))
MPXIN10	ANALOG6		Multiplexer 1 input pin 0 (Configurable amplifier Ch1 input pin 0 (-))
AGND3	–	–	GND pin for variable output voltage regulator and reference voltage generator
BGR_OUT	ANALOG9	Output	Reference voltage generator output pin
AV_{DD2}	–	–	Power supply pin for variable output voltage regulator and reference voltage generator
LDO_OUT	ANALOG3	Output	Variable output voltage regulator output pin
TEMP_OUT	ANALOG4	Output	Temperature sensor output pin
$\overline{ARESET}$	ANALOG5	Input	External reset signal input for the functions of analog block
DV_{DD}	–	–	Power supply pin for SPI
$\overline{SCLK}$	ANALOG8	Input	Serial clock input pin for SPI
SDO	ANALOG12	Output	Serial data output pin for SPI
SDI	ANALOG8	Input	Serial data input pin for SPI
$\overline{CS}$	ANALOG8	Input	Chip select input pin for SPI
DGND	–	–	GND pin for SPI
DAC4_OUT/ VREFIN4	ANALOG13	I/O	D/A converter Ch4 output pin/gain adjustment amplifier, filter reference voltage input pin
HPF_OUT	ANALOG1	Output	High-pass filter output pin
CLK_HPF	ANALOG7	Input	Pin for inputting high-pass filter control clock
CLK_LPF	ANALOG7	Input	Pin for inputting low-pass filter control clock
AGND4	–	–	GND pin for filter
LPF_OUT	ANALOG1	Output	Low-pass filter output pin

2. 3 Connection of Unused Pins

Table 2-3 shows the recommended connections of unused pins.

Remark The provided pins differ depending on the products. See **1. 3 Pin Configuration (Top View)**, **2. 1 Pin Functions in Microcontroller Block**, and **2. 2 Pin Functions in Analog Block**.

Table 2-3. Connections of Unused Pins

(1/2)

<R>

Pin Name	I/O	Recommended Connection of Unused Pins
P00	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open
P01	I/O	
P02	I/O	
P03	I/O	
P04	I/O	
P10	I/O	
P11	I/O	
P12	I/O	
P13	I/O	
P14	I/O	
P15	I/O	
P20	I/O	Input: Independently connect to AV_{DD} or AV_{SS} via a resistor. Output: Leave open
P21	I/O	
P22	I/O	
P23	I/O	
P24	I/O	
P40	I/O	Input: Independently connect to V_{DD} via a resistor, or leave open. Output: Leave open
P41	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open
P42	I/O	
P50	I/O	
P51	I/O	
P70	I/O	
P71	I/O	
P72	I/O	
P73	I/O	
P121	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122	Input	
P130	Output	Leave open
P137	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P140	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open
$\overline{\text{RESET}}$	Input	Connect directly or via a resistor to V_{DD}.

(2/2)

<R>

Pin Name	I/O	Recommended Connection of Unused Pins
SC_IN	Input	Connect to AGND4.
CLK_SYNCH	Input	Leave open
SYNCH_OUT	Output	
GAINAMP_OUT	Output	
GAINAMP_IN	Input	Connect to AGND2.
MPXIN61	Input	Connect to AGND1.
MPXIN51	Input	
MPXIN60	Input	
MPXIN50	Input	
AMP3_OUT	Output	Leave open
DAC3_OUT/ VREFIN3	I/O	Leave open
AMP2_OUT	Output	Leave open
AMP1_OUT	Output	Connect to AGND1.
DAC2_OUT/ VREFIN2	I/O	Leave open
DAC1_OUT/VREFIN1	I/O	
MPXIN41	Input	Connect to AGND1.
MPXIN31	Input	
MPXIN40	Input	
MPXIN30	Input	
MPXIN21	Input	
MPXIN11	Input	
MPXIN20	Input	
MPXIN10	Input	
TEMP_OUT	Output	Leave open
$\overline{SCLK}$	Input	
SDO	Output	
SDI	Input	
$\overline{CS}$	Input	
DAC4_OUT/ VREFIN4	I/O	
HPF_OUT	Output	
CLK_HPF	Input	
CLK_LPF	Input	
LPF_OUT	Output	
LDO_OUT	Output	
BGR_OUT	Output	
I.C	–	
$\overline{ARESET}$	Input	– Note

<R> **Note** When the resource pin for $\overline{ARESET}$ is to be Hi-Z, connect $\overline{ARESET}$ to DGND via a resistor.
For details of functions, see **2. 5. 31 $\overline{ARESET}$**.

<R> 2. 4 Block Diagrams of Pins

Figures 2-1 to 2-12 show the block diagrams of the pins described in **2. 1. 1 Port functions**.

Figure 2-13 shows the I/O circuit type described in **2. 2 Pin Functions in Analog Block**.

Figure 2-1. Pin Block Diagram for Pin Type 1-1-1

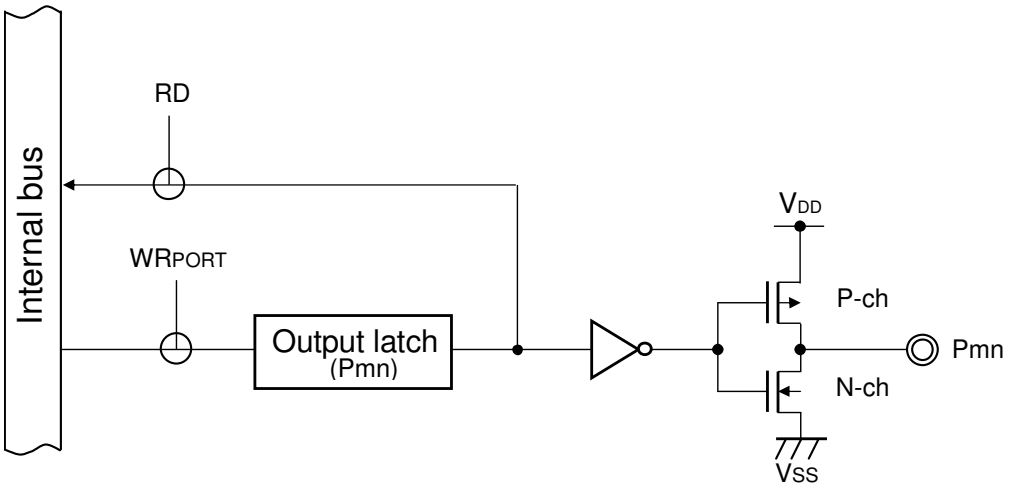


Figure 2-2. Pin Block Diagram for Pin Type 2-1-1

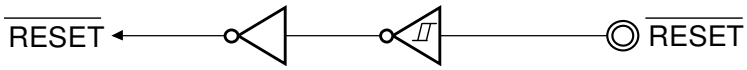
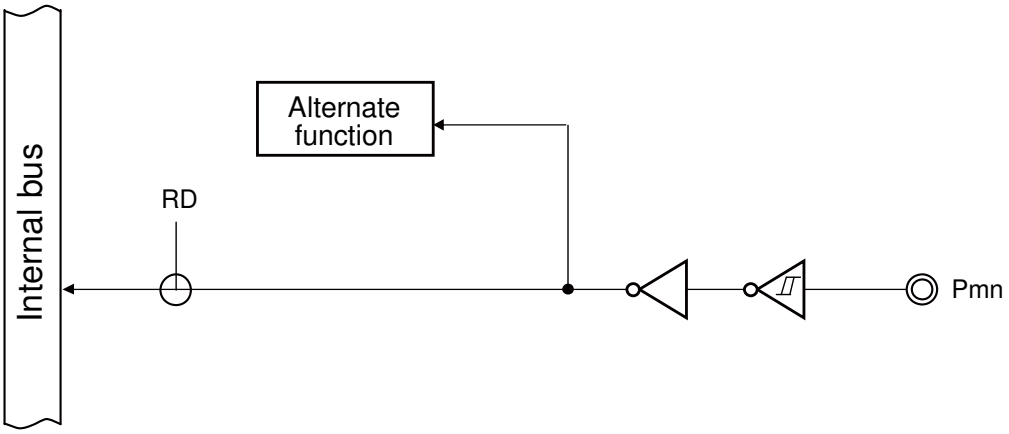


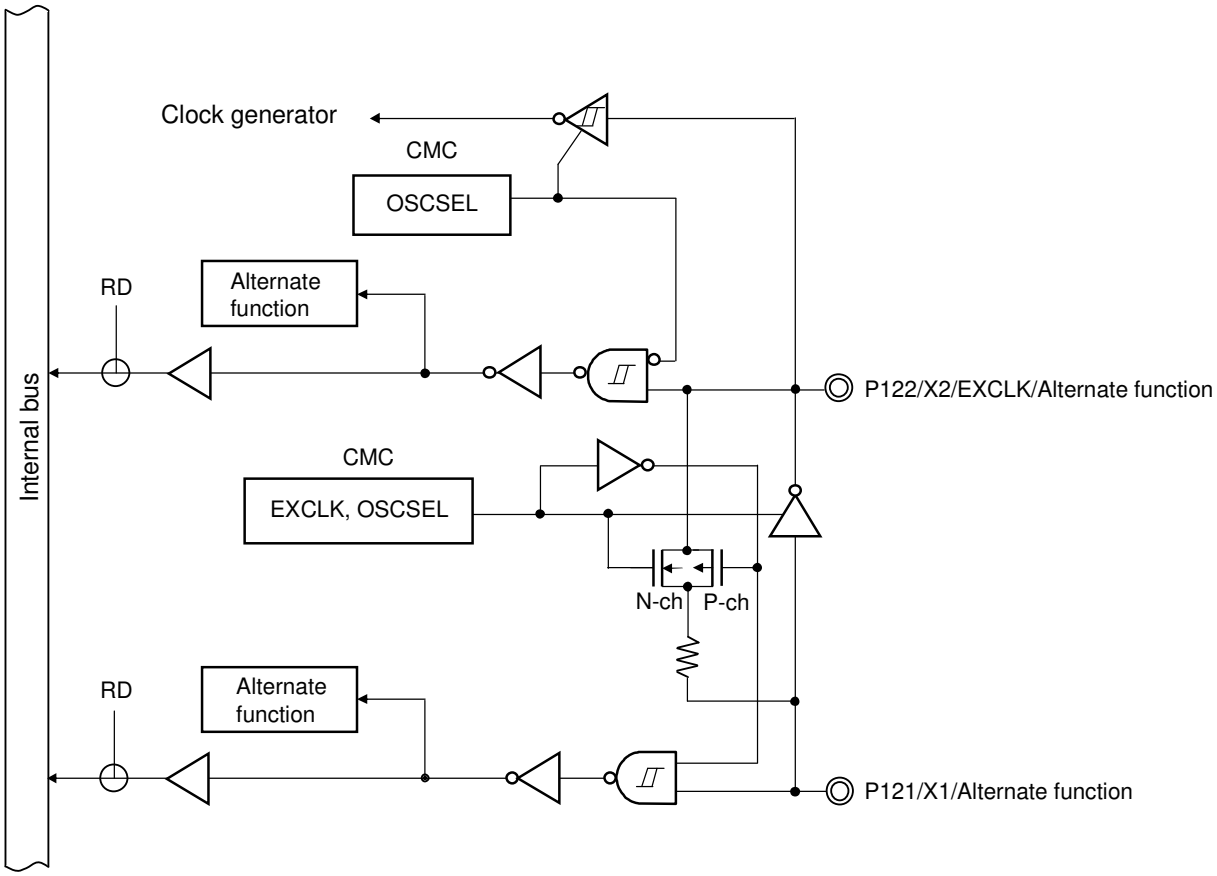
Figure 2-3. Pin Block Diagram for Pin Type 2-1-2



Remark For alternate functions, see **2. 1. 1 Port functions**.

<R>

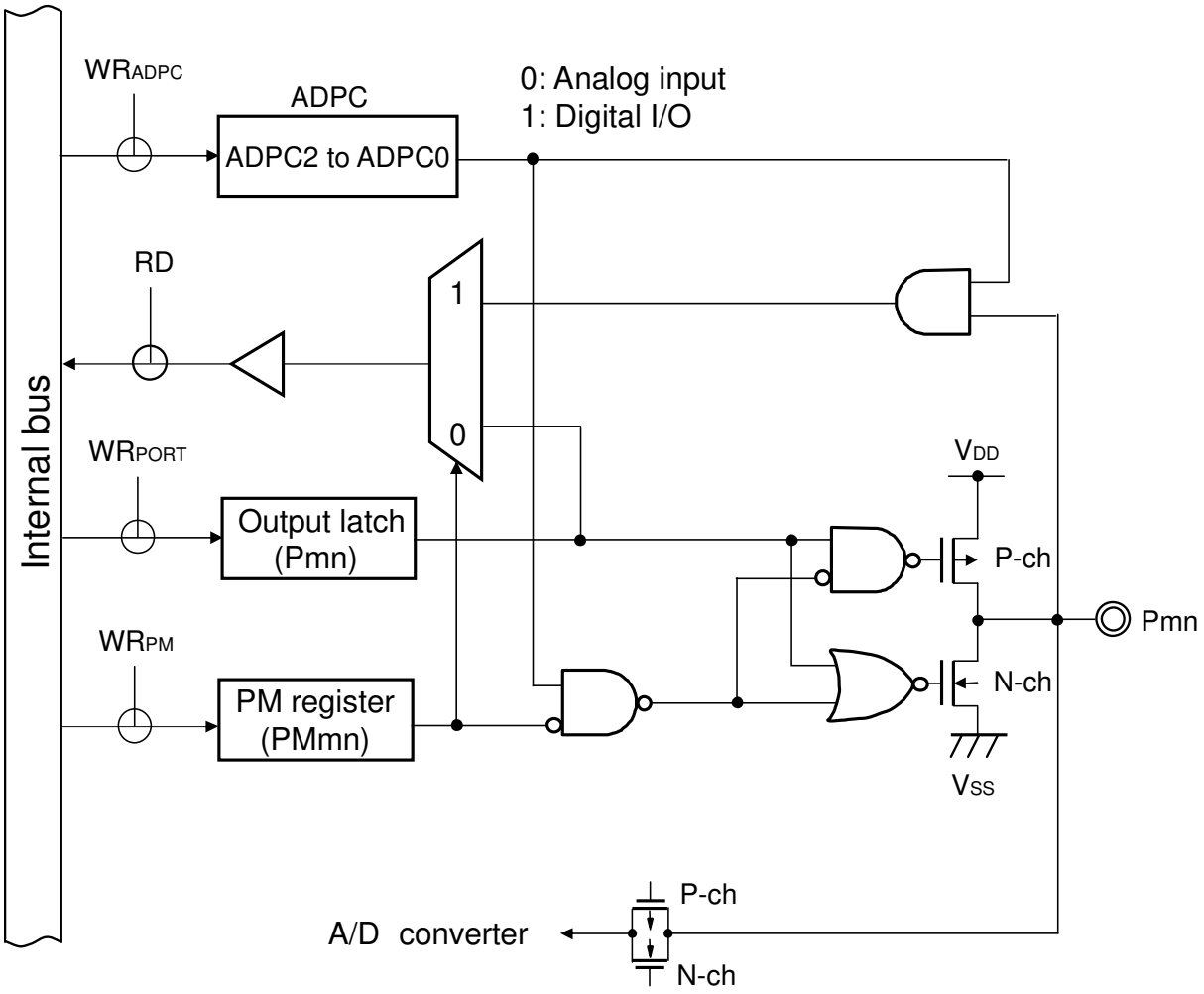
Figure 2-4. Pin Block Diagram for Pin Type 2-2-1



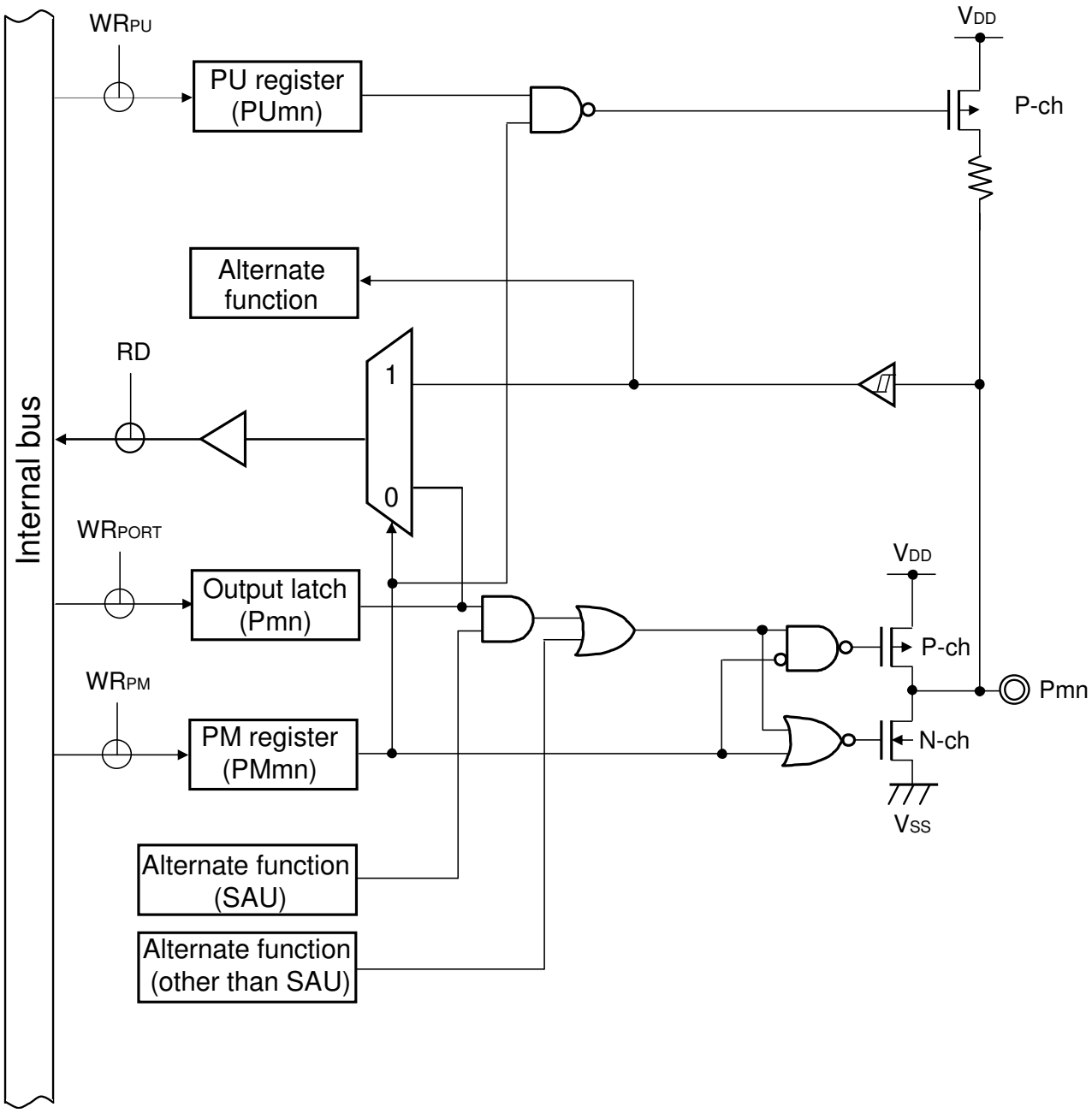
Remark For alternate functions, see **2. 1. 1 Port functions**.

<R>

Figure 2-5. Pin Block Diagram for Pin Type 4-3-1



<R> **Figure 2-6. Pin Block Diagram for Pin Type 7-1-1**

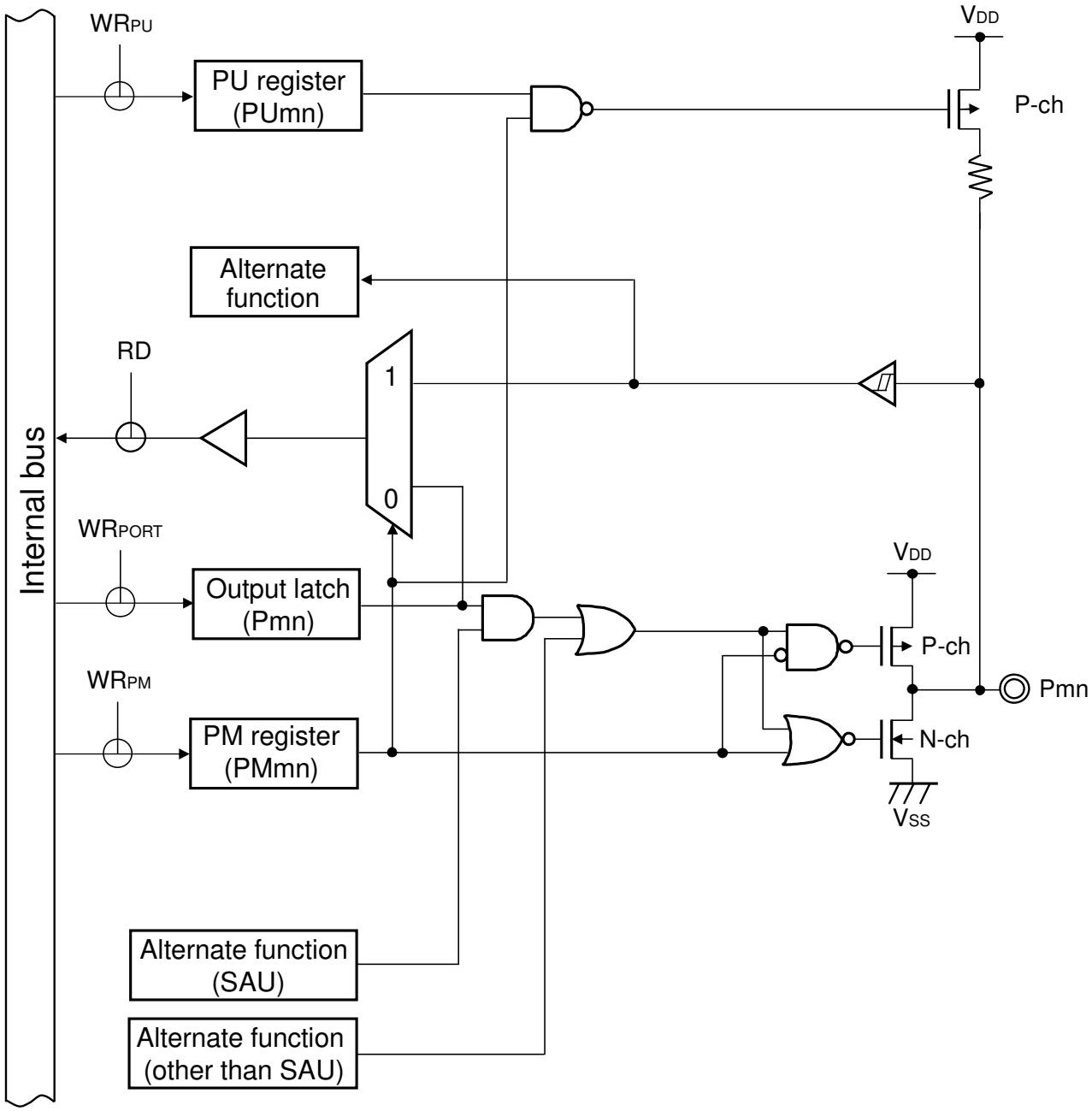


Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

<R>

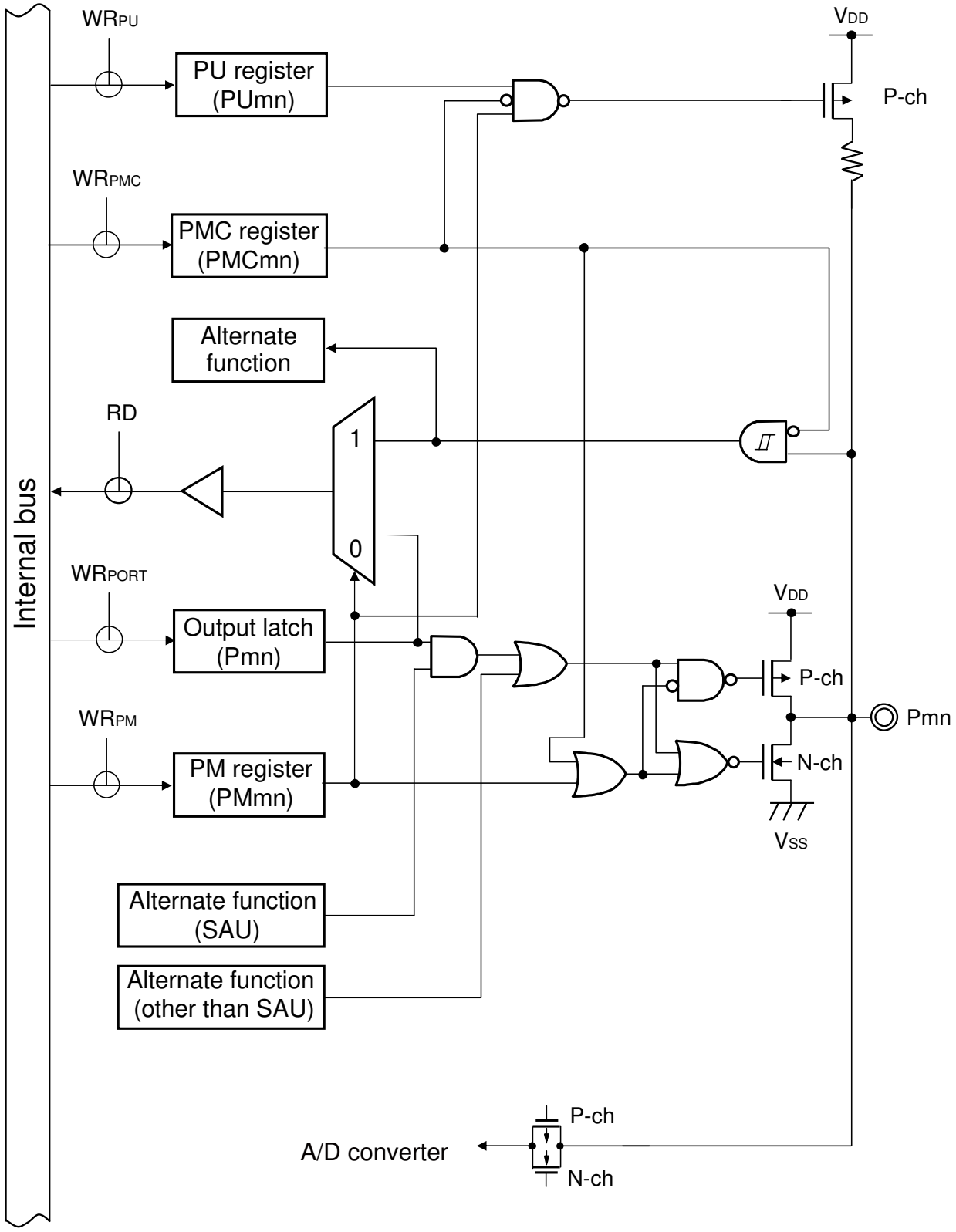
Figure 2-7. Pin Block Diagram for Pin Type 7-1-2



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

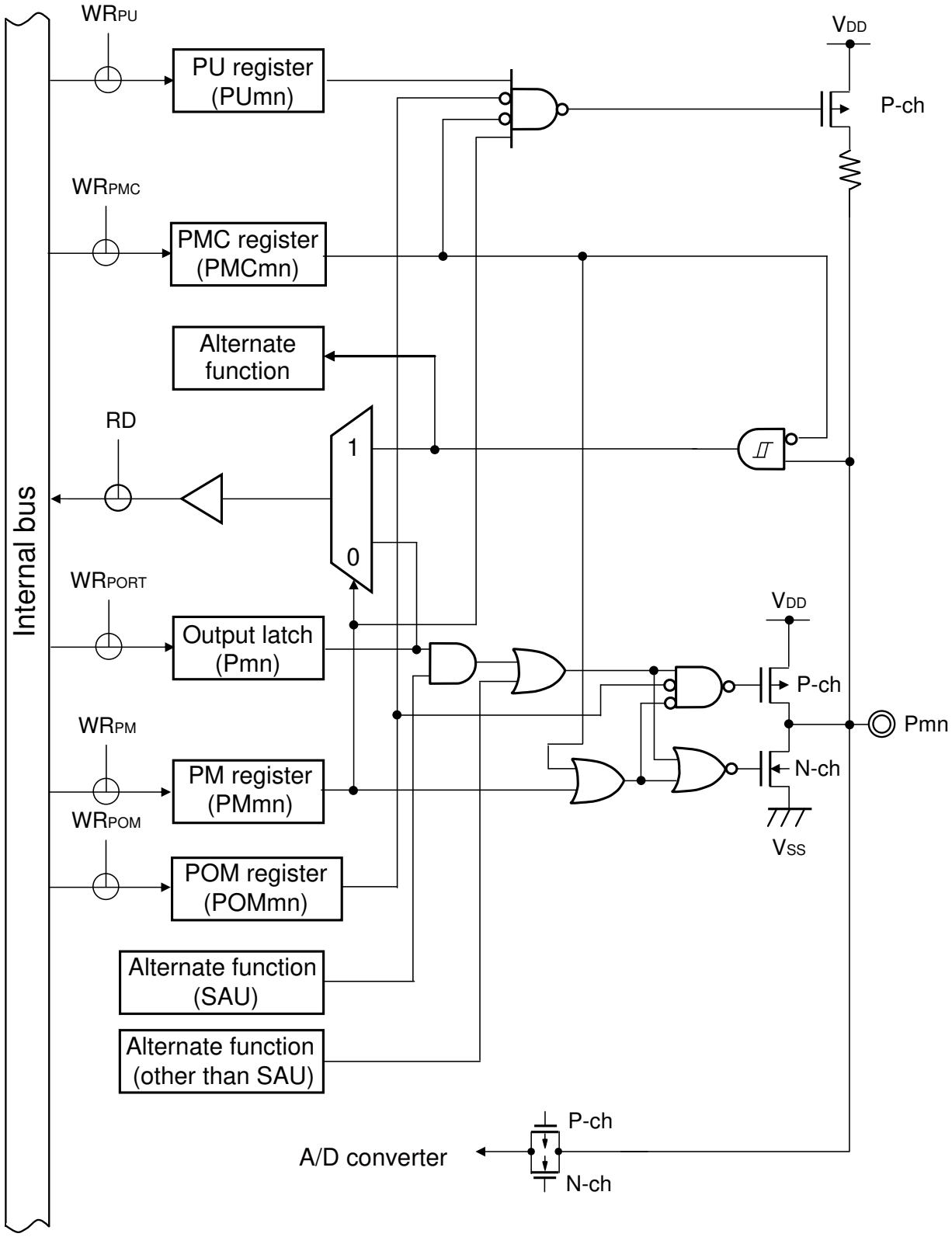
<R> **Figure 2-8. Pin Block Diagram for Pin Type 7-3-1**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

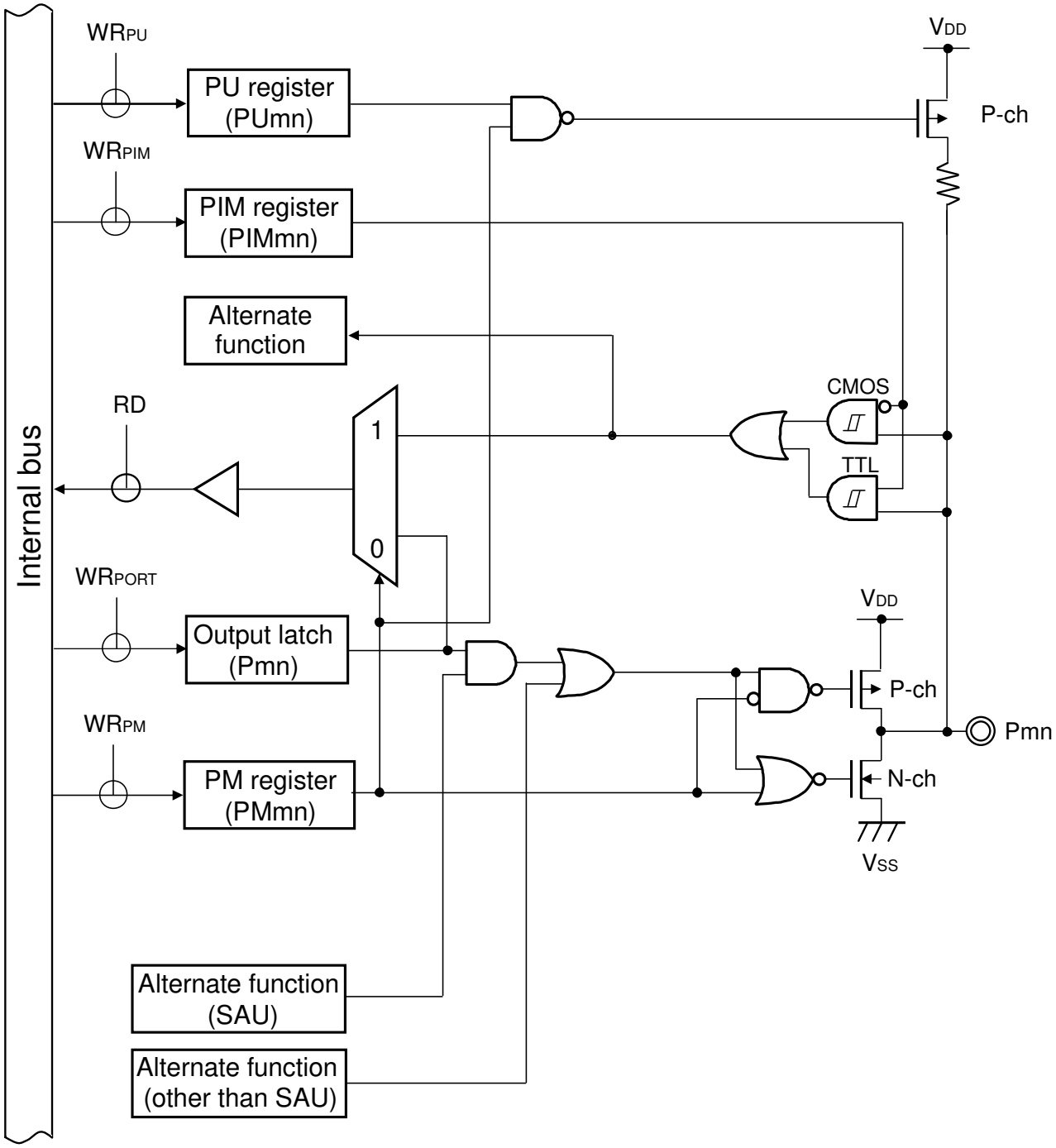
<R> **Figure 2-9. Pin Block Diagram for Pin Type 7-3-2**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

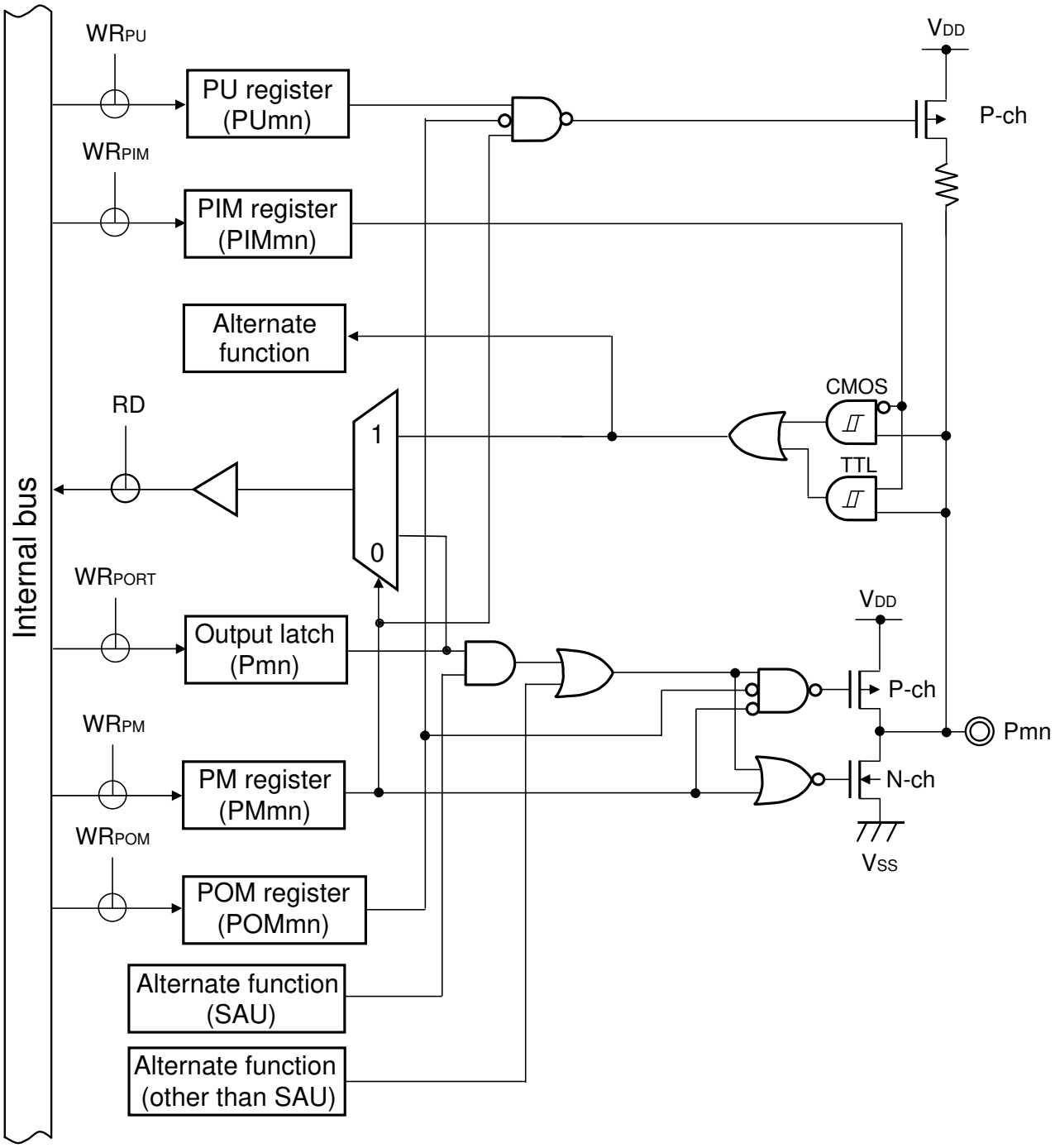
<R> **Figure 2-10. Pin Block Diagram for Pin Type 8-1-1**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

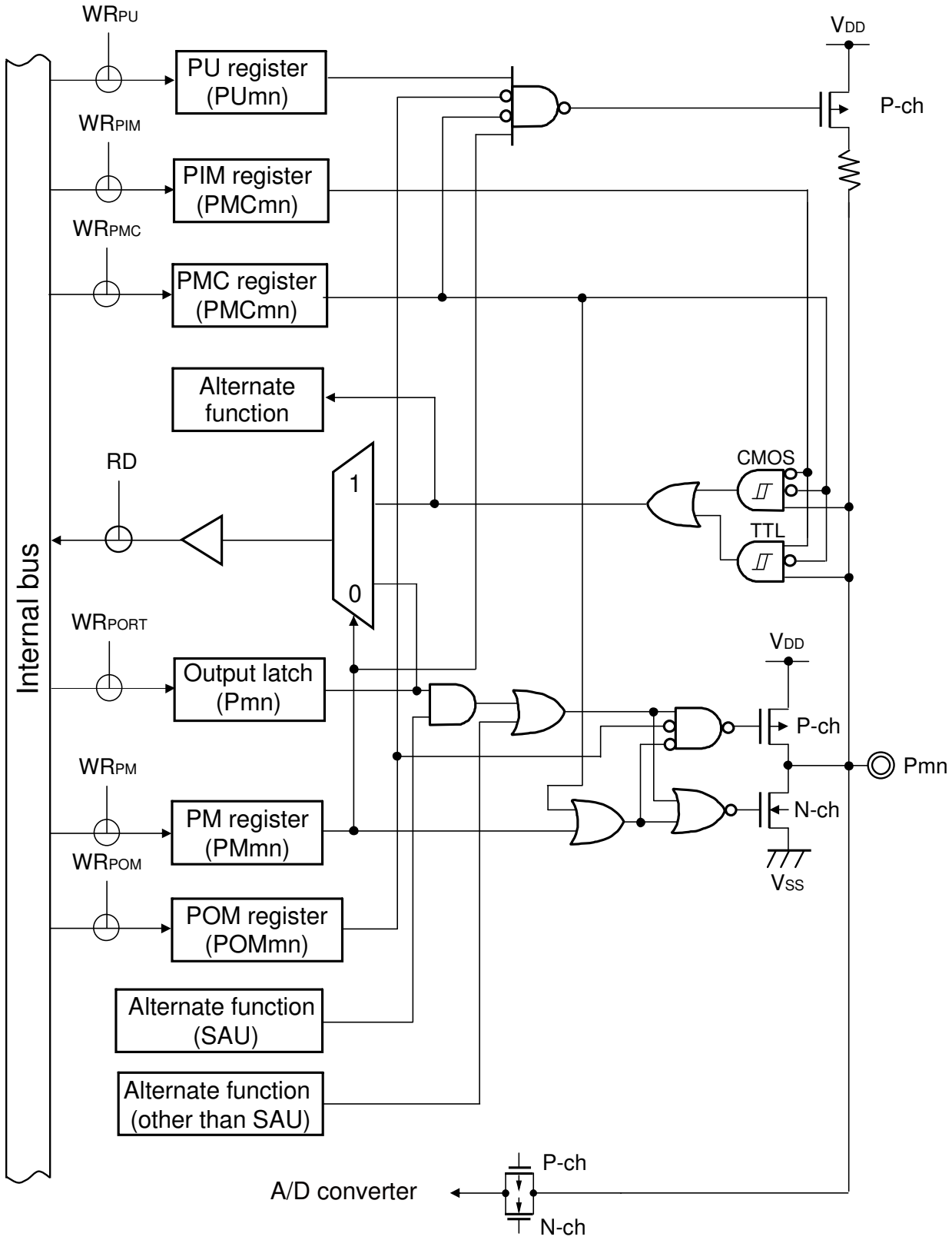
<R> **Figure 2-11. Pin Block Diagram for Pin Type 8-1-2**



Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

<R> **Figure 2-12. Pin Block Diagram for Pin Type 8-3-2**



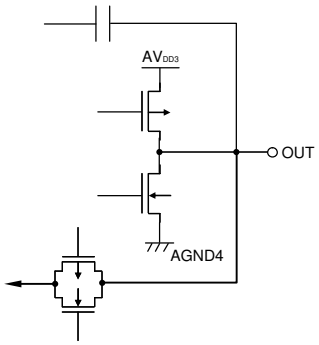
Remarks 1. For alternate functions, see **2. 1. 1 Port functions**.

2. SAU: Serial array unit

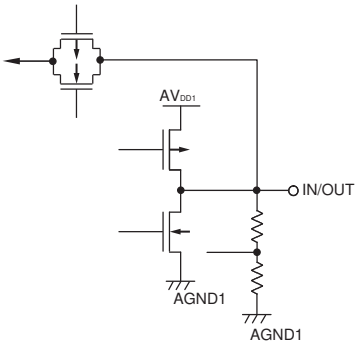
Figure 2-13. Pin I/O Circuit List (1/2)

<R>

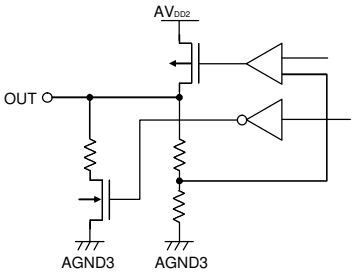
ANALOG1



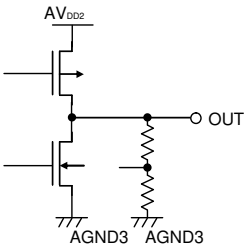
ANALOG2



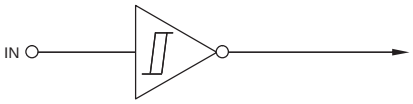
ANALOG3



ANALOG4

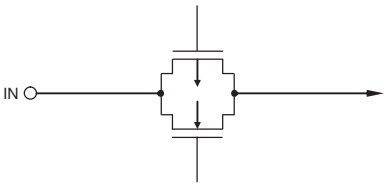


ANALOG5

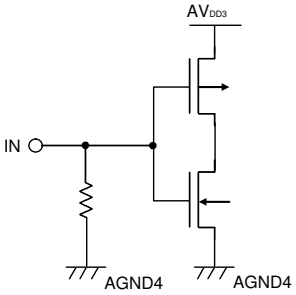


Schmitt-triggered input with hysteresis characteristics

ANALOG6



ANALOG7



ANALOG8

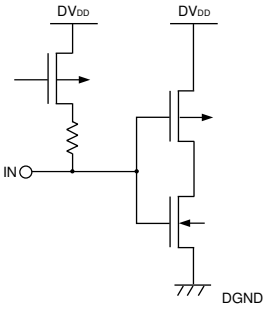
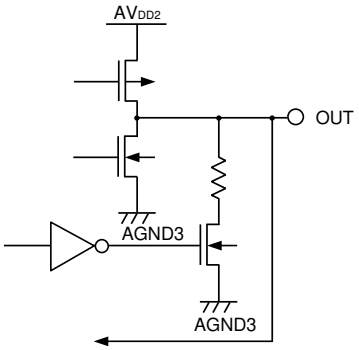
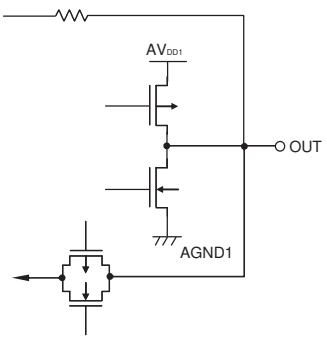


Figure 2-13. Pin I/O Circuit List (2/2)

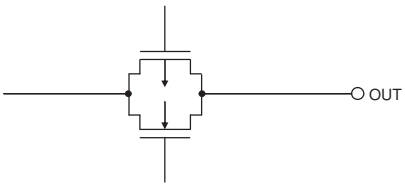
ANALOG9



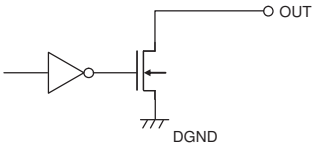
ANALOG10



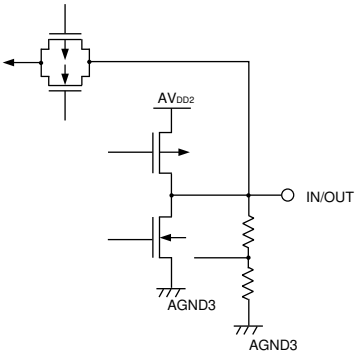
ANALOG11



ANALOG12



ANALOG13



2. 5 Instruction of Pin Functions

Remark The pins mounted depend on the product. See **1. 3 Pin Configuration (Top View)**, **2. 1 Pin Functions in Microcontroller Block**, and **2. 2 Pin Functions in Analog Block**.

2. 5. 1 Port 0 (P00 to P04)

(1) Port mode

P00 to P04 function as an I/O port. P00 to P04 can be set to input or output port in 1-bit units using port mode register 0 (PM0).

(2) Control mode

P00 to P04 function as A/D converter analog input, serial interface data I/O, clock I/O, and key return input.

(a) ANI16, ANI17

These are the analog input pins of A/D converter.

(b) SI10

This is a serial data input pin of serial interface CSI10.

(c) SO10

This is a serial data output pin of serial interface CSI10.

(d) SCK10

This is a serial clock I/O pin of serial interface CSI10.

(e) TxD1

This is a serial data output pin of serial interface UART1.

(f) RxD1

This is a serial data input pin of serial interface UART1.

(g) SDA10

This is a serial data I/O pin of serial interface IIC10.

(h) SCL10

This is a serial clock output pin of serial interface IIC10.

(i) TI00

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 00.

(j) TO00

This is the timer output pin of 16-bit timer 00.

(k) KR0 to KR4

These are the key interrupt input pins.

2. 5. 2 Port 1 (P10 to P15)

(1) Port mode

P10 to P15 function as an I/O port. P10 to P15 can be set to input or output port in 1-bit units using port mode register 1 (PM1).

(2) Control mode

P10 to P15 function as A/D converter analog input, serial interface data I/O, clock I/O, and programming UART I/O.

(a) ANI18, ANI20 to ANI24

These are the analog input pins of A/D converter.

(b) TxD0, TxD2

These are the serial data output pins of serial interface UART0 and UART2.

(c) RxD0, RxD2

These are the serial data input pins of serial interface UART0 and UART2.

<R> **(d) SCK00, SCK20**

These are the serial clock I/O pins of serial interface CSI00 and CSI20.

(e) SI00, SI20

These are the serial data input pins of serial interface CSI00 and CSI20.

(f) SO00, SO20

These are the serial data output pins of serial interface CSI00 and CSI20.

(g) TOOLTxD

This UART serial data output pin for an external device connection is used during flash memory programming.

(h) TOOLRxD

This UART serial data input pin for an external device connection is used during flash memory programming.

(i) SDA00, SDA20

These are the serial data I/O pins of serial interface IIC00 and IIC20.

(j) SCL00, SCL20

These are the serial clock output pins of serial interface IIC00 and IIC20.

(k) KR0 to KR5

These are the key interrupt input pins.

2. 5. 3 Port 2 (P20 to P24)

(1) Port mode

P20 to P24 function as an I/O port. P20 to P24 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P24 function as A/D converter analog input, and reference voltage input.

(a) ANI0 to ANI4

These are the analog input pins of A/D converter.

(b) AV_{REFP}

This is a pin that inputs the A/D converter reference potential (+ side).

(c) AV_{REFM}

This is a pin that inputs the A/D converter reference potential (– side).

(d) KR5 to KR7

These are the key interrupt input pins.

2. 5. 4 Port 4 (P40 to P42)

(1) Port mode

P40 to P42 function as an I/O port. P40 to P42 can be set to input or output port in 1-bit units using port mode register 4 (PM4).

(2) Control mode

P40 to P42 function as A/D converter analog input, data I/O for a flash memory programmer/debugger, and timer I/O.

(a) TI04, TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 04 and 07.

(b) TO04, TO07

These are the timer output pins from 16-bit timers 04 and 07.

(c) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

(d) ANI30

This is an analog input pin of A/D converter.

2. 5. 5 Port 5 (P50, P51)

(1) Port mode

P50 and P51 function as an I/O port. P50 and P51 can be set to input or output port in 1-bit units using port mode register 5 (PM5).

(2) Control mode

P50 and P51 function as A/D converter analog input, and external interrupt request input.

(a) ANI25, ANI26

These are the analog input pins of A/D converter.

(b) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2. 5. 6 Port 7 (P70 to P73)

(1) Port mode

P70 to P73 function as an I/O port. P70 to P73 can be set to input or output port in 1-bit units using port mode register 7 (PM7).

(2) Control mode

P70 to P73 function as key interrupt input, A/D converter analog input, serial interface data I/O, and clock I/O.

(a) ANI28

This is the analog input pin of A/D converter.

(b) KR0 to KR2

These are the key interrupt input pins.

(c) SI21

This is the serial data input pin of serial interface CSI21.

(d) SO21

This is the serial data output pin of serial interface CSI21.

<R> **(e) SCK21**

This is the serial clock I/O pin of serial interface CSI21.

2. 5. 7 Port 12 (P121, P122)

(1) Port mode

P121 and P122 function as an input port.

(2) Control mode

P121 and P122 function as connecting resonator for main system clock, and external clock input for main system clock.

(a) X1, X2

These are the pins for connecting a resonator for main system clock.

(c) EXCLK

This is an external clock input pin for main system clock.

2. 5. 8 Port 13 (P130, P137)

(1) Port mode

P130 functions as an output port.

P137 functions as an input port.

(2) Control mode

P137 functions as external interrupt request input.

(a) INTP0

This is an external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

2. 5. 9 Port 14 (P140)

(1) Port mode

P140 functions as an I/O port. P140 can be set to input or output port in 1-bit units using port mode register 14 (PM14).

(2) Control mode

P140 functions as clock/buzzer output, and external interrupt request input.

(a) INTP6

This is the external interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) PCLBUZ0

This is the clock/buzzer output pin.

2. 5. 10 AV_{DD}, AV_{SS}, V_{DD}, V_{SS}

(a) AV_{DD}

This is the A/D converter reference voltage input pin and the positive power supply pin of P20 to P24, and A/D converter.

(b) AV_{SS}

This is the A/D converter ground potential pin. Even when the A/D converter is not used, always use this pin with the same potential as the V_{SS} pin.

(c) V_{DD}

This is the positive power supply pin.

(d) V_{SS}

This is the ground potential pin.

Remark Use bypass capacitors (about 0.1 μF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to V_{DD} to V_{SS} line.

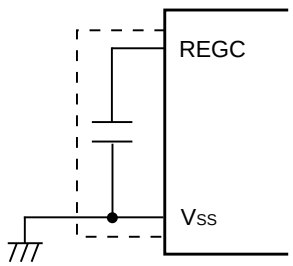
2. 5. 11 $\overline{\text{RESET}}$

This is the active-low system reset input pin for the functions of microcontroller block. When the external reset pin is not used, connect this pin directly or via a resistor to V_{DD}. When the external reset pin is used, design the circuit based on V_{DD}. For details of the functions, see **3. 5. 5 Clock generator operation, 3. 19 Reset Function, 3. 20 Power-On-Reset Circuit**.

2. 5. 12 REGC

This is the pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2. 5. 13 AV_{DD3}

This is the power supply pin for high-pass filter[Note] and low-pass filter.

2. 5. 14 SC_IN

This is the input pin for filter signal processing.

2. 5. 15 CLK_SYNCH

This is the pin for inputting synchronous detector control clock.

2. 5. 16 SYNCH_OUT

This is the synchronous detector output pin.

2. 5. 17 AGND2

This is the ground pin for gain adjustment amplifier.

2. 5. 18 GAINAMP_OUT

This is the output pin for gain adjustment amplifier.

2. 5. 19 GAINAMP_IN

This is the input pin for gain adjustment amplifier.

2. 5. 20 MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61

These are the input pins for multiplexer.

2. 5. 21 AMP1_OUT, AMP2_OUT, AMP3_OUT

These are the output pins for configurable amplifiers Ch1 to Ch3.

2. 5. 22 DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT

These are the output pins for D/A converters Ch1 to Ch4.

2. 5. 23 VREFIN1, VREFIN2, VREFIN3, VREFIN4

These are the reference voltage input pins for configurable amplifiers Ch1 to Ch3, gain adjustment amplifier, low-pass filer, and high-pass filter[Note].

Note 80-pin products only

2. 5. 24 AGND1

This is the ground pin for configurable amplifiers Ch1 to Ch3.

2. 5. 25 AV_{DD1}

This is the power supply pin for configurable amplifiers Ch1 to Ch3.

2. 5. 26 AGND3

This is the GND pin for variable output voltage regulator and reference voltage generator.

2. 5. 27 BGR_OUT

This is the output pin for reference voltage generator.

2. 5. 28 AV_{DD2}

This is the power supply pin for variable output voltage regulator and reference voltage generator.

2. 5. 29 LDO_OUT

This is the output pin for variable output voltage regulator.

2. 5. 30 TEMP_OUT

This is the output pin for temperature sensor.

2. 5. 31 $\overline{\text{ARESET}}$

This is the active-low system reset input pin for the function of analog block. After turning on DV_{DD}, it is necessary to input the external reset signal to this pin before starting SPI communication. When controlling the external reset signal by the microcontroller block of this package, it is recommended to directly connect this pin to P130 which is to be a low-level output port on reset. If the resource pin of $\overline{\text{ARESET}}$ is to be Hi-Z at a short moment, this pin must be connected to DGND via a resistor. For details of the functions, see **4. 10 Analog Reset**.

2. 5. 32 DV_{DD}

This is the power supply pin for SPI.

2. 5. 33 $\overline{\text{SCLK}}$

This is the serial clock input pin for SPI.

2. 5. 34 SDO

This is the serial data output pin for SPI.

2. 5. 35 SDI

This is the serial data input pin for SPI.

2. 5. 36 $\overline{CS}$

This is the chip select input pin for SPI.

2. 5. 37 DGND

This is the GND pin for SPI.

2. 5. 38 HPF_OUT

This is the output pin for high-pass filter.

2. 5. 39 CLK_HPF

This is the control clock input pin for high-pass filter.

2. 5. 40 CLK_LPF

This is the control clock input pin for low-pass filter.

2. 5. 41 AGND4

This is the GND pin for low-pass filter and high-pass filter.

2. 5. 42 LPF_OUT

This is the output pin for low-pass filter.

2. 5. 43 I.C

The I.C (internally connected) pin has no function and is simply connected inside the chip. This pin must always be left open.

CHAPTER 3 MICROCONTROLLER BLOCK

3. 1 Outline of This Chapter

The 16-bit microcontroller block in the RL78/G1E corresponds to the RL78/G1A (64-pin products). For the details of each function in microcontroller block, see the **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Not all of the functions of the RL78/G1A are available to be used in the RL78/G1E package because not all pins of function are drawn out of the package. In this chapter, the differences in functions and registers between the RL78/G1A and the RL78/G1E are described.

3. 2 Comparison of Each Function with RL78/G1A (64-pin products)

The differences of each function between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are as follows. For details, see the section showed in column of Remarks in the tables below.

(1/4)

Item		RL78/G1E		RL78/G1A	Remarks
		64-pin products	80-pin products	(64-pin products)	
Code flash memory (KB)		32 to 64	32 to 64	32 to 64	See the section 3. 3 about details.
Data flash memory (KB)		4	4	4	
RAM (KB)		2 to 4	2 to 4	2 to 4	
Memory space		1 MB		1 MB	
Processor registers		Control registers; PC, PSW, SP		Control registers; PC, PSW, SP	
		General-purpose register; (8-bit register × 8) × 4 banks		General-purpose register; (8-bit register × 8) × 4 banks	
		Special function registers (SFRs)		Special function registers (SFRs)	Some differences. See the section 3. 3 about details.
		Extended special function registers (2nd SFRs)		Extended special function registers (2nd SFRs)	
I/O port	Total	24	30	56	Some differences. See the section 3. 4 about details.
	COMS I/O	20	26	46	
	COMS input	3		5	
	COMS output	1		1	
	N-ch open-drain I/O (6 V tolerance)	–		4	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V		X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 3.6 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V	There are some differences between RL78/G1E and RL78/G1A. See the section 3. 5 about details. Subsystem clock is not available for RL78/G1E.
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)		HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)	
Subsystem clock		–		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.6 to 3.6 V	

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Item		RL78/G1E		RL78/G1A	Remarks
		64-pin products	80-pin products	(64-pin products)	
Low-speed on-chip oscillator		15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V		15 kHz (TYP.): V_{DD} = 1.6 to 3.6 V	Some differences. See the section 3. 5 about details. Subsystem clock is not available for RL78/G1E.
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)	
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Timer	16-bit timer	8 channels		8 channels	Some differences. See the section 3. 6 about details.
	Watchdog Timer	1 channel		1 channel	See the section 3. 10 about details.
	Real-time clock (RTC)	–		1 channel	RTC is not provided in RL78/G1E. (See 3. 7)
	12-bit Interval timer (IT)	1 channel		1 channel	See the section 3. 8 about details.
	Timer output	3 channels (PWM outputs: 2 Note)		7 channels (PWM outputs: 6 Note)	See the section 3. 6 about details.
	RTC output	–		1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	RTC is not provided in RL78/G1E. (See 3. 7)

Note The number of PWM outputs varies depending on the setting of channels in use.

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Item		RL78/G1E		RL78/G1A	Remarks
		64-pin products	80-pin products	(64-pin products)	
Clock output / Buzzer output		–	1 channel •2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)	2 channels • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	There are some differences between RL78/G1E and RL78/G1A. See the section 3. 9 about details.
8/12-bit resolution A/D converter (AV_{DD} = 1.6 to 3.6 V)		13 channels	17 channels	28 channels	Some differences. See the section 3. 11 about details.
Serial array unit		<Unit 0> • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel • UART: 1 channel <Unit 1> • CSI: 1 channel/ UART: 1 channel (LIN-bus supported)	<Unit 0> • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel • CSI: 1 channel/ simplified I^2C: 1 channel/ UART: 1 channel <Unit 1> • CSI: 2 channel/ simplified I^2C: 1 channel/ UART: 1 channel (LIN-bus supported)	<Unit 0> • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel <Unit 1> • CSI: 2 channel/ simplified I^2C: 2 channel/ UART: 1 channel (LIN-bus supported)	Some differences. See the section 3. 12 about details.
	I^2C bus	–		1 channel	Not provided in RL78/G1E. (See 3. 13)
Multiplier and divider/ multiply accumulator		5 functions (Multiplier, divider, multiply accumulator)		5 functions (Multiplier, divider, multiply accumulator)	See the section 3. 14 about details.
DMA controller		2 channels		2 channels	See the section 3. 15 about details.
Vectored interrupt sources	Internal	25		27	Some differences. See the section 3. 16 about details.
	External	2	5	13	
Key interrupt		4 (7)[Note] channels	4 (8)[Note] channels	10 channels	Some differences. See the section 3. 17 about details.

Note Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

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Item	RL78/G1E		RL78/G1A	Remarks
	64-pin products	80-pin products	(64-pin products)	
Standby function	HALT, STOP, SNOOZE mode		HALT, STOP, SNOOZE mode	See 3. 18.
Reset function	7 reset source		7 reset source	See 3. 19.
Power-on-reset circuit	Power-on-reset: 1.51 +/- 0.03V Power-down-reset: 1.50 +/- 0.03V		Power-on-reset: 1.51 +/- 0.03V Power-down-reset: 1.50 +/- 0.03V	See 3. 20.
Voltage detector	Detection level: 3 stages		Detection level: 12 stages	Some differences. See the section 3. 21 about details.
Safety functions	- Flash memory CRC operation function - CRC operation function - RAM parity error detection function - RAM guard function - SFR guard function - Invalid memory access detection function - Frequency detection function - A/D test function		- Flash memory CRC operation function - CRC operation function - RAM parity error detection function - RAM guard function - SFR guard function - Invalid memory access detection function - Frequency detection function - A/D test function	Some differences. See the section 3. 22 about details.
Regulator	1 channel		1 channel	See 3. 23
Option byte	Available		Available	Some differences. See the section 3. 24 about details.
Flash memory	Available		Available	Some differences. See the section 3. 25 about details.
On-chip debug function	Available		Available	See 3. 26
BCD correction circuit	Available		Available	See 3. 27
Instruction set	• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		• Data transfer (8/16 bits) • Adder and subtractor / logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.	See 3. 28
Power supply voltage	V_{DD} = 1.6 to 5.5 V		V_{DD} = 1.6 to 3.6 V	V_{DD} range is different.

3. 3 CPU Architecture

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 3 CPU ARCHITECURE** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 1 Memory space

See **3. 1 Memory Space** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2 Processor registers

3. 3. 2. 1 Control registers

See **3. 2. 1 Control registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 2 General-purpose registers

See **3. 2. 2 General-purpose registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 3 ES and CS registers

See **3. 2. 3 ES and CS registers** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 2. 4 Special function registers (SFRs)

The differences in special function registers (SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-1. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H				Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH				Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H				Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-1. List of Differences in Special Function Registers (SFRs) (2/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF34H	Same as RL78/G1A (64-pin products)	KRCTL		Key return control register	KRCTL	
FFF35H	Same as RL78/G1A (64-pin products)	KRF		Key return flag register	KRF	
FFF36H				Key return mode control register 1	KRM1	
FFF37H	Key return mode control register 0 Note	KRM0		Key return mode control register 0	KRM0	
FFF38H	External interrupt rising edge enable register 0 Note	EGP0		External interrupt rising edge enable register 0	EGP0	
FFF39H	External interrupt falling edge enable register 0 Note	EGN0		External interrupt falling edge enable register 0	EGN0	
FFF3AH				External interrupt rising edge enable register 1	EGP1	
FFF3BH				External interrupt falling edge enable register 1	EGN1	
FFF44H	Same as RL78/G1A (64-pin products)	TXD1/ SIO10	SDR02	Serial data register 02	TXD1/ SIO10	SDR02
FFF45H		—			—	
FFF46H	Same as RL78/G1A (64-pin products)	RXD1/ SIO11	SDR03	Serial data register 03	RXD1/ SIO11	SDR03
FFF47H		—			—	
FFF48H	Same as RL78/G1A (64-pin products)	TXD2/ SIO20	SDR10	Serial data register 10	TXD2/ SIO20	SDR10
FFF49H		—			—	
FFF4AH	Same as RL78/G1A (64-pin products)	RXD2/ SIO21	SDR11	Serial data register 11	RXD2/ SIO21	SDR11
FFF4BH		—			—	
FFF50H				IICA shift register 0	IICA0	
FFF51H				IICA status register 0	IICS0	
FFF52H				IICA flag register 0	IICF0	
FFF64H	Same as RL78/G1A (64-pin products)	TDR02		Timer data register 02	TDR02	
FFF65H						
FFF66H	Same as RL78/G1A (64-pin products)	TDR03L	TDR03	Timer data register 03	TDR03L	TDR03
FFF67H		TDR03H			TDR03H	
FFF68H	Same as RL78/G1A (64-pin products)	TDR04		Timer data register 04	TDR04	
FFF69H						
FFF6AH	Same as RL78/G1A (64-pin products)	TDR05		Timer data register 05	TDR05	
FFF6BH						
FFF6CH	Same as RL78/G1A (64-pin products)	TDR06		Timer data register 06	TDR06	
FFF6DH						
FFF6EH	Same as RL78/G1A (64-pin products)	TDR07		Timer data register 07	TDR07	
FFF6FH						

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-1. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H			Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-1. List of Differences in Special Function Registers (SFRs) (4/4)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFFB0H	Same as RL78/G1A (64-pin products)	DSA0		DMA SFR address register 0	DSA0	
FFFB1H	Same as RL78/G1A (64-pin products)	DSA1		DMA SFR address register 1	DSA1	
FFFB2H	Same as RL78/G1A (64-pin products)	DRA0L	DRA0	DMA RAM address register 0L	DRA0L	DRA0
FFFB3H	Same as RL78/G1A (64-pin products)	DRA0H		DMA RAM address register 0H	DRA0H	
FFFB4H	Same as RL78/G1A (64-pin products)	DRA1L	DRA1	DMA RAM address register 1L	DRA1L	DRA1
FFFB5H	Same as RL78/G1A (64-pin products)	DRA1H		DMA RAM address register 1H	DRA1H	
FFFB6H	Same as RL78/G1A (64-pin products)	DBC0L	DBC0	DMA byte count register 0L	DBC0L	DBC0
FFFB7H	Same as RL78/G1A (64-pin products)	DBC0H		DMA byte count register 0H	DBC0H	
FFFB8H	Same as RL78/G1A (64-pin products)	DBC1L	DBC1	DMA byte count register 1L	DBC1L	DBC1
FFFB9H	Same as RL78/G1A (64-pin products)	DBC1H		DMA byte count register 1H	DBC1H	
FFFBAH	Same as RL78/G1A (64-pin products)	DMC0		DMA mode control register 0	DMC0	
FFFBBH	Same as RL78/G1A (64-pin products)	DMC1		DMA mode control register 1	DMC1	
FFFBCH	Same as RL78/G1A (64-pin products)	DRC0		DMA operation control register 0	DRC0	
FFFBDH	Same as RL78/G1A (64-pin products)	DRC1		DMA operation control register 1	DRC1	
FFFD0H	Interrupt mask flag register 2L Note	IF2L	IF2	Interrupt mask flag register 2L	IF2L	IF2
FFFD1H	Interrupt mask flag register 2H Note	IF2H		Interrupt mask flag register 2H	IF2H	
FFFD4H	Interrupt mask flag register 0L Note	MK2L	MK2	Interrupt mask flag register 0L	MK2L	MK2
FFFD5H	Interrupt mask flag register 2H Note	MK2H		Interrupt mask flag register 2H	MK2H	
FFFD8H	Priority specification flag register 02L Note	PR02L	PR02	Priority specification flag register 02L	PR02L	PR02
FFFD9H	Priority specification flag register 02H Note	PR02H		Priority specification flag register 02H	PR02H	
FFFDCH	Priority specification flag register 12L Note	PR12L	PR12	Priority specification flag register 12L	PR12L	PR12
FFFDDH	Priority specification flag register 12H Note	PR12H		Priority specification flag register 12H	PR12H	
FFFE0H	Interrupt mask flag register 0L Note	IF0L	IF0	Interrupt mask flag register 0L	IF0L	IF0
FFFE1H	Interrupt mask flag register 0H Note	IF0H		Interrupt mask flag register 0H	IF0H	
FFFE2H	Interrupt mask flag register 1L Note	IF1L	IF1	Interrupt mask flag register 1L	IF1L	IF1
FFFE3H	Interrupt mask flag register 1H Note	IF1H		Interrupt mask flag register 1H	IF1H	
FFFE4H	Interrupt mask flag register 0L Note	MK0L	MK0	Interrupt mask flag register 0L	MK0L	MK0
FFFE5H	Interrupt mask flag register 0H Note	MK0H		Interrupt mask flag register 0H	MK0H	
FFFE6H	Interrupt mask flag register 1L Note	MK1L	MK1	Interrupt mask flag register 1L	MK1L	MK1
FFFE7H	Interrupt mask flag register 1H Note	MK1H		Interrupt mask flag register 1H	MK1H	
FFFE8H	Priority specification flag register 00L Note	PR00L	PR00	Priority specification flag register 00L	PR00L	PR00
FFFE9H	Priority specification flag register 00H Note	PR00H		Priority specification flag register 00H	PR00H	
FFFEAH	Priority specification flag register 01L Note	PR01L	PR01	Priority specification flag register 01L	PR01L	PR01
FFFEBH	Priority specification flag register 01H Note	PR01H		Priority specification flag register 01H	PR01H	
FFFECH	Priority specification flag register 10L Note	PR10L	PR10	Priority specification flag register 10L	PR10L	PR10
FFFEDH	Priority specification flag register 10H Note	PR10H		Priority specification flag register 10H	PR10H	
FFFEEH	Priority specification flag register 11L Note	PR11L	PR11	Priority specification flag register 11L	PR11L	PR11
FFFEFH	Priority specification flag register 11H Note	PR11H		Priority specification flag register 11H	PR11H	
FFFF0H FFFF1H	Same as RL78/G1A (64-pin products)	MDAL		Multiplication/division data register A (L)	MDAL	
FFFF2H FFFF3H	Same as RL78/G1A (64-pin products)	MDAH		Multiplication/division data register A (H)	MDAH	
FFFF4H FFFF5H	Same as RL78/G1A (64-pin products)	MDBH		Multiplication/division data register B (L)	MDBH	
FFFF6H FFFF7H	Same as RL78/G1A (64-pin products)	MDBL		Multiplication/division data register B (H)	MDBL	
FFFFEH	Same as RL78/G1A (64-pin products)	PMC		Processor mode control register	PMC	

Note The bit setting is different from that of RL78/G1A (64-pin products).

(2) 80-pin products

Table 3-2. List of Differences in Special Function Registers (SFRs) (1/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF00H	Port register 0 Note	P0		Port register 0	P0	
FFF01H	Port register 1 Note	P1		Port register 1	P1	
FFF02H	Port register 2 Note	P2		Port register 2	P2	
FFF03H				Port register 3	P3	
FFF04H	Port register 4 Note	P4		Port register 4	P4	
FFF05H	Same as RL78/G1A (64-pin products)	P5		Port register 5	P5	
FFF06H				Port register 6	P6	
FFF07H	Port register 7 Note	P7		Port register 7	P7	
FFF0CH	Port register 12 Note	P12		Port register 12	P12	
FFF0DH	Same as RL78/G1A (64-pin products)	P13		Port register 13	P13	
FFF0EH	Port register 14 Note	P14		Port register 14	P14	
FFF0FH				Port register 15	P15	
FFF10H	Same as RL78/G1A (64-pin products)	TXD0/ SIO00	SDR00	Serial data register 00	TXD0/ SIO00	SDR00
FFF11H		—			—	
FFF12H	Same as RL78/G1A (64-pin products)	RXD0/ SIO01	SDR01	Serial data register 01	RXD0/ SIO01	SDR01
FFF13H		—			—	
FFF18H	Same as RL78/G1A (64-pin products)	TDR00		Timer data register 00	TDR00	
FFF19H						
FFF1AH	Same as RL78/G1A (64-pin products)	TDR01L	TDR01	Timer data register 01	TDR01L	TDR01
FFF1BH		TDR01H			TDR01H	
FFF1EH	Same as RL78/G1A (64-pin products)	ADCR		12-bit A/D conversion result register	ADCR	
FFF1FH	Same as RL78/G1A (64-pin)	ADCRH		8-bit A/D conversion result register	ADCRH	
FFF20H	Port mode register 0 Note	PM0		Port mode register 0	PM0	
FFF21H	Port mode register 1 Note	PM1		Port mode register 1	PM1	
FFF22H	Port mode register 2 Note	PM2		Port mode register 2	PM2	
FFF23H				Port mode register 3	PM3	
FFF24H	Port mode register 4 Note	PM4		Port mode register 4	PM4	
FFF25H	Same as RL78/G1A (64-pin products)	PM5		Port mode register 5	PM5	
FFF26H	Port mode register 6 Note	PM6		Port mode register 6	PM6	
FFF27H	Port mode register 7 Note	PM7		Port mode register 7	PM7	
FFF2CH				Port mode register 12	PM12	
FFF2EH	Port mode register 14 Note	PM14		Port mode register 14	PM14	
FFF2FH	Port mode register 15 Note	PM15		Port mode register 15	PM15	
FFF30H	Same as RL78/G1A (64-pin products)	ADM0		A/D converter mode register 0	ADM0	
FFF31H	Analog input channel specification register Note	ADS		Analog input channel specification register	ADS	
FFF32H	A/D converter mode register 1 Note	ADM1		A/D converter mode register 1	ADM1	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-2. List of Differences in Special Function Registers (SFRs) (2/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFF34H	Same as RL78/G1A (64-pin products)	KRCTL		Key return control register	KRCTL	
FFF35H	Same as RL78/G1A (64-pin products)	KRF		Key return flag register	KRF	
FFF36H				Key return mode control register 1	KRM1	
FFF37H	Same as RL78/G1A (64-pin products)	KRM0		Key return mode control register 0	KRM0	
FFF38H	External interrupt rising edge enable register 0 Note	EGP0		External interrupt rising edge enable register 0	EGP0	
FFF39H	External interrupt falling edge enable register 0 Note	EGN0		External interrupt falling edge enable register 0	EGN0	
FFF3AH				External interrupt rising edge enable register 1	EGP1	
FFF3BH				External interrupt falling edge enable register 1	EGN1	
FFF44H	Same as RL78/G1A (64-pin products)	TXD1/ SIO10	SDR02	Serial data register 02	TXD1/ SIO10	SDR02
FFF45H		—			—	
FFF46H	Same as RL78/G1A (64-pin products)	RXD1/ SIO11	SDR03	Serial data register 03	RXD1/ SIO11	SDR03
FFF47H		—			—	
FFF48H	Same as RL78/G1A (64-pin products)	TXD2/ SIO20	SDR10	Serial data register 10	TXD2/ SIO20	SDR10
FFF49H		—			—	
FFF4AH	Same as RL78/G1A (64-pin products)	RXD2/ SIO21	SDR11	Serial data register 11	RXD2/ SIO21	SDR11
FFF4BH		—			—	
FFF50H				IICA shift register 0	IICA0	
FFF51H				IICA status register 0	IICS0	
FFF52H				IICA flag register 0	IICF0	
FFF64H	Same as RL78/G1A (64-pin products)	TDR02		Timer data register 02	TDR02	
FFF65H						
FFF66H	Same as RL78/G1A (64-pin products)	TDR03L	TDR03	Timer data register 03	TDR03L	TDR03
FFF67H		TDR03H			TDR03H	
FFF68H	Same as RL78/G1A (64-pin products)	TDR04		Timer data register 04	TDR04	
FFF69H						
FFF6AH	Same as RL78/G1A (64-pin products)	TDR05		Timer data register 05	TDR05	
FFF6BH						
FFF6CH	Same as RL78/G1A (64-pin products)	TDR06		Timer data register 06	TDR06	
FFF6DH						
FFF6EH	Same as RL78/G1A (64-pin products)	TDR07		Timer data register 07	TDR07	
FFF6FH						

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-2. List of Differences in Special Function Registers (SFRs) (3/4)

Address	RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
	SFRs Name	Symbol	SFRs Name	Symbol
FFF90H	Same as RL78/G1A (64-pin products)	ITMC	Interval timer control register	ITMC
FFF91H				
FFF92H			Second count register	SEC
FFF93H			Minute count register	MIN
FFF94H			Hour count register	HOUR
FFF95H			Week count register	WEEK
FFF96H			Day count register	DAY
FFF97H			Month count register	MONTH
FFF98H			Year count register	YEAR
FFF99H			Watch error correction register	SUBCUD
FFF9AH			Alarm minute register	ALARMWM
FFF9BH			Alarm hour register	ALARMWH
FFF9CH			Alarm week register	ALARMWW
FFF9DH			Real-time clock control register 0	RTCC0
FFF9EH			Real-time clock control register 1	RTCC1
FFFA0H	Clock operation mode control register Note	CMC	Clock operation mode control register	CMC
FFFA1H	Clock operation status control register Note	CSC	Clock operation status control register	CSC
FFFA2H	Same as RL78/G1A (64-pin products)	OSTC	Oscillation stabilization time counter status register	OSTC
FFFA3H	Same as RL78/G1A (64-pin products)	OSTS	Oscillation stabilization time select register	OSTS
FFFA4H	System clock control register Note	CKC	System clock control register	CKC
FFFA5H	Clock output select register 0 Note	CKS0	Clock output select register 0	CKS0
FFFA6H			Clock output select register 1	CKS1
FFFA8H	Same as RL78/G1A (64-pin products)	RESF	Reset control flag register	RESF
FFFA9H	Same as RL78/G1A (64-pin products)	LVIM	Voltage detection register	LVIM
FFFAAH	Same as RL78/G1A (64-pin products)	LVIS	Voltage detection level register	LVIS
FFFABH	Same as RL78/G1A (64-pin products)	WDTE	Watchdog timer enable register	WDTE
FFFACH	Same as RL78/G1A (64-pin products)	CRCIN	CRC input register	CRCIN

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-2. List of Differences in Special Function Registers (SFRs) (4/4)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	SFRs Name	Symbol		SFRs Name	Symbol	
FFFB0H	Same as RL78/G1A (64-pin products)	DSA0		DMA SFR address register 0	DSA0	
FFFB1H	Same as RL78/G1A (64-pin products)	DSA1		DMA SFR address register 1	DSA1	
FFFB2H	Same as RL78/G1A (64-pin products)	DRA0L	DRA0	DMA RAM address register 0L	DRA0L	DRA0
FFFB3H	Same as RL78/G1A (64-pin products)	DRA0H		DMA RAM address register 0H	DRA0H	
FFFB4H	Same as RL78/G1A (64-pin products)	DRA1L	DRA1	DMA RAM address register 1L	DRA1L	DRA1
FFFB5H	Same as RL78/G1A (64-pin products)	DRA1H		DMA RAM address register 1H	DRA1H	
FFFB6H	Same as RL78/G1A (64-pin products)	DBC0L	DBC0	DMA byte count register 0L	DBC0L	DBC0
FFFB7H	Same as RL78/G1A (64-pin products)	DBC0H		DMA byte count register 0H	DBC0H	
FFFB8H	Same as RL78/G1A (64-pin products)	DBC1L	DBC1	DMA byte count register 1L	DBC1L	DBC1
FFFB9H	Same as RL78/G1A (64-pin products)	DBC1H		DMA byte count register 1H	DBC1H	
FFFBAH	Same as RL78/G1A (64-pin products)	DMC0		DMA mode control register 0	DMC0	
FFFBBH	Same as RL78/G1A (64-pin products)	DMC1		DMA mode control register 1	DMC1	
FFFBCH	Same as RL78/G1A (64-pin products)	DRC0		DMA operation control register 0	DRC0	
FFFBDH	Same as RL78/G1A (64-pin products)	DRC1		DMA operation control register 1	DRC1	
FFFD0H	Interrupt mask flag register 2L Note	IF2L	IF2	Interrupt mask flag register 2L	IF2L	IF2
FFFD1H	Interrupt mask flag register 2H Note	IF2H		Interrupt mask flag register 2H	IF2H	
FFFD4H	Interrupt mask flag register 0L Note	MK2L	MK2	Interrupt mask flag register 0L	MK2L	MK2
FFFD5H	Interrupt mask flag register 2H Note	MK2H		Interrupt mask flag register 2H	MK2H	
FFFD8H	Priority specification flag register 02L Note	PR02L	PR02	Priority specification flag register 02L	PR02L	PR02
FFFD9H	Priority specification flag register 02H Note	PR02H		Priority specification flag register 02H	PR02H	
FFFDCH	Priority specification flag register 12L Note	PR12L	PR12	Priority specification flag register 12L	PR12L	PR12
FFFDDH	Priority specification flag register 12H Note	PR12H		Priority specification flag register 12H	PR12H	
FFFE0H	Interrupt mask flag register 0L Note	IF0L	IF0	Interrupt mask flag register 0L	IF0L	IF0
FFFE1H	Interrupt mask flag register 0H Note	IF0H		Interrupt mask flag register 0H	IF0H	
FFFE2H	Interrupt mask flag register 1L Note	IF1L	IF1	Interrupt mask flag register 1L	IF1L	IF1
FFFE3H	Interrupt mask flag register 1H Note	IF1H		Interrupt mask flag register 1H	IF1H	
FFFE4H	Interrupt mask flag register 0L Note	MK0L	MK0	Interrupt mask flag register 0L	MK0L	MK0
FFFE5H	Interrupt mask flag register 0H Note	MK0H		Interrupt mask flag register 0H	MK0H	
FFFE6H	Interrupt mask flag register 1L Note	MK1L	MK1	Interrupt mask flag register 1L	MK1L	MK1
FFFE7H	Interrupt mask flag register 1H Note	MK1H		Interrupt mask flag register 1H	MK1H	
FFFE8H	Priority specification flag register 00L Note	PR00L	PR00	Priority specification flag register 00L	PR00L	PR00
FFFE9H	Priority specification flag register 00H Note	PR00H		Priority specification flag register 00H	PR00H	
FFFEAH	Priority specification flag register 01L Note	PR01L	PR01	Priority specification flag register 01L	PR01L	PR01
FFFEBH	Priority specification flag register 01H Note	PR01H		Priority specification flag register 01H	PR01H	
FFFECH	Priority specification flag register 10L Note	PR10L	PR10	Priority specification flag register 10L	PR10L	PR10
FFFEDH	Priority specification flag register 10H Note	PR10H		Priority specification flag register 10H	PR10H	
FFFEEH	Priority specification flag register 11L Note	PR11L	PR11	Priority specification flag register 11L	PR11L	PR11
FFFEFH	Priority specification flag register 11H Note	PR11H		Priority specification flag register 11H	PR11H	
FFFF0H FFFF1H	Same as RL78/G1A (64-pin products)	MDAL		Multiplication/division data register A (L)	MDAL	
FFFF2H FFFF3H	Same as RL78/G1A (64-pin products)	MDAH		Multiplication/division data register A (H)	MDAH	
FFFF4H FFFF5H	Same as RL78/G1A (64-pin products)	MDBH		Multiplication/division data register B (L)	MDBH	
FFFF6H FFFF7H	Same as RL78/G1A (64-pin products)	MDBL		Multiplication/division data register B (H)	MDBL	
FFFFEH	Same as RL78/G1A (64-pin products)	PMC		Processor mode control register	PMC	

Note The bit setting is different from that of RL78/G1A (64-pin products).

3. 3. 2. 5 Expanded special function registers (2nd SFRs)

The differences in expanded special function registers (2nd SFRs) between RL78/G1E (64-pin products, 80-pin products) and RL78/G1A (64-pin products) are shown in the tables below.

(1) 64-pin products

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (1/6)

Address	RL78/G1E (64-pin products)		RL78/G1A (64-pin products)	
	2nd SFRs Name	Symbol	2nd SFRs Name	Symbol
F0010H	Same as RL78/G1A (64-pin products)	ADM2	A/D converter mode register 2	ADM2
F0011H	Same as RL78/G1A (64-pin products)	ADUL	Conversion result comparison upper limit setting register	ADUL
F0012H	Same as RL78/G1A (64-pin products)	ADLL	Conversion result comparison lower limit setting register	ADLL
F0013H	Same as RL78/G1A (64-pin products)	ADTES	A/D test register	ADTES
F0030H	Pull-up resistor option register 0 Note	PU0	Pull-up resistor option register 0	PU0
F0031H	Pull-up resistor option register 1 Note	PU1	Pull-up resistor option register 1	PU1
F0033H			Pull-up resistor option register 3	PU3
F0034H	Pull-up resistor option register 4 Note	PU4	Pull-up resistor option register 4	PU4
F0035H			Pull-up resistor option register 5	PU5
F0037H	Pull-up resistor option register 7 Note	PU7	Pull-up resistor option register 7	PU7
F003CH			Pull-up resistor option register 12	PU12
F003EH			Pull-up resistor option register 14	PU14
F0040H	Port input mode register 0 Note	PIM0	Port input mode register 0	PIM0
F0041H	Port input mode register 1 Note	PIM1	Port input mode register 1	PIM1
F0050H	Port output mode register 0 Note	POM0	Port output mode register 0	POM0
F0051H	Port output mode register 1 Note	POM1	Port output mode register 1	POM1
F0055H			Port output mode register 5	POM5
F0057H			Port output mode register 7	POM7
F0060H	Same as RL78/G1A (64-pin products)	PMC0	Port mode control register 0	PMC0
F0061H	Port mode control register 1 Note	PMC1	Port mode control register 1	PMC1
F0063H			Port mode control register 3	PMC3
F0064H	Same as RL78/G1A (64-pin products)	PMC4	Port mode control register 4	PMC4
F0065H			Port mode control register 5	PMC5
F0067H	Same as RL78/G1A (64-pin products)	PMC7	Port mode control register 7	PMC7
F006CH			Port mode control register 12	PMC12
F0070H	Same as RL78/G1A (64-pin products)	NFEN0	Noise filter enable register 0	NFEN0
F0071H	Noise filter enable register 1 Note	NFEN1	Noise filter enable register 1	NFEN1

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (2/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0073H	Same as RL78/G1A (64-pin products)	ISC		Input switch control register	ISC	
F0074H	Timer input select register 0 Note	TIS0		Timer input select register 0	TIS0	
F0076H	A/D port configuration register Note	ADPC		A/D port configuration register	ADPC	
F0077H	Peripheral I/O redirection register Note	PIOR		Peripheral I/O redirection register	PIOR	
F0078H	Same as RL78/G1A (64-pin products)	IAWCTL		Invalid memory access detection control register	IAWCTL	
F007CH	Same as RL78/G1A (64-pin products)	GAIDIS		Global analog input disable register	GAIDIS	
F007DH				Global digital input disable register	GDIDIS	
F0090H	Same as RL78/G1A (64-pin products)	DFLCTL		Data flash control register	DFLCTL	
F00A0H	Same as RL78/G1A (64-pin products)	HIOTRM		High-speed on-chip oscillator trimming register	HIOTRM	
F00A8H	Same as RL78/G1A (64-pin products)	HOCODIV		High-speed on-chip oscillator frequency select register	HOCODIV	
F00E0H	Same as RL78/G1A (64-pin products)	MDCL		Multiplication/division data register C (L)	MDCL	
F00E2H	Same as RL78/G1A (64-pin products)	MDCH		Multiplication/division data register C (H)	MDCH	
F00E8H	Same as RL78/G1A (64-pin products)	MDUC		Multiplication/division control register	MDUC	
F00F0H	Peripheral enable register 0 Note	PER0		Peripheral enable register 0	PER0	
<R> F00F3H	Subsystem clock supply mode control register Note	OSMC		Subsystem clock supply mode control register	OSMC	
F00F5H	Same as RL78/G1A (64-pin products)	RPECTL		RAM parity error control register	RPECTL	
F00FEH	Same as RL78/G1A (64-pin products)	BCDADJ		BCD adjust result register	BCDADJ	
F0100H	Same as RL78/G1A (64-pin products)	SSR00L	SSR00	Serial status register 00	SSR00L	SSR00
F0101H		—			—	
F0102H	Same as RL78/G1A (64-pin products)	SSR01L	SSR01	Serial status register 01	SSR01L	SSR01
F0103H		—			—	
F0104H	Same as RL78/G1A (64-pin products)	SSR02L	SSR02	Serial status register 02	SSR02L	SSR02
F0105H		—			—	
F0106H	Same as RL78/G1A (64-pin products)	SSR03L	SSR03	Serial status register 03	SSR03L	SSR03
F0107H		—			—	
F0108H	Same as RL78/G1A (64-pin products)	SIR00L	SIR00	Serial flag clear trigger register 00	SIR00L	SIR00
F0109H		—			—	
F010AH	Same as RL78/G1A (64-pin products)	SIR01L	SIR01	Serial flag clear trigger register 01	SIR01L	SIR01
F010BH		—			—	
F010CH	Same as RL78/G1A (64-pin products)	SIR02L	SIR02	Serial flag clear trigger register 02	SIR02L	SIR02
F010DH		—			—	
F010EH	Same as RL78/G1A (64-pin products)	SIR03L	SIR03	Serial flag clear trigger register 03	SIR03L	SIR03
F010FH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (3/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0110H	Same as RL78/G1A (64-pin products)	SMR00		Serial mode register 00	SMR00	
F0111H						
F0112H	Serial mode register 01 Note	SMR01		Serial mode register 01	SMR01	
F0113H						
F0114H	Serial mode register 02 Note	SMR02		Serial mode register 02	SMR02	
F0115H						
F0116H	Serial mode register 03 Note	SMR03		Serial mode register 03	SMR03	
F0117H						
F0118H	Same as RL78/G1A (64-pin products)	SCR00		Serial communication operation setting register 00	SCR00	
F0119H						
F011AH	Serial communication operation setting register 01 Note	SCR01		Serial communication operation setting register 01	SCR01	
F011BH						
F011CH	Serial communication operation setting register 02 Note	SCR02		Serial communication operation setting register 02	SCR02	
F011DH						
F011EH	Serial communication operation setting register 03 Note	SCR03		Serial communication operation setting register 03	SCR03	
F011FH						
F0120H	Same as RL78/G1A (64-pin products)	SE0L	SE0	Serial channel enable status register 0	SE0L	SE0
F0121H		—			—	
F0122H	Same as RL78/G1A (64-pin products)	SS0L	SS0	Serial channel start register 0	SS0L	SS0
F0123H		—			—	
F0124H	Same as RL78/G1A (64-pin products)	ST0L	ST0	Serial channel stop register 0	ST0L	ST0
F0125H		—			—	
F0126H	Same as RL78/G1A (64-pin products)	SPS0L	SPS0	Serial clock select register 0	SPS0L	SPS0
F0127H		—			—	
F0128H	Same as RL78/G1A (64-pin products)	SO0		Serial output register 0	SO0	
F0129H						
F012AH	Same as RL78/G1A (64-pin products)	SOE0L	SOE0	Serial output enable register 0	SOE0L	SOE0
F012BH		—			—	
F0134H	Same as RL78/G1A (64-pin products)	SOL0L	SOL0	Serial output level register 0	SOL0L	SOL0
F0135H		—			—	
F0138H	Same as RL78/G1A (64-pin products)	SSC0L	SSC0	Serial standby control register 0	SSC0L	SSC0
		—			—	
F0140H	Same as RL78/G1A (64-pin products)	SSR10L	SSR10	Serial status register 10	SSR10L	SSR10
F0141H		—			—	
F0142H	Same as RL78/G1A (64-pin products)	SSR11L	SSR11	Serial status register 11	SSR11L	SSR11
F0143H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Serial mode register 10 Note	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Serial communication operation setting register 10 Note	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0180H	Same as RL78/G1A (64-pin products)	TCR00		Timer counter register 00	TCR00	
F0181H						
F0182H	Same as RL78/G1A (64-pin products)	TCR01		Timer counter register 01	TCR01	
F0183H						
F0184H	Same as RL78/G1A (64-pin products)	TCR02		Timer counter register 02	TCR02	
F0185H						
F0186H	Same as RL78/G1A (64-pin products)	TCR03		Timer counter register 03	TCR03	
F0187H						
F0188H	Same as RL78/G1A (64-pin products)	TCR04		Timer counter register 04	TCR04	
F0189H						
F018AH	Same as RL78/G1A (64-pin products)	TCR05		Timer counter register 05	TCR05	
F018BH						
F018CH	Same as RL78/G1A (64-pin products)	TCR06		Timer counter register 06	TCR06	
F018DH						
F018EH	Same as RL78/G1A (64-pin products)	TCR07		Timer counter register 07	TCR07	
F018FH						
F0190H	Same as RL78/G1A (64-pin products)	TMR00		Timer mode register 00	TMR00	
F0191H						
F0192H	Timer mode register 01 Note	TMR01		Timer mode register 01	TMR01	
F0193H						
F0194H	Timer mode register 02 Note	TMR02		Timer mode register 02	TMR02	
F0195H						
F0196H	Timer mode register 03 Note	TMR03		Timer mode register 03	TMR03	
F0197H						
F0198H	Same as RL78/G1A (64-pin products)	TMR04		Timer mode register 04	TMR04	
F0199H						
F019AH	Timer mode register 05 Note	TMR05		Timer mode register 05	TMR05	
F019BH						
F019CH	Timer mode register 06 Note	TMR06		Timer mode register 06	TMR06	
F019DH						
F019EH	Same as RL78/G1A (64-pin products)	TMR07		Timer mode register 07	TMR07	
F019FH						
F01A0H	Same as RL78/G1A (64-pin products)	TSR00L	TSR00	Timer status register 00	TSR00L	TSR00
F01A1H		—			—	
F01A2H	Same as RL78/G1A (64-pin products)	TSR01L	TSR01	Timer status register 01	TSR01L	TSR01
F01A3H		—			—	
F01A4H	Same as RL78/G1A (64-pin products)	TSR02L	TSR02	Timer status register 02	TSR02L	TSR02
F01A5H		—			—	
F01A6H	Same as RL78/G1A (64-pin products)	TSR03L	TSR03	Timer status register 03	TSR03L	TSR03
F01A7H		—			—	
F01A8H	Same as RL78/G1A (64-pin products)	TSR04L	TSR04	Timer status register 04	TSR04L	TSR04
F01A9H		—			—	
F01AAH	Same as RL78/G1A (64-pin products)	TSR05L	TSR05	Timer status register 05	TSR05L	TSR05
F01ABH		—			—	
F01ACH	Same as RL78/G1A (64-pin products)	TSR06L	TSR06	Timer status register 06	TSR06L	TSR06
F01ADH		—			—	
F01AEH	Same as RL78/G1A (64-pin products)	TSR07L	TSR07	Timer status register 07	TSR07L	TSR07
F01AFH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-3. List of Differences in Expanded Special Function Registers (2nd SFRs) (6/6)

Address	RL78/G1E (64-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F01B0H	Same as RL78/G1A (64-pin products)	TE0L	TE0	Timer channel enable status register 0	TE0L	TE0
F01B1H		–			–	
F01B2H	Same as RL78/G1A (64-pin products)	TS0L	TS0	Timer channel start register 0	TS0L	TS0
F01B3H		–			–	
F01B4H	Same as RL78/G1A (64-pin products)	TT0L	TT0	Timer channel stop register 0	TT0L	TT0
F01B5H		–			–	
F01B6H	Same as RL78/G1A (64-pin products)	TPS0		Timer clock select register 0	TPS0	
F01B7H						
F01B8H	Timer output register 0 Note	TO0L	TO0	Timer output register 0	TO0L	TO0
F01B9H		–			–	
F01BAH	Timer output enable register 0 Note	TOE0L	TOE0	Timer output enable register 0	TOE0L	TOE0
F01BBH		–			–	
F01BCH	Timer output level register 0 Note	TOL0L	TOL0	Timer output level register 0	TOL0L	TOL0
F01BDH		–			–	
F01BEH	Timer output mode register 0 Note	TOM0L	TOM0	Timer output mode register 0	TOM0L	TOM0
F01BFH		–			–	
F0230H				IICA control register 00	IICCTL00	
F0231H				IICA control register 01	IICCTL01	
F0232H				IICA low-level width setting register 0	IICWL0	
F0233H				IICA high-level width setting register 0	IICWH0	
F0234H				Slave address register 0	SVA40	
F02F0H	Same as RL78/G1A (64-pin products)	CRC0CTL		Flash memory CRC control register	CRC0CTL	
F02F2H	Same as RL78/G1A (64-pin products)	PGCRCL		Flash memory CRC operation result register	PGCRCL	
F02FAH	Same as RL78/G1A (64-pin products)	CRCD		CRC data register	CRCD	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

(2) 80-pin products

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (1/6)

Address	RL78/G1E (80-pin products)		RL78/G1A (64-pin products)	
	2nd SFRs Name	Symbol	2nd SFRs Name	Symbol
F0010H	Same as RL78/G1A (64-pin products)	ADM2	A/D converter mode register 2	ADM2
F0011H	Same as RL78/G1A (64-pin products)	ADUL	Conversion result comparison upper limit setting register	ADUL
F0012H	Same as RL78/G1A (64-pin products)	ADLL	Conversion result comparison lower limit setting register	ADLL
F0013H	Same as RL78/G1A (64-pin products)	ADTES	A/D test register	ADTES
F0030H	Pull-up resistor option register 0 Note	PU0	Pull-up resistor option register 0	PU0
F0031H	Pull-up resistor option register 1 Note	PU1	Pull-up resistor option register 1	PU1
F0033H			Pull-up resistor option register 3	PU3
F0034H	Pull-up resistor option register 4 Note	PU4	Pull-up resistor option register 4	PU4
F0035H	Same as RL78/G1A (64-pin products)	PU5	Pull-up resistor option register 5	PU5
F0037H	Pull-up resistor option register 7 Note	PU7	Pull-up resistor option register 7	PU7
F003CH			Pull-up resistor option register 12	PU12
F003EH	Pull-up resistor option register 14 Note	PU14	Pull-up resistor option register 14	PU14
F0040H	Same as RL78/G1A (64-pin products)	PIM0	Port input mode register 0	PIM0
F0041H	Port input mode register 1 Note	PIM1	Port input mode register 1	PIM1
F0050H	Same as RL78/G1A (64-pin products)	POM0	Port output mode register 0	POM0
F0051H	Same as RL78/G1A (64-pin products)	POM1	Port output mode register 1	POM1
F0055H	Same as RL78/G1A (64-pin products)	POM5	Port output mode register 5	POM5
F0057H			Port output mode register 7	POM7
F0060H	Same as RL78/G1A (64-pin products)	PMC0	Port mode control register 0	PMC0
F0061H	Same as RL78/G1A (64-pin products)	PMC1	Port mode control register 1	PMC1
F0063H			Port mode control register 3	PMC3
F0064H	Same as RL78/G1A (64-pin products)	PMC4	Port mode control register 4	PMC4
F0065H	Same as RL78/G1A (64-pin products)	PMC5	Port mode control register 5	PMC5
F0067H	Same as RL78/G1A (64-pin products)	PMC7	Port mode control register 7	PMC7
F006CH			Port mode control register 12	PMC12
F0070H	Same as RL78/G1A (64-pin products)	NFEN0	Noise filter enable register 0	NFEN0
F0071H	Noise filter enable register 1 Note	NFEN1	Noise filter enable register 1	NFEN1

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (2/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0073H	Same as RL78/G1A (64-pin products)	ISC		Input switch control register	ISC	
F0074H	Timer input select register 0 Note	TIS0		Timer input select register 0	TIS0	
F0076H	A/D port configuration register Note	ADPC		A/D port configuration register	ADPC	
F0077H	Peripheral I/O redirection register Note	PIOR		Peripheral I/O redirection register	PIOR	
F0078H	Same as RL78/G1A (64-pin products)	IAWCTL		Invalid memory access detection control register	IAWCTL	
F007CH	Same as RL78/G1A (64-pin products)	GAIDIS		Global analog input disable register	GAIDIS	
F007DH				Global digital input disable register	GDIDIS	
F0090H	Same as RL78/G1A (64-pin products)	DFLCTL		Data flash control register	DFLCTL	
F00A0H	Same as RL78/G1A (64-pin products)	HIOTRM		High-speed on-chip oscillator trimming register	HIOTRM	
F00A8H	Same as RL78/G1A (64-pin products)	HOCODIV		High-speed on-chip oscillator frequency select register	HOCODIV	
F00E0H	Same as RL78/G1A (64-pin products)	MDCL		Multiplication/division data register C (L)	MDCL	
F00E2H	Same as RL78/G1A (64-pin products)	MDCH		Multiplication/division data register C (H)	MDCH	
F00E8H	Same as RL78/G1A (64-pin products)	MDUC		Multiplication/division control register	MDUC	
F00F0H	Peripheral enable register 0 Note	PER0		Peripheral enable register 0	PER0	
<R> F00F3H	Subsystem clock supply mode control registerr Note	OSMC		Subsystem clock supply mode control register	OSMC	
F00F5H	Same as RL78/G1A (64-pin products)	RPECTL		RAM parity error control register	RPECTL	
F00FEH	Same as RL78/G1A (64-pin products)	BCDADJ		BCD adjust result register	BCDADJ	
F0100H	Same as RL78/G1A (64-pin products)	SSR00L	SSR00	Serial status register 00	SSR00L	SSR00
F0101H		—			—	
F0102H	Same as RL78/G1A (64-pin products)	SSR01L	SSR01	Serial status register 01	SSR01L	SSR01
F0103H		—			—	
F0104H	Same as RL78/G1A (64-pin products)	SSR02L	SSR02	Serial status register 02	SSR02L	SSR02
F0105H		—			—	
F0106H	Same as RL78/G1A (64-pin products)	SSR03L	SSR03	Serial status register 03	SSR03L	SSR03
F0107H		—			—	
F0108H	Same as RL78/G1A (64-pin products)	SIR00L	SIR00	Serial flag clear trigger register 00	SIR00L	SIR00
F0109H		—			—	
F010AH	Same as RL78/G1A (64-pin products)	SIR01L	SIR01	Serial flag clear trigger register 01	SIR01L	SIR01
F010BH		—			—	
F010CH	Same as RL78/G1A (64-pin products)	SIR02L	SIR02	Serial flag clear trigger register 02	SIR02L	SIR02
F010DH		—			—	
F010EH	Same as RL78/G1A (64-pin products)	SIR03L	SIR03	Serial flag clear trigger register 03	SIR03L	SIR03
F010FH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (3/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0110H	Same as RL78/G1A (64-pin products)	SMR00		Serial mode register 00	SMR00	
F0111H						
F0112H	Serial mode register 01 Note	SMR01		Serial mode register 01	SMR01	
F0113H						
F0114H	Same as RL78/G1A (64-pin products)	SMR02		Serial mode register 02	SMR02	
F0115H						
F0116H	Serial mode register 03 Note	SMR03		Serial mode register 03	SMR03	
F0117H						
F0118H	Same as RL78/G1A (64-pin products)	SCR00		Serial communication operation setting register 00	SCR00	
F0119H						
F011AH	Serial communication operation setting register 01 Note	SCR01		Serial communication operation setting register 01	SCR01	
F011BH						
F011CH	Same as RL78/G1A (64-pin products)	SCR02		Serial communication operation setting register 02	SCR02	
F011DH						
F011EH	Serial communication operation setting register 03 Note	SCR03		Serial communication operation setting register 03	SCR03	
F011FH						
F0120H	Same as RL78/G1A (64-pin products)	SE0L	SE0	Serial channel enable status register 0	SE0L	SE0
F0121H		—			—	
F0122H	Same as RL78/G1A (64-pin products)	SS0L	SS0	Serial channel start register 0	SS0L	SS0
F0123H		—			—	
F0124H	Same as RL78/G1A (64-pin products)	ST0L	ST0	Serial channel stop register 0	ST0L	ST0
F0125H		—			—	
F0126H	Same as RL78/G1A (64-pin products)	SPS0L	SPS0	Serial clock select register 0	SPS0L	SPS0
F0127H		—			—	
F0128H	Same as RL78/G1A (64-pin products)	SO0		Serial output register 0	SO0	
F0129H						
F012AH	Same as RL78/G1A (64-pin products)	SOE0L	SOE0	Serial output enable register 0	SOE0L	SOE0
F012BH		—			—	
F0134H	Same as RL78/G1A (64-pin products)	SOL0L	SOL0	Serial output level register 0	SOL0L	SOL0
F0135H		—			—	
F0138H	Same as RL78/G1A (64-pin products)	SSC0L	SSC0	Serial standby control register 0	SSC0L	SSC0
		—			—	
F0140H	Same as RL78/G1A (64-pin products)	SSR10L	SSR10	Serial status register 10	SSR10L	SSR10
F0141H		—			—	
F0142H	Same as RL78/G1A (64-pin products)	SSR11L	SSR11	Serial status register 11	SSR11L	SSR11
F0143H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (4/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0148H	Same as RL78/G1A (64-pin products)	SIR10L	SIR10	Serial flag clear trigger register 10	SIR10L	SIR10
F0149H		—			—	
F014AH	Same as RL78/G1A (64-pin products)	SIR11L	SIR11	Serial flag clear trigger register 11	SIR11L	SIR11
F014BH		—			—	
F0150H	Same as RL78/G1A (64-pin products)	SMR10		Serial mode register 10	SMR10	
F0151H						
F0152H	Serial mode register 11 Note	SMR11		Serial mode register 11	SMR11	
F0153H						
F0158H	Same as RL78/G1A (64-pin products)	SCR10		Serial communication operation setting register 10	SCR10	
F0159H						
F015AH	Serial communication operation setting register 11 Note	SCR11		Serial communication operation setting register 11	SCR11	
F015BH						
F0160H	Same as RL78/G1A (64-pin products)	SE1L	SE1	Serial channel enable status register 1	SE1L	SE1
F0161H		—			—	
F0162H	Same as RL78/G1A (64-pin products)	SS1L	SS1	Serial channel start register 1	SS1L	SS1
F0163H		—			—	
F0164H	Same as RL78/G1A (64-pin products)	ST1L	ST1	Serial channel stop register 1	ST1L	ST1
F0165H		—			—	
F0166H	Same as RL78/G1A (64-pin products)	SPS1L	SPS1	Serial clock select register 1	SPS1L	SPS1
F0167H		—			—	
F0168H	Same as RL78/G1A (64-pin products)	SO1		Serial output register 1	SO1	
F0169H						
F016AH	Same as RL78/G1A (64-pin products)	SOE1L	SOE1	Serial output enable register 1	SOE1L	SOE1
F016BH		—			—	
F0174H	Same as RL78/G1A (64-pin products)	SOL1L	SOL1	Serial output level register 1	SOL1L	SOL1
F0175H		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (5/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F0180H	Same as RL78/G1A (64-pin products)	TCR00		Timer counter register 00	TCR00	
F0181H						
F0182H	Same as RL78/G1A (64-pin products)	TCR01		Timer counter register 01	TCR01	
F0183H						
F0184H	Same as RL78/G1A (64-pin products)	TCR02		Timer counter register 02	TCR02	
F0185H						
F0186H	Same as RL78/G1A (64-pin products)	TCR03		Timer counter register 03	TCR03	
F0187H						
F0188H	Same as RL78/G1A (64-pin products)	TCR04		Timer counter register 04	TCR04	
F0189H						
F018AH	Same as RL78/G1A (64-pin products)	TCR05		Timer counter register 05	TCR05	
F018BH						
F018CH	Same as RL78/G1A (64-pin products)	TCR06		Timer counter register 06	TCR06	
F018DH						
F018EH	Same as RL78/G1A (64-pin products)	TCR07		Timer counter register 07	TCR07	
F018FH						
F0190H	Same as RL78/G1A (64-pin products)	TMR00		Timer mode register 00	TMR00	
F0191H						
F0192H	Timer mode register 01 Note	TMR01		Timer mode register 01	TMR01	
F0193H						
F0194H	Timer mode register 02 Note	TMR02		Timer mode register 02	TMR02	
F0195H						
F0196H	Timer mode register 03 Note	TMR03		Timer mode register 03	TMR03	
F0197H						
F0198H	Same as RL78/G1A (64-pin products)	TMR04		Timer mode register 04	TMR04	
F0199H						
F019AH	Timer mode register 05 Note	TMR05		Timer mode register 05	TMR05	
F019BH						
F019CH	Timer mode register 06 Note	TMR06		Timer mode register 06	TMR06	
F019DH						
F019EH	Same as RL78/G1A (64-pin products)	TMR07		Timer mode register 07	TMR07	
F019FH						
F01A0H	Same as RL78/G1A (64-pin products)	TSR00L	TSR00	Timer status register 00	TSR00L	TSR00
F01A1H		—			—	
F01A2H	Same as RL78/G1A (64-pin products)	TSR01L	TSR01	Timer status register 01	TSR01L	TSR01
F01A3H		—			—	
F01A4H	Same as RL78/G1A (64-pin products)	TSR02L	TSR02	Timer status register 02	TSR02L	TSR02
F01A5H		—			—	
F01A6H	Same as RL78/G1A (64-pin products)	TSR03L	TSR03	Timer status register 03	TSR03L	TSR03
F01A7H		—			—	
F01A8H	Same as RL78/G1A (64-pin products)	TSR04L	TSR04	Timer status register 04	TSR04L	TSR04
F01A9H		—			—	
F01AAH	Same as RL78/G1A (64-pin products)	TSR05L	TSR05	Timer status register 05	TSR05L	TSR05
F01ABH		—			—	
F01ACH	Same as RL78/G1A (64-pin products)	TSR06L	TSR06	Timer status register 06	TSR06L	TSR06
F01ADH		—			—	
F01AEH	Same as RL78/G1A (64-pin products)	TSR07L	TSR07	Timer status register 07	TSR07L	TSR07
F01AFH		—			—	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Table 3-4. List of Differences in Expanded Special Function Registers (2nd SFRs) (6/6)

Address	RL78/G1E (80-pin products)			RL78/G1A (64-pin products)		
	2nd SFRs Name	Symbol		2nd SFRs Name	Symbol	
F01B0H	Same as RL78/G1A (64-pin products)	TE0L	TE0	Timer channel enable status register 0	TE0L	TE0
F01B1H		–			–	
F01B2H	Same as RL78/G1A (64-pin products)	TS0L	TS0	Timer channel start register 0	TS0L	TS0
F01B3H		–			–	
F01B4H	Same as RL78/G1A (64-pin products)	TT0L	TT0	Timer channel stop register 0	TT0L	TT0
F01B5H		–			–	
F01B6H	Same as RL78/G1A (64-pin products)	TPS0		Timer clock select register 0	TPS0	
F01B7H						
F01B8H	Timer output register 0 Note	TO0L	TO0	Timer output register 0	TO0L	TO0
F01B9H		–			–	
F01BAH	Timer output enable register 0 Note	TOE0L	TOE0	Timer output enable register 0	TOE0L	TOE0
F01BBH		–			–	
F01BCH	Timer output level register 0 Note	TOL0L	TOL0	Timer output level register 0	TOL0L	TOL0
F01BDH		–			–	
F01BEH	Timer output mode register 0 Note	TOM0L	TOM0	Timer output mode register 0	TOM0L	TOM0
F01BFH		–			–	
F0230H				IICA control register 00	IICCTL00	
F0231H				IICA control register 01	IICCTL01	
F0232H				IICA low-level width setting register 0	IICWL0	
F0233H				IICA high-level width setting register 0	IICWH0	
F0234H				Slave address register 0	SVA40	
F02F0H	Same as RL78/G1A (64-pin products)	CRC0CTL		Flash memory CRC control register	CRC0CTL	
F02F2H	Same as RL78/G1A (64-pin products)	PGCRCL		Flash memory CRC operation result register	PGCRCL	
F02FAH	Same as RL78/G1A (64-pin products)	CRCD		CRC data register	CRCD	

Note The bit setting is different from that of RL78/G1A (64-pin products).

Caution Do not write data to the registers which is in the row with painted gray.

3. 3. 3 Instruction address addressing

See **3. 3 Instruction Address Addressing** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 3. 4 Addressing for processing data addresses

See **3. 4 Addressing for Processing Data Addresses** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4 Port Functions

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 4 PORT FUNCTIONS** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 1 Port functions

The RL78/G1E microcontrollers (64-pin products, 80-pin products) are provided with digital I/O ports, which enable variety of control operations. In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, see **CHAPTER 2 PIN FUNCTIONS**.

3. 4. 2 Port configuration

Ports include the following hardware.

Table 3-5. Port Configuration

Item	Configuration
Control registers	Port mode registers (PM0 to PM2, PM4 to PM7, PM14, PM15) Port registers (P0 to P2, P4, P5, P7, P12 to P14) Pull-up resistor option registers (PU0, PU1, PU4, PU5, PU7, PU14) Port input mode registers (PIM0, PIM1) Port output mode registers (POM0, POM1, POM5) Port mode control registers (PMC0, PMC1, PMC3, PMC5, PMC7) A/D port configuration register (ADPC) Peripheral I/O redirection register (PIOR) Global analog input disable register (GAIDIS)
Port	· 64-pin products Total: 24 (CMOS I/O: 20, CMOS input: 3, CMOS output: 1) · 80-pin products Total: 30 (CMOS I/O: 26, CMOS input: 3, CMOS output: 1)
Pull-up resistor	· 64-pin products Total: 16 · 80-pin products Total: 21

For details of each port, also see **4. 2 Port Configuration** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 2. 1 Port 0

Port 0 is an I/O port with an output latch. Port 0 can be set to the input mode or output mode in 1-bit units using port mode register 0 (PM0). When the P00 to P04 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 0 (PU0). Input to the P00, P01, P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 0 (PIM0). Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 0 (POM0). The P02 and P03 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 0 (PMC0). This port can be also used for timer I/O, A/D converter analog input, serial interface data I/O, clock I/O, and key interrupt input.

When reset signal is generated, the following configuration will be set.

- P00, P01 and P04 pins ⋯ Input mode
- P02 and P03 pins ⋯ Analog input

3. 4. 2. 2 Port 1

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P15 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1). Input to the P10, P11, P14 to P15 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 1 (PIM1). Output from the P10 to P15 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in
<R> 1-bit units using port output mode register 1 (POM1). The P10 to P15 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 1 (PMC1). This port can be also used for A/D converter analog input, serial interface data I/O, programming UART I/O, and key return input.

When reset signal is generated, the P10 to P15 pins will be set to analog input.

3. 4. 2. 3 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2). This port can be also used for A/D converter analog input and reference voltage input, and key return input pin. Setting digital or analog to each pin can be done in A/D port configuration register (ADPC).

When reset signal is generated, the P20/ANI0 to P24/ANI4 pins will be set to analog input.

3. 4. 2. 4 Port 3

Port 3 is not available for RL78/G1E.

3. 4. 2. 5 Port 4

Port 4 is an I/O port with an output latch. Port 4 can be set to the input mode or output mode in 1-bit units using port mode register 4 (PM4). When the P40 to P42 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 4 (PU4). The P41 pin can be specified as digital input/output or analog input, using port mode control register 4 (PMC4). This port can be also used for A/D converter analog input, data I/O for a flash memory programmer/debugger, and timer I/O. Be sure to connect an external pull-up resistor to the P40 pins when on-chip debugging is enabled to P40 (by using an option byte).

When reset signal is generated, the P40 to P42 pins will be set to input mode.

3. 4. 2. 6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 and P51 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 5 (PU5). Output from the P50 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units using port output mode register 5 (POM5). The P50 and P51 pins can be specified as digital input/output or analog input in 1-bit units, using port mode control register 5 (PMC5). This port can be also used for A/D converter analog input, and external interrupt request input.

When reset signal is generated, the P50 and P51 pins will be set to input mode.

3. 4. 2. 7 Port 6

Port 6 is not available for RL78/G1E.

3. 4. 2. 8 Port 7

Port 7 is an I/O port with an output latch. Port 7 can be set to the input mode or output mode in 1-bit units using port mode register 7 (PM7). When the P70 to P73 pins are used as an input port, use of an on-chip pull-up resistor can be
<R> specified in 1-bit units by pull-up resistor option register 7 (PU7). The P70 pin can be specified as digital input/output or analog input, using port mode control register 7 (PMC7). This port can be also used for A/D converter analog input, serial interface data I/O, and clock I/O.

When reset signal is generated, the P70 to P73 pins will be set to input mode.

3. 4. 2. 9 Port 12

P121 and P122 pins are specified as an input-only port. This port can be also used for the pin connecting resonator for main system clock, and external clock input for main system clock.

When reset signal is generated, the P121 and P122 pins will be set to input mode.

3. 4. 2. 10 Port 13

P130 pin is specified as a 1-bit output-only port with an output latch. P137 pin is specified as a 1-bit input-only port and can be also used for external interrupt request input.

3. 4. 2. 11 Port 14

Port 14 is an I/O port with an output latch. Port 14 can be set to the input mode or output mode in 1-bit units using port mode register 14 (PM14). When the P140 pin is used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 14 (PU14). This port can be also used for clock/buzzer output, and external interrupt request input.

When reset signal is generated, the P140 pin will be set to input mode.

3. 4. 2. 12 Port 15

Port 15 is not available for RL78/G1E.

3. 4. 3 Registers controlling port function

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **4. 3 Registers Controlling Port Function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (1/2)**

Port		Bit Name						RL78/G1E		RL78/G1A
		PMxx Register	Pxx Register	PUxx Register	PIMxx Register	POMxx Register	PMCxx Register	(64-pin products)	(80-pin products)	(64-pin products)
Port 0	0	PM00	P00	PU00	PIM00	–	–	√	√	√
	1	PM01	P01	PU01	PIM01	–	–	√	√	√
	2	PM02	P02	PU02	–	POM02	PMC02	√	√	√
	3	PM03	P03	PU03	PIM03	POM03	PMC03	√	√	√
	4	PM04	P04 Note 2	PU04 Note 2	PIM04 Note2	POM04 Note 2	–	*	√	√
	5	PM05	P05 Note 1	PU05 Note1	–	–	–	*	*	√
	6	PM06	P06 Note 1	PU06 Note 1	–	–	–	*	*	√
Port 1	0	PM10	P10	PU10	PIM10	POM10	PMC10	√	√	√
	1	PM11	P11	PU11	PIM11	POM11	PMC11	√	√	√
	2	PM12	P12	PU12	–	POM12	PMC12	√	√	√
	3	PM13	P13	PU13	–	POM13	PMC13	√	√	√
	4	PM14	P14	PU14	PIM14	POM14	PMC14	√	√	√
	5	PM15	P15	PU15	PIM15	POM15	PMC15	–	√	√
	6	PM16	P16 Note 1	PU16 Note 1	PIM16 Note 1	–	–	*	*	√
Port 2	0	PM20	P20	_	_	_	_	√	√	√
	1	PM21	P21	_	_	_	_	√	√	√
	2	PM22	P22	_	_	_	_	√	√	√
	3	PM23	P23	_	_	_	_	√	√	√
	4	PM24	P24 Note 2	_	_	_	_	*	√	√
	5	PM25	P25 Note 1	_	_	_	_	*	*	√
	6	PM26	P26 Note 1	_	_	_	_	*	*	√
	7	PM27	P27 Note 1	_	_	_	_	*	*	√

<R> **Notes 1.** Not supported by RL78/G1E(Both 64-pin products and 80-pin products)

2. Not supported by RL78/G1E(64-pin products)

<R> **Remark** √: Mounted

*: Mounted but there are some differences between RL78/G1E and RL78/G1A

–: Not mounted

<R> **PMxx, Pxx, PUxx, PIMxx, POMxx, PMCxx registers and the bits mounted on each product (2/2)**

Port		Bit Name						RL78/G1E		RL78/G1A
		PMxx Register	Pxx Register	PUxx Register	PIMxx Register	POMxx Register	PMCxx Register	(64-pin products)	(80-pin products)	(64-pin products)
Port 3	0	PM30	P30	PU30	–	–	PMC30	–	–	√
	1	PM31	P31	PU31	–	–	PMC31	–	–	√
Port 4	0	PM40	P40	PU40	–	–	–	√	√	√
	1	PM41	P41	PU41	–	–	PMC41	√	√	√
	2	PM42	P42	PU42	–	–	–	√	√	√
	3	PM43	P43 Note 1	PU43 Note 1	–	–	–	*	*	√
Port 5	0	PM50	P50	PU50	–	POM50	PMC50	–	√	√
	1	PM51	P51	PU51	–	–	PMC51	–	√	√
Port 6	0	PM60	P60 Note 1	–	–	–	–	*	*	√
	1	PM61	P61 Note 1	–	–	–	–	*	*	√
	2	PM62	P62 Note 1	–	–	–	–	*	*	√
	3	PM63	P63 Note 1	–	–	–	–	*	*	√
Port 7	0	PM70	P70	PU70	–	–	PMC70	√	√	√
	1	PM71	P71	PU71	–	POM71 Note 1	–	*	*	√
	2	PM72	P72	PU72	–	–	–	√	√	√
	3	PM73	P73	PU73	–	–	–	√	√	√
	4	PM74	P74 Note 1	PU74 Note 1	–	POM74 Note 1	–	*	*	√
	5	PM75	P75 Note 1	PU75 Note 1	–	–	–	*	*	√
	6	PM76	P76 Note 1	PU76 Note 1	–	–	–	*	*	√
	7	PM77	P77 Note 1	PU77 Note 1	–	–	–	*	*	√
Port 12	0	PM120	P120	PU120	–	–	PMC120	–	–	√
	1	–	P121	–	–	–	–	√	√	√
	2	–	P122	–	–	–	–	√	√	√
	3	–	P123	–	–	–	–	–	–	√
	4	–	P124	–	–	–	–	–	–	√
Port 13	0	–	P130	–	–	–	–	√	√	√
	7	–	P137	–	–	–	–	√	√	√
Port 14	0	PM140	P140 Note 2	PU140 Note 2	–	–	–	*	√	√
	1	PM141	P141 Note 1	PU141 Note 1	–	–	–	*	*	√
Port 15	0	PM150	P150 Note 1	–	–	–	–	*	*	√
	1	PM151	P151 Note 1	–	–	–	–	*	*	√
	2	PM152	P152 Note 1	–	–	–	–	*	*	√
	3	PM153	P153 Note 1	–	–	–	–	*	*	√
	4	PM154	P154 Note 1	–	–	–	–	*	*	√

<R> **Notes 1.** Not supported by RL78/G1E(Both 64-pin products and 80-pin products)

2. Not supported by RL78/G1E(64-pin products)

<R> **Remark** √: Mounted

*: Mounted but there are some differences between RL78/G1E and RL78/G1A

–: Not mounted

3. 4. 3. 1 Port mode register (PMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	1	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bits 0 and 1 of the PM14 register, and bits 0 to 4 of the PM15 register to "0".

2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register, bits 4 to 7 of the PM4 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to "1".

(2) 80-pin products

	Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
	PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
	PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
	PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
	PM4	1	1	1	1	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
<R>	PM5	1	1	1	1	1	1	PM51	PM50	FFF25H	FFH	R/W
	PM6	1	1	1	1	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
	PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
	PM14	1	1	1	1	1	1	PM141	PM140	FFF2EH	FFH	R/W
	PM15	1	1	1	PM154	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bit 3 of the PM4 register, bits 0 to 3 of the PM6 register, bits 4 to 7 of the PM7 register, bit 1 of the PM14 register, and bits 0 to 4 of the PM15 register to "0".

2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register, bits 4 to 7 of the PM4 register,
<R> **bits 2 to 7 of the PM5 register, bits 4 to 7 of the PM6 register, bits 2 to 7 of the PM14 register, and bits 5 to 7 of the PM15 register to "1".**

3. 4. 3. 2 Port register (Pxx)

(1) 64-pin products

	Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
	P0	0	0	0	0	P03	P02	P01	P00	FFF00H	00H	R/W
	P1	0	0	0	P14	P13	P12	P11	P10	FFF01H	00H	R/W
	P2	0	0	0	0	P23	P22	P21	P20	FFF02H	00H	R/W
	P4	0	0	0	0	0	P42	P41	P40	FFF04H	00H	R/W
	P7	0	0	0	0	P73	P72	P71	P70	FFF07H	00H	R/W
	P12	0	0	0	0	0	P122	P121	0	FFF0CH	Undefined	R/W Note 1
<R>	P13	P137	0	0	0	0	0	0	P130	FFF0DH	Note2	R/W Note 1

<R> **Notes 1.** P121, P122 and P137 are read-only.

2. P137: Undefined

P130: 0 (output latch)

Cautions Be sure to clear bits 4 to 7 of the P0 register, bits 5 to 7 of the P1 register, bits 4 to 7 of the P2 register, bits 3 to 7 of the P4 register, bits 4 to 7 of the P7 register, and bits 0 and 3 to 7 of the P12 register, bits 1 to 6 of the P13 register to "0".

(2) 80-pin products

	Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
	P0	0	0	0	P04	P03	P02	P01	P00	FFF00H	00H	R/W
	P1	0	0	P15	P14	P13	P12	P11	P10	FFF01H	00H	R/W
	P2	0	0	0	P24	P23	P22	P21	P20	FFF02H	00H	R/W
	P4	0	0	0	0	0	P42	P41	P40	FFF04H	00H	R/W
<R>	P5	0	0	0	0	0	0	P51	P50	FFF05H	00H	R/W
	P7	0	0	0	0	P73	P72	P71	P70	FFF07H	00H	R/W
	P12	0	0	0	0	0	P122	P121	0	FFF0CH	Undefined	R/W Note 1
	P13	P137	0	0	0	0	0	0	P130	FFF0DH	Note 2	R/W Note 1
	P14	0	0	0	0	0	0	0	P140	FFF0EH	00H	R/W

<R> **Notes 1.** P121, P122 and P137 are read-only.

2. P137: Undefined

P130: 0 (output latch)

<R> **Cautions Be sure to clear bits 5 to 7 of the P0 register, bits 6 and 7of the P1 register, bits 5 to 7 of the P2 register, bits 3 to 7 of the P4 register, bits 2 to 7 of the P5 register, bits 4 to 7 of the P7 register, bits 0 and 3 to 7 of the P12 register, bits 1 to 6 of the P13 register, and bits 1 to 7 of the P14 register to "0".**

3. 4. 3. 3 Pull-up resistor option register (PUxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	0	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	0	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W

Caution Be sure to clear bits 4 to 7 of the PU0 register, bits 5 to 7 of the PU1 register, bits 3 to 7 of the PU4 register, and bits 4 to 7 of the PU7 register to "0".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PU0	0	0	0	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	0	0	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU4	0	0	0	0	0	PU42	PU41	PU40	F0034H	01H	R/W
<R> PU5	0	0	0	0	0	0	PU51	PU50	F0035H	00H	R/W
PU7	0	0	0	0	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU14	0	0	0	0	0	0	0	PU140	F003EH	00H	R/W

<R> **Caution Be sure to clear bits 5 to 7 of the PU0 register, bits 6 and 7of the PU1 register, bits 3 to 7 of the PU4 register, bits 2 to 7 of the PU5 register, bits 4 to 7 of the PU7 register, and bits 1 to 7 of the PU14 register to "0".**

3. 4. 3. 4 Port input mode register (PIMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PIM0	0	0	0	0	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	0	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 4 to 7 of the PIM0 register, and bits 2, 3 and 5 to 7 of the PIM1 register to "0".**

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
<R> PIM0	0	0	0	PIM04	PIM03	0	PIM01	PIM00	F0040H	00H	R/W
PIM1	0	0	PIM15	PIM14	0	0	PIM11	PIM10	F0041H	00H	R/W

<R> **Caution Be sure to clear bits 2 and 5 to 7 of the PIM0 register, and bits 2, 3, 6 and 7 of the PIM1 register to "0".**

3. 4. 3. 5 Port output mode register (POMxx)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	0	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	0	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W

<R> **Caution Be sure to clear bits 0, 1 and 4 to 7 of the POM0 register, and bits 5 to 7 of the POM1 register to "0".**

<R> (2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
POM0	0	0	0	POM04	POM03	POM02	0	0	F0050H	00H	R/W
POM1	0	0	POM15	POM14	POM13	POM12	POM11	POM10	F0051H	00H	R/W
POM5	0	0	0	0	0	0	0	POM50	F0055H	00H	R/W

Caution Be sure to clear bits 0, 1 and 5 to 7 of the POM0 register, bits 6 and 7 of the POM1 register, and bits 1 to 7 of the POM5 register to "0".

3. 4. 3. 6 Port mode control register (PMCxx)

<R> (1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	1	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 5 to 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, and bits 1 to 7 of the PMC7 register to "0".

<R> (2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PMC0	1	1	1	1	PMC03	PMC02	1	1	F0060H	FFH	R/W
PMC1	1	1	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	F0061H	FFH	R/W
PMC4	1	1	1	1	1	1	PMC41	1	F0064H	FFH	R/W
PMC5	1	1	1	1	1	1	PMC51	PMC50	F0065H	FFH	R/W
PMC7	1	1	1	1	1	1	1	PMC70	F0067H	FFH	R/W

Caution Be sure to set bits 0, 1 and 4 to 7 of the PMC0 register, bits 6 and 7 of the PMC1 register, bits 0 and 2 to 7 of the PMC4 register, bits 2 to 7 of the PMC5 register, and bits 1 to 7 of the PMC7 register to "0".

3. 4. 3. 7 A/D port configuration register (ADPC)

(1) 64-pin products

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching			
			ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	A	A	A	A
0	0	1	D	D	D	D
0	1	0	D	D	D	A
0	1	1	D	D	A	A
1	0	0	D	A	A	A
Other than above			Setting prohibited			

Cautions 1. Be sure to clear bits 3 to 7 to "0".

2. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

3. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

4. When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

(2) 80-pin products

Address: F0076H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	0	0	ADPC2	ADPC1	ADPC0

ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching				
			ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	A	A	A	A	A
0	0	1	D	D	D	D	D
0	1	0	D	D	D	D	A
0	1	1	D	D	D	A	A
1	0	0	D	D	A	A	A
1	0	1	D	A	A	A	A
Other than above			Setting prohibited				

Cautions 1. Be sure to clear bits 3 to 7 to "0".

2. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

3. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

4. When using AV_{REFP} and AV_{REFM}, specify ANI0 and ANI1 as the analog input channels and specify input mode by using the port mode register.

3. 4. 3. 8 Peripheral I/O redirection register (PIOR)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR	0	0	0	0	0	0	PIOR1	PIOR0

Function	64-pin products				80-pin products			
	Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0			
	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1
KR0	P70	Setting prohibited	P00	P10	P70	Setting prohibited	P00	P10
KR1	P71		P01	P11	P71		P01	P11
KR2	P72		P02	P12	P72		P02	P12
KR3	P73		P03	P13	P73		P03	P13
KR4	–		–	P14	–		P04	P14
KR5	–		P22	–	–		P22	P15
KR6	–		P23	–	–		P23	–
KR7	–		–	–	–		P24	–

<R> **Remark** –: These functions are not available for use.

3. 4. 3. 9 Global digital input disable register (GDIDIS)

GDIDIS is not available for RL78/G1E.

3. 4. 3. 10 Global analog input disable register (GAIDIS)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **4. 3. 10 Global analog input disable register (GAIDIS)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 4 Port function operation

The operations which are different from that of RL78/G1A (64-pin products) are described below.

3. 4. 4. 1 Writing to I/O port

See **4. 4. 1 Writing to I/O port** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 4. 2 Reading from I/O port

See **4. 4. 2 Reading from I/O port** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 4. 3 Operation on I/O port

See **4. 4. 3 Operation on I/O port** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 4. 4. 4 Handling different potential (1.8 V,2.5 V or 3 V) by using $EV_{DD} \leq V_{DD}$

This function is not available, because the EV_{DD} pin is not provided in the RL78/G1E.

<R> **3. 4. 4. 5 Handling different potential (1.8 V ,2.5 V or 3V) by using I/O buffers**

It is possible to connect an external device operating on a different potential (1.8 V, 2.5 V or 3V) by switching I/O buffers with the port input mode register (PIMxx) and port output mode register (POMxx).

When receiving input from an external device with a different potential (1.8 V, 2.5 V or 3V), set the port input mode registers 0 and 1 (PIM0 and PIM1) on a bit-by-bit basis to enable normal input (CMOS)/TTL input buffer switching.

When outputting data to an external device with a different potential (1.8 V, 2.5 V or 3V), set the port output mode registers 0 and 1 (POM0 and POM1) on a bit-by-bit basis to enable N-ch open drain (V_{DD} tolerance) switching.

Following, describes the connection of a serial interface.

(1) Setting procedure when using input ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions for the TTL input buffer

In case of UART0: P11
In case of UART1: P03
In case of UART2: P14
In case of CSI00: P10, P11
In case of CSI10: P03, P04
In case of CSI20: P14, P15

<1> Using an external resistor, pull up externally the input pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).

<2> Set the corresponding bit of the PIM0 and PIM1 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.

<3> Enable the operation of the serial array unit and set the mode to the UART/CSI mode.

<R> **(2) Setting procedure when using output ports of UART0 to UART2, CSI00, CSI10, and CSI20 functions in N-ch open-drain output mode**

In case of UART0: P12
In case of UART1: P02
In case of UART2: P13
In case of CSI00: P10, P12
In case of CSI10: P02, P04
In case of CSI20: P13, P15

<1> Using an external resistor, pull up externally the output pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode changes to the input mode (Hi-Z).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} withstand voltage) mode.
<5> Enable the operation of the serial array unit and set the mode to the UART/CSI mode.
<6> Set the output mode by manipulating the PM0 and PM1 registers. At this time, the output data is high level, so the pin is in the Hi-Z state.

<R> **(3) Setting procedure when using I/O ports of IIC00, IIC10, and IIC20 functions with a different potential (1.8 V ,2.5 V or 3V)**

In case of IIC00: P10, P11
In case of IIC10: P03, P04
In case of IIC20: P14, P15

<1> Using an external resistor, pull up externally the input pin to be used to the power supply of the target device (on-chip pull-up resistor cannot be used).
<2> After reset release, the port mode is the input mode (Hi-Z).
<3> Set the output latch of the corresponding port to 1.
<4> Set the corresponding bit of the POM0 and POM1 registers to 1 to set the N-ch open drain output (V_{DD} tolerance) mode.
<5> Set the corresponding bit of the PIM0 and PIM1 registers to 1 to switch to the TTL input buffer. For V_{IH} and V_{IL}, refer to the DC characteristics when the TTL input buffer is selected.
<6> Enable the operation of the serial array unit and set the mode to the simplified I^2C mode.
<7> Set the corresponding bit of the PM0 and PM1 registers to the output mode (data I/O is possible in the output mode).
At this time, the output data is high level, so the pin is in the Hi-Z state.

<R> **3. 4. 5 Register settings when using alternate function**

See **4. 5 Register Settings When Using Alternate Function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 4. 6 Cautions when using port function

See **4. 6 Cautions When Using Port Function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5 Clock Generator

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 5 CLOCK GENERATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 1 Functions of clock generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following two kinds of system clocks and clock oscillators are selectable.

Caution The subsystem clock is not provided in the RL78/G1E (64-pin products, 80-pin products).

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 20 MHz by connecting a resonator to X1 and X2.

Oscillation can be stopped by executing the STOP instruction or setting of the MSTOP bit (bit 7 of the clock operation status control register (CSC)).

<2> High-speed on-chip oscillator (High-speed OCD)

<R> The frequency at which to oscillate can be selected from among f_{IH} = 32, 24, 16, 12, 8, 6, 4, 3, 2 or 1 MHz (typ.) by using the option byte (000C2H). After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting the HIOSTOP bit (bit 0 of the CSC register).

The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV). For details about the frequency, see **3. 5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)**.

The frequencies that can be specified for the high-speed on-chip oscillator by using the option byte and the high-speed on-chip oscillator frequency select register (HOCODIV) are shown below.

Power Supply Voltage	Flash Operation Mode	Oscillation Frequency (MHz)									
		1	2	3	4	6	8	12	16	24	32
2.7 V ≤ V_{DD} ≤ 5.5 V	HS (high-speed main) mode	√	√	√	√	√	√	√	√	√	√
2.4 V ≤ V_{DD} ≤ 5.5 V		√	√	√	√	√	√	√	√	–	–
1.8 V ≤ V_{DD} ≤ 5.5 V	LS (low-speed main) mode	√	√	√	√	√	√	–	–	–	–
1.6 V ≤ V_{DD} ≤ 5.5 V	LV (low-voltage main) mode	√	√	–	√	–	–	–	–	–	–

An external main system clock (f_{EX} = 1 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

As the main system clock, a high-speed system clock (X1 clock or external main system clock) or high-speed on-chip oscillator clock can be selected by setting of the MCM0 bit (bit 4 of the system clock control register (CKC)).

<R> **(2) Low-speed on-chip oscillator clock (Low-speed on-chip oscillator)**

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

The low-speed on-chip oscillator clock cannot be used as the CPU clock.

Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.

- Watchdog timer
- 12-bit Interval timer

<R> This clock operates when bit 4 (WDTON) of the option byte (000C0H), bit 4 (WUTMMCK0) of the subsystem clock supply mode control register (OSMC), or both are set to 1.

However, when WDTON = 1, WUTMMCK0 = 0, and bit 0 (WDSTBYON) of the option byte (000C0H) is 0, oscillation of the low-speed on-chip oscillator stops if the HALT or STOP instruction is executed.

Remark f_X: X1 clock oscillation frequency

f_{IH}: High-speed on-chip oscillator clock frequency

f_{EX}: External main system clock frequency

f_{IL}: Low-speed on-chip oscillator clock frequency

3. 5. 2 Configuration of clock generator

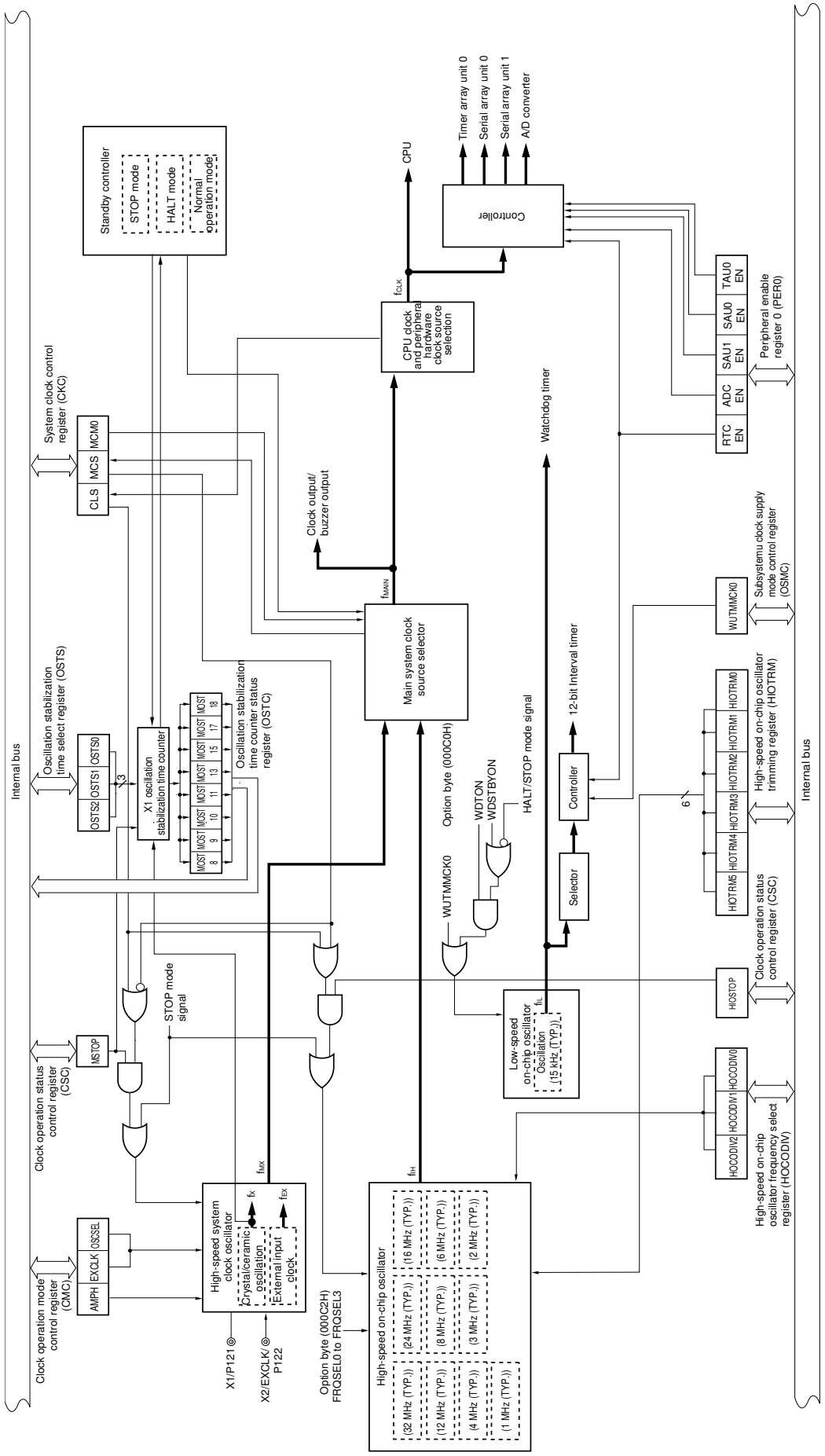
The clock generator includes the following hardware.

Table 3-6. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode control register (CMC) System clock control register (CKC) Clock operation status control register (CSC) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Peripheral enable register 0 (PER0) <R> Subsystem clock supply mode control register (OSMC) High-speed on-chip oscillator frequency select register (HOCODIV) High-speed on-chip oscillator trimming register (HIOTRM)
Oscillators	X1 oscillator High-speed on-chip oscillator Low-speed on-chip oscillator

Figure 3-1. Block Diagram of Clock Generator

<R>



(**Remark** is listed on the next page)

Remark f_X: X1 clock oscillation frequency
f_{IH}: High-speed on-chip oscillator clock frequency
f_{EX}: External main system clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency
f_{CLK}: CPU/peripheral hardware clock frequency
f_{IL}: Low-speed on-chip oscillator clock frequency

3. 5. 3 Registers controlling clock generator

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **5. 3 Registers Controlling Clock Generator** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 5. 3. 1 Clock operation mode control register (CMC)

Address: FFFA0H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	0	0	0	0	0	AMPH

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

AMPH	Control of X1 clock oscillation frequency
0	1 MHz ≤ fx ≤ 10 MHz
1	10 MHz < fx ≤ 20 MHz

Cautions 1. Be sure to clear bits 1 to 3 and 5 to "0".

2. The CMC register can be written only once after reset release, by an 8-bit memory manipulation instruction. When using the CMC register with its initial value (00H), be sure to set the register to 00H after a reset ends in order to prevent malfunction due to a program loop. Such a malfunction becomes unrecoverable when a value other than 00H is mistakenly written.

3. After reset release, set the CMC register before X1 oscillation is started as set by the clock operation status control register (CSC).

4. Be sure to set the AMPH bit to 1 if the X1 clock oscillation frequency exceeds 10 MHz.

5. Specify the settings for the AMPH, AMPHS1, and AMPHS0 bits while f_{IH} is selected as f_{CLK} after a reset ends (before f_{CLK} is switched to f_{MX}).

6. Although the maximum system clock frequency is 32 MHz, the maximum frequency of the X1 oscillator is 20 MHz.

Remark fx: X1 clock oscillation frequency

3. 5. 3. 2 System clock control register (CKC)

Address: FFFA4H After reset: 00H R/W[Note]

Symbol	<7>	6	<5>	<4>	3	2	1	0
CKC	CLS	0	MCS	MCM0	0	0	0	0

CLS	Status of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1	–

MCS	Status of main system clock (f_{MAIN})
0	High-speed on-chip oscillator clock (f_{IH})
1	High-speed system clock (f_{MX})

MCM0	Main system clock (f_{MAIN}) operation control
0	Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

Note Bits 7 and 5 are read-only.

Caution Be sure to clear bits 0 to 3 and 6 to "0".

Remark f_{IH}: High-speed on-chip oscillator clock frequency
f_{MX}: High-speed system clock frequency
f_{MAIN}: Main system clock frequency

3. 5. 3. 3 Clock operation status control register (CSC)

Address: FFFA1H After reset: C0H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
CSC	MSTOP	1	0	0	0	0	0	HIOSTOP

MSTOP	High-speed system clock operation control		
	X1 oscillation mode	External clock input mode	Input port mode
0	X1 oscillator operating	External clock from EXCLK pin is valid	Input port
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

HIOSTOP	High-speed on-chip oscillator clock operation control
0	High-speed on-chip oscillator operating
1	High-speed on-chip oscillator stopped

Cautions 1. Be sure to set bit 6 to "1".

2. Set the oscillation stabilization time select register (OSTS) before setting the MSTOP bit to 0 after releasing reset. Note that if the OSTS register is being used with its default settings, the OSTS register is not required to be set here.

3. To start X1 oscillation as set by the MSTOP bit, check the oscillation stabilization time of the X1 clock by using the oscillation stabilization time counter status register (OSTC).

4. Do not stop the clock selected for the CPU/peripheral hardware clock (f_{CLK}) with the CSC register.

5. The setting of the flags of the register to stop clock oscillation (invalidate the external clock input) and the condition before clock oscillation is to be stopped are as Table 3-7.

Table 3-7. Stopping Clock Method

Clock	Condition Before Stopping Clock (Invalidating External Clock Input)	Setting of CSC Register Flags
X1 clock External main system clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed system clock. (CLS = 0 and MCS = 0)	MSTOP = 1
High-speed on-chip oscillator clock	CPU and peripheral hardware clocks operate with a clock other than the high-speed on-chip oscillator clock. (CLS = 0 and MCS = 1)	HIOSTOP = 1

3. 5. 3. 4 Oscillation stabilization time counter status register (OSTC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 4 Oscillation stabilization time counter status register (OSTC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 3. 5 Oscillation stabilization time select register (OSTS)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 5 Oscillation stabilization time select register (OSTS)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 3. 6 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

RTCEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply. • SFR used by the 12-bit interval timer cannot be written. • The 12-bit interval timer is in the reset status.
1	Enables input clock supply. • SFR used by the 12-bit interval timer can be written.

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be written.

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 1 can be written.

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be written.

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be written.

Caution Be sure to clear bits 1, 4, and 6 to "0".

<R> 3. 5. 3. 7 Subsystem clock supply mode control register (OSMC)

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0	Operation clock for12-bit interval timer
0	Initial value
1	Low-speed on-chip oscillator clock

Cautions 1. Be sure to clear bit 7 to "0".

2. To use 12-bit interval timer, after reset release, set the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) to "1" before setting the RTCEN bit of the peripheral enable register0 (PER0) to "1".

Remark The subsystem clock is not supported by RL78/G1E, but the subsystem clock supply mode control register is used to control the clock of 12-bit interval timer.

3. 5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 8 High-speed on-chip oscillator frequency select register (HOCODIV)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 3. 9 High-speed on-chip oscillator trimming register (HIOTRM)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **5. 3. 9 High-speed on-chip oscillator trimming register (HIOTRM)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 4 System clock oscillator

See **5. 4 System Clock Oscillator** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 5 Clock generator operation

See **5. 5 Clock Generator Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 6 Controlling clock

See **5. 6 Controlling Clock** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 5. 7 Resonator and oscillator constants

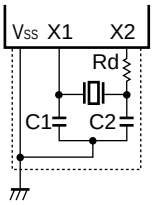
The resonators for which the operation is verified and their oscillator constants are shown below.

Cautions 1. The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. Be sure to apply to the resonator manufacturer for evaluation on the actual circuit before using these constants for your application.
Also apply to the resonator manufacturer for re-evaluation on the actual circuit if you have changed the make of the microcontroller or the board.

2. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the RL78/G1E so that the internal operation conditions are within the specifications of the DC and AC characteristics.

<R> **Figure 3-2. External Oscillation Circuit Example**

(a) X1 oscillation



(1) X1 oscillation: **As of March, 2013 (1/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
KYOCERA rystal Device Corporation Note 3	Crystal resonator	CX8045GB04000D0HEQZ1	SMD	4.0	LV	12	12	0	1.6	5.5
		CX8045GB04000D0HEQZ1	SMD	4.0	LS	12	12	0	1.8	5.5
		CX8045GB04000D0HEQZ1	SMD	4.0	HS	12	12	0	2.4	5.5
		CX8045GB08000D0HEQZ1	SMD	8.0	LS	12	12	0	1.8	5.5
		CX8045GB08000D0HEQZ1	SMD	8.0	HS	12	12	0	2.4	5.5
		CX8045GB12000D0HEQZ1	SMD	12.0	HS	10	10	0	2.4	5.5
		CX3225GB16000D0HEQZ1	SMD	16.0	HS	10	10	0	2.4	5.5
		CX3225GB20000D0HEQZ1	SMD	20.0	HS	8	8	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. C1, C2 columns indicate a reference value.

3. When using these oscillators, contact KYOCERA Crystal Device Corporation (http://www.kyocera-crystal.jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

(1) X1 oscillation: **As of March, 2013(2/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Murata Manufacturing Co., Ltd. Note 3	Ceramic resonator	CSTCC2M00G56-R0	SMD	2.0	LV	(47)	(47)	0	1.6	5.5
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0	1.6	5.5
		CSTLS4M00G53-B0	Lead	4.0		(15)	(15)	0	1.6	5.5
		CSTCC2M00G56-R0	SMD	2.0	LS	(47)	(47)	0	1.8	5.5
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0	1.8	5.5
		CSTLS4M00G53-B0	Lead	4.0		(15)	(15)	0	1.8	5.5
		CSTCR4M19G55-R0	SMD	4.194		(39)	(39)	0	1.8	5.5
		CSTLS4M19G53-B0	Lead	4.194		(15)	(15)	0	1.8	5.5
		CSTCR4M91G53-R0	SMD	4.915		(15)	(15)	0	1.8	5.5
		CSTLS4M91G53-B0	Lead	4.915		(15)	(15)	0	1.8	5.5
		CSTCR5M00G53-R0	SMD	5.0		(15)	(15)	0	1.8	5.5
		CSTLS5M00G53-B0	Lead	5.0		(15)	(15)	0	1.8	5.5
		CSTCR6M00G53-R0	SMD	6.0		(15)	(15)	0	1.8	5.5
		CSTLS6M00G53-B0	Lead	6.0		(15)	(15)	0	1.8	5.5
		CSTCE8M00G52-R0	SMD	8.0		(10)	(10)	0	1.8	5.5
		CSTLS8M00G53-B0	Lead	8.0		(15)	(15)	0	1.8	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. Values in parentheses in the C1, C2 columns indicate an internal capacitance.

3. When using these oscillators, contact Murata Manufacturing Co., Ltd. (http://www.murata.co.jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

(1) X1 oscillation: **As of March, 2013(3/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Murata Manufacturing Co., Ltd.Note 3	Ceramic resonator	CSTCC2M00G56-R0	SMD	2.0	HS	(47)	(47)	0	2.4	5.5
		CSTCR4M00G55-R0	SMD	4.0		(39)	(39)	0	2.4	5.5
		CSTLS4M00G53-B0	Lead	4.0		(15)	(15)	0	2.4	5.5
		CSTCR4M19G55-R0	SMD	4.194		(39)	(39)	0	2.4	5.5
		CSTLS4M19G53-B0	Lead	4.194		(15)	(15)	0	2.4	5.5
		CSTCR4M91G53-R0	SMD	4.915		(15)	(15)	0	2.4	5.5
		CSTLS4M91G53-B0	Lead	4.915		(15)	(15)	0	2.4	5.5
		CSTCR5M00G53-R0	SMD	5.0		(15)	(15)	0	2.4	5.5
		CSTLS5M00G53-B0	Lead	5.0		(15)	(15)	0	2.4	5.5
		CSTCR6M00G53-R0	SMD	6.0		(15)	(15)	0	2.4	5.5
		CSTLS6M00G53-B0	Lead	6.0		(15)	(15)	0	2.4	5.5
		CSTCE8M00G52-R0	SMD	8.0		(10)	(10)	0	2.4	5.5
		CSTLS8M00G53-B0	Lead	8.0		(15)	(15)	0	2.4	5.5
		CSTCE8M38G52-R0	SMD	8.388		(10)	(10)	0	2.4	5.5
		CSTLS8M38G53-B0	Lead	8.388		(15)	(15)	0	2.4	5.5
		CSTCE10M0G52-R0	SMD	10.0		(10)	(10)	0	2.4	5.5
		CSTLS10M0G53-B0	Lead	10.0		(15)	(15)	0	2.4	5.5
		CSTCE12M0G52-R0	SMD	12.0		(10)	(10)	0	2.4	5.5
		CSTCE16M0V53-R0	SMD	16.0		(15)	(15)	0	2.4	5.5
		CSTLS16M0X51-B0	Lead	16.0		(5)	(5)	0	2.4	5.5
		CSTCE20M0V51-R0	SMD	20.0		(5)	(5)	0	2.7	5.5
		CSTLS20M0X51-B0	Lead	20.0		(5)	(5)	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. Values in parentheses in the C1, C2 columns indicate an internal capacitance.

3. When using these oscillators, contact Murata Manufacturing Co., Ltd. (http://www.murata.co.jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

(1) X1 oscillation: **As of March, 2013(4/4)**

Manufacturer	Resonator	Part Number	SMD/ Lead	Frequency (MHz)	Flash operation mode Note 1	Recommended Circuit Constants Note 2 (reference)			Oscillation Voltage Range (V)	
						C1 (pF)	C2 (pF)	Rd (kΩ)	MIN.	MAX.
Nihon Dempa Kogyo Co., Ltd. Note 3	Crystal resonator	NX8045GB	SMD	8	LS	1	1	0	1.8	5.5
		NX8045GB	SMD	8	HS	1	1	0	2.4	5.5
		NX3225GB	SMD	16		2	2	0	2.4	5.5
		NX2520SA	SMD	20		1	1	0	2.7	5.5

<R> **Notes 1.** Set the flash operation mode by using CMODE1 and CMODE0 bits of the option byte (000C2H).

2. C1, C2 columns indicate a reference value.

3. When using these oscillators, contact Nihon Dempa Kogyo Co., Ltd. (http://www.ndk.com/jp/).

Remark Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (High speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz (When X1 oscillation: 1 MHz to 20 MHz)
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

LS (Low speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz

LV (Low voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

3. 6 Timer Array Unit

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 6 TIMER ARRAY UNIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

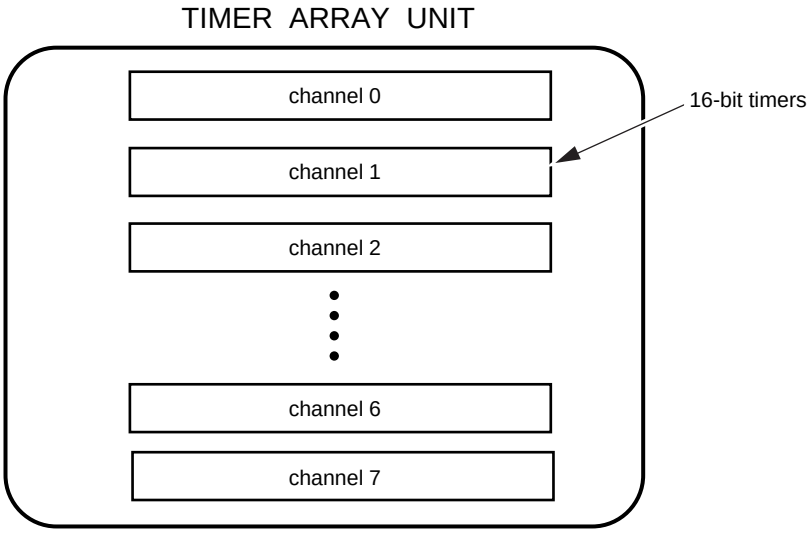
The timer array unit is provided in all products (Unit 0, Channels 0 to 7).

Units	Channels	64-pin products, 80-pin products
Unit 0	Channel 0	√
	Channel 1	√
	Channel 2	√
	Channel 3	√
	Channel 4	√
	Channel 5	√
	Channel 6	√
	Channel 7	√

Caution Most of the following descriptions in this section use the case of 80-pin products as an example.

The timer array unit has eight 16-bit timers.

Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.



For the details of each function, see the section shown below.

Independent channel operation function	Simultaneous channel operation function
• Interval timer (-> see 3. 6. 8) • Square wave output (-> see 3. 6. 8) • External event counter (-> see 3. 6. 8) • Divider function [Note] (-> see 3. 6. 8) • Input pulse interval measurement (-> see 3. 6. 8) • Measurement of high/low-level width of input signal (-> see 3. 6. 8) • Delay counter (-> see 3. 6. 8)	• One-shot pulse output (-> see 3. 6. 9) • PWM output (-> see 3. 6. 9) • Multiple PWM output (-> see 3. 6. 9)

Note Only channel 0 of unit 0.

It is possible to use the 16-bit timer of channels 1 and 3 of unit 0 as two 8-bit timers (higher and lower). The functions that can use channels 1 and 3 as 8-bit timers are as follows:

- Interval timer (higher/lower 8-bit timer)/square wave output (lower 8-bit timer only)
- External event counter (lower 8-bit timer only)
- Delay counter (lower 8-bit timer only)

Channel 7 of unit 0 can be used to realize LIN-bus communication operating in combination with UART2 of the serial array unit.

3. 6. 1 Functions of timer array unit

Timer array unit has the following functions.

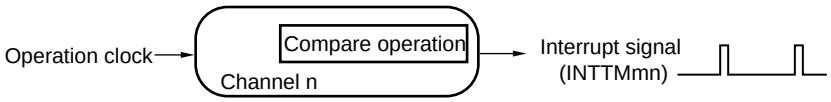
3. 6. 1. 1 Independent channel operation function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

Remark The presence or absence of timer I/O pins of channels 0 to 7 depends on the product. See **Table 3-9 Timer I/O Pins provided in Each Product** for details.

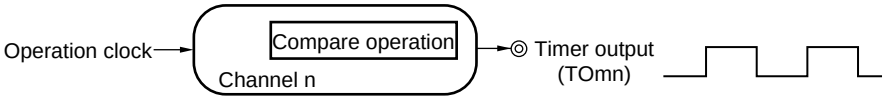
<1> Interval timer

Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.



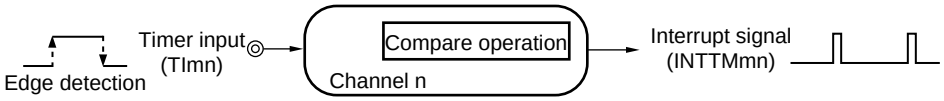
<2> Square wave output

A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn).



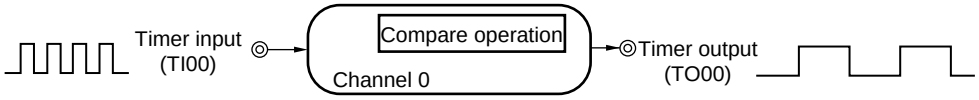
<3> External event counter

Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn) has reached a specific value.



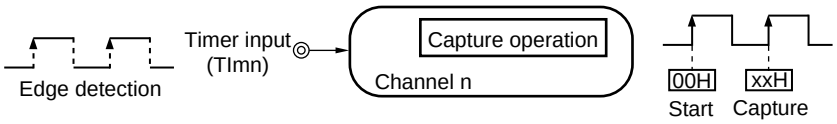
<4> Divider function (channel 0 of unit 0 only)

A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).



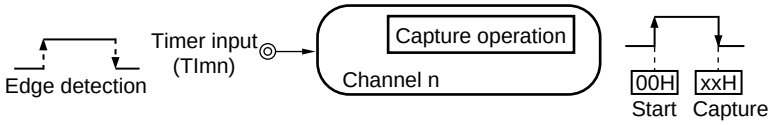
<5> Input pulse interval measurement

Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.



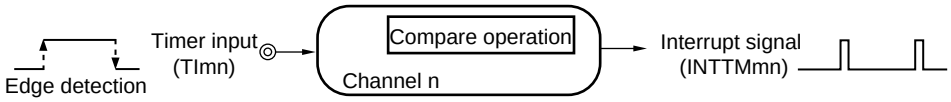
<6> Measurement of high/low-level width of input signal

Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.



<7> Delay counter

Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.



Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn) , timer output pin (TOmn) : n = 0, 4, 7))

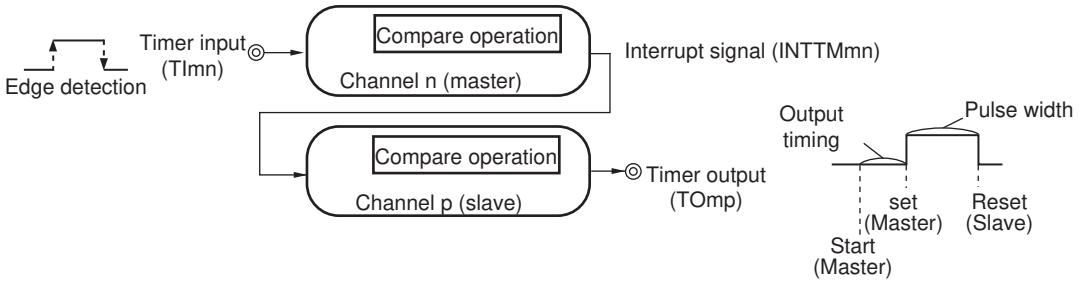
3. 6. 1. 2 Simultaneous channel operation function

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

<1> One-shot pulse output

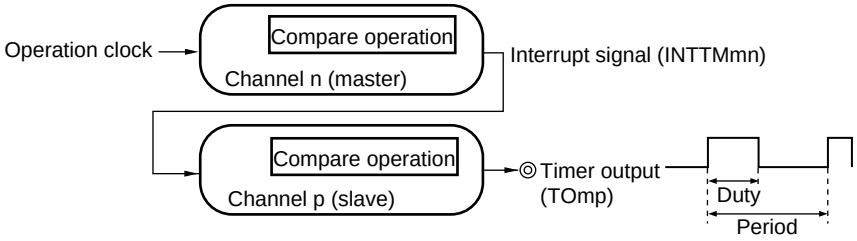
Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.

<R>



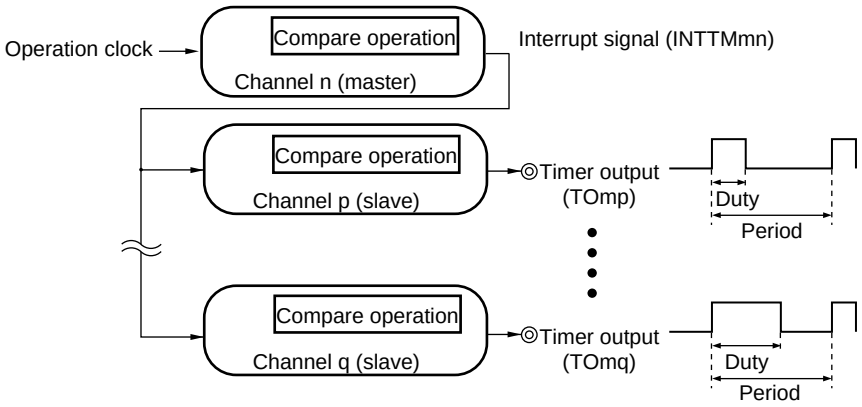
<2> PWM (Pulse Width Modulation) output

Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.



<3> Multiple PWM (Pulse Width Modulation) output

By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.



Caution For details about the rules of simultaneous channel operation function, see 3. 6. 4 Basic rules of timer array unit.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn) , timer output pin (TOmn) : n = 0, 4, 7)), p, q: Slave channel number (4, 7)

3. 6. 1. 3 8-bit timer operation function (channels 1 and 3 only)

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

Caution There are several rules for using 8-bit timer operation function. For details, see 3. 6. 4 Basic rules of timer array unit.

3. 6. 1. 4 LIN-bus supporting function (channel 7 of unit 0 only)

Timer array unit is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

<1> Detection of wakeup signal

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.

<2> Detection of break field

The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD2) of UART2 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.

<3> Measurement of pulse width of sync field

After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD2) of UART2 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

Remark For details about setting up the operations used to implement the LIN-bus, see **3. 6. 3. 13 Input switch control register (ISC)** and **3. 6. 8 Independent channel operation function of timer array unit.**

3. 6. 2 Configuration of timer array unit

Timer array unit includes the following hardware.

Table 3-8. Configuration of Timer Array Unit

Item	Configuration
Timer/counter	Timer count register mn (TCRmn)
Register	Timer data register mn (TDRmn)
Timer input	TI00, TI04, TI07, RxD2 pin (for LIN-bus)
Timer output	TO00, TO04, TO07, output controller
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Timer clock select register m (TPSm) • Timer channel enable status register m (TEm) • Timer channel start register m (TSm) • Timer channel stop register m (TTm) • Timer input select register 0 (TIS0) • Timer output enable register m (TOEm) • Timer output register m (TOm) • Timer output level register m (TOLm) • Timer output mode register m (TOMm)
	<Registers of each channel> • Timer mode register mn (TMRmn) • Timer status register mn (TSRmn) • Input switch control register (ISC) • Noise filter enable register 1 (NFEN1) • Port mode control register (PMCxx) • Port mode register (PMxx) • Port register (Pxx)

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7)

The presence or absence of timer I/O pins in each timer array unit channel is as follows.

Table 3-9. Timer I/O Pins provided in Each Product

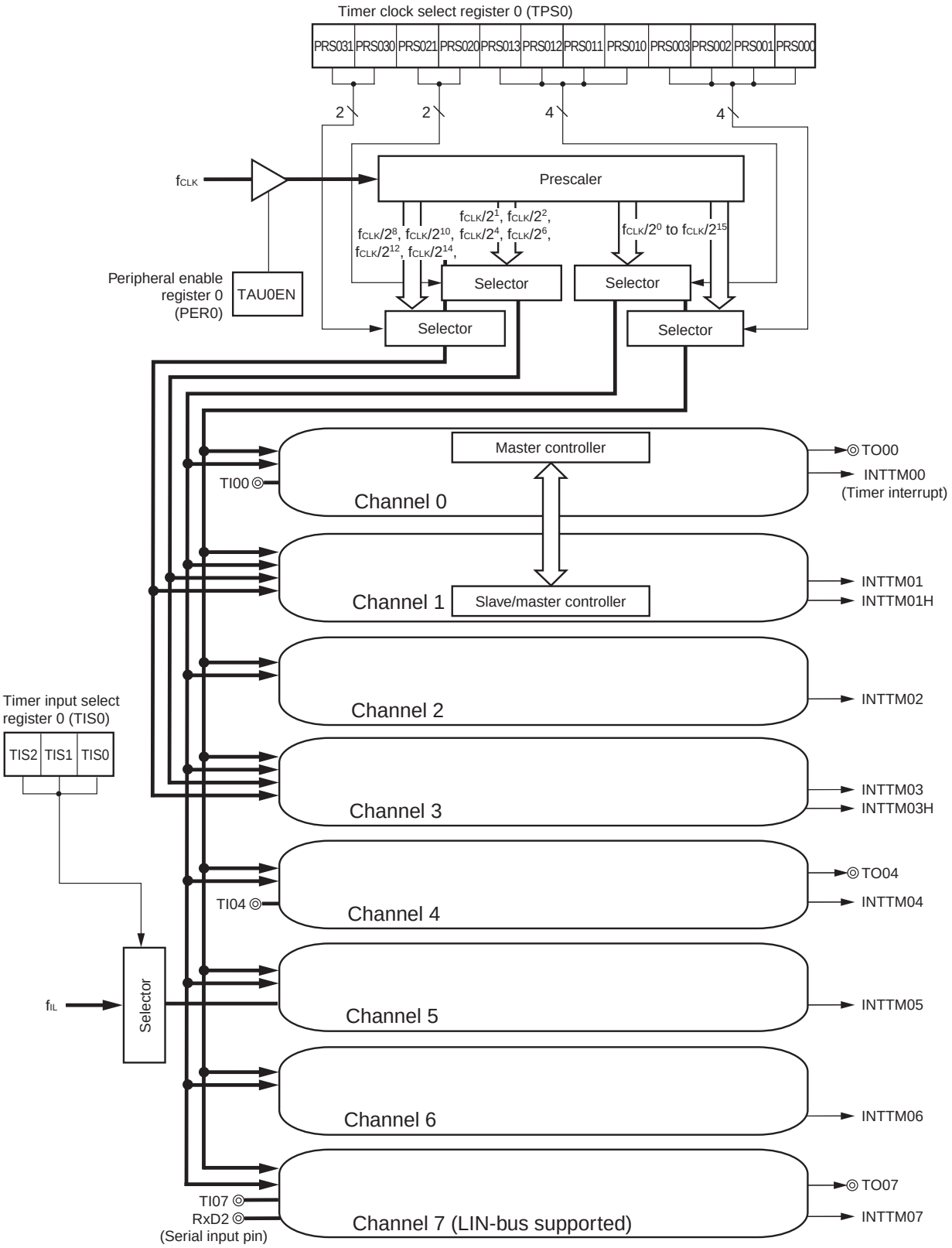
Timer array unit channels		64-pin products, 80-pin products
Unit 0	Channel 0	P00/TI00, P01/TO00
	Channel 1	–
	Channel 2	–
	Channel 3	–
	Channel 4	P42/TI04/TO04
	Channel 5	–
	Channel 6	–
	Channel 7	P41/TI07/TO07

Remarks 1. When timer input and timer output are shared by the same pin, either only timer input or only timer output can be used.

2. –: here is no timer I/O pin, but the channel is available. (However, the channel can only be used as an interval timer.)

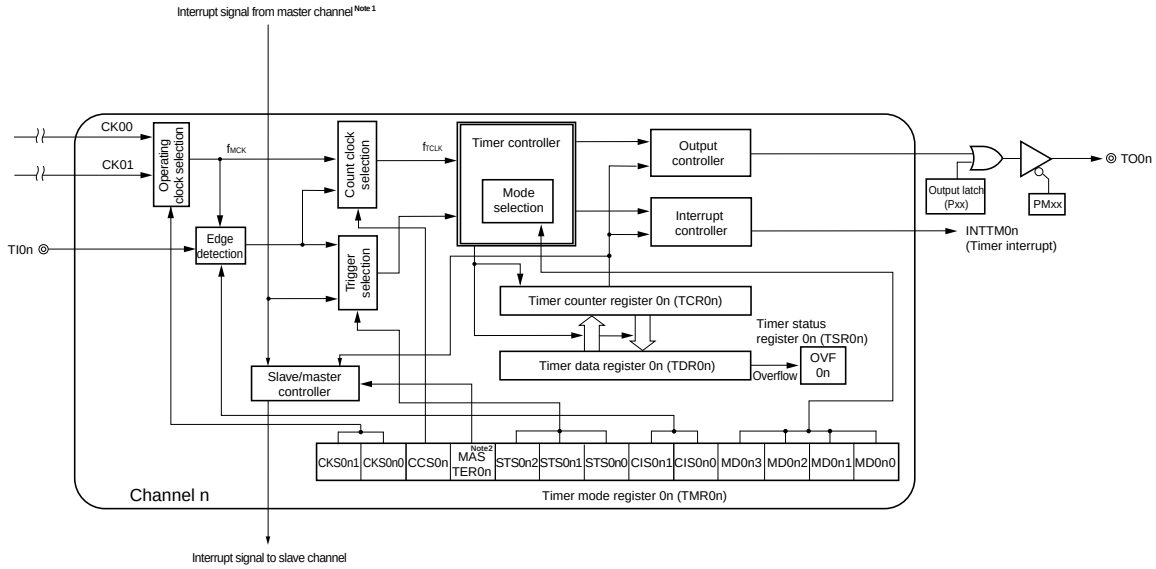
Figures 3-3 show the block diagrams of the timer array unit of the 80-pin products.

Figure 3-3. Entire Configuration of Timer Array Unit 0 (Example: 80-pin products)



Remark f_{IL}: ow-speed on-chip oscillator clock frequency

Figure 3-4. Internal Block Diagram of Channel 0, 4 of Timer Array Unit 0

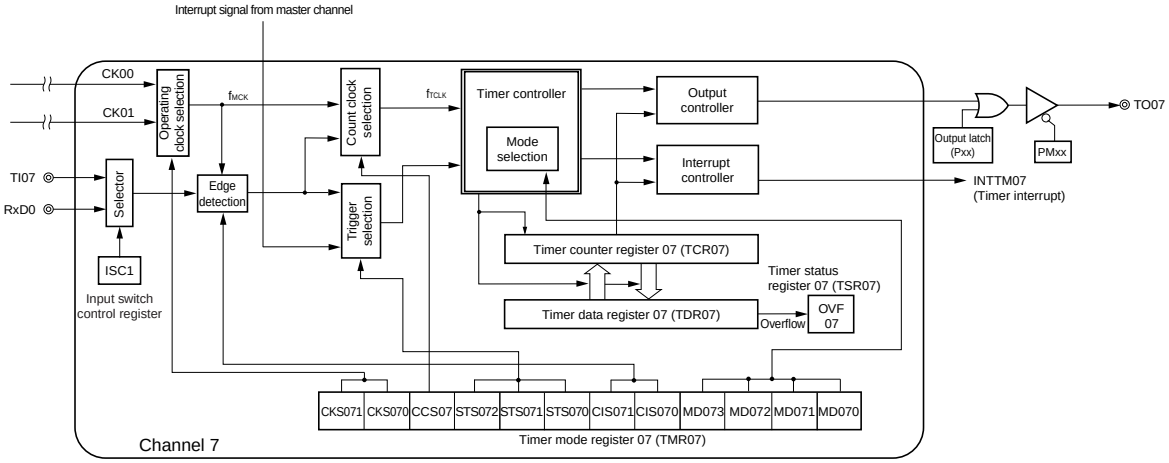


Notes 1. Channels 4 only

2. n = 4 only

Remark n = 0, 4

Figure 3-5. Internal Block Diagram of Channel 7 of Timer Array Unit 0



3. 6. 2. 1 Timer count register mn (TCRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 1 Timer count register mn (TCRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 2. 2 Timer data register mn (TDRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 2. 2 Timer data register mn (TDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3 Registers controlling timer array unit

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **6. 3 Registers Controlling Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 6. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

TAU0EN	Control of timer array 0 unit input clock
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read/written.

Cautions 1. When setting the timer array unit, be sure to set the TAUmEN bit to 1 first. If TAUmEN = 0, writing to a control register of timer array unit is ignored, and all read values are default values (except for the timer input select register 0 (TIS0), input switch control register (ISC), noise filter enable register 1 (NFEN1), port mode control registers 0, 1, 4 (PMC0, PMC1, PMC4), port mode registers 0, 1, 4 (PM0, PM1, PM4), and port registers 0, 1, 4 (P0, P1, P4)).

- **Timer clock select register m (TPSm)**
- **Timer mode register mn (TMRmn)**
- **Timer status register mn (TSRmn)**
- **Timer channel enable status register m (TEm)**
- **Timer channel start register m (TSm)**
- **Timer channel stop register m (TTm)**
- **Timer output enable register m (TOEm)**
- **Timer output register m (TOm)**
- **Timer output level register m (TOLm)**
- **Timer output mode register m (TOMm)**

2. Be sure to clear bits 1, 4, and 6 to "0".

3. 6. 3. 2 Timer clock select register m (TPSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 2 Timer clock select register m (TPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 3 Timer mode register mn (TMRmn)

- Format of Timer Mode Register mn (TMRmn) (1/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MAS TER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0Note	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CKSmn1	CKSmn0	Selection of operation clock (f_{MCK}) of channel n
0	0	Operation clock CKm0 set by timer clock select register m (TPSm)
0	1	Operation clock CKm2 set by timer clock select register m (TPSm)
1	0	Operation clock CKm1 set by timer clock select register m (TPSm)
1	1	Operation clock CKm3 set by timer clock select register m (TPSm)
Operation clock (f_{MCK}) is used by the edge detector. A count clock (f_{TCLK}) and a sampling clock are generated depending on the setting of the CCSmn bit. The operation clocks CKm2 and CKm3 can only be selected for channels 1 and 3.		

CCSmn	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by the CKSmn0 and CKSmn1 bits
1	Valid edge of input signal input from the TImn pin When channel 5 is used, the valid edge of the input signal selected by the TIS0
Count clock (f_{TCLK}) is used for the timer/counter, output controller, and interrupt controller.	

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Cautions 1. Be sure to clear bits 13, 5, and 4 to "0".

2. The timer array unit must be stopped (TTm = 00FFH) if the clock selected for f_{CLK} is changed (by changing the value of the system clock control register (CKC)), even if the operating clock specified by using the CKSmn0 and CKSmn1 bits (f_{MCK}) or the valid edge of the signal input from the TImn pin is selected as the count clock (f_{TCLK}).

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

- Format of Timer Mode Register mn (TMRmn) (2/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0Note	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Bit 11 of TMRmn (n = 2, 4, 6)

MASTER mn	Selection between using channel n independently or simultaneously with another channel (as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the channel 2, 4, 6 can be set as a master channel (MASTERmn = 1). Be sure to use channel 0, 5, 7 are fixed to 0 (Regardless of the bit setting, channel 0 operates as master, because it is the highest channel). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

Bit 11 of TMRmn (n = 1, 3)

SPLITmn	Selection of 8 or 16-bit timer operation for channels 1 and 3
0	Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

STS mn2	STS mn1	STS mn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

- Format of Timer Mode Register mn (TMRmn) (3/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

- Format of Timer Mode Register mn (TMRmn) (4/4)

Address: F0190H, F0191H (TMR00) - F019EH, F019FH (TMR07) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 2, 4, 6)	CKS mn1	CKS mn0	0	CCS mn	MASTER mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 1, 3)	CKS mn1	CKS mn0	0	CCS mn	SPLIT mn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn (n = 0, 5, 7)	CKS mn1	CKS mn0	0	CCS mn	0[Note]	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

MD mn3	MD mn2	MD mn1	MD mn0	Operation mode of channel n	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/Square wave output/ Divider function/PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/ PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high/low-level width of input signal	Counting up
Other than above				Setting prohibited		
The operation of the MDmn0 bit varies depending on each operation mode (see table below).						

<R> **Note** Bit 11 is fixed at 0 of read only, write is ignored.

(**Remark** is on the next page.)

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode 0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 1 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 2. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Notes 1. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

2. If the start trigger (TSmn = 1) is issued during operation, the counter is initialized, an interrupt is generated, and recounting is started (does not occur the interrupt request). <R>

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 4 Timer status register mn (TSRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 4 Timer status register mn (TSRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 5 Timer channel enable status register m (TEm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 5 Timer channel enable status register m (TEm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 6 Timer channel start register m (TSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 6 Timer channel start register m (TSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 7 Timer channel stop register m (TTm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 7 Timer channel stop register m (TTm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 8 Timer input select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	TIS02	TIS01	TIS00

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Default value
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
Other than above			Setting prohibited

Caution High-level width, low-level width of timer input selected will require more than 1/f_{MCK} +10 ns.

3. 6. 3. 9 Timer output enable register m (TOEm)

Address: F01BAH, F01BBH (TOE0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOEm	0	0	0	0	0	0	0	0	TOEm7	0	0	TOEm4	0	0	0	TOEm0

TOEmn	Timer output enable/disable of channel n
0	The TOmn operation stopped by count operation (timer channel output bit). Writing to the TOmn bit is enabled. The TOmn pin functions as data output, and it outputs the level set to the TOmn bit. The output level of the TOmn pin can be manipulated by software.
1	The TOmn operation enabled by count operation (timer channel output bit). Writing to the TOmn bit is disabled (writing is ignored). The TOmn pin functions as timer output, and the TOEmn bit is set or reset depending on the timer operation. The TOmn pin outputs the square-wave or PWM depending on the timer operation.

Caution Be sure to clear bits 15 to 8, 6, 5, 3 to 1 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 10 Timer output register m (TOm)

Address: F01B8H, F01B9H (TO0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOm	0	0	0	0	0	0	0	0	TOm7	0	0	TOm4	0	0	0	TOm0

TOmn	Timer output of channel n
0	Timer output value is “0”.
1	Timer output value is “1”.

Caution Be sure to clear bits 15 to 8, 6, 5, 3 to 1 to “0”.

Remark m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 11 Timer output level register m (TOLm)

Address: F01BCH, F01BDH (TOL0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOLm	0	0	0	0	0	0	0	0	TOL m7	0	0	TOL m4	0	0	0	0

TOLmn	Control of timer output level of channel n
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Caution Be sure to clear bits 15 to 8, 6, 5, 3 to 0 to "0".

Remarks 1. If the value of this register is rewritten during timer operation, the timer output logic is inverted when the timer output signal changes next, instead of immediately after the register value is rewritten.

2. m: Unit number (m = 0), n: Channel number (n = 0 to 7 (however, timer input pin (TImn), timer output pin (TOmn): n = 0, 4, 7))

3. 6. 3. 12 Timer output mode register m (TOMm)

Address: F01BEH, F01BFH (TOM0) After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOMm	0	0	0	0	0	0	0	0	TOM m7	0	0	TOM m4	0	0	0	0

TOMmn	Control of timer output mode of channel n
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTMmn))
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTMmn) of the master channel, and reset by the timer interrupt request signal (INTTMmp) of the slave channel)

Caution Be sure to clear bits 15 to 8 and 0 to "0".

Remark m: Unit number (m = 0)
n: Channel number
n = 0, 1 (n = 0, 2, 4, 6)
p: Slave channel number
n = 4, 7
(For details of the relation between the master channel and slave channel, refer to **3. 6. 4 Basic rules of timer array unit**.)

3. 6. 3. 13 Input switch control register (ISC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **6. 3. 13 Input switch control register (ISC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 3. 14 Noise filter enable register 1 (NFEN1)

Address: F0071H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	0	0	TNFEN04	0	0	0	TNFEN00

TNFEN07	Enable/disable using noise filter of TI07/TO07/P41 pin or RxD2/P14 pin input signal[Note]
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN00	Enable/disable using noise filter of TI00/P00 pin input signal
0	Noise filter OFF
1	Noise filter ON

Note The applicable pin can be switched by setting the ISC1 bit of the ISC register.
ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.
ISC1 = 1: Whether or not to use the noise filter of the RxD2 pin can be selected.

Caution Be sure to clear bits 6, 5, 3 to 1 to "0".

<R> 3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O

Using port pins for the timer array unit functions requires setting of the registers that control the port functions multiplexed on the target pins (port mode register (PMxx), port register (Pxx), and port mode control register (PMCxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **6. 3. 15 Registers controlling port functions of pins to be used for timer I/O** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 4 Basic rules of timer array unit

See **6. 4 Basic Rules of Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 5 Operation of counter

See **6. 5 Operation of Counter** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 6 Channel output (TOmn pin) control

See **6. 6 Channel Output (TOmn pin) Control** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 7 Timer input (TImn) control

See **6. 7 Timer Input (TImn) Control** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 8 Independent channel operation function of timer array unit

See **6. 8 Independent Channel Operation Function of Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 9 Simultaneous channel operation function of timer array unit

See **6. 9 Simultaneous Channel Operation Function of Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 6. 10 Cautions when using timer array unit

See **6. 10 Cautions When Using Timer Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 7 Real-Time Clock

Real-time clock is not provided in RL78/G1E (64-pin products, 80-pin products).

3. 8 12-bit Interval Timer

3. 8. 1 Functions of 12-bit interval timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from STOP mode and triggering an A/D converter's SNOOZE mode.

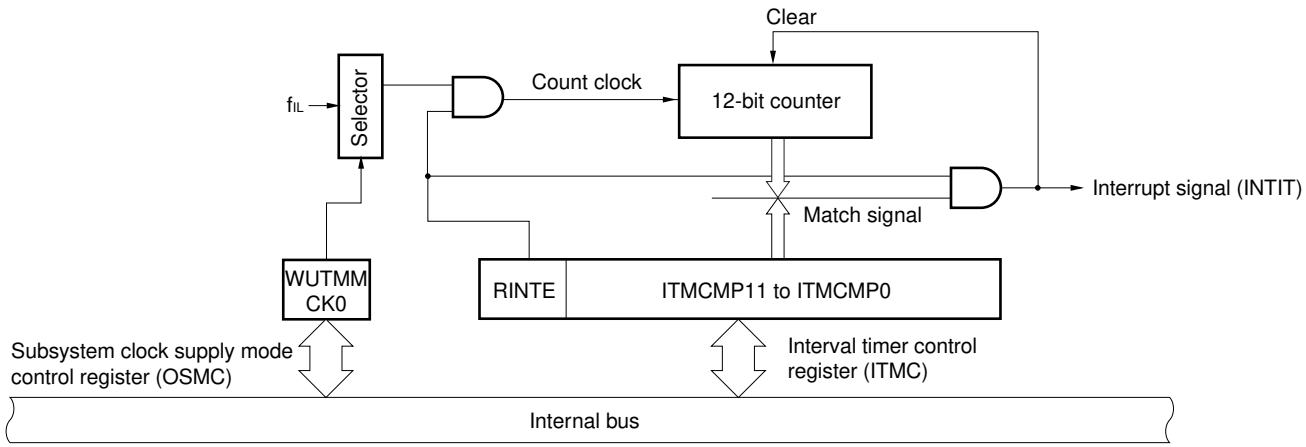
<R> 3. 8. 2 Configuration of 12-bit interval timer

The 12-bit interval timer includes the following hardware.

Table 3-10. Configuration of 12-bit Interval Timer

Item	Configuration
Counter	12-bit counter
Control registers	Peripheral enable register 0 (PER0)
	Subsystem clock supply mode control register (OSMC)
	Interval timer control register (ITMC)

Figure 3-6. Block Diagram of 12-bit Interval Timer



3. 8. 3 Registers controlling 12-bit interval timer

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **8. 3 Registers Controlling 12-bit Interval Timer** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 8. 3. 1 Peripheral enable register0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

RTCEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply. • SFR used by the 12-bit interval timer cannot be written. • The 12-bit interval timer is in the reset status.
1	Enables input clock supply. • SFR used by the 12-bit interval timer can be written.

<R> **3. 8. 3. 2 Subsystem clock supply mode control register (OSMC)**

Address: F00F3H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
OSMC	0	0	0	WUTMMCK0	0	0	0	0

WUTMMCK0	Operation clock for 12-bit interval timer
0	Default value
1	Low-speed on-chip oscillator clock

Cautions 1. Be sure to clear bit 7 to "0".

2. To use 12-bit interval timer, after reset release, set the WUTMMCK0 bit of the subsystem clock supply mode control register (OSMC) to "1" before setting the RTCEN bit of the peripheral enable register0 (PER0) to "1".

3. 8. 3. 3 Interval timer control register (ITMC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **8. 3. 3 Interval timer control register (ITMC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 8. 4 12- bit interval timer operation

See **8. 4 12- bit Interval Timer Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9 Clock Output/Buzzer Output Controller

The number of output pins of the clock output and buzzer output controllers differs, depending on the product.

Output Pin	64-pin products	80-pin products
PCLBUZ0	–	√
PCLBUZ1	–	–

Caution The output pins for clock output/buzzer output controller are not provided in the 64-pin products.

3. 9. 1 Functions of clock output/buzzer output controller

The clock output controller is intended for clock output for supply to peripheral ICs.

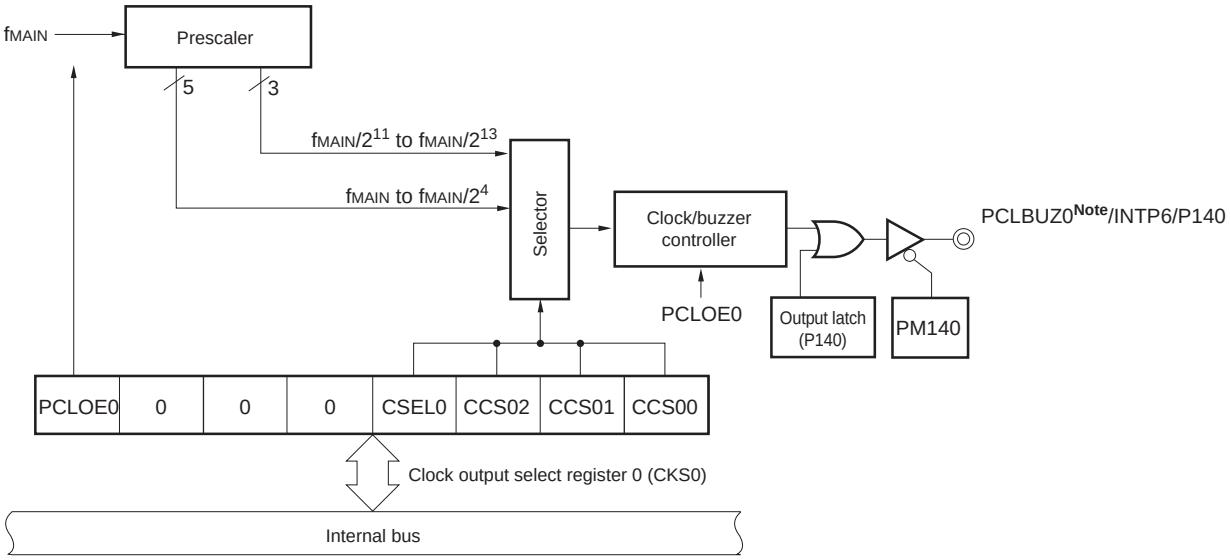
Buzzer output is a function to output a square wave of buzzer frequency.

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock selected by clock output select register 0 (CKS0).

Figure 3-7 shows the block diagram of clock output/buzzer output controller.

Figure 3-7. Block Diagram of Clock Output/Buzzer Output Controller



Note For output frequencies available from PCLBUZ0, see **CHAPTER 5 ELECTRICAL SPECIFICATIONS**.

3. 9. 2 Configuration of clock output/buzzer output controller

The clock output/buzzer output controller includes the following hardware.

Table 3-11. Configuration of Clock Output/Buzzer Output Controller

Item	Configuration
Control registers	Clock output select register n (CKS0) Port mode register 14 (PM14) Port register 14 (P14)

3. 9. 3 Registers controlling clock output/buzzer output controller

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **9. 3 Registers Controlling Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 3. 1 Clock output select register 0 (CKS0)

Address: FFFA5H (CKS0) After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKS0	PCLOE0	0	0	0	CSEL0	CCS02	CCS01	CCS00

PCLOE0	PCLBUZ0 pin output enable/disable specification
0	Output disable (default)
1	Output enable

CSEL0	CCS 02	CCS 01	CCS 00		PCLBUZ0 pin output clock selection			
					f_{MAIN} = 5 MHz	f_{MAIN} = 10 MHz	f_{MAIN} = 20 MHz	f_{MAIN} = 32 MHz
0	0	0	0	f_{MAIN}	5 MHz	10 MHz[Note]	Setting prohibited[Note]	Setting prohibited[Note]
0	0	0	1	$f_{MAIN}/2$	2.5 MHz	5 MHz	10 MHz[Note]	16 MHz[Note]
0	0	1	0	$f_{MAIN}/2^2$	1.25 MHz	2.5 MHz	5 MHz	8 MHz[Note]
0	0	1	1	$f_{MAIN}/2^3$	625 kHz	1.25 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{MAIN}/2^4$	312.5 kHz	625 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{MAIN}/2^{11}$	2.44 kHz	4.88 kHz	9.77 kHz	15.63 kHz
0	1	1	0	$f_{MAIN}/2^{12}$	1.22 kHz	2.44 kHz	4.88 kHz	7.81 kHz
0	1	1	1	$f_{MAIN}/2^{13}$	610 Hz	1.22 kHz	2.44 kHz	3.91 kHz
Other than above				Setting prohibited				

Note Use the output clock within a range of 16 MHz. Furthermore, when using the output clock at 2.7 V ≤ V_{DD} < 4.0 V, can be use it within 8 MHz only. See **5. 2. 3 AC characteristics** for details.

Cautions 1. Change the output clock after disabling clock output (PCLOEn = 0).

2. To shift to STOP mode when the main system clock is selected (CSELn = 0), set PCLOEn = 0 before executing the STOP instruction.

Remark f_{MAIN}: Main system clock frequency

<R> **3. 9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output**

Using a port pin for clock or buzzer output requires setting of the registers that control the port functions multiplexed on the target pin (port mode register (PMxx), port register (Pxx)). For details, see **3. 4. 3. 1 Port mode registers (PMxx)** and **3. 4. 3. 2 Port registers (Pxx)**.

For details of setting example, see **9. 3. 2 Registers controlling port functions of pins to be used for clock or buzzer output** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 4 Operations of clock output/buzzer output controller

See **9. 4 Operations of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 9. 5 Cautions of clock output/buzzer output controller

See **9. 5 Cautions of Clock Output/Buzzer Output Controller** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 10 Watchdog Timer

See **CHAPTER 10 WATCHDOG TIMER** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11 A/D Converter

The number of analog input channels of the A/D converter differs, depending on the product.

			64-pin products	80-pin products
Analog input channels		Total	13 channels	17 channels
	High accuracy channel	Pins based on input buffer power supply AV_{DD}	4 channels (ANI0 to ANI3)	5 channels (ANI0 to ANI4)
	Standard channel	Pins based on input buffer power supply V_{DD}	9 channels (ANI16 to ANI18, ANI20 to ANI23, ANI28, ANI30)	12 channels (ANI16 to ANI18, ANI20 to ANI26, ANI28, ANI30)

Remark In this section, most of the following descriptions, such as function of A/D converter, block diagram and configuration, are based on the case of the 80-pin products as an example. For the case of the 64-pin products, ignore the descriptions which are not available for 64-pin products.

3. 11. 1 Function of A/D converter

The A/D converter converts analog input signals into digital values, and is configured to control analog inputs, including up to 17 channels of A/D converter analog inputs (ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30). 12-bit resolution or 8-bit resolution can also be selected by using the ADTYP bit of A/D converter mode register 2 (ADM2). The A/D converter has the following functions.

<R> • 12-bit/8-bit resolution A/D conversion

A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, ANI30. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated (when in the select mode).

<R> **Caution The valid resolution differs depending on the voltage conditions of AV_{DD} and AV_{REFP}. For details, see 5. 2. 5. 1 A/D converter characteristics.**

<R> **Remark** When using the converter with a resolution of 10 bits, select the 12-bit resolution mode (ADTYP = 0). Use the higher 10 bits of the conversion result. Do not use the lower 2 bits.

<R> Various A/D conversion modes can be specified by using the mode combinations below.

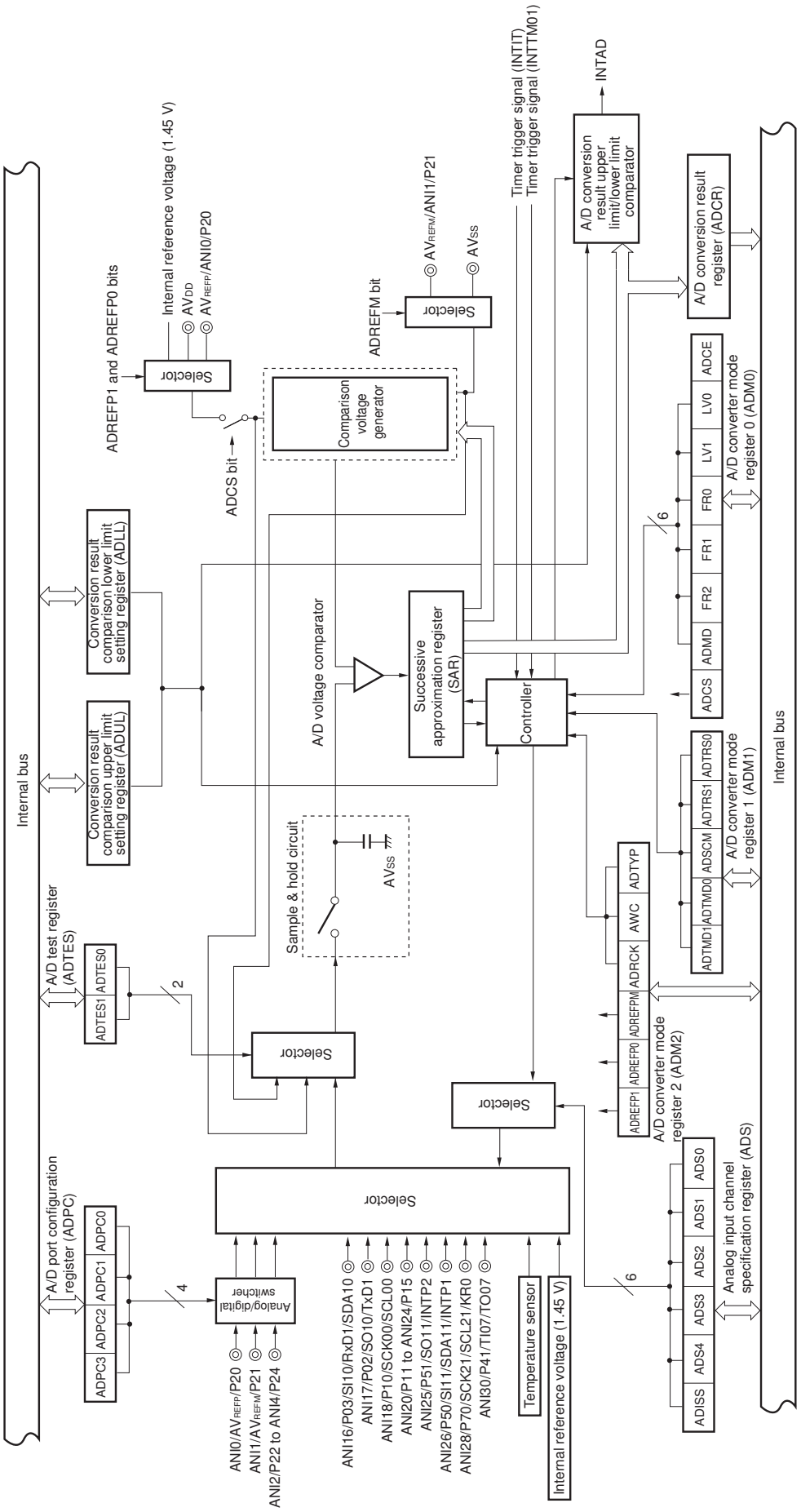
Trigger mode	Software trigger	Conversion is started by software manipulation.
	Hardware trigger no-wait mode	Conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the A/D power supply stabilization wait time passes. When using the SNOOZE mode function, specify the hardware trigger wait mode.
Channel selection mode	Select mode	A/D conversion is performed on the analog input of one selected channel.
	Scan mode	A/D conversion is performed on the analog input of four channels in order.
Conversion operation mode	One-shot conversion mode	A/D conversion is performed on the selected channel once.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.

Operation Mode[Note]	Number of Sampling Clock	
Normal 1	11 f_{AD}	Set a value to the number of sampling clocks, at which the sampling capacitor is fully charged, depending on the output impedance of the analog input source.
Normal 2	23 f_{AD}	
Low-voltage 1	33 f_{AD}	
Low-voltage 2	187 f_{AD}	

Note The operation modes selectable differ depending on the analog input channel, AV_{DD} voltage, trigger mode, and f_{CLK}. For details, see 3. 11. 3. 2 A/D converter mode register 0 (ADM0) and check A/D conversion time selection.

<R>

Figure 3-8. Block Diagram of A/D Converter



Remark Analog input pins drawn in this figure is for the case of 80-pin products

3. 11. 2 Configuration of A/D converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 pins

These are the analog input pins of the 17 channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

(3) A/D voltage comparator

This A/D voltage comparator compares output from the voltage tap of the comparison voltage generator with the sampled voltage value.

If the analog input voltage is found to be greater than the reference voltage (1/2 AV_{REF}) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage (1/2 AV_{REF}), the MSB bit of the SAR is reset.

After that, bit 10 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the comparison voltage generator is selected by the value of bit 11, to which the result has been already set.

Bit 11 = 0: (1/4 AV_{REF})
Bit 11 = 1: (3/4 AV_{REF})

The voltage tap of the comparison voltage generator and the analog input voltage are compared and bit 10 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage ≥ Voltage tap of comparison voltage generator: Bit 10 = 1
Analog input voltage ≤ Voltage tap of comparison voltage generator: Bit 10 = 0

Comparison is continued like this to bit 0 of the SAR register.

When performing A/D conversion at a resolution of 8 bits, the comparison continues until bit 4 of the SAR register.

Remark AV_{REF}: The + side reference voltage of the A/D converter.
(This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and AV_{DD}.)

(4) Comparison voltage generator

The comparison voltage generator generates the comparison voltage input from an analog input pin.

(5) Successive approximation register (SAR)

The SAR register is a register that sets voltage tap data whose values from the comparison voltage generator match the voltage values of the analog input pins, 1 bit at a time starting from the most significant bit (MSB).

If data is set in the SAR register all the way to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register (conversion results) are held in the A/D conversion result register (ADCR). When all the specified A/D conversion operations have ended, an A/D conversion end interrupt request signal (INTAD) is generated.

(6) 12-bit A/D conversion result register (ADCR)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCR register holds the A/D conversion result in its lower 12 bits (the higher 4 bits are fixed to 0).

(7) 8-bit A/D conversion result register (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the higher 8 bits of the A/D conversion result.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REFP} pin

This pin inputs an external reference voltage (AV_{REFP}).

If using AV_{REFP} as the + side reference voltage of the A/D converter, set the ADREFP1 and ADREFP0 bits of A/D converter mode register 2 (ADM2) to 1.

The analog signals input to ANI0 to ANI12 and ANI16 to ANI30 are converted to digital signals based on the voltage applied between AV_{REFP} and the – side reference voltage (AV_{REFM}/AV_{SS}).

In addition to AV_{REFP}, it is possible to select AV_{DD}, or the internal reference voltage (1.45 V) as the + side reference voltage of the A/D converter.

(10) AV_{REFM} pin

This pin inputs an external reference voltage (AV_{REFM}). If using AV_{REFM} as the – side reference voltage of the A/D converter, set the ADREFM bit of the ADM2 register to 1.

In addition to AV_{REFM}, it is possible to select AV_{SS} as the – side reference voltage of the A/D converter.

3. 11. 3 Registers used in A/D converter

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **11. 3 Registers Used in A/D Converter** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read/written.

<R>

Caution Be sure to clear bits 1, 4, and 6 to "0".

3. 11. 3. 2 A/D converter mode register 0 (ADM0)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 2 A/D converter mode register 0 (ADM0)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 3 A/D converter mode register 1 (ADM1)

Address: FFF32H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADM1	ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0

<R>

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	×	Software trigger mode
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

ADSCM	Specification of the A/D conversion mode
0	Sequential conversion mode
1	One-shot conversion mode

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	0	End of timer channel 1 count or capture interrupt signal (INTTM01)
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Interval timer interrupt signal (INTIT)

Cautions 1. Rewrite the value of the ADM1 register while conversion is stopped (ADCS = 0, ADCE = 0).

<R>

2. To complete A/D conversion, specify at least the following time as the hardware trigger interval:
Hardware trigger no wait mode: 2 f_{CLK} clock + A/D conversion time
Hardware trigger wait mode: 2 f_{CLK} clock + A/D power supply stabilization wait time +A/D conversion time

3. In modes other than SNOOZE mode, input of the next INTRTC or INTIT will not be recognized as a valid hardware trigger for up to four f_{CLK} cycles after the first INTRTC or INTIT is input.

Remarks 1. ×: don't care

2. f_{CLK}: CPU/peripheral hardware clock frequency

3. 11. 3. 4 A/D converter mode register 2 (ADM2)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 4 A/D converter mode register 2 (ADM2)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 5 12-bit A/D conversion result register (ADCR)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 5 12-bit A/D conversion result register (ADCR)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 6 8-bit A/D conversion result register (ADCRH)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 6 8-bit A/D conversion result register (ADCRH)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 7 Analog input channel specification register (ADS)

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

• Select mode (64-pin products, ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AVREFP pin
0	0	0	0	0	1	ANI1	P21/ANI1/AVREFM pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	Setting prohibited	
0	0	0	1	0	1	Setting prohibited	
0	0	0	1	1	0	Setting prohibited	
0	0	0	1	1	1	Setting prohibited	
0	0	1	0	0	0	Setting prohibited	
0	0	1	0	0	1	Setting prohibited	
0	0	1	0	1	0	Setting prohibited	
0	0	1	0	1	1	Setting prohibited	
0	0	1	1	0	0	Setting prohibited	
0	0	1	1	0	1	Setting prohibited	
0	0	1	1	1	0	Setting prohibited	
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	0	1	1	Setting prohibited	
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	Setting prohibited	
0	1	1	0	0	1	Setting prohibited	
0	1	1	0	1	0	Setting prohibited	
0	1	1	0	1	1	Setting prohibited	
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	0	1	Setting prohibited	
0	1	1	1	1	0	ANI30	P41/ANI30 pin
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output Note
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V) Note
Other than above						Setting prohibited	

Note This setting can be used only in HS (high-speed main) mode.

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

• Scan mode (64-pin products, ADMD = 1)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	0	0	0	0	0	ANI0	ANI1	ANI2	ANI3
0	1	0	1	0	0	ANI20	ANI21	ANI22	ANI23
Other than above						Setting prohibited			

Cautions 1. Be sure to clear bits 5 and 6 to 0.

2. Set a channel to be used for A/D conversion in the input mode by using port mode registers 0 to 2, 4, or 7 (PM0 to PM2, PM4, PM7).

3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.

4. Do not set the pin that is set by port mode control register 0, 4, or 7 (PMC0, PMC4, PMC7) as digital I/O by the ADS register.

5. Rewrite the value of the ADISS bit while conversion operation is stopped (ADCS = 0, ADCE = 0).

6. If using AV_{REFP} as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.

7. If using AV_{REFM} as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.

8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source. Also, after setting the ADISS to 1, the result of the first conversion cannot be used. For details about the setting flow, refer to 3. 11. 7 A/D converter setup flowchart.

9. Do not set the ADISS bit to 1 when shifting from STOP mode to HALT mode. Also, if the ADISS bit is set to 1, the temperature sensor operating current indicated in 5. 2. 2. 2 Supply current characteristics (I_{TMPS}) will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.

10. Ignore the conversion result if the corresponding ANI pin does not exist in the product used.

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

• Select mode (80-pin products, ADMD = 0)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel	Input source
0	0	0	0	0	0	ANI0	P20/ANI0/AVREFP pin
0	0	0	0	0	1	ANI1	P21/ANI1/AVREFM pin
0	0	0	0	1	0	ANI2	P22/ANI2 pin
0	0	0	0	1	1	ANI3	P23/ANI3 pin
0	0	0	1	0	0	ANI4	P24/ANI4 pin
0	0	0	1	0	1	Setting prohibited	
0	0	0	1	1	0	Setting prohibited	
0	0	0	1	1	1	Setting prohibited	
0	0	1	0	0	0	Setting prohibited	
0	0	1	0	0	1	Setting prohibited	
0	0	1	0	1	0	Setting prohibited	
0	0	1	0	1	1	Setting prohibited	
0	0	1	1	0	0	Setting prohibited	
0	0	1	1	0	1	Setting prohibited	
0	0	1	1	1	0	Setting prohibited	
0	0	1	1	1	1	Setting prohibited	
0	1	0	0	0	0	ANI16	P03/ANI16 pin
0	1	0	0	0	1	ANI17	P02/ANI17 pin
0	1	0	0	1	0	ANI18	P10/ANI18 pin
0	1	0	0	1	1	Setting prohibited	
0	1	0	1	0	0	ANI20	P11/ANI20 pin
0	1	0	1	0	1	ANI21	P12/ANI21 pin
0	1	0	1	1	0	ANI22	P13/ANI22 pin
0	1	0	1	1	1	ANI23	P14/ANI23 pin
0	1	1	0	0	0	ANI24	P15/ANI24 pin
0	1	1	0	0	1	ANI25	P51/ANI25 pin
0	1	1	0	1	0	ANI26	P50/ANI26 pin
0	1	1	0	1	1	Setting prohibited	
0	1	1	1	0	0	ANI28	P70/ANI28 pin
0	1	1	1	0	1	Setting prohibited	
0	1	1	1	1	0	ANI30	P41/ANI30 pin
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	–	Temperature sensor output[Note]
1	0	0	0	0	1	–	Internal reference voltage output (1.45 V)[Note]
Other than above						Setting prohibited	

Note This setting can be used only in HS (high-speed main) mode.

Address: FFF31H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADS	ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0

• Scan mode (80-pin products, ADMD = 1)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	0	0	0	0	0	ANI0	ANI1	ANI2	ANI3
0	0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
0	1	0	1	0	0	ANI20	ANI21	ANI22	ANI23
0	1	0	1	0	1	ANI21	ANI22	ANI23	ANI24
0	1	0	1	1	0	ANI22	ANI23	ANI24	ANI25
0	1	0	1	1	1	ANI23	ANI24	ANI25	ANI26
Other than above						Setting prohibited			

Cautions 1. Be sure to clear bits 5 and 6 to 0.

2. Set a channel to be used for A/D conversion in the input mode by using port mode registers 0 to 2, 4, or 7 (PM0 to PM2, PM4, PM7).

3. Do not set the pin that is set by the A/D port configuration register (ADPC) as digital I/O by the ADS register.

4. Do not set the pin that is set by port mode control register 0, 4, or 7 (PMC0, PMC4, PMC7) as digital I/O by the ADS register.

5. Rewrite the value of the ADISS bit while conversion operation is stopped (ADCS = 0, ADCE = 0).

6. If using AV_{REFP} as the + side reference voltage source of the A/D converter, do not select ANI0 as an A/D conversion channel.

7. If using AV_{REFM} as the – side reference voltage source of the A/D converter, do not select ANI1 as an A/D conversion channel.

8. If ADISS is set to 1, the internal reference voltage (1.45 V) cannot be used for the + side reference voltage source. Also, after setting the ADISS to 1, the result of the first conversion cannot be used. For details about the setting flow, refer to 3. 11. 7 A/D converter setup flowchart.

9. Do not set the ADISS bit to 1 when shifting from STOP mode to HALT mode. Also, if the ADISS bit is set to 1, the temperature sensor operating current indicated in 5. 2. 2. 2 Supply current characteristics (I_{TMPS}) will be added to the current consumption when shifting to HALT mode while the CPU is operating on the main system clock.

10. Ignore the conversion result if the corresponding ANI pin does not exist in the product used.

3. 11. 3. 8 Conversion result comparison upper limit setting register (ADUL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 8 Conversion result comparison upper limit setting register (ADUL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 9 Conversion result comparison lower limit setting register (ADLL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 9 Conversion result comparison lower limit setting register (ADLL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 3. 10 A/D test register (ADTES)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **11. 3. 10 A/D test register (ADTES)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 11. 3. 11 Registers controlling port function of analog input pins

Set up the registers for controlling the functions of the ports shared with the analog input pins of the A/D converter (port mode registers (PMxx), port mode control registers (PMCxx), and A/D port configuration register (ADPC)).

For details, see as follows.

- **3. 4. 3. 1 Port mode registers (PMxx)**
- **3. 4. 3. 6 Port mode control registers (PMCxx)**
- **3. 4. 3. 7 A/D port configuration register (ADPC)**

For details of setting example, see **11. 3. 11 Registers controlling port function of analog input pins** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 4 A/D converter conversion operations

See **11. 4 A/D Converter Conversion Operations** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 5 Input voltage and conversion results

See **11. 5 Input Voltage and Conversion Results** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 6 A/D converter operation modes

See **11. 6 A/D Converter Operation Modes** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 7 A/D converter setup flowchart

See **11. 7 A/D Converter Setup Flowchart** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 8 SNOOZE mode function

See **11. 8 SNOOZE Mode Function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 9 How to read A/D converter characteristics table

See **11. 9 How to Read A/D Converter Characteristics Table** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 11. 10 Cautions for A/D converter

See **11. 10 Cautions for A/D Converter** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12 Serial Array Unit

Serial array unit 0 has four serial channels, and serial array unit 1 has two. Each channel can achieve 3-wire serial (CSI), UART, and simplified I^2C communication.

Function assignment of each channel supported by the RL78/G1E (64-pin products, 80-pin products) is as shown below.

- 64-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	–	UART1	–
	3	–		–
1	0	–	UART2	–
	1	CSI21 Note	(LIN-bus supported)	–

Note Connected to the pins of the chip of analog block inside the package.

- 80-pin products

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	IIC00
	1	–		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	CSI21 Note	(LIN-bus supported)	–

Note Connected to the pins of the chip of analog block inside the package.

When “UART0” is used for channels 0 and 1 of unit 0, CSI00 cannot be used, but CSI10, UART1, or IIC10 of channel 2 or 3 can be used.

Caution Most of the descriptions in this section use the units and channels of the 80-pin products as an example.

3. 12. 1 Functions of serial array unit

Each serial interface supported by the RL78/G1E (64-pin products, 80-pin products) has the following features.

3. 12. 1. 1 3-wire serial I/O (CSI00, CSI10, CSI20, CSI21)

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **3. 12. 5 Operation of 3-Wire serial I/O (CSI00, CSI10, CSI20, CSI21) Communication**.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate During master communication (CSI00): Max. $f_{CLK}/2$[Note]
  During master communication (other than CSI00): Max. $f_{CLK}/4$[Note]
  During slave communication: Max. $f_{MCK}/6$[Note]

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

In addition, CSI00 of following channels supports the SNOOZE mode. When SCK input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only CSI00 can be specified for asynchronous reception.

Note Use the clocks within a range satisfying the SCK cycle time (t_{KCY}) characteristics (see **CHAPTER 5 ELECTRICAL SPECIFICATIONS**).

3. 12. 1. 2 UART (UART0 to UART2)

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit with an external interrupt (INTP0).

For details about the settings, see **3. 12. 6 Operation of UART (UART0 to UART2) Communication**.

[Data transmission/reception]

- Data length of 7, 8, or 9 bits [Note]
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

In addition, UARTs of following channels support the SNOOZE mode. When RxD input is detected while in the STOP mode, the SNOOZE mode makes data reception that does not require the CPU possible. Only UART0 can be specified for asynchronous reception.

The LIN-bus is accepted in UART2 (0 and 1 channels of unit 1).

[LIN-bus functions]

- Wakeup signal detection
- Sync break field (SBF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit

Note Only UART0 can be specified for the 9-bit data length.

3. 12. 1. 3 Simplified I²C (IIC00, IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function Note and ACK detection function
- Data length of 8 bits

(When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)

- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error), or overrun error

[Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. For details, see **3. 12. 8 Operation of simplified I²C (IIC00, IIC10, IIC20)**.

3. 12. 2 Configuration of serial array unit

The serial array unit includes the following hardware.

Table 3-12. Configuration of Serial Array Unit

Item	Configuration
Shift register	8 bits or 9 bits[Note 1]
Buffer register	Lower 8 bits or 9 bits of serial data register mn (SDRmn)[Notes 1, 2]
<R> Serial clock I/O	SCK00, SCK10, SCK20, SCK21 pins (for 3-wire serial I/O), SCL00, SCL10, SCL20, SCL21 pins (for simplified I^2C)
Serial data input	SI00, SI10, SI20, SI21 pins (for 3-wire serial I/O), RxD0, RxD1 pins (for UART), RxD2 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO10, SO20, SO21 pins (for 3-wire serial I/O), TxD0, TxD1 pins (for UART), TxD2 pin (for UART supporting LIN-bus), output controller
Serial data I/O	SDA00, SDA10, SDA20 pins (for simplified I^2C)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Serial standby control register m (SSCm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn)
	• Port input mode registers 0, 1 (PIM0, PIM1) • Port output mode registers 0, 1 (POM0, POM1) • Port mode registers 0, 1, 7 (PM0, PM1, PM7) • Port registers 0, 1, 7 (P0, P1, P7)

(**Notes** and **Remark** are on the next page.)

Notes 1. The number of bits used as the shift register and buffer register differs depending on the unit and channel.

- mn = 00, 01: lower 9 bits
- Other than above: lower 8 bits

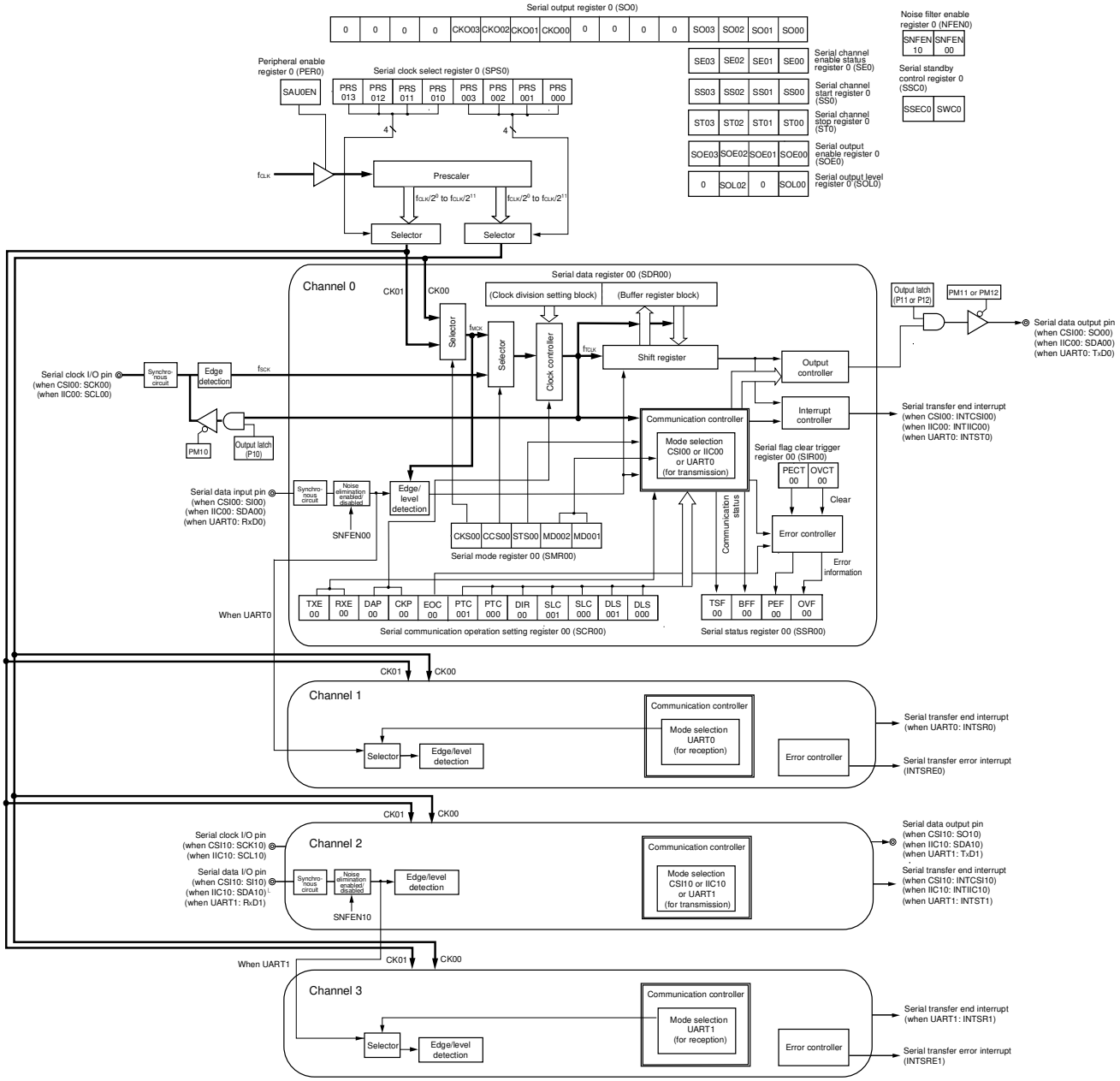
2. The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

Remark m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

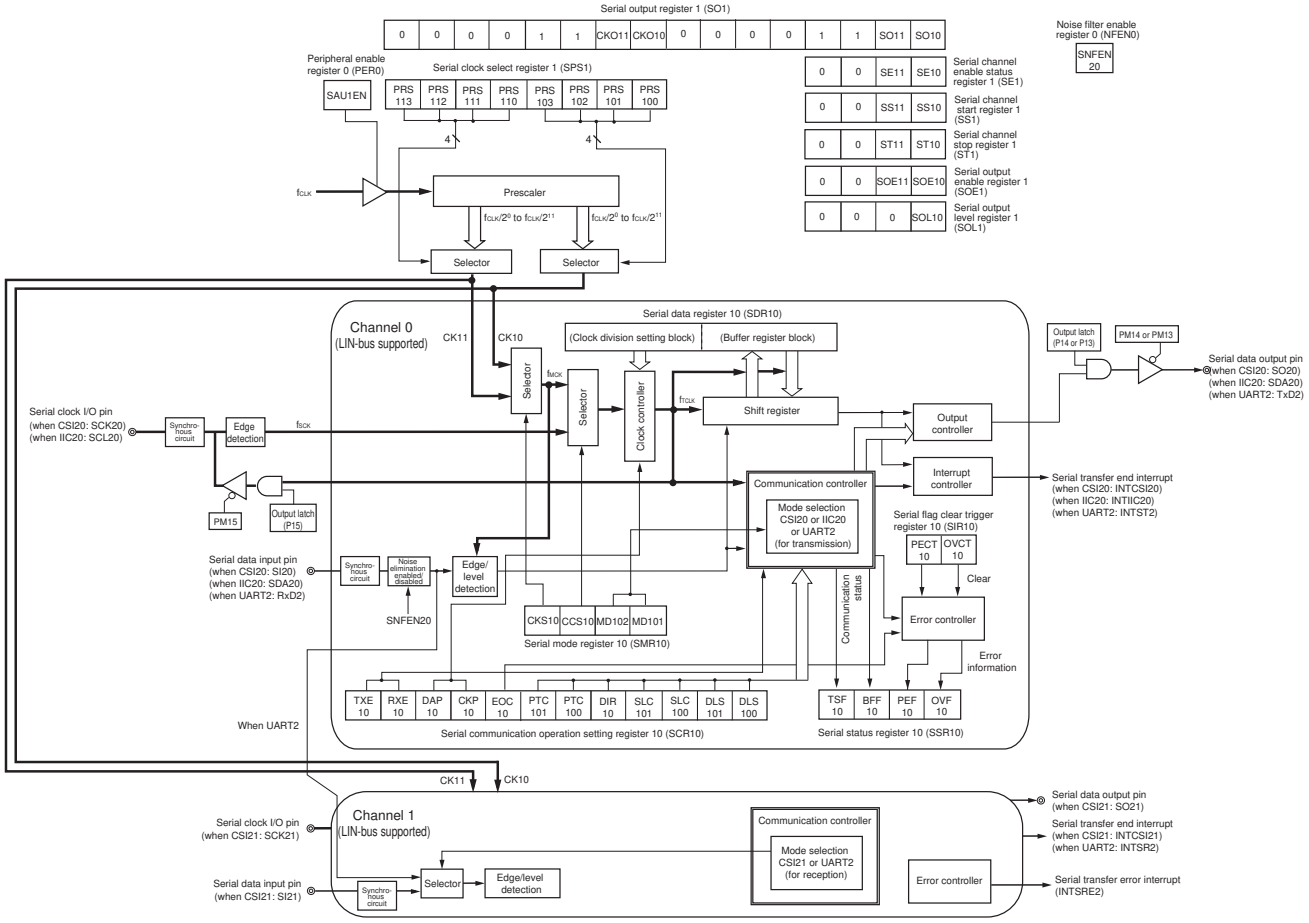
<R> Figure 3-9 shows the block diagram of the serial array unit 0.

Figure 3-9. Block Diagram of Serial Array Unit 0



<R> Figure 3-10 shows the block diagram of the serial array unit 1.

Figure 3-10. Block Diagram of Serial Array Unit 1



<R> 3. 12. 2. 1 Shift register

This is a 9-bit register that converts parallel data into serial data or vice versa.

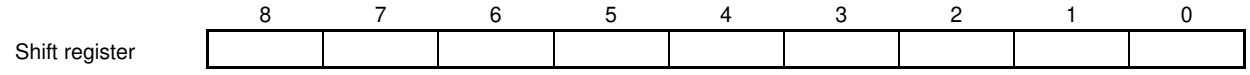
In case of the UART communication of nine bits of data, nine bits (bits 0 to 8) are used[Note 1].

The shift register cannot be directly manipulated by program.

During reception, it converts data input to the serial pin into parallel data, and stores to the lower 8/9 bits of the SDRmn register.

When data is transmitted, the value transferred from the lower 8/9 bits of the SDRmn register to this register is output as serial data from the serial output pin.

For details, see **3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)**.



<R> 3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 8 to 0 of SDR00, SDR01 (lower 9 bits) or bits 7 to 0 of SDR02, SDR03, SDR10Note 1, and SDR11Note 1 (lower 8 bits) function as a transmit/receive buffer register, and bits 15 to 9 (higher 7 bits) are used as a register that sets the division ratio of the operation clock (f_{MCK}).

Remark For the function of the higher 7 bits of the SDRmn register, see **12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

When data is received, parallel data converted by the shift register is stored in the lower 8/9 bits. When data is to be transmitted, set transmit to be transferred to the shift register to the lower 8/9 bits.

The data stored in the lower 8/9 bits of this register is as follows, depending on the setting of bits 0 and 1 (DLSmn0, DLSmn1) of serial communication operation setting register mn (SCRmn), regardless of the output sequence of the data.

- 7-bit data length (stored in bits 0 to 6 of SDRmn register)
- 8-bit data length (stored in bits 0 to 7 of SDRmn register)
- 9-bit data length (stored in bits 0 to 8 of SDRmn register)[Note 1]

The SDRmn register can be read or written in 16-bit units.

The lower 8/9 bits of the SDRmn register can be read or written[Note 2] as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

The SDRmn register can be read or written in 16-bit units.

Reset signal generation clears the SDRmn register to 0000H.

Notes 1. Only following UART0 can be specified for the 9-bit data length.

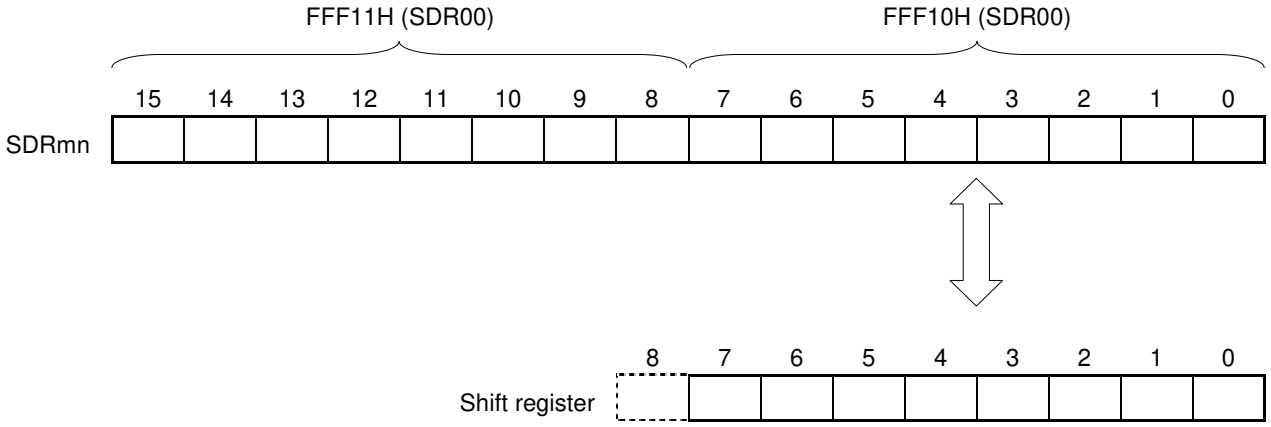
2. Writing in 8-bit units is prohibited when the operation is stopped (SEmn = 0).

Remarks 1. After data is received, "0" is stored in bits 0 to 8 in bit portions that exceed the data length.

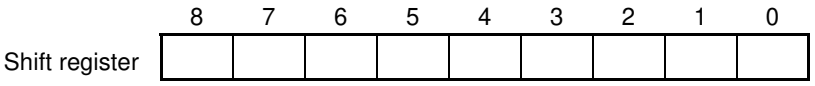
2. m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

<R> **Figure 3-11. Format of Serial Data Register mn (SDRmn) (mn = 00, 01, 02, 03, 10, 11)**

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01) After reset: 0000H R/W
FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03),
FFF48H, FFF49H (SDR10)Note, FFF4AH, FFF4BH (SDR11)Note



- For 9-bit data communication with UART0 (mn = 00, 01)



Caution For 9-bit data communication, be sure to clear bit 8 of the SDRmn register to "0".

<R> **3. 12. 3 Registers controlling serial array unit**

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **12. 3 Registers Controlling Serial Array Unit** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 1 Peripheral enable register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	4	<3>	<2>	1	<0>
PER0	RTCEN	0	ADCEN	0	SAU1EN	SAU0EN	0	TAU0EN

SAU1EN	Control of serial array unit 1 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 1 cannot be written. • The serial array unit 1 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 1 can be read/written.

<R>

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be read/written.

<R>

Caution Be sure to clear bits 1, 4, and 6 to "0".

3. 12. 3. 2 Serial clock select register m (SPSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 2 Serial clock select register m (SPSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 3 Serial mode register mn (SMRmn)

- Setting of serial mode register mn (SMRmn) (1/2)

<R> Address: F0110H, F0111H (SMR00) - F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10), F0152H, F0153H (SMR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn[Note]	0	SIS mn0[Note]	1	0	0	MD mn2	MD mn1	MD mn0

CKSmn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

CCSmn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the SCKp pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STSmn[Note]	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to "0". Be sure to set bit 5 to "1".

Remark m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

- Setting of serial mode register mn (SMRmn) (2/2)

<R> Address: F0110H, F0111H (SMR00) - F0116H, F0117H (SMR03), After reset: 0020H R/W
F0150H, F0151H (SMR10), F0152H, F0153H (SMR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn[Note]	0	SIS mn0[Note]	1	0	0	MD mn2	MD mn1	MD mn0

SISmn0[Note]	Controls inversion of level of receive data of channel n in UART mode
0	Falling edge is detected as the start bit. The input communication data is captured as is.
1	Rising edge is detected as the start bit. The input communication data is inverted and captured.

MDmn2	MDmn1	Setting of operation mode of channel n
0	0	CSI mode
0	1	UART mode
1	0	Simplified I^2C mode
1	1	Setting prohibited

MDmn0	Selection of interrupt source of channel n
0	Transfer end interrupt
1	Buffer empty interrupt (Occurs when data is transferred from the SDRmn register to the shift register.)
For successive transmission, the next transmit data is written by setting the MDmn0 bit to 1 when SDRmn data has run out.	

Note The SMR01, SMR03, and SMR11 registers only.

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 (or bits 13 to 6, 4, and 3 for the SMR00, SMR02, or SMR10 register) to "0". Be sure to set bit 5 to "1".

Remark m: Unit number (m = 0, 1)
n: Channel number (n = 0 to 3)
p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)
q: UART number (q = 0 to 2)
r: IIC number (80-pin products: r = 00, 10, 20 64-pin products: r = 00)

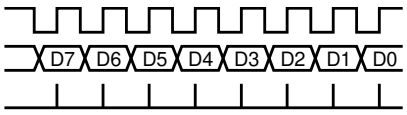
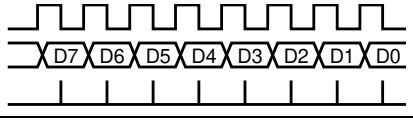
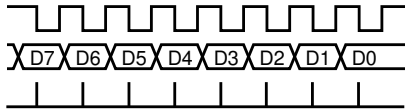
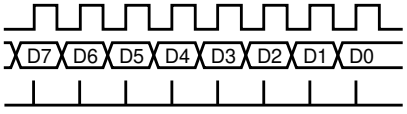
3. 12. 3. 4 Serial communication operation setting register mn (SCRmn)

- Setting of serial communication operation setting register mn (SCRmn) (1/2)

<R> Address: F0118H, F0119H (SCR00) - F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXEmn	RXEmn	DAPmn	CKPmn	0	EOCmn	PTCmn1	PTCmn0	DIRmn	0	SLCmn1 Note 1	SLCmn0	0	1	DLSmn1 Note 2	DLSmn0

TXEmn	RXEmn	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAPmn	CKPmn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I^2C mode.			

EOCmn	Selection of masking of error interrupt signal (INTSREx (x = 0 to 2))
0	Masks error interrupt INTSREx (INTSRx is not masked).
1	Enables generation of error interrupt INTSREx (INTSRx is masked if an error occurs).
Set EOCmn = 0 in the CSI mode, simplified I^2C mode, and during UART transmission Note 3. Set EOCmn = 1 during UART reception.	

(**Notes**, **Caution** and **Remark** are on the next page.)

<R> **Notes 1.** The SCR00, SCR02, and SCR10 registers only. Others are fixed to 0.

2. The SCR00 and SCR01 registers only. Others are fixed to 1.

3. When using CSImn not with EOCmn = 0, error interrupt INTSRE0 may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)

• Setting of serial communication operation setting register mn (SCRmn) (2/2)

<R> Address: F0118H, F0119H (SCR00) - F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10), F015AH, F015BH (SCR11)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1 Note 1	SLC mn0	0	1	DLS mn1 Note 2	DLS mn0

PTCmn1	PTCmn0	Setting of parity bit in UART mode	
		Transmission	Reception
0	0	Does not output the parity bit.	Receives without parity
0	1	Outputs 0 parity Note 3.	No parity judgment
1	0	Outputs even parity.	Judged as even parity.
1	1	Outputs odd parity.	Judges as odd parity.
Be sure to set PTCmn1, PTCmn0 = 0, 0 in the CSI mode and simplified I^2C mode.			

DIRmn	Selection of data transfer sequence in CSI and UART modes
0	Inputs/outputs data with MSB first.
1	Inputs/outputs data with LSB first.
Be sure to clear DIRmn = 0 in the simplified I^2C mode.	

SLCmn1 Note 1	SLCmn0	Setting of stop bit in UART mode
0	0	No stop bit
0	1	Stop bit length = 1 bit
1	0	Stop bit length = 2 bits (mn = 00, 02, 10 only)
1	1	Setting prohibited
When the transfer end interrupt is selected, the interrupt is generated when all stop bits have been completely transferred. Set 1 bit (SLCmn1, SLCmn0 = 0, 1) during UART reception and in the simplified I^2C mode. Set no stop bit (SLCmn1, SLCmn0 = 0, 0) in the CSI mode.		

DLSmn1 Note 2	DLSmn0	Setting of data length in CSI and UART modes
0	1	9-bit data length (stored in bits 0 to 8 of the SDRmn register) (settable in UART mode only)
1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above		Setting prohibited
Be sure to set DLSmn1, DLSmn0 = 1, 1 in the simplified I^2C mode.		

(**Notes**, **Caution** and **Remark** are on the next page.)

Notes 1. The SCR00, SCR02, and SCR10 registers only.

2. The SCR00 and SCR01 registers only. Others are fixed to 1.

3. 0 is always added regardless of the data contents.

Caution Be sure to clear bits 3, 6, and 11 to "0". (Also clear bit 5 of the SCR01, SCR03, or SCR11 register to 0, as well as bit 1 of the SCR02, SCR03, SCR10, SCR11 registers). Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0, 1)

n: Channel number (n = 0 to 3)

p: CSI number (80-pin products: p = 00, 10, 20, 21 64-pin products: p = 00, 21)

3. 12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 5 Higher 7 bits of the serial data register mn (SDRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 6 Serial flag clear trigger register mn (SIRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 6 Serial flag clear trigger register mn (SIRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 7 Serial status register mn (SSRmn)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 7 Serial status register mn (SSRmn)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 8 Serial channel start register m (SSm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 8 Serial channel start register m (SSm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 9 Serial channel stop register m (STm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 9 Serial channel stop register m (STm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 10 Serial channel enable status register m (SEm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 10 Serial channel enable status register m (SEm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 11 Serial output enable register m (SOEm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 11 Serial output enable register m (SOEm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 12 Serial output register m (SOm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 12 Serial output register m (SOm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 13 Serial output level register m (SOLm)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 13 Serial output level register m (SOLm)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 14 Serial standby control register 0 (SSC0)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 14 Serial standby control register 0 (SSC0)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 15 Input switch control register (ISC)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 15 Input switch control register (ISC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 3. 16 Noise filter enable register 0 (NFEN0)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **12. 3. 16 Noise filter enable register 0 (NFEN0)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> 3. 12. 3. 17 Registers controlling port functions of serial input/output pins

Using the serial array unit requires setting of the registers that control the port functions multiplexed on the target channel (port mode register (PMxx), port register (Pxx), port input mode register (PIMxx), port output mode register (POMxx), port mode control register (PMCxx)).

For details, see **3. 4. 3. 1 Port mode registers (PMxx)**, **3. 4. 3. 2 Port registers (Pxx)**, **3. 4. 3. 4 Port input mode registers (PIMxx)**, **3. 4. 3. 5 Port output mode registers (POMxx)**, and **3. 4. 3. 6 Port mode control registers (PMCxx)**.

For details of setting example, see **12. 3. 17 Registers controlling port functions of serial Input/output pins** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 4 Operation stop mode

See **12. 4 Operation Stop Mode** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 5 Operation of 3-Wire serial I/O (CSI00, CSI10, CSI20, CSI21) communication

See **12. 5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21) Communication** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 6 Operation of UART (UART0 to UART2) communication

See **12. 6 Operation of UART (UART0 to UART2) Communication** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 7 LIN communication operation

See **12. 7 LIN Communication Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 12. 8 Operation of simplified I^2C (IIC00, IIC10, IIC20) communication

See **12. 8 Operation of Simplified I^2C (IIC00, IIC01, IIC10, IIC11, IIC20, IIC21) Communication** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 13 Serial Interface IICA

Serial interface IICA is not provided in RL78/G1E (64-pin products, 80-pin products).

3. 14 Multiplier and Divider/Multiply-Accumulator

See **CHAPTER 14 MULTIPLIER AND DIVIDER/MULTIPLY-ACCUMULATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 15 DMA Controller

See **CHAPTER 15 DMA CONTROLLER** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 16 Interrupt Functions

The interrupt function switches the program execution to other processing. When the branch processing is finished, the program returns to the interrupted processing. The number of interrupt sources differs, depending on the product.

		64-pin products	80-pin products
Maskable interrupts	External	2	5
	Internal	25	

3. 16. 1 Interrupt function types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the default priority of vectored interrupt servicing. Default priority, see **Table 3-13**.

A standby release signal is generated and STOP, HALT, and SNOOZE modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

3. 16. 2 Interrupt sources and configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to seven reset sources (see **Table 3-13**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

Table 3-13. Interrupt Source List (1/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	0	INTWDTI	Watchdog timer interval[Note 3] (75% of overflow time + 1/2f_{IL})	Internal	0004H	(A)	√	√
	1	INTLVI	Voltage detection[Note 4]		0006H		√	√
	2	INTP0	Pin input edge detection	External	0008H	(B)	√	√
	3	INTP1			000AH		–	√
	4	INTP2			000CH		–	√
	5	INTP3			000EH		–	–
	6	INTP4			0010H		–	–
	7	INTP5			0012H		–	–
	8	INTST2/ INTCSI20/ INTIIC20	UART2 transmission transfer end or buffer empty interrupt/ CSI20 transfer end or buffer empty interrupt/ IIC20 transfer end	Internal	0014H	(A)	√[Note 5]	√
	9	INTSR2/ INTCSI21/ INTIIC21	UART2 reception transfer end or buffer empty interrupt/ CSI21 transfer end or buffer empty interrupt/ IIC21 transfer end		0016H		√[Note 6]	√[Note 6]
	10	INTSRE2	UART2 reception communication error occurrence		0018H		√	√
	11	INTDMA0	End of DMA0 transfer		001AH		√	√
	12	INTDMA1	End of DMA1 transfer		001CH		√	√
	13	INTST0/ INTCSI00/ INTIIC00	UART0 transmission transfer end or buffer empty interrupt/ CSI00 transfer end or buffer empty interrupt/ IIC00 transfer end		001EH		√	√
	14	INTSR0/ INTCSI01/ INTIIC01	UART0 reception transfer end or buffer empty interrupt/ CSI01 transfer end or buffer empty interrupt/ IIC01 transfer end		0020H		√[Note 7]	√[Note 7]
	15	INTSRE0	UART0 reception communication error occurrence		0022H		√	√
<R>		INTTM01H	End of timer channel 1 count or capture (at higher 8-bit timer operation)				√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 53 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

3. When bit 7 (WDTINT) of the option byte (000C0H) is set to 1.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is cleared to 0.

5. INTST2 only.

6. INTSR2 and INTCSI21 only.

7. INTSR0 only.

Table 3-13. Interrupt Source List (2/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	16	INTST1/ INTCSI10/ INTIIC10	UART1 transmission transfer end or buffer empty interrupt/ CSI10 transfer end or buffer empty interrupt/ IIC10 transfer end	Internal	0024H	(A)	√[Note 3]	√
	17	INTSR1/ INTCSI11/ INTIIC11	UART1 reception transfer end/ CSI11 transfer end or buffer empty interrupt/ IIC11 transfer end		0026H		√[Note 4]	√[Note 4]
	18	INTSRE1	UART1 reception communication error occurrence		0028H		√	√
<R>		INTTM03H	End of timer channel 3 count or capture (at higher 8-bit timer operation)				√	√
	19	INTIICA0	End of IICA0 communication		002AH		–	–
	20	INTTM00	End of timer channel 0 count or capture		002CH		√	√
<R>	21	INTTM01	End of timer channel 1 count or capture (at 16-bit/lower 8-bit timer operation)		002EH		√	√
	22	INTTM02	End of timer channel 2 count or capture		0030H		√	√
<R>	23	INTTM03	End of timer channel 3 count or capture (at 16-bit/lower 8-bit timer operation)		0032H		√	√
	24	INTAD	End of A/D conversion		0034H		√	√
	25	INTRTC	Fixed-cycle signal of real-time clock/alarm match detection		0036H		–	–
	26	INTIT	Interval signal of 12-bit interval timer detection		0038H		√	√
	27	INTKR	Key return signal detection	External	003AH	(C)	√	√
	28	INTTM04	End of timer channel 4 count or capture	Internal	0042H	(A)	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

3. INTST1 only.

4. INTSR1 only.

Table 3-13. Interrupt Source List (3/3)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]	RL78/G1E	
		Name	Trigger				64-pin	80-pin
Maskable	29	INTTM05	End of timer channel 5 count or capture	Internal	0044H	(A)	√	√
	30	INTTM06	End of timer channel 6 count or capture		0046H		√	√
	31	INTTM07	End of timer channel 7 count or capture		0048H		√	√
	32	INTP6	Pin input edge detection	External	004AH	(B)	–	√
	33	INTP7			004CH		–	–
	34	INTP8			004EH		–	–
	35	INTP9			0050H		–	–
	36	INTP10			0052H		–	–
	37	INTP11			0054H		–	–
<R>	38	INTMD	End of division operation/Overflow of multiplyaccumulation result occurs	Internal	005EH	(A)	√	√
	39	INTFL	Reserved[Note 3]		0062H		√	√
Software	–	BRK	Execution of BRK instruction	–	007EH	(D)	√	√
Reset	–	RESET	$\overline{\text{RESET}}$ pin input	–	0000H	–	√	√
		POR	Power-on-reset				√	√
		LVD	Voltage detection[Note 4]				√	√
		WDT	Overflow of watchdog timer				√	√
		TRAP	Execution of illegal instruction[Note 5]				√	√
		IAW	Illegal-memory access				√	√
		RAMTOP	RAM parity error				√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 39 indicates the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 3-13.

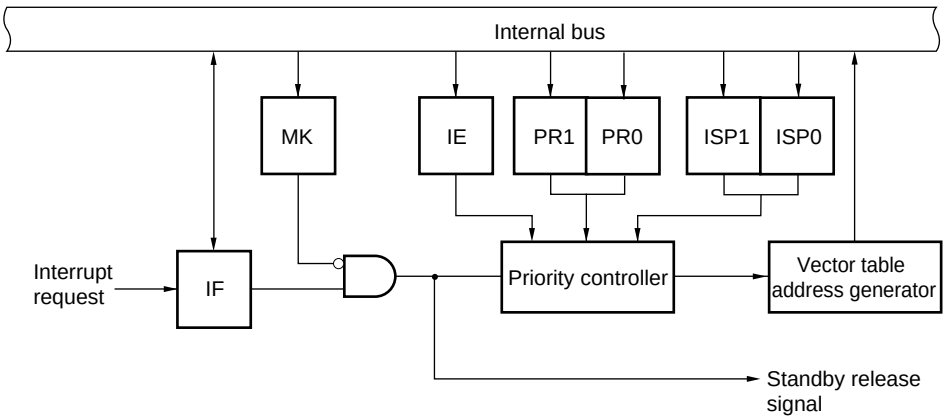
<R> **3.** Be used at the flash self programming library or the data flash library.

4. When bit 7 (LVIMD) of the voltage detection level register (LVIS) is set to 1.

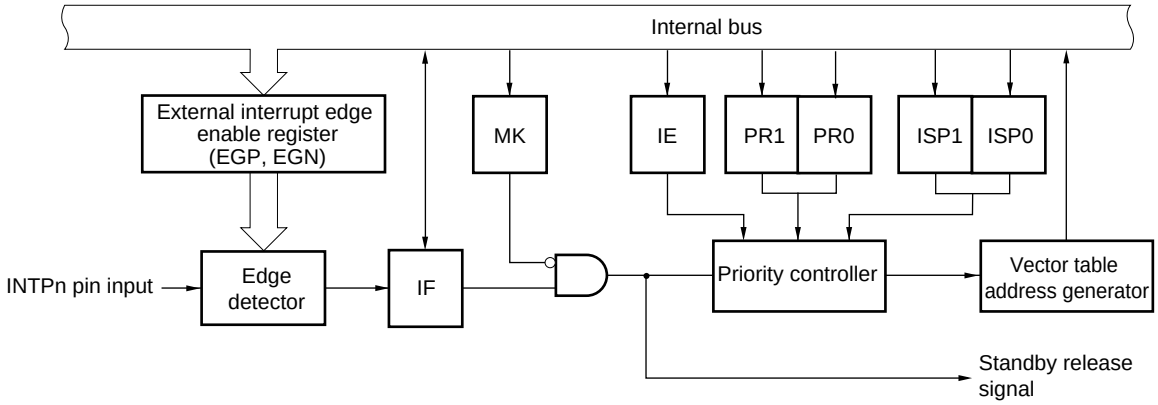
5. When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Figure 3-13. Basic Configuration of Interrupt Function (1/2)

(a) Internal maskable interrupt



(b) External maskable interrupt (INTPn)

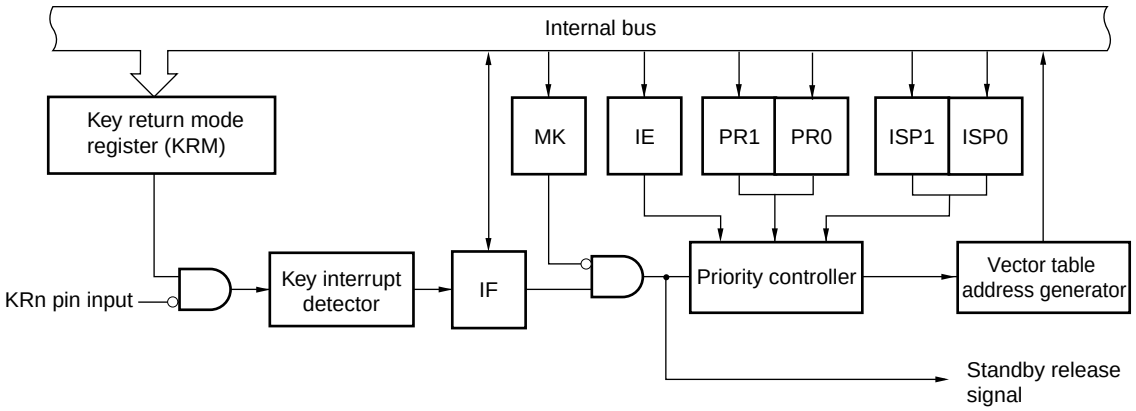


IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

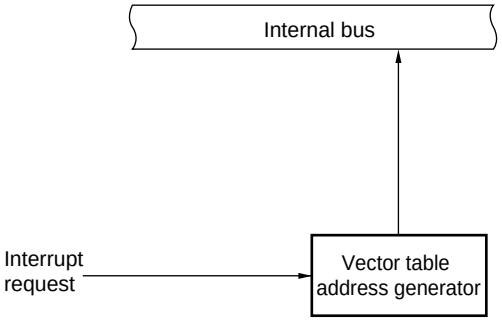
Remark 64-pin products: n = 0
80-pin products: n = 0 to 3, 6

Figure 3-13. Basic Configuration of Interrupt Function (2/2)

(c) External maskable interrupt (INTKR)



(d) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP0: In-service priority flag 0
ISP1: In-service priority flag 1
MK: Interrupt mask flag
PR0: Priority specification flag 0
PR1: Priority specification flag 1

Remark 64-pin products: n = 0 to 6
80-pin products: n = 0 to 7

3. 16. 3 Registers controlling interrupt functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag register (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
- Program status word (PSW)

Table 3-14 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 3-14. Flags Corresponding to Interrupt Request Sources (1/4)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag		RL78/G1E	
		Register		Register		Register	64-pin	80-pin
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L	√	√
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1		√	√
INTP0	PIF0		PMK0		PPR00, PPR10		√	√
INTP1	PIF1		PMK1		PPR01, PPR11		–	√
INTP2	PIF2		PMK2		PPR02, PPR12		–	√
INTP3	PIF3		PMK3		PPR03, PPR13		–	–
INTP4	PIF4		PMK4		PPR04, PPR14		–	–
INTP5	PIF5		PMK5		PPR05, PPR15		–	–
INTST2[Note 1]	STIF2[Note 1]	IF0H	STMK2[Note 1]	MK0H	STPR02, STPR12[Note 1]	PR00H, PR10H	√	√
INTCSI20[Note 1]	CSIIF20[Note 1]		CSIMK20[Note 1]		CSIPR020, CSIPR120[Note 1]		–	√
INTIIC20[Note 1]	IICIF20[Note 1]		IICMK20[Note 1]		IICPR020, IICPR120[Note 1]		–	√
INTSR2[Note 2]	SRIF2[Note 2]		SRMK2[Note 2]		SRPR02, SRPR12[Note 2]		–	√
INTCSI21[Note 2]	CSIIF21[Note 2]		CSIMK21[Note 2]		CSIPR021, CSIPR121[Note 2]		√	√
INTIIC21[Note 2]	IICIF21[Note 2]		IICMK21[Note 2]		IICPR021, IICPR121[Note 2]		–	–

Notes 1. If one of the interrupt sources INTST2, INTCSI20, and INTIIC20 is generated, bit 0 of the IF0H register is set to 1. Bit 0 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR2, INTCSI21, and INTIIC21 is generated, bit 1 of the IF0H register is set to 1. Bit 1 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

Table 3-14. Flags Corresponding to Interrupt Request Sources (2/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTSRE2	SREIF2	IF0H	SREMK2	MK0H	SREPR02, SREPR12	PR00H, PR10H	√	√
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10		√	√
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11		√	√
INTST0Note 1	STIF0Note 1		STMK0Note 1		STPR00, STPR10Note 1		√	√
INTCSI00Note 1	CSIIF00Note 1		CSIMK00Note 1		CSIPR000, CSIPR100Note 1		√	√
INTIIC00Note 1	IICIF00Note 1		IICMK00Note 1		IICPR000, IICPR100Note 1		√	√
INTSR0Note 2	SRIF0Note 2		SRMK0Note 2		SRPR00, SRPR10Note 2		√	√
INTCSI01Note 2	CSIIF01Note 2		CSIMK01Note 2		CSIPR001, CSIPR101Note 2		–	–
INTIIC01Note 2	IICIF01Note 2		IICMK01Note 2		IICPR001, IICPR101Note 2		–	–
INTSRE0Note 3	SREIF0Note 3		SREMK0Note 3		SREPR00, SREPR10Note 3		√	√
INTTM01HNote 3	TMIF01HNote 3		TMMK01HNote 3		TMPR001H, TMPR101HNote 3		√	√

Notes 1. If one of the interrupt sources INTST0, INTCSI00, and INTIIC00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR0, INTCSI01, and INTIIC01 is generated, bit 6 of the IF0H register is set to 1. Bit 6 of the MK0H, PR00H, and PR10H registers can be used for all three of these interrupt sources.

<R> **3.** Do not use the error interrupt of UART0 reception and the interrupt of channel 1 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART0 reception is not used (EOC01 = 0), UART0 and channel 1 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE0 or INTTM01H is generated, bit 7 of the IF0H register is set to 1. Bit 7 of the MK0H, PR00H, and PR10H registers can be used for both these interrupt sources.

Table 3-14. Flags Corresponding to Interrupt Request Sources (3/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTST1[Note 1]	STIF1[Note 1]	IF1L	STMK1[Note 1]	MK1L	STPR01, STPR11[Note 1]	PR01L, PR11L	√	√
INTCSI10[Note 1]	CSIIF10[Note 1]		CSIMK10[Note 1]		CSIPR010, CSIPR110[Note 1]		–	√
INTIIC10[Note 1]	IICIF10[Note 1]		IICMK10[Note 1]		IICPR010, IICPR110[Note 1]		–	√
INTSR1[Note 2]	SRIF1[Note 2]		SRMK1[Note 2]		SRPR01, SRPR11[Note 2]		√	√
INTCSI11[Note 2]	CSIIF11[Note 2]		CSIMK11[Note 2]		CSIPR011, CSIPR111[Note 2]		–	–
INTIIC11[Note 2]	IICIF11[Note 2]		IICMK11[Note 2]		IICPR011, IICPR111[Note 2]		–	–
INTSRE1[Note 3]	SREIF1[Note 3]		SREMK1[Note 3]		SREPR01, SREPR11[Note 3]		√	√
INTTM03H[Note 3]	TMIF03H[Note 3]		TMMK03H[Note 3]		TMPR003H, TMPR103H[Note 3]		√	√
INTIICA0	IICAIF0		IICAMK0		IICAPR00, IICAPR10		–	–
INTTM00	TMIF00		TMMK00		TMPR000, TMPR100		√	√
INTTM01	TMIF01		TMMK01		TMPR001, TMPR101		√	√
INTTM02	TMIF02		TMMK02		TMPR002, TMPR102		√	√
INTTM03	TMIF03		TMMK03		TMPR003, TMPR103		√	√
INTAD	ADIF	IF1H	ADMK	MK1H	ADPR0, ADPR1	PR01H, PR11H	√	√
INTRTC	RTCIF		RTCMK		RTCPR0, RTCPR1		–	–
INTIT	ITIF		ITMK		ITPR0, ITPR1		√	√
INTKR	KRIF		KRMK		KRPR0, KRPR1		√	√
INTTM04	TMIF04		TMMK04		TMPR004, TMPR104		√	√

(**Notes** are on the next page.)

Notes 1. If one of the interrupt sources INTST1, INTCSI10, and INTIIC10 is generated, bit 0 of the IF1L register is set to 1. Bit 0 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

2. If one of the interrupt sources INTSR1, INTCSI11, and INTIIC11 is generated, bit 1 of the IF1L register is set to 1. Bit 1 of the MK1L, PR01L, and PR11L registers can be used for all three of these interrupt sources.

<R> **3.** Do not use the error interrupt of UART1 reception and the interrupt of channel 3 of TAU0 (while the higher 8 bits are operating at a timer) at the same time because they share flags for the interrupt request sources. If the error interrupt of UART1 reception is not used (EOC03 = 0), UART1 and channel 3 of TAU0 (while the higher 8 bits are operating at a timer) can be used at the same time. If the interrupt source INTSRE1 or INTTM03H is generated, bit 2 of the IF1L register is set to 1. Bit 2 of the MK1L, PR01L, and PR11L registers can be used for both these interrupt sources.

Table 3-14. Flags Corresponding to Interrupt Request Sources (4/4)

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register	RL78/G1E 64-pin	RL78/G1E 80-pin
INTTM05	TMIF05	IF2L	TMMK05	MK2L	TMPR005, TMPR105	PR02L, PR12L	√	√
INTTM06	TMIF06		TMMK06		TMPR006, TMPR106		√	√
INTTM07	TMIF07		TMMK07		TMPR007, TMPR107		√	√
INTP6	PIF6		PMK6		PPR06, PPR16		–	√
INTP7	PIF7		PMK7		PPR07, PPR17		–	–
INTP8	PIF8		PMK8		PPR08, PPR18		–	–
INTP9	PIF9		PMK9		PPR09, PPR19		–	–
INTP10	PIF10		PMK10		PPR010, PPR110		–	–
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H	–	–
INTMD	MDIF		MDMK		MDPR0, MDPR1		√	√
INTFL	FLIF		FLMK		FLPR0, FLPR1		√	√

The bit settings which are different from that of RL78/G1A (64-pin products) are shown on the next page. For details of each register, see **16. 3 Registers Controlling Interrupt Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **16. 3 Registers Controlling Interrupt Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 16. 3. 1 Interrupt request flag register (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)

- 64-pin products

Address: FFFE0H After reset: 00H R/W

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
IF0L	0	0	0	0	0	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF01H SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2	SRIF2 CSIIF21	STIF2

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	0	SREIF1 TMIF03H	SRIF1	STIF1

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
IF1H	TMIF04	0	0	0	KRIF	ITIF	0	ADIF

Address: FFFD0H After reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
IF2L	0	0	0	0	0	TMIF07	TMIF06	TMIF05

Address: FFFD1H After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
IF2H	FLIF	0	MDIF	0	0	0	0	0

Cautions 1. Be sure to clear bits 3 to 7 of the IF0L register to "0".

2. Be sure to clear bit 3 of the IF1L register to "0".

3. Be sure to clear bits 1 and 4 to 6 of the IF1H register to "0".

4. Be sure to clear bits 3 to 7 of the IF2L register to "0".

5. Be sure to clear bits 0 to 4 and 6 of the IF2H register to "0".

- 80-pin products

Address: FFFE0H After reset: 00H R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
IF0L	0	0	0	PIF2	PIF1	PIF0	LVIIF	WDTIIF

Address: FFFE1H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IF0H	TMIF01H SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2	SRIF2 CSIIF21	STIF2 CSIIF20 IICIF20

Address: FFFE2H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
IF1L	TMIF03	TMIF02	TMIF01	TMIF00	0	SREIF1 TMIF03H	SRIF1	STIF1 CSIIF10 IICIF10

Address: FFFE3H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
IF1H	TMIF04	0	0	0	KRIF	ITIF	0	ADIF

Address: FFFD0H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
IF2L	0	0	0	0	PIF6	TMIF07	TMIF06	TMIF05

Address: FFFD1H After reset: 00H R/W

Symbol	<7>	6	<5>	4	3	2	1	0
IF2H	FLIF	0	MDIF	0	0	0	0	0

Cautions 1. Be sure to clear bits 5 to 7 of the IF0L register to “0”.

2. Be sure to clear bit 3 of the IF1L register to “0”.

3. Be sure to clear bits 1 and 4 to 6 of the IF1H register to “0”.

4. Be sure to clear bits 4 to 7 of the IF2L register to “0”.

5. Be sure to clear bits 0 to 4 and 6 of the IF2H register to “0”.

3. 16. 3. 2 Interrupt mask flag register (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)

- 64-pin products

Address: FFFE4H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
MK0L	1	1	1	1	1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK01H SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21	STMK2

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	1	SREMK1 TMMK03H	SRMK1	STMK1

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	1	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
MK2L	1	1	1	1	1	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
MK2H	FLMK	1	MDMK	1	1	1	1	1

Cautions 1. Be sure to set bits 3 to 7 of the MK0L register to “1”.

2. Be sure to set bit 3 of the MK1L register to “1”.

3. Be sure to set bits 1 and 4 to 6 of the MK1H register to “1”.

4. Be sure to set bits 3 to 7 of the MK2L register to “1”.

5. Be sure to set bits 0 to 4 and 6 of the MK2H register to “1”.

- 80-pin products

Address: FFFE4H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
MK0L	1	1	1	PMK2	PMK1	PMK0	LVIMK	WDTIMK

Address: FFFE5H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
MK0H	TMMK01H SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2	SRMK2 CSIMK21	STMK2 CSIMK20 IICMK20

Address: FFFE6H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
MK1L	TMMK03	TMMK02	TMMK01	TMMK00	1	SREMK1 TMMK03H	SRMK1	STMK1 CSIMK10 IICMK10

Address: FFFE7H After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
MK1H	TMMK04	1	1	1	KRMK	ITMK	1	ADMK

Address: FFFD4H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK2L	1	1	1	1	PMK6	TMMK07	TMMK06	TMMK05

Address: FFFD5H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
MK2H	FLMK	1	MDMK	1	1	1	1	1

Cautions 1. Be sure to set bits 5 to 7 of the MK0L register to “1”.

2. Be sure to set bit 3 of the MK1L register to “1”.

3. Be sure to set bits 1 and 4 to 6 of the MK1H register to “1”.

4. Be sure to set bits 4 to 7 of the MK2L register to “1”.

5. Be sure to set bits 0 to 4 and 6 of the MK2H register to “1”.

3. 16. 3. 3 Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H, PR02L, PR02H)

- 64-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR00L	1	1	1	1	1	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR10L	1	1	1	1	1	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 CSIPR000 IICPR00	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR02L	1	1	1	1	1	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
PR12L	1	1	1	1	1	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR02H	FLPR0	1	MDPR0	1	1	1	1	1

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR12H	FLPR1	1	MDPR1	1	1	1	1	1

Cautions 1. Be sure to set bits 3 to 7 of the PR00L register to “1”.

2. Be sure to set bits 3 to 7 of the PR10L register to “1”.

3. Be sure to set bit 3 of the PR01L register to “1”.

4. Be sure to set bit 3 of the PR11L register to “1”.

5. Be sure to set bits 1 and 4 to 6 of the PR01H register to “1”.

6. Be sure to set bits 1 and 4 to 6 of the PR11H register to “1”.

7. Be sure to set bits 3 to 7 of the PR02L register to “1”.

8. Be sure to set bits 3 to 7 of the PR12L register to “1”.

9. Be sure to set bits 0 to 4 and 6 of the PR02H register to “1”.

10. Be sure to set bits 0 to 4 and 6 of the PR12H register to “1”.

- 80-pin products

Address: FFFE8H After reset: FFH R/W

Symbol	7	6	5	<4>	<3>	<2>	<1>	<0>
PR00L	1	1	1	PPR02	PPR01	PPR00	LVIPR0	WDTIPR0

Address: FFFECH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR10L	1	1	1	PPR12	PPR11	PPR10	LVIPR1	WDTIPR1

Address: FFFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR00H	TMPR001H SREPR00	SRPR00	STPR00 IICPR000	DMAPR01	DMAPR00	SREPR02	SRPR02 CSIPR021	STPR02 CSIPR020 IICPR020

Address: FFFEDH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR10H	TMPR101H SREPR10	SRPR10	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12	SRPR12 CSIPR121	STPR12 CSIPR120 IICPR120

Address: FFFEAH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR01L	TMPR003	TMPR002	TMPR001	TMPR000	1	SREPR01 TMPR003H	SRPR01	STPR01 CSIPR010 IICPR010

Address: FFFEEH After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	3	<2>	<1>	<0>
PR11L	TMPR103	TMPR102	TMPR101	TMPR100	1	SREPR11 TMPR103H	SRPR11	STPR11 CSIPR110 IICPR110

Address: FFFEBH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR01H	TMPR004	1	1	1	KRPR0	ITPR0	1	ADPR0

Address: FFFEFH After reset: FFH R/W

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
PR11H	TMPR104	1	1	1	KRPR1	ITPR1	1	ADPR1

Address: FFFD8H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR02L	1	1	1	1	PPR06	TMPR007	TMPR006	TMPR005

Address: FFFDCH After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR12L	1	1	1	1	PPR16	TMPR107	TMPR106	TMPR105

Address: FFFD9H After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR02H	FLPR0	1	MDPR0	1	1	1	1	1

Address: FFFDDH After reset: FFH R/W

Symbol	<7>	6	<5>	4	3	2	1	0
PR12H	FLPR1	1	MDPR1	1	1	1	1	1

Cautions 1. Be sure to set bits 5 to 7 of the PR00L register to “1”.

2. Be sure to set bits 5 to 7 of the PR10L register to “1”.

3. Be sure to set bit 3 of the PR01L register to “1”.

4. Be sure to set bit 3 of the PR11L register to “1”.

5. Be sure to set bits 1 and 4 to 6 of the PR01H register to “1”.

6. Be sure to set bits 1 and 4 to 6 of the PR11H register to “1”.

7. Be sure to set bits 4 to 7 of the PR02L register to “1”.

8. Be sure to set bits 4 to 7 of the PR12L register to “1”.

9. Be sure to set bits 4 to 7 of the PR02H register to “1”.

10. Be sure to set bits 0 to 4 and 6 of the PR12H register to “1”.

3. 16. 3. 4 External interrupt rising edge enable register (EGP0), External interrupt falling edge enable register (EGN0)

- 64-pin products

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	0	0	0	0	0	0	0	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	0	0	0	0	0	0	0	EGN0

- 80-pin products

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	0	EGP6	0	0	0	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	0	EGN6	0	0	0	EGN2	EGN1	EGN0

Table 3-15 shows the ports corresponding to the EGPn and EGNn bits.

Table 3-15. Ports Corresponding to EGPn and EGNn Bits

Detection Enable Bit		Edge Detection Port	Interrupt Request Signal	RL78/G1E	
				64-pin	80-pin
EGP0	EGN0	P137	INTP0	√	√
EGP1	EGN1	P50	INTP1	–	√
EGP2	EGN2	P51	INTP2	–	√
EGP6	EGN6	P140	INTP6	–	√

Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 2, 6

3. 16. 3. 5 Program status word (PSW)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **16. 3. 5 Program status word (PSW)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 16. 4 Interrupt servicing operations

See **16. 4 Interrupt Servicing Operations** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17 Key Interrupt Function

The number of key interrupt input channels differs, depending on the product.

	64-pin products	80-pin products
Key interrupt input channels	4 ch (7 ch)	4 ch (8 ch)

Remarks 1. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. Most of the following descriptions in this section use the case of 80-pin products as an example.

3. 17. 1 Functions of key interrupt

A key interrupt (INTKR) can be generated by inputting a rising/falling edge to the key interrupt input pins (KR0 to KR7).

There are two ways to identify the channel(s) to which a valid edge has been input:

- Identify the channel(s) (KR0 to KR7) by using the port input level.
- Identify the channel(s) (KR0 to KR5) by using the key interrupt flag.

Table 3-16. Assignment of Key Interrupt Detection Pins

Key Interrupt Pins	Key return mode register (KRM0)	Key return flag register (KRF)
KR0	KRM00	KRF0
KR1	KRM01	KRF1
KR2	KRM02	KRF2
KR3	KRM03	KRF3
KR4	KRM04	KRF4
KR5	KRM05	KRF5
KR6	KRM06	–
KR7	KRM07	–

Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

3. 17. 2 Configuration of key interrupt

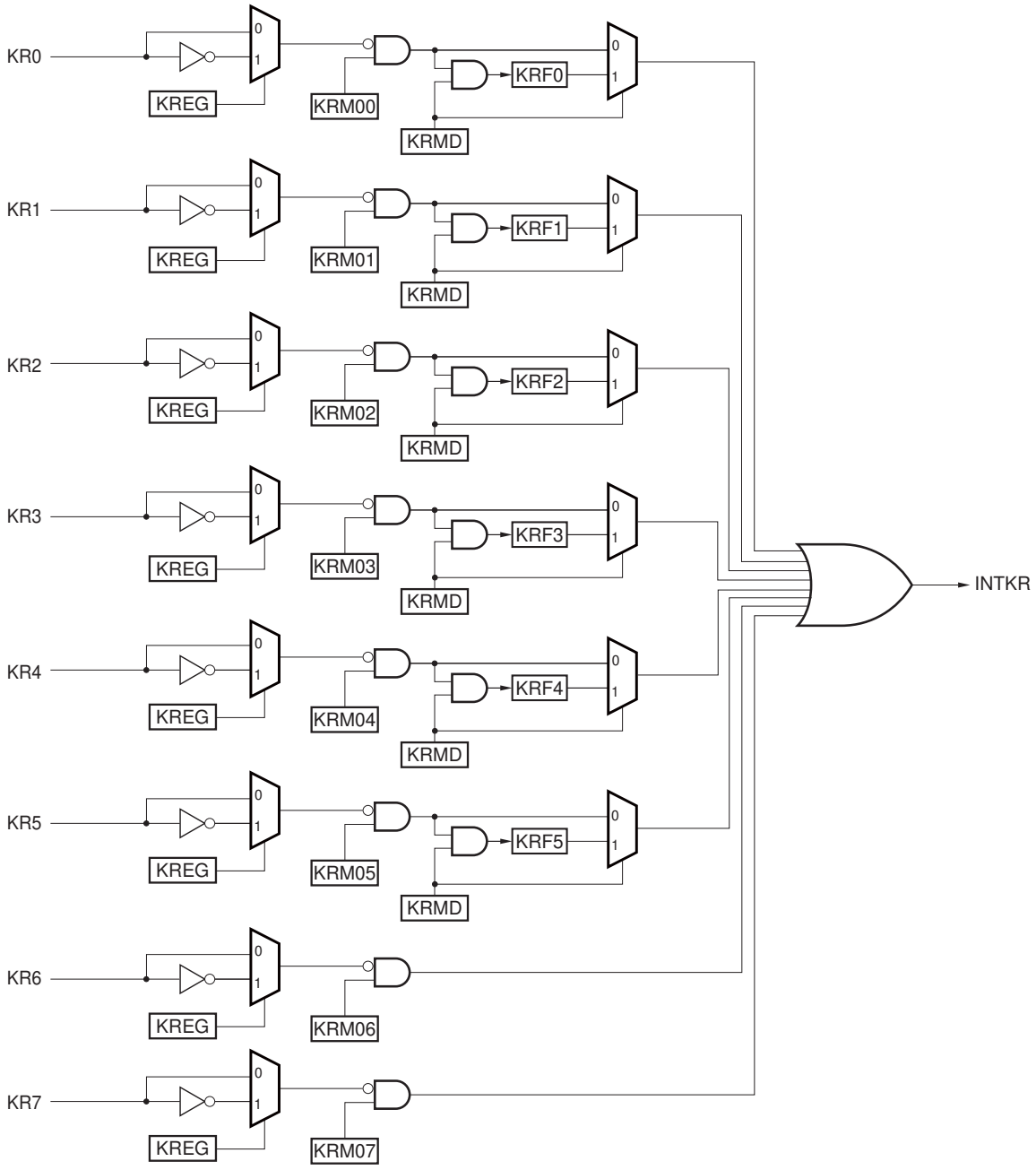
The key interrupt includes the following hardware.

Table 3-17. Configuration of Key Interrupt

Item	Configuration
Control register	Key interrupt control register (KRCTL)
	Key interrupt mode control register 0 (KRM0)
	Key interrupt flag register (KRF)
	Port mode registers 0, 1, 2, 7 (PM0, PM1, PM2, PM7)
	Peripheral I/O redirection register (PIOR)

<R>

Figure 3-14. Block Diagram of Key Interrupt



Remark KR0 to KR3 (KR0 to KR6): 64-pin products
KR0 to KR3 (KR0 to KR7): 80-pin products
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR)

3. 17. 3 Register controlling key interrupt

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **17. 3 Register Controlling Key Interrupt** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 1 Key return control register (KRCTL)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 1 Key return control register (KRCTL)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 2 Key return mode register 0 (KRM0)

(1) 64-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	0	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

Caution Be sure to clear bit 7 of the KRM0 register to "0".

<R> (2) 80-pin products

Address: FFF37H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
KRM0	KRM07	KRM06	KRM05	KRM04	KRM03	KRM02	KRM01	KRM00

3. 17. 3. 3 Key return flag register (KRF)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **17. 3. 3 Key return flag register (KRF)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 17. 3. 4 Port mode registers 0 to 2, 7 (PM0 to PM2, PM7)

(1) 64-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	1	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 4 to 6 of the PM0 register, bit 6 of the PM1 register, bits 4 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bits 5 and 7 of the PM1 register to "1".

(2) 80-pin products

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00	FFF20H	FFH	R/W
PM1	1	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W

Cautions 1. Be sure to clear bits 5 and 6 of the PM0 register, bit 6 of the PM1 register, bits 5 to 7 of the PM2 register, bits 4 to 7 of the PM7 register to "0".

2. Be sure to set bit 7 of the PM0 register, bit 7 of the PM1 register to "1".

3. 17. 3. 5 Peripheral I/O redirection register (PIOR)

Address: F0077H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIOR	0	0	0	0	0	0	PIOR1	PIOR0

Function	64-pin products				80-pin products			
	Setting value of PIOR1, PIOR0				Setting value of PIOR1, PIOR0			
	0, 0	0, 1	1, 0	1, 1	0, 0	0, 1	1, 0	1, 1
KR0	P70	Setting prohibited	P00	P10	P70	Setting prohibited	P00	P10
KR1	P71		P01	P11	P71		P01	P11
KR2	P72		P02	P12	P72		P02	P12
KR3	P73		P03	P13	P73		P03	P13
KR4	–		–	P14	–		P04	P14
KR5	–		P22	–	–		P22	P15
KR6	–		P23	–	–		P23	–
KR7	–		–	–	–		P24	–

3. 17. 4 Key interrupt operation

See **17. 4 Key Interrupt Operation** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 18 Standby Function

See **CHAPTER 18 STANDBY FUNCTION** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 19 Reset Function

See **CHAPTER 19 RESET FUNCTION** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 20 Power-On-Reset Circuit

See **CHAPTER 20 POWER-ON-RESET CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21 Voltage Detector

<R> **3. 21. 1 Functions of voltage detector**

The operation mode and detection voltages (V_{LVDH}, V_{LVDL}, V_{LVD}) for the voltage detector is set by using the option byte (000C1H).

The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}), and generates an internal reset or interrupt request signal.
- The detection level for the power supply detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) can be selected by using the option byte as one of 3 levels (For details, see **3. 24 Option Byte**).
- Operable in STOP mode.
- After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in **5. 2. 3 AC characteristics**. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

(a) Interrupt & reset mode (option byte LVIMDS1, LVIMDS0 = 1, 0)

The two detection voltages (V_{LVDH}, V_{LVDL}) are selected by the option byte 000C1H. The high-voltage detection level (V_{LVDH}) is used for releasing resets and generating interrupts. The low-voltage detection level (V_{LVDL}) is used for generating resets.

(b) Reset mode (option byte LVIMDS1, LVIMDS0 = 1, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for generating/releasing resets.

(c) Interrupt mode (option byte LVIMDS1, LVIMDS0 = 0, 1)

The detection voltage (V_{LVD}) selected by the option byte 000C1H is used for releasing resets/generating interrupts.

<R> The reset and internal interrupt signals are generated in each mode as follows.

Interrupt & reset mode (LVIMDS1, LVIMDS0 = 1, 0)	Reset mode (LVIMDS1, LVIMDS0 = 1, 1)	Interrupt mode (LVIMDS1, LVIMDS0 = 0, 1)
Generates an interrupt request signal by detecting $V_{DD} < V_{LVDH}$ when the operating voltage falls, and an internal reset by detecting $V_{DD} < V_{LVDL}$. Releases an internal reset by detecting $V_{DD} \geq V_{LVDH}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$.	Releases an internal reset by detecting $V_{DD} \geq V_{LVD}$ at power on after the first release of the POR. Generates an interrupt request signal by detecting $V_{DD} < V_{LVD}$ or $V_{DD} \geq V_{LVD}$ at power on after the second release of the POR.

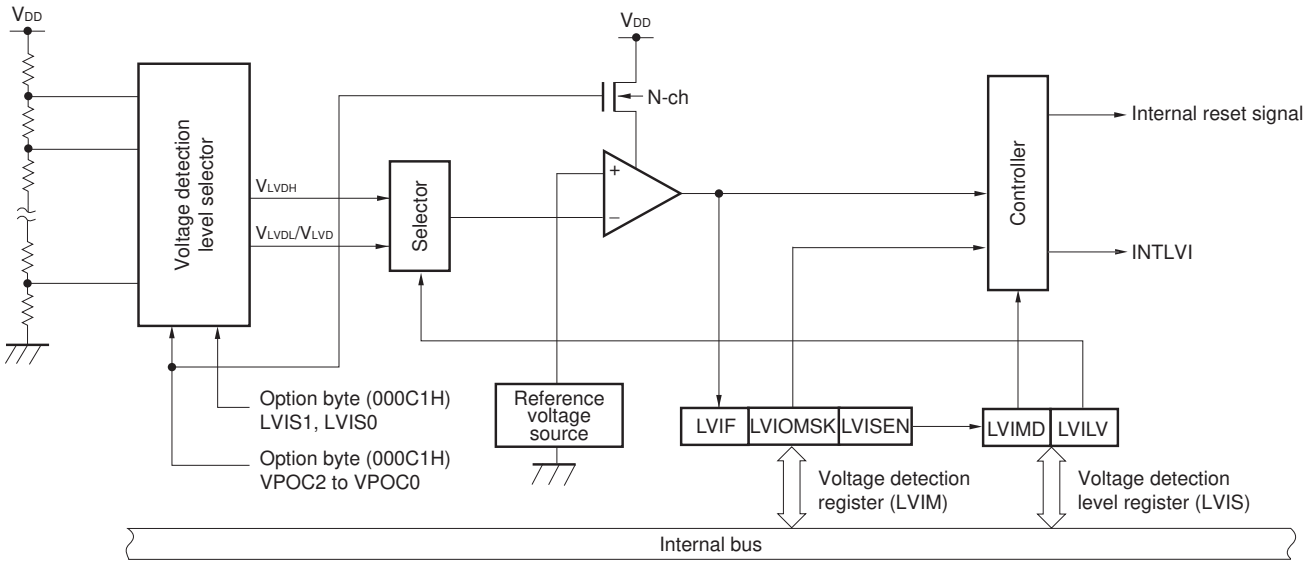
While the voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the voltage detection flag (LVIF: bit 0 of the voltage detection register (LVIM)).

Bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of the RESF register, see **3. 19 Reset Function**.

3. 21. 2 Configuration of voltage detector

The block diagram of the voltage detector is shown in Figure 3-15.

<R> **Figure 3-15. Block Diagram of Voltage Detector**



3. 21. 3 Registers controlling voltage detector

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below. For details of each register, see **21. 3 Registers Controlling Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 1 Voltage detection register (LVIM)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 1 Voltage detection register (LVIM)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 3. 2 Voltage detection level register (LVIS)

The bit setting is same as that of RL78/G1A (64-pin products). For details, see **21. 3. 2 Voltage detection level register (LVIS)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

Format of User Option Byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt & reset mode)

<R>

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	1.84	0	0	1	0	0	1	0
3.75	3.67	2.45	0	1	0	0	0		
4.06	3.98	2.75	0	1	1	0	0		
–			Value other than above is setting prohibited.						

- LVD setting (reset mode)

<R>

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	1	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Remarks 1.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

2. The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics.**

(**Cautions** are listed on the next page.)

Format of User Option Byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H[Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

- LVD setting (interrupt mode)

<R>

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	0	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

- LVD off (use of external reset input via $\overline{\text{RESET}}$ pin)

<R>

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
–	–	1	×	×	×	×	×	1
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

<R> **Cautions1. Set bit 4 to 1.**

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detector or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detector or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

<R> **Remarks 1.** ×: don't care

2. For details on the LVD circuit, see **3. 21 Voltage Detector**.

3. The detection voltage is a TYP. value. For details, see **5. 2. 5. 4 LVD circuit characteristics**.

3. 21. 4 Operation of voltage detector

See **21. 4 Operation of Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 21. 5 Cautions for voltage detector

See **21. 5 Cautions for Voltage Detector** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22 Safety Functions

3. 22. 1 Overview of safety functions

The following safety functions are provided in the RL78/G1E to comply with the IEC60730 and IEC61508 safety standards. These functions enable the microcontroller to self-diagnose abnormalities and stop operating if an abnormality is detected.

(1) Flash memory CRC operation function (high-speed CRC, general-purpose CRC)

This detects data errors in the flash memory by performing CRC operations.

<R> Two CRC functions are provided in the RL78/G1E that can be used according to the application or purpose of use.

- High-speed CRC: The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC: This can be used for checking various data in addition to the code flash memory area while the CPU is running.

(2) RAM parity error detection function

This detects parity errors when reading RAM data.

(3) RAM guard function

This prevents RAM data from being rewritten when the CPU freezes.

(4) SFR guard function

This prevents SFRs from being rewritten when the CPU freezes.

(5) Invalid memory access detection function

This detects illegal accesses to invalid memory areas (such as areas where no memory is allocated and areas to which access is restricted).

<R> **(6) Frequency detection function**

This function allows a self-check of the CPU/peripheral hardware clock frequencies using the timer array unit.

<R> **(7) A/D test function**

This is used to perform a self-check of the A/D converter by performing A/D conversion of the A/D converter's positive and negative reference voltages, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage.

Remark See the self-testing library application note for the RL78 MCU series (R01AN0749, R01AN1062, R01AN1296) for use examples of the safety functions compliant with the safety standard IEC60730.

3. 22. 2 Registers used by safety functions

See **22. 2 Registers Used by Safety Functions** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3 Operation of safety functions

3. 22. 3. 1 Flash memory CRC operation function (high-speed CRC)

See **22. 3. 1 Flash memory CRC operation function (high-speed CRC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 2 CRC operation function (general-purpose CRC)

See **22. 3. 2 CRC operation function (general-purpose CRC)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 3 RAM parity error detection function

See **22. 3. 3 RAM parity error detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 4 RAM guard function

See **22. 3. 4 RAM guard function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 5 SFR guard function

See **22. 3. 5 SFR guard function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 6 Invalid memory access detection function

See **22. 3. 6 Invalid memory access detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 22. 3. 7 Frequency detection function

For details of each register, see **22. 3. 7 Frequency detection function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below.

(1) Timer input select register 0 (TIS0)

Address: F0074H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TIS0	0	0	0	0	0	TIS02	TIS01	TIS00

TIS02	TIS01	TIS00	Selection of timer input used with channel 5
0	0	0	Default value
1	0	0	Low-speed on-chip oscillator clock (f_{IL})
Other than above			Setting prohibited

Caution High-level width, low-level width of timer input is selected, will require more than 1/f_{MCK} +10 ns. Therefore, when selecting f_{SUB} to f_{CLK} (CSS bit of CKS register = 1), can not TIS02 bit set to 1.

3. 22. 3. 8 A/D test function

See **22. 3. 8 A/D test function** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 23 Regulator

See **CHAPTER 23 REGULATOR** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 24 Option Byte

3. 24. 1 Functions of option bytes

Addresses 000C0H to 000C3H of the flash memory of the RL78/G1E form an option byte area.

Option bytes consist of user option byte (000C0H to 000C2H) and on-chip debug option byte (000C3H).

Upon power application or resetting and starting, an option byte is automatically referenced and a specified function is set. For the bits to which no function is allocated, be sure to set the value specified in this manual.

To use the boot swap operation during self programming, 000C0H to 000C3H are replaced by 010C0H to 010C3H. Therefore, set the same values as 000C0H to 000C3H to 010C0H to 010C3H.

Caution Be sure to specify option byte settings regardless of whether they are used or not.

3. 24. 1. 1 User option byte (000C0H to 000C2H/010C0H to 010C2H)

<R> **(1) 000C0H/010C0H**

- ○ Setting of watchdog timer operation
  - Enabling or disabling of counter operation
  - Enabling or disabling of counter operation in the HALT or STOP mode
- ○ Setting of overflow time of watchdog timer
- ○ Setting of window open period of watchdog timer
- ○ Setting of interval interrupt of watchdog timer
  - Whether or not to use the interval interrupt is selectable

Caution Set the same value as 000C0H to 010C0H when the boot swap operation is used because 000C0H is replaced by 010C0H.

<R> **(2) 000C1H/010C1H**

- ○ Setting of LVD operation mode
  - Interrupt & reset mode.
  - Reset mode.
  - Interrupt mode.
  - LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)
- ○ Setting of LVD detection level (V_{LVDH}, V_{LVDL}, V_{LVD})

<R> **Cautions1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).**

2. Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

(3) 000C2H/010C2H

- Setting of flash operation mode
  - LV (low voltage main) mode
  - LS (low speed main) mode
  - HS (high speed main) mode
- Setting of the frequency of the high-speed on-chip oscillator

<R>
  - Select from 32 MHz/24 MHz/16 MHz/12 MHz/8 MHz/6 MHz/4 MHz/3 MHz/2 MHz/1 MHz (TYP.).

Caution Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

3. 24. 1. 2 On-chip debug option byte (000C3H/010C3H)

- Control of on-chip debug operation
  - On-chip debug operation is disabled or enabled.
- Handling of data of flash memory in case of failure in on-chip debug security ID authentication
  - Data of flash memory is erased or not erased in case of failure in on-chip debug security ID authentication.

Caution Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

3. 24. 2 Format of user option byte

For details of each register, see **24. 2 Format of User Option Byte** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

The bit settings which are different from that of RL78/G1A (64-pin products) are shown below.

Format of user option byte (000C1H/010C1H) (1/2)

Address: 000C1H/010C1H [Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

<R> • LVD setting (interrupt & reset mode)

Detection voltage			Option byte setting value						
V_{LVDH}		V_{LVDL}	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	1.84	0	0	1	0	0	1	0
3.75	3.67	2.45	0	1	0	0	0		
4.06	3.98	2.75	0	1	1	0	0		
–			Value other than above is setting prohibited.						

<R> • LVD setting (reset mode)

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	1	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Cautions 1. Be sure to set bit 4 to "1".

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC Characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

<R> **Remarks 1.** For details on the LVD circuit, see **3. 21 Voltage Detector**.

2. The detection voltage is a typical value. For details, see **5. 2. 5. 4 LVD circuit characteristics.**

Format of user option byte (000C1H/010C1H) (2/2)

Address: 000C1H/010C1H [Note]

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0

<R> • LVD setting (interrupt mode)

Detection voltage		Option byte setting value						
V_{LVDH}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
3.13	3.06	0	0	1	0	0	0	1
3.75	3.67	0	1	0	0	0		
4.06	3.98	0	1	1	0	0		
–		Value other than above is setting prohibited.						

<R> • LVD off (by controlling the externally input reset signal on the $\overline{\text{RESET}}$ pin)

Detection voltage		Option byte setting value						
V_{LVD}		VPOC2	VPOC1	VPOC0	LVIS1	LVIS0	Mode setting	
Rising edge	Falling edge						LVIMDS1	LVIMDS0
–	–	1	×	×	×	×	×	1
–		Value other than above is setting prohibited.						

Note Set the same value as 000C1H to 010C1H when the boot swap operation is used because 000C1H is replaced by 010C1H.

Cautions 1. Be sure to set bit 4 to "1".

2. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in 5. 2. 3 AC characteristics. This is done by utilizing the voltage detection circuit or controlling the externally input reset signal. After the power supply is turned off, this LSI should be placed in the STOP mode, or placed in the reset state by utilizing the voltage detection circuit or controlling the externally input reset signal, before the voltage falls below the operating range. The range of operating voltage varies with the setting of the user option byte (000C2H or 010C2H).

<R> **Remarks 1.** ×: don't care

2. For details on the LVD circuit, see **3. 21 Voltage Detector**.

3. The detection voltage is a typical value. For details, see **5. 2. 5. 4 LVD circuit characteristics**.

Format of user option byte (000C2H/010C2H)

Address: 000C2H/010C2H **Note**

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

CMODE1	CMODE0	Setting of flash operation mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 to 4 MHz	1.6 to 5.5 V
1	0	LS (low speed main) mode	1 to 8 MHz	1.8 to 5.5 V
1	1	HS (high speed main) mode	1 to 16 MHz	2.4 to 5.5 V
			1 to 32 MHz	2.7 to 5.5 V
Other than above		Setting prohibited		

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	Frequency of the high-speed on-chip oscillator
1	0	0	0	32 MHz
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
0	0	1	0	6 MHz
1	0	1	1	4 MHz
0	0	1	1	3 MHz
1	1	0	0	2 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note Set the same value as 000C2H to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

<R> **Cautions 1. Be sure to set bits 5, 4 to "10B".**

2. The ranges of operation frequency and operation voltage vary depending on the flash operation mode. For details, see 5. 2. 3 AC characteristics.

3. 24. 3 Format of on-chip debug option byte

See **24. 3 Format of On-chip Debug Option Byte** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 24. 4 Setting of option byte

See **24. 4 Setting of Option Byte** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25 Flash Memory

In this section, the differences of the functions and registers from RL78/G1A (64-pin products) are described. For details, see **CHAPTER 25 FLASH MEMORY** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> ### 3. 25. 1 Serial Programming Using Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the RL78/G1E.

- PG-FP5, FL-PR5
- E1 on-chip debugging emulator

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the RL78/G1E has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the RL78/G1E is mounted on the target system.

Remark FL-PR5 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

<R> **Table 3-18. Wiring Between RL78/G1E and Dedicated Flash Memory Programmer**

Pin Configuration of Dedicated Flash Memory Programmer		I/O	Pin Function	Pin Name	Pin No.	
Signal Name					64-pin products	80-pin products
PG-FP5 FL-PR5	E1 On-chip Debugging Emulator				WQFN (9 × 9)	LQFP (12 × 12)
–	TOOL0	I/O	Transmit/receive signal	TOOL0/P40	15	18
SI / RxD	–	I/O				
–	$\overline{\text{RESET}}$	Output	Reset signal	$\overline{\text{RESET}}$	16	19
/RESET	–	Output				
V_{DD}		I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	22	25
GND		–	Ground	V_{SS}	21	24
				EV_{SS0}	–	–
				REGC Note	20	23
EMV_{DD}		–	Driving power for TOOL0 pin	V_{DD}	22	25
				EV_{DD0}	–	–

<R> **Note** Connect REGC pin to ground via a capacitor (0.47 to 1 μF).

Remark Pins that are not indicated in the above table can be left open when using the flash memory programmer for flash programming.

3. 25. 1. 1 Programming environment

See **25. 1. 1 Programming environment** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25. 1. 2 Communication mode

See **25. 1. 2 Communication mode** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 2 Serial programming using external device (that Incorporates UART)**

See **25. 2 Serial Programming Using External Device (that Incorporates UART)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 25. 3 Connection of pins on board

See **25. 3 Connection of Pins on Board** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 4 Serial programming method**

See **25. 4 Serial Programming Method** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 5 Processing time for each command when PG-FP5 Is in use (Reference value)**

See **25. 5 Processing Time for Each Command When PG-FP5 Is in Use (Reference Value)** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 6 Self-programming**

See **25. 6 Self-Programming** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 7 Security Settings**

See **25. 7 Security Settings** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

<R> **3. 25. 8 Data flash**

See **25. 8 Data Flash** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 26 On-chip Debug Function

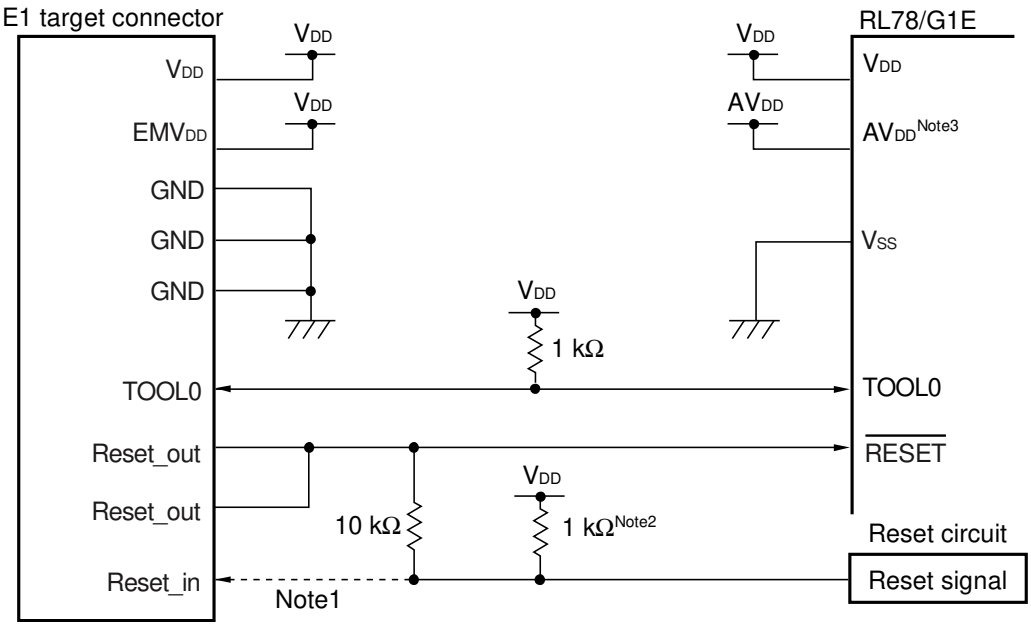
3. 26. 1 Connecting E1 on-chip debugging emulator to RL78/G1E

The RL78/G1A uses the V_{DD}, $\overline{RESET}$, TOOL0, and V_{SS} pins to communicate with the host machine via an E1 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin.

Caution The RL78/G1E has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 3-16. Connection Example of E1 On-chip Debugging Emulator and RL78/G1E

<R>



Notes 1. Connecting the dotted line is not necessary during serial flash programming..

2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

3. $AV_{DD} \leq 3.6$ V.

Cautions 1. This circuit diagram is assumed that the reset signal outputs from an N-ch open drain buffer (output resistor: 100 Ω or less).

2. For the details of $\overline{ARESET}$ pin, see 2. 5. 31 $\overline{ARESET}$.

3. 26. 2 On-chip debug security ID

See **26. 2 On-Chip Debug Security ID** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 26. 3 Securing of user resources

See **26. 3 Securing of User Resources** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 27 BCD Correction Circuit

See **CHAPTER 27 BCD CORRECTION CIRCUIT** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

3. 28 Instruction Set

See **CHAPTER 28 INSTRUCTION SET** in **RL78/G1A Hardware User's Manual (R01UH0305E)**.

CHAPTER 4 ANALOG BLOCK

4. 1 Configurable Amplifier

The RL78/G1E (64-pin products, 80-pin products) has three on-chip configurable amplifier channels.

4. 1. 1 Overview of configurable amplifier features

By specifying settings in the SPI control registers, the configurable amplifiers can be used to realize the following features:

- Single-channel operation
  - Non-inverting amplifier
    - The gain can be specified between 9.5 dB and 40.1 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Inverting amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Differential amplifier
    - The gain can be specified between 6 dB and 40 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function
  - Transimpedance amplifier
    - The feedback resistance can be specified between 20 kΩ and 640 kΩ in 6 steps
    - Four operating modes are available
    - Includes a power-off function

- Multiple-channel operation
  - Instrumentation amplifier
    - The gain can be specified between 20 dB and 54 dB in 18 steps
    - Four operating modes are available
    - Includes a power-off function

And also, the DACn_OUT output signals can be used as the reference voltage for each configurable amplifier.
If D/A converter is powered off, the external reference voltage is to be input to DACn_OUT/VREFINn pin.
For details about use of D/A converter, see **4. 3 D/A Converter**.

Remark n = 1 to 3

4. 1. 2 Block diagram

Figure 4-1. Block Diagram of Configurable Amplifier Ch1

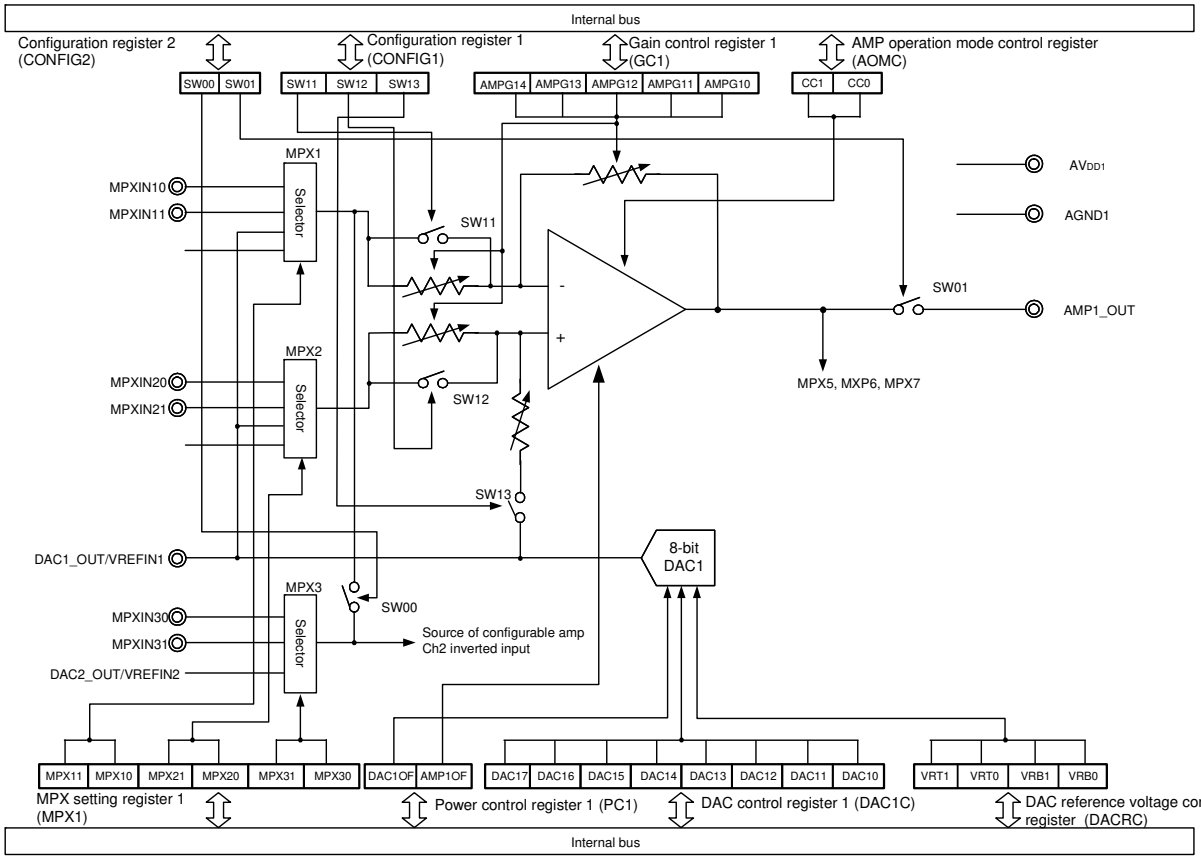


Figure 4-2. Block Diagram of Configurable Amplifier Ch2

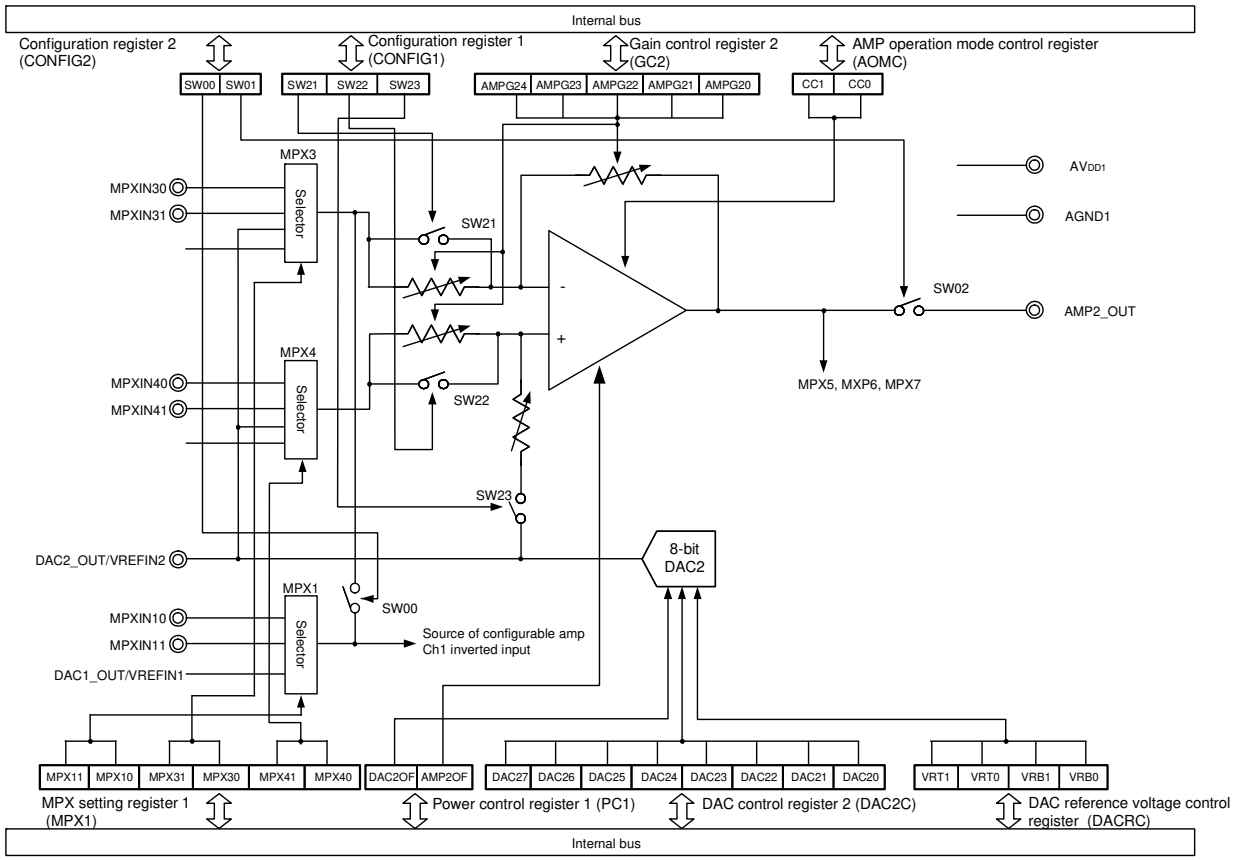
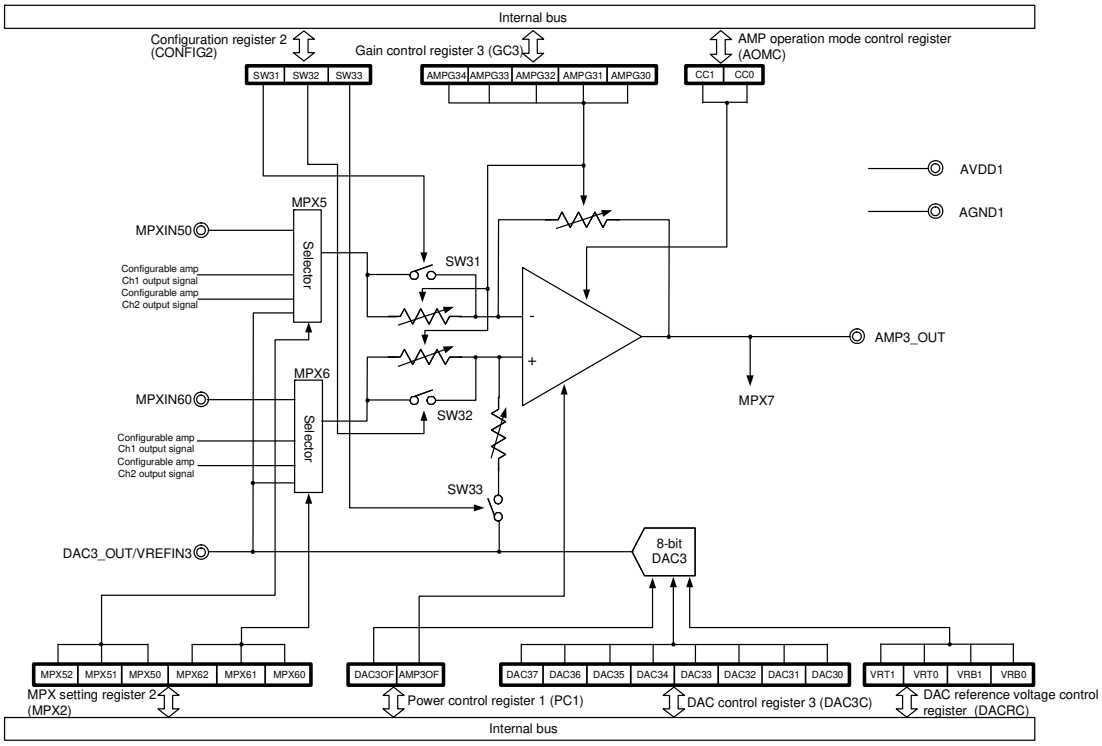
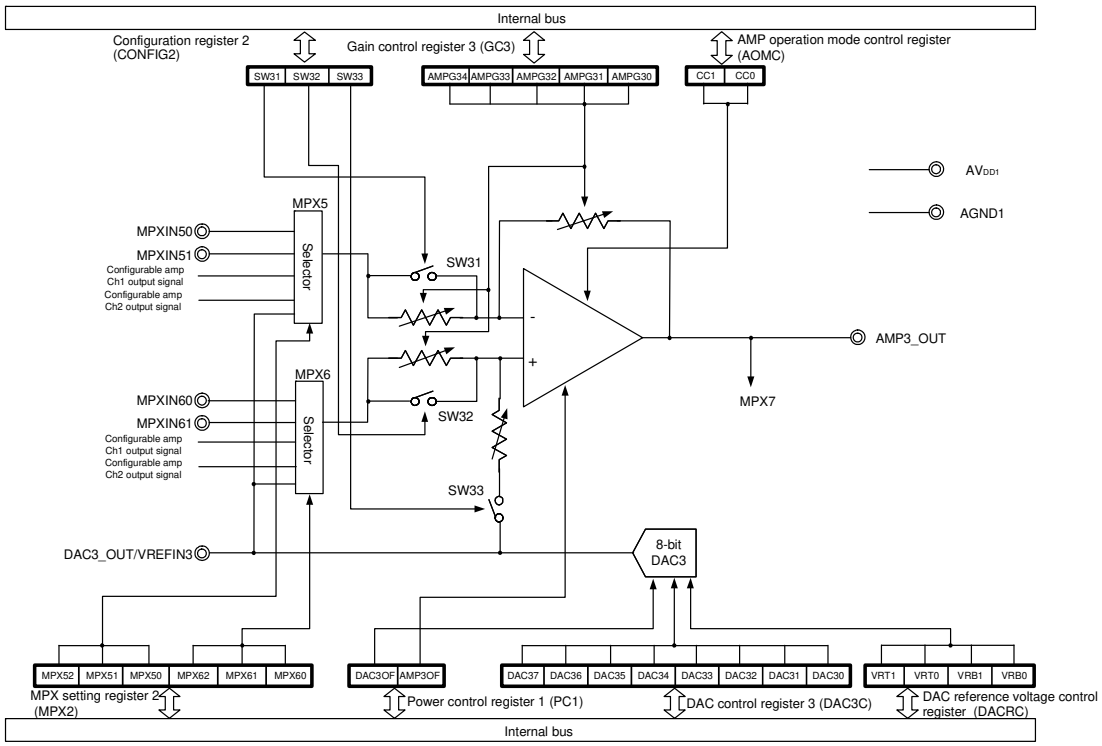


Figure 4-3. Block Diagram of Configurable Amplifier Ch3

- **64-pin products**



- **80-pin products**



4. 1. 3 Registers controlling the configurable amplifiers

The configurable amplifiers are controlled by the following 9 registers:

- Configuration register 1 (CONFIG1)
- Configuration register 2 (CONFIG2)
- MPX setting register 1 (MPX1)
- MPX setting register 2 (MPX2)
- Gain control register 1 (GC1)
- Gain control register 2 (GC2)
- Gain control register 3 (GC3)
- AMP operation mode control register (AOMC)
- Power control register 1 (PC1)

(1) Configuration register 1 (CONFIG1)

This register is used to turn on or off each switch of configurable amplifiers Ch1 and Ch2.

Reset signal input clears this register to 00H.

Address: 00H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CONFIG1	0	SW11	SW12	SW13	0	SW21	SW22	SW23

SW11	Control of SW11
0	Turn off SW11.
1	Turn on SW11.

SW12	Control of SW12
0	Turn off SW12.
1	Turn on SW12.

SW13	Control of SW13
0	Turn off SW13.
1	Turn on SW13.

SW21	Control of SW21
0	Turn off SW21.
1	Turn on SW21.

SW22	Control of SW22
0	Turn off SW22.
1	Turn on SW22.

SW23	Control of SW23
0	Turn off SW23.
1	Turn on SW23.

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(2) Configuration register 2 (CONFIG2)

This register is used to turn on or off each switch of configurable amplifiers Ch1 to Ch3.

Reset signal input clears this register to 00H.

Address: 01H After reset: 00H R/W

	7	6	5	4	3	2	1	0
CONFIG2	0	SW31	SW32	SW33	0	SW02	SW01	SW00

SW31	Control of SW31
0	Turn off SW31.
1	Turn on SW31.

SW32	Control of SW32
0	Turn off SW32.
1	Turn on SW32.

SW33	Control of SW33
0	Turn off SW33.
1	Turn on SW33.

SW02	Control of SW02
0	Turn off SW02.
1	Turn on SW02.

SW01	Control of SW01
0	Turn off SW01.
1	Turn on SW01.

SW00	Control of SW00
0	Turn off SW00.
1	Turn on SW00.

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(3) MPX setting register 1 (MPX1)

This register is used to control MPX1, MPX2, MPX3, and MPX4.

This register is used to select the signal input to configurable amplifiers Ch1 and Ch2.

Reset signal input clears this register to 00H.

Address: 03H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX1	MPX11	MPX10	MPX21	MPX20	MPX31	MPX30	MPX41	MPX40

MPX11	MPX10	Source of configurable amplifier Ch1 inverse input
0	0	MPXIN10 pin
0	1	MPXIN11 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX21	MPX20	Source of configurable amplifier Ch1 non-inverted input
0	0	MPXIN20 pin
0	1	MPXIN21 pin
1	0	D/A converter Ch1 output signal or VREFIN1 pin
1	1	Open pin

MPX31	MPX30	Source of configurable amplifier Ch2 inverse input
0	0	MPXIN30 pin
0	1	MPXIN31 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

MPX41	MPX40	Source of configurable amplifier Ch2 non-inverted input
0	0	MPXIN40 pin
0	1	MPXIN41 pin
1	0	D/A converter Ch2 output signal or VREFIN2 pin
1	1	Open pin

(4) MPX setting register 2 (MPX2)

This register is used to control MPX5 and MPX6.

This register is used to select the signal input to configurable amplifier Ch3.

Reset signal input clears this register to 00H.

- 64-pin products

Address: 04H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverse input
0	0	0	MPXIN50 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

- 80-pin products

Address: 04H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX2	0	MPX52	MPX51	MPX50	0	MPX62	MPX61	MPX60

MPX52	MPX51	MPX50	Source of configurable amplifier Ch3 inverse input
0	0	0	MPXIN50 pin
0	0	1	MPXIN51 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

MPX62	MPX61	MPX60	Source of configurable amplifier Ch3 non-inverted input
0	0	0	MPXIN60 pin
0	0	1	MPXIN61 pin
0	1	0	Configurable amplifier Ch1 output signal
0	1	1	Configurable amplifier Ch2 output signal
1	0	0	D/A converter Ch3 output signal or VREFIN3 pin
Other than above			Setting prohibited

Remark Bits 7 and 3 can be set to 1, but this has no effect on the function.

(5) Gain control register 1 (GC1)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch1.

The value to specify depends on the configuration of configurable amplifier Ch1.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) to 03H.

Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC1	0	0	0	AMPG14	AMPG13	AMPG12	AMPG11	AMPG10

Table 4-1. Gain of Configurable Amplifier Ch1 (Non-Inverting Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

Table 4-2. Gain of Configurable Amplifier Ch1 (Inverting Amplifier and Differential Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Gain of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 4-3. Feedback Resistance of Configurable Amplifier Ch1 (Transimpedance Amplifier)

AMPG14	AMPG13	AMPG12	AMPG11	AMPG10	Feedback Resistance of Configurable Amplifier Ch1 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(6) Gain control register 2 (GC2)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch2.

The value to specify depends on the configuration of configurable amplifier Ch2.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 2 (GC2) to 03H.

Reset signal input clears this register to 00H.

Address: 07H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC2	0	0	0	AMPG24	AMPG23	AMPG22	AMPG21	AMPG20

Table 4-4. Gain of Configurable Amplifier Ch2 (Non-Inverting Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

Table 4-5. Gain of Configurable Amplifier Ch2 (Inverting Amplifier and Differential Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Gain of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 4-6. Feedback Resistance of Configurable Amplifier Ch2 (Transimpedance Amplifier)

AMPG24	AMPG23	AMPG22	AMPG21	AMPG20	Feedback Resistance of Configurable Amplifier Ch2 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

(7) Gain control register 3 (GC3)

This register is used to specify the gain and feedback resistance of configurable amplifier Ch3.

The value to specify depends on the configuration of configurable amplifier Ch3.

When using configurable amplifiers Ch1 to Ch3 together as an instrumentation amplifier, be sure to set gain control register 1 (GC1) and gain control register 2 (GC2) to 03H, respectively.

Reset signal input clears this register to 00H.

Address: 08H After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC3	0	0	0	AMPG34	AMPG33	AMPG32	AMPG31	AMPG30

Table 4-7. Gain of Configurable Amplifier Ch3 (Non-Inverting Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	9.5 dB
0	0	0	0	1	10.9 dB
0	0	0	1	0	12.4 dB
0	0	0	1	1	14.0 dB
0	0	1	0	0	15.6 dB
0	0	1	0	1	17.3 dB
0	0	1	1	0	19.0 dB
0	0	1	1	1	20.8 dB
0	1	0	0	0	22.7 dB
0	1	0	0	1	24.5 dB
0	1	0	1	0	26.4 dB
0	1	0	1	1	28.3 dB
0	1	1	0	0	30.3 dB
0	1	1	0	1	32.2 dB
0	1	1	1	0	34.2 dB
0	1	1	1	1	36.1 dB
1	0	0	0	0	38.1 dB
1	0	0	0	1	40.1 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

Table 4-8. Gain of Configurable Amplifier Ch3 (Inverting Amplifier and Differential Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

Table 4-9. Feedback Resistance of Configurable Amplifier Ch3 (Transimpedance Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Feedback Resistance of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 kΩ
0	0	0	0	1	
0	0	0	1	0	
0	0	0	1	1	40 kΩ
0	0	1	0	0	
0	0	1	0	1	
0	0	1	1	0	80 kΩ
0	0	1	1	1	
0	1	0	0	0	
0	1	0	0	1	160 kΩ
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	320 kΩ
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	640 kΩ
1	0	0	0	0	
1	0	0	0	1	
Other than above					Setting prohibited

Table 4-10. Gain of Configurable Amplifier Ch3 (Instrumentation Amplifier)

AMPG34	AMPG33	AMPG32	AMPG31	AMPG30	Gain of Configurable Amplifier Ch3 (Typ.)
0	0	0	0	0	20 dB
0	0	0	0	1	22 dB
0	0	0	1	0	24 dB
0	0	0	1	1	26 dB
0	0	1	0	0	28 dB
0	0	1	0	1	30 dB
0	0	1	1	0	32 dB
0	0	1	1	1	34 dB
0	1	0	0	0	36 dB
0	1	0	0	1	38 dB
0	1	0	1	0	40 dB
0	1	0	1	1	42 dB
0	1	1	0	0	44 dB
0	1	1	0	1	46 dB
0	1	1	1	0	48 dB
0	1	1	1	1	50 dB
1	0	0	0	0	52 dB
1	0	0	0	1	54 dB
Other than above					Setting prohibited

(8) AMP operation mode control register (AOMC)

This register is used to specify the operating mode of configurable amplifiers Ch1 to Ch3.

Reset signal input clears this register to 00H.

Address: 09H After reset: 00H R/W

	7	6	5	4	3	2	1	0
AOMC	0	0	0	0	0	0	CC1	CC0

CC1	CC0	Operating mode of configurable amplifiers Ch1 to Ch3
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

<R> **Remarks 1.** Bits 5 to 2 can be set to 1, but this has no effect on the function.

2. Bits 7 and 6 are fixed at 0 of read only.

(9) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers and the D/A converters.

Use this register to stop unused functions to reduce power consumption and noise.

When using one of configurable amplifier channels Ch1 to Ch3, be sure to set the control bit that corresponds to the channel (bits 0 to 2) to 1.

Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF

AMP3OF	Operation of configurable amplifier Ch3
0	Stop operation of configurable amplifier Ch3.
1	Enable operation of configurable amplifier Ch3.

AMP2OF	Operation of configurable amplifier Ch2
0	Stop operation of configurable amplifier Ch2.
1	Enable operation of configurable amplifier Ch2.

AMP1OF	Operation of configurable amplifier Ch1
0	Stop operation of configurable amplifier Ch1.
1	Enable operation of configurable amplifier Ch1.

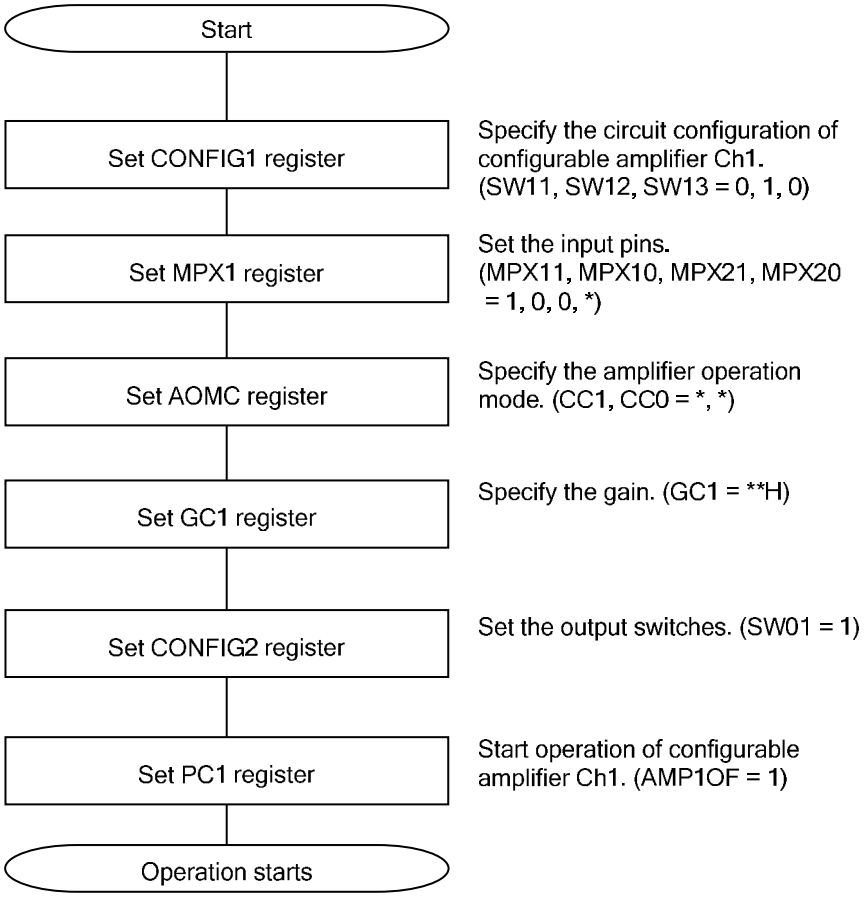
Caution Be sure to clear bit 3 to "0".

4. 1. 4 Procedure for operating the configurable amplifiers

(1) Procedure when using the amplifiers as non-inverting amplifiers

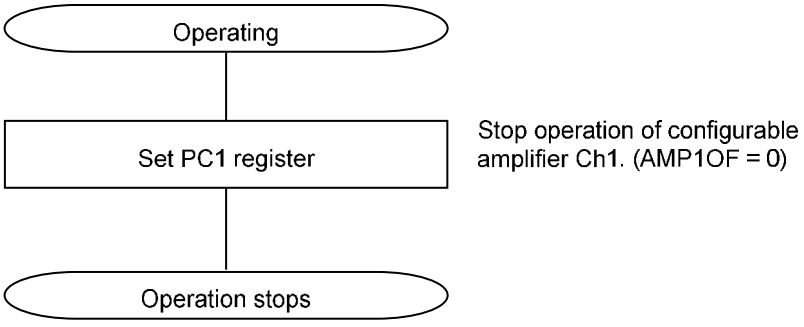
When using the configurable amplifiers as non-inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (non-inverting amplifier)

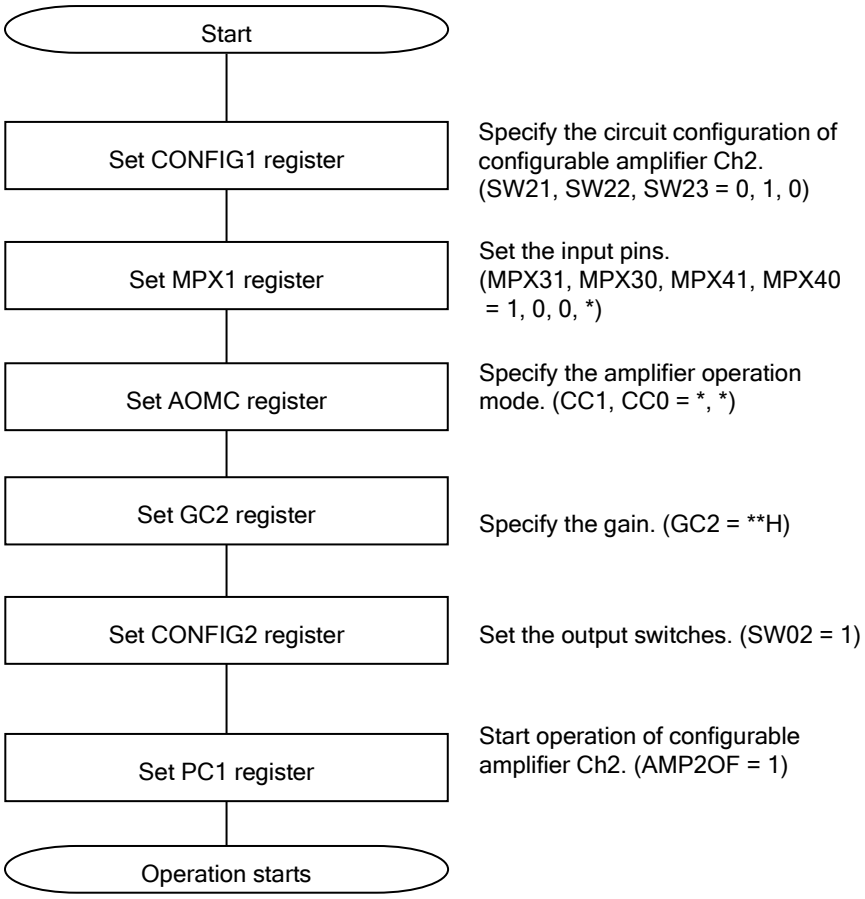


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (non-inverting amplifier)

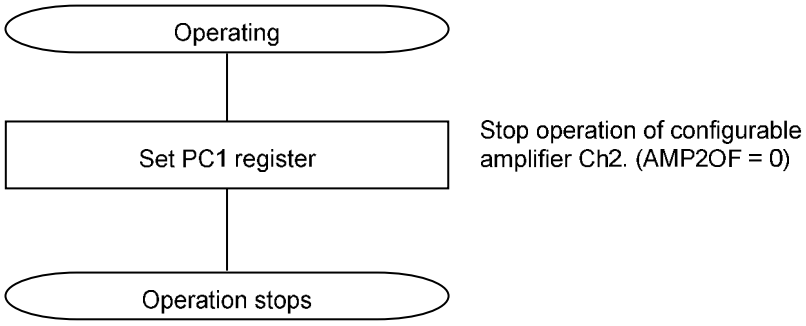


Example of procedure for starting configurable amplifier Ch2 (non-inverting amplifier)

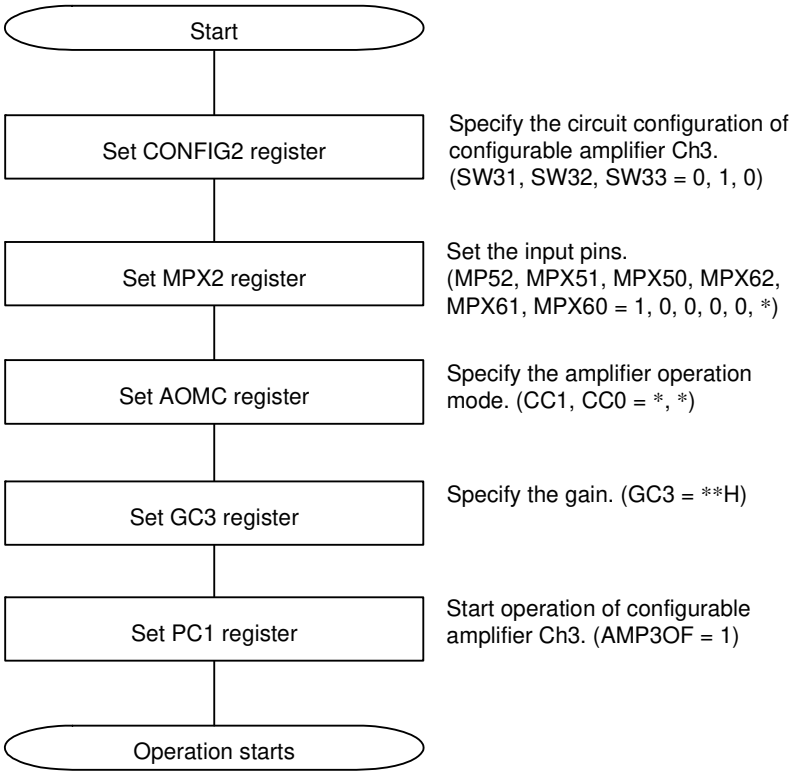


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (non-inverting amplifier)

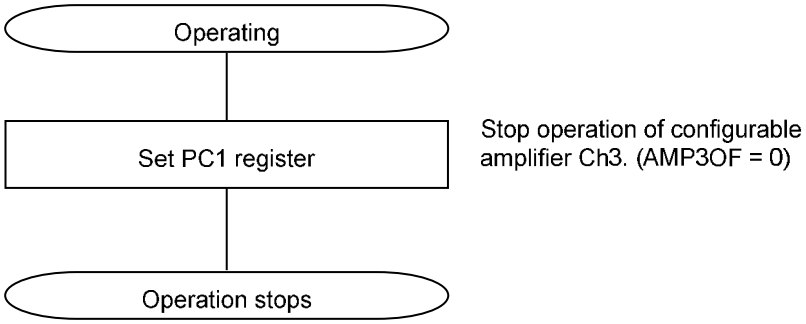


Example of procedure for starting configurable amplifier Ch3 (non-inverting amplifier)



Remark *: don't care

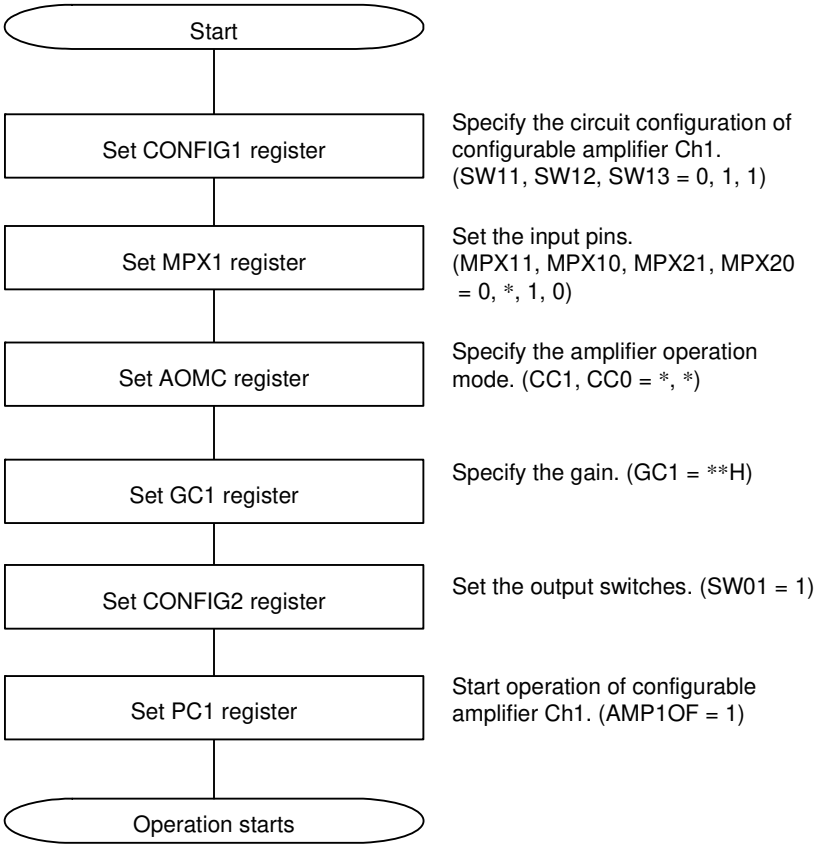
Example of procedure for stopping configurable amplifier Ch3 (non-inverting amplifier)



(2) Procedure when using the amplifiers as inverting amplifiers

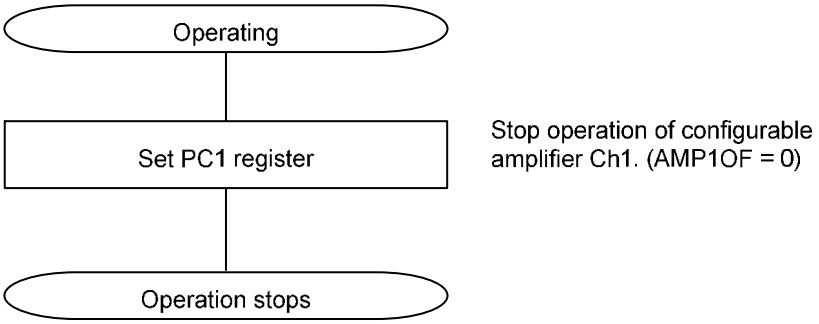
When using the configurable amplifiers as inverting amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (inverting amplifier)

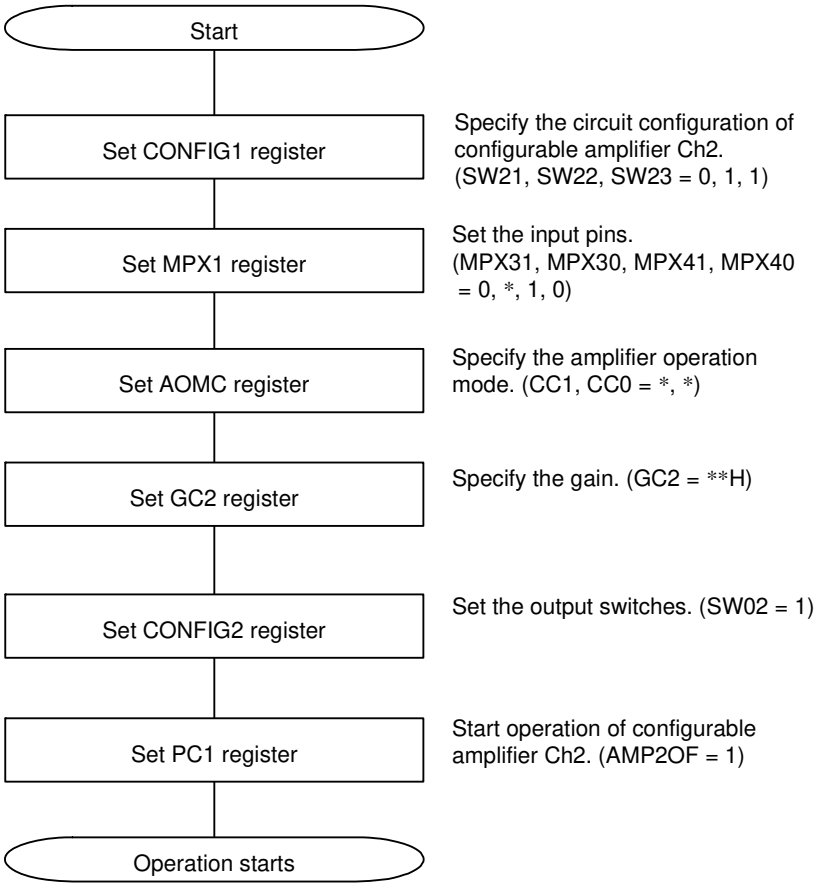


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (inverting amplifier)

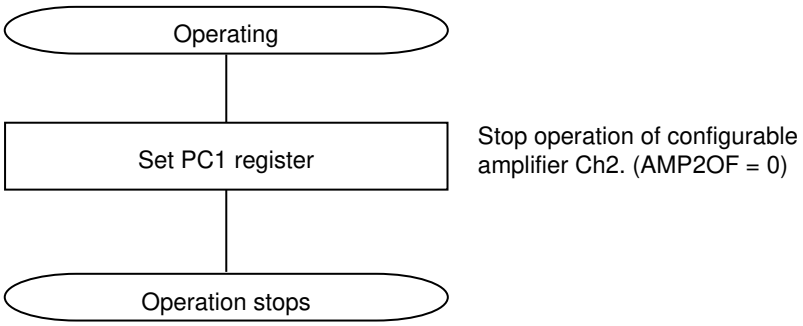


Example of procedure for starting configurable amplifier Ch2 (inverting amplifier)

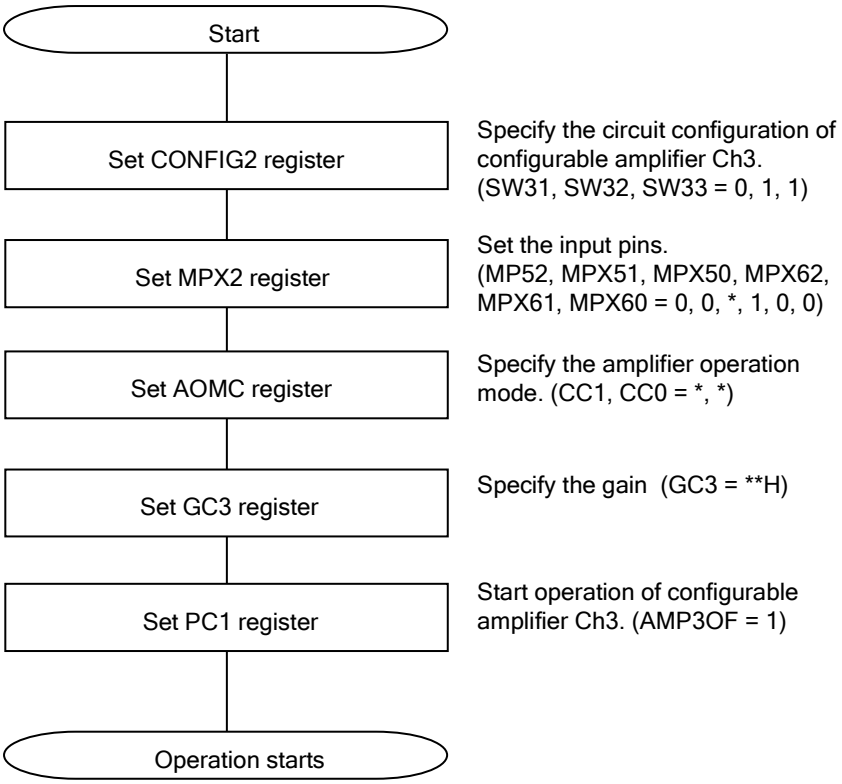


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (inverting amplifier)

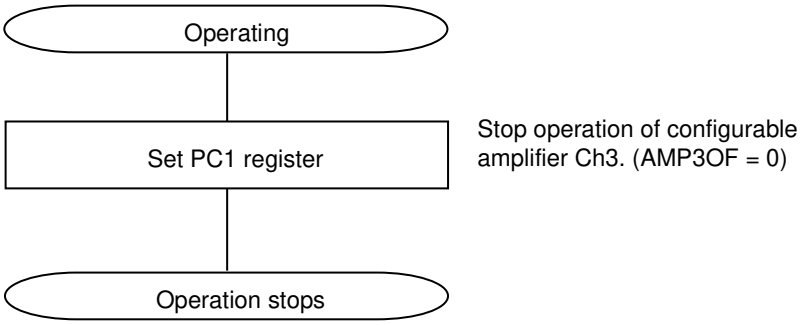


Example of procedure for starting configurable amplifier Ch3 (inverting amplifier)



Remark *: don't care

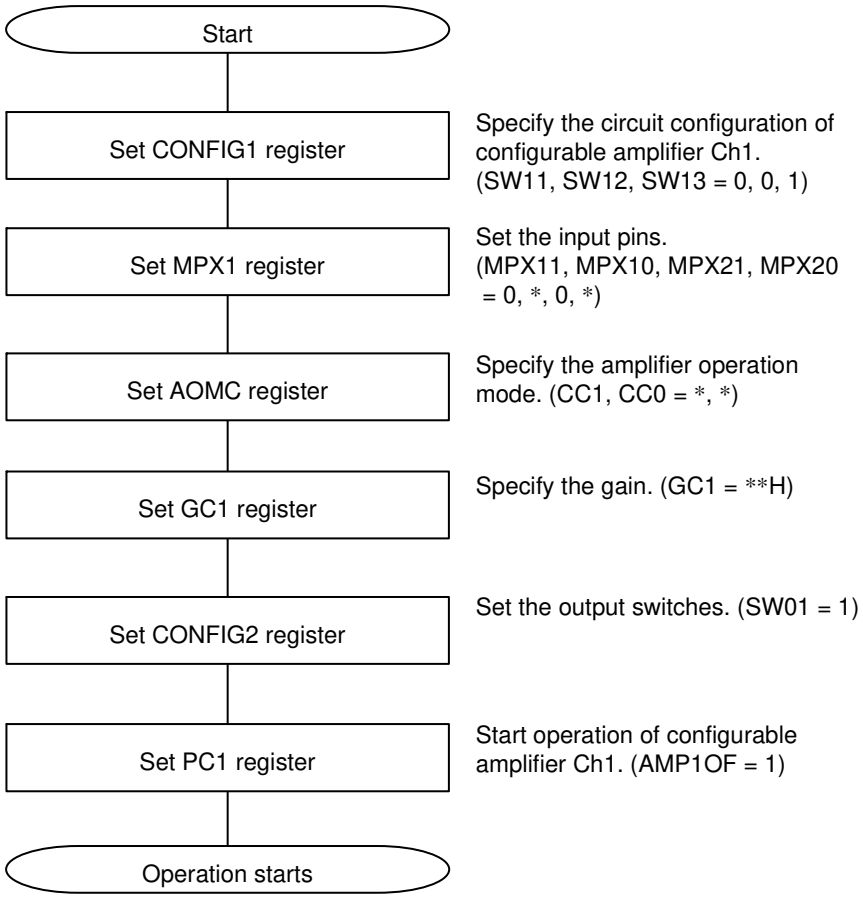
Example of procedure for stopping configurable amplifier Ch3 (inverting amplifier)



(3) Procedure when using the amplifiers as differential amplifiers

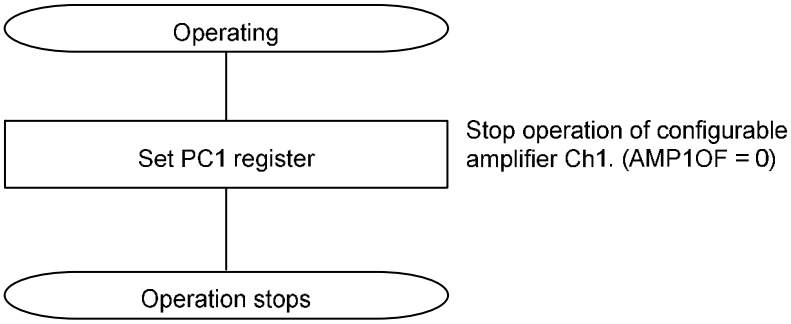
When using the configurable amplifiers together as a differential amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifier Ch1 (differential amplifier)

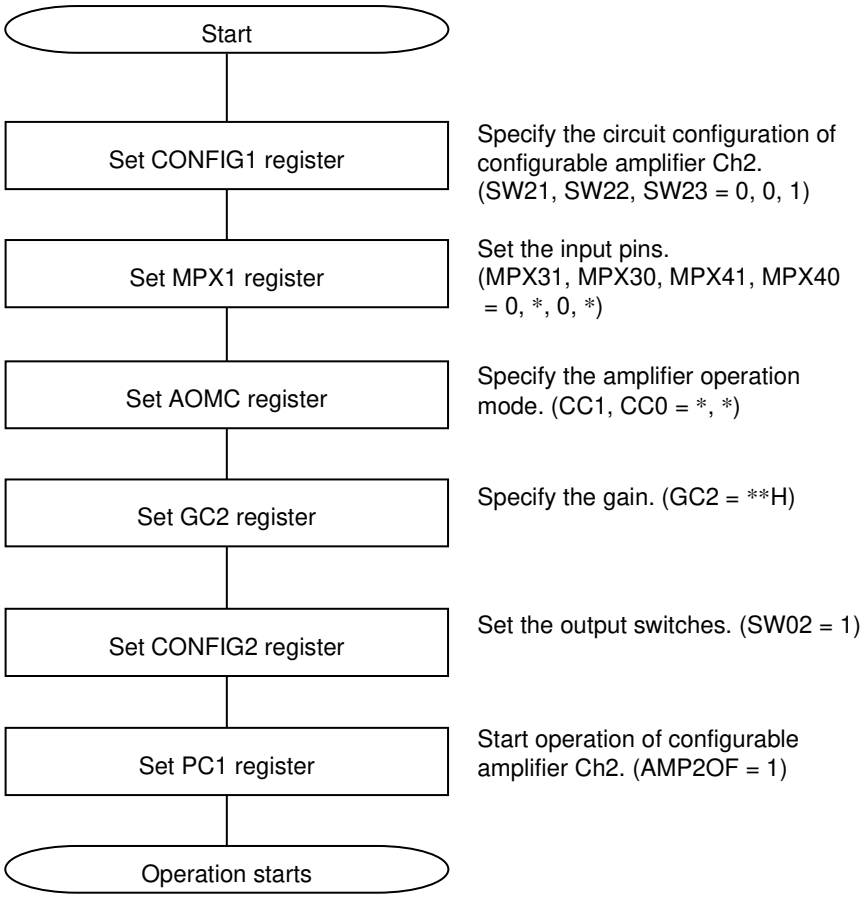


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (differential amplifier)

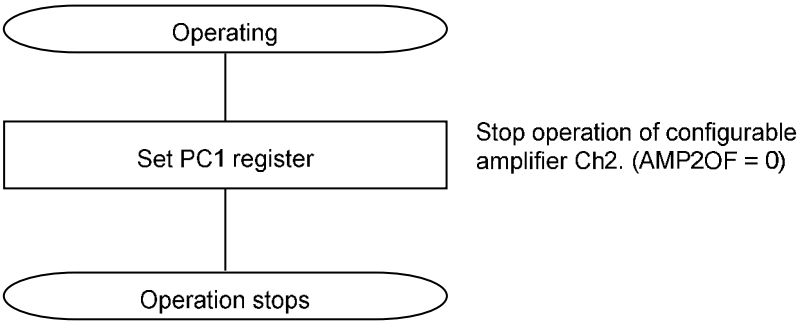


Example of procedure for starting configurable amplifier Ch2 (differential amplifier)

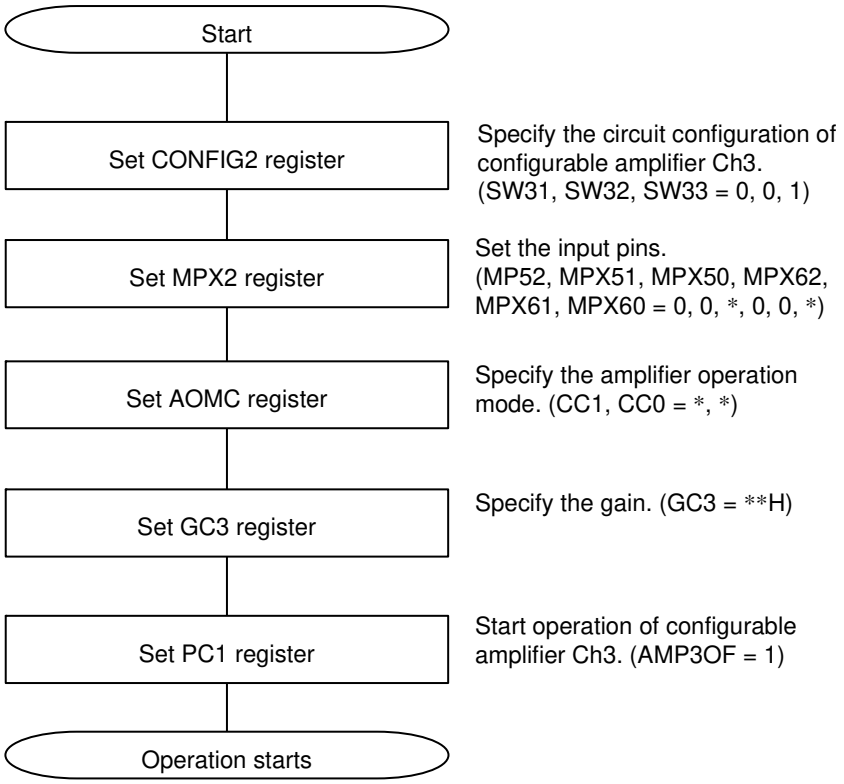


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (differential amplifier)

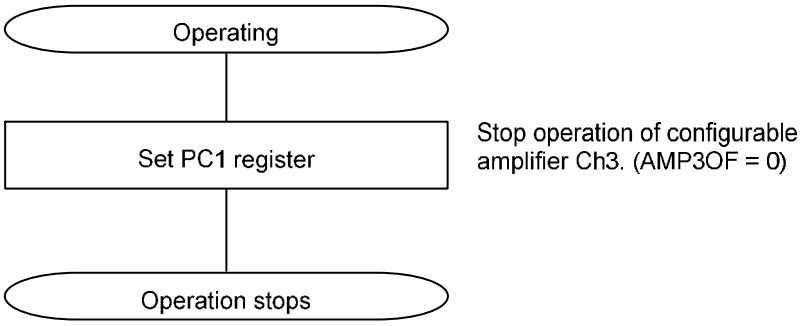


Example of procedure for starting configurable amplifier Ch3 (differential amplifier)



Remark *: don't care

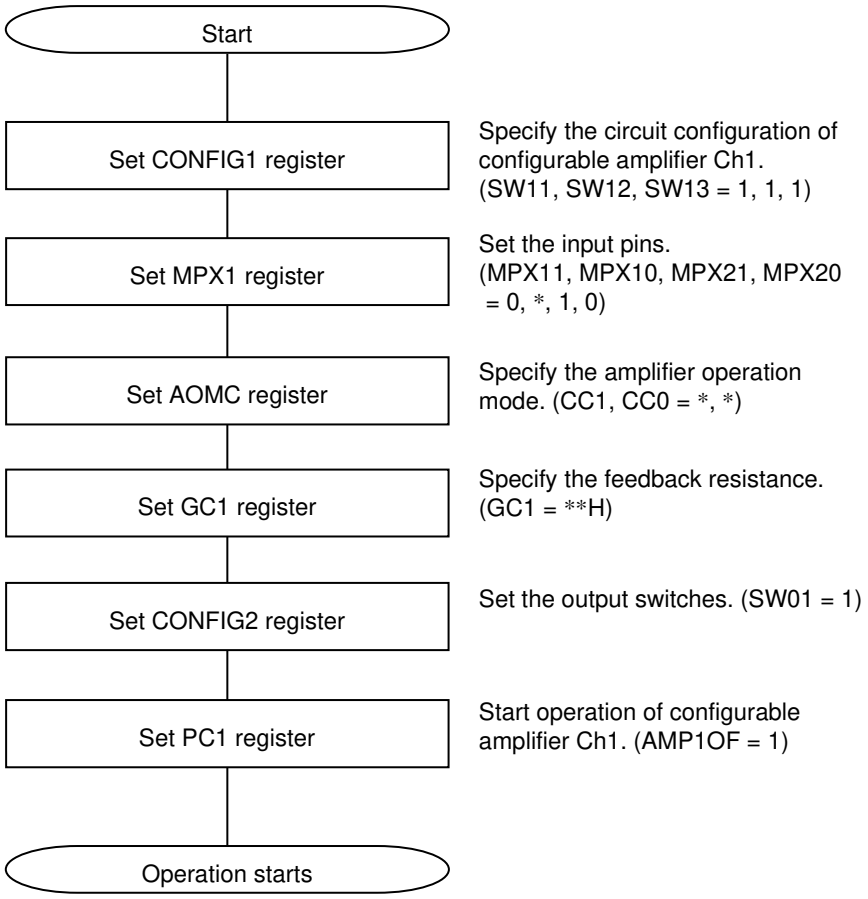
Example of procedure for stopping configurable amplifier Ch3 (differential amplifier)



(4) Procedure when using the amplifiers as a transimpedance amplifier

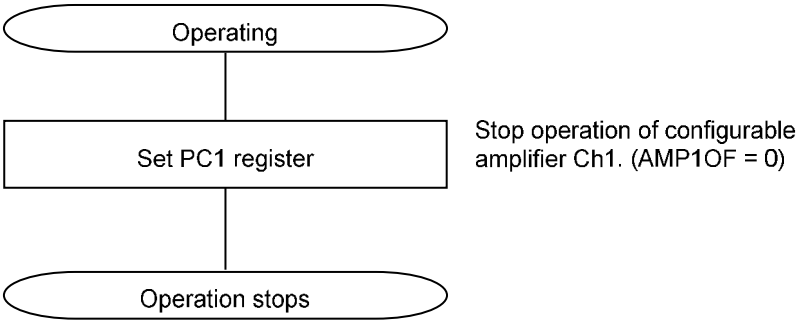
When using the configurable amplifiers as transimpedance amplifiers, follow the procedures below to start and stop the amplifiers.

Example of procedure for starting configurable amplifier Ch1 (transimpedance amplifier)

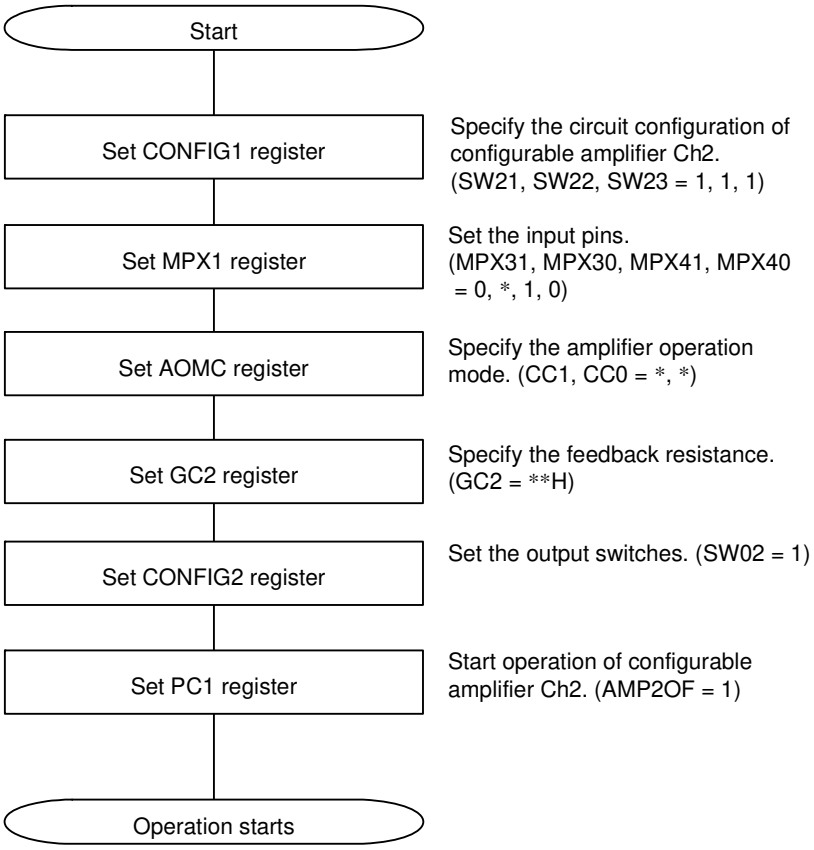


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch1 (transimpedance amplifier)

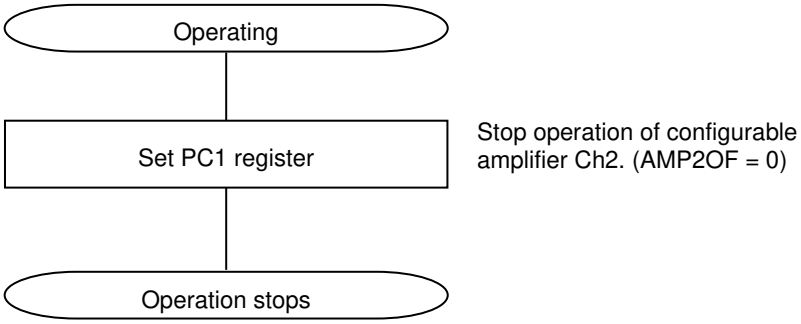


Example of procedure for starting configurable amplifier Ch2 (transimpedance amplifier)

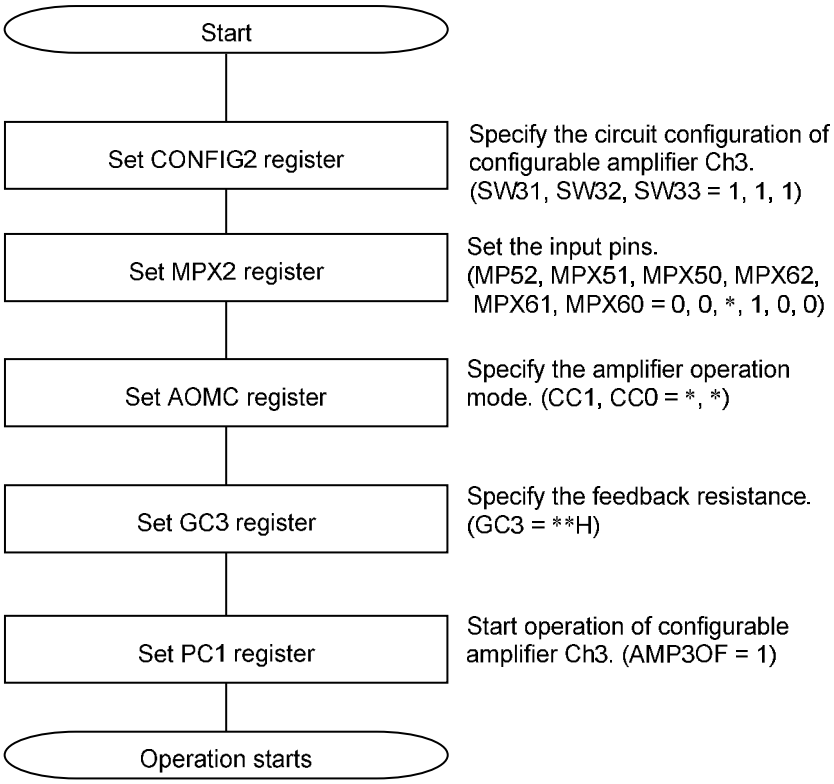


Remark *: don't care

Example of procedure for stopping configurable amplifier Ch2 (transimpedance amplifier)

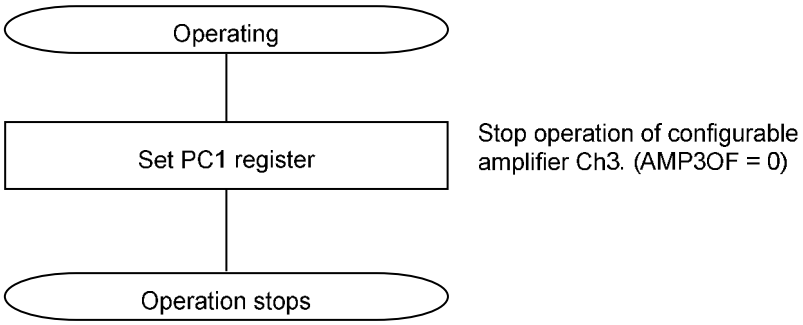


Example of procedure for starting configurable amplifier Ch3 (transimpedance amplifier)



Remark *: don't care

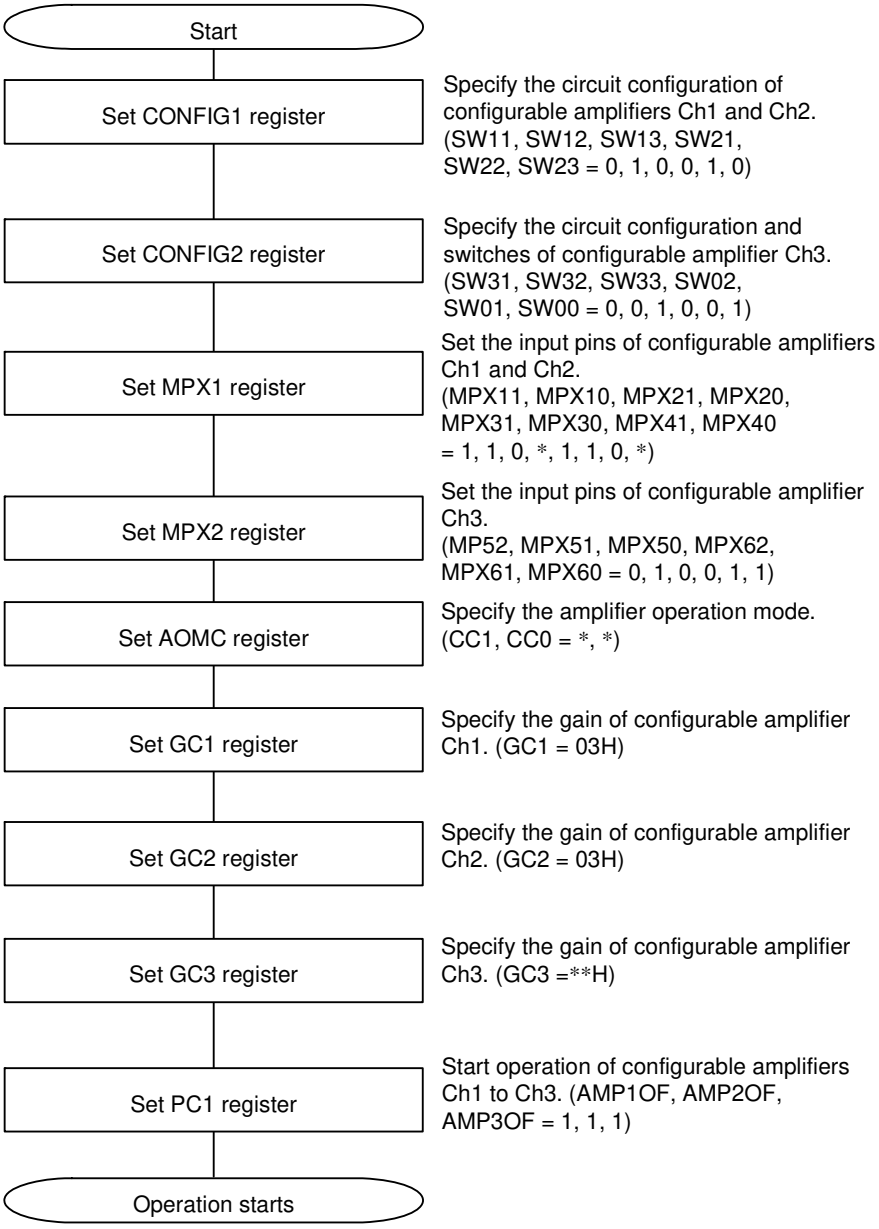
Example of procedure for stopping configurable amplifier Ch3 (transimpedance amplifier)



(5) Procedure when using the amplifiers as an instrumentation amplifier

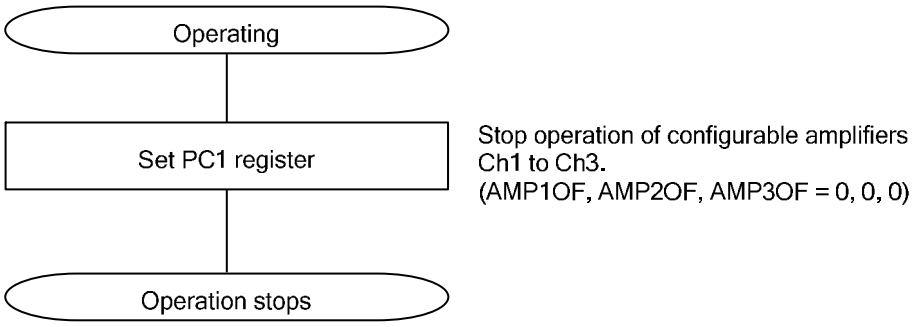
When using the configurable amplifiers together as an instrumentation amplifier, follow the procedures below to start and stop the amplifier.

Example of procedure for starting configurable amplifiers (instrumentation amplifier)



Remark *: don't care

Example of procedure for stopping configurable amplifiers (instrumentation amplifier)



4. 2 Gain Adjustment Amplifier

The RL78/G1E (64-pin products, 80-pin products) has one on-chip gain adjustment amplifier channel.

4. 2. 1 Overview of gain adjustment amplifier features

The features of gain adjustment amplifier are described below.

- Rail-to-rail I/O
- The gain can be specified between 6 dB and 40 dB in 18 steps.
- Includes a power-off function.
- Includes a synchronous detector **Note**.

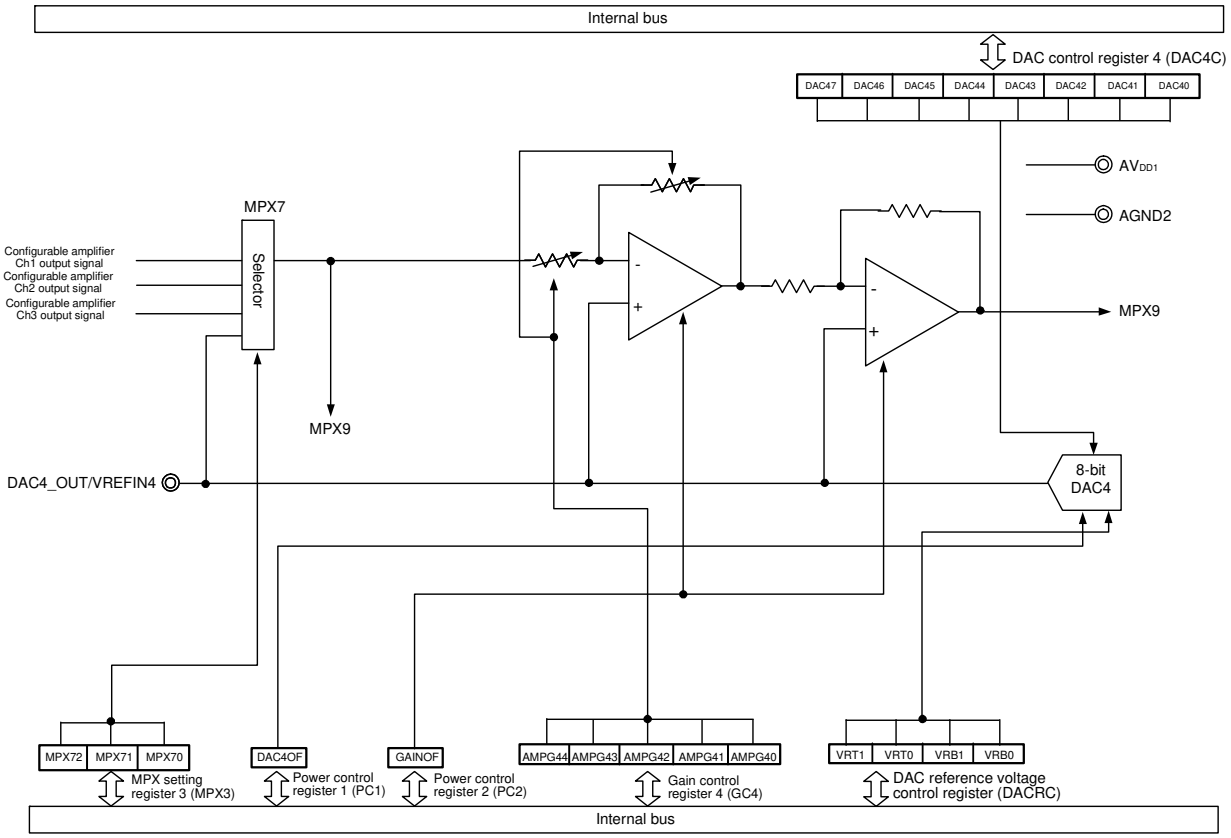
<R>
- CLK_SYNCH = H: Inverted output signal (SYNCH_OUT pin)
- CLK_SYNCH = L: Non-inverted output signal (SYNCH_OUT pin)

<R> **Note** 80-pin products only. There are two output pins (GAINAMP_OUT pin, SYNCH_OUT pin), the output from SYNCH_OUT pin can be inverted output or non-inverted output according to the input of CLK_SYNCH pin.

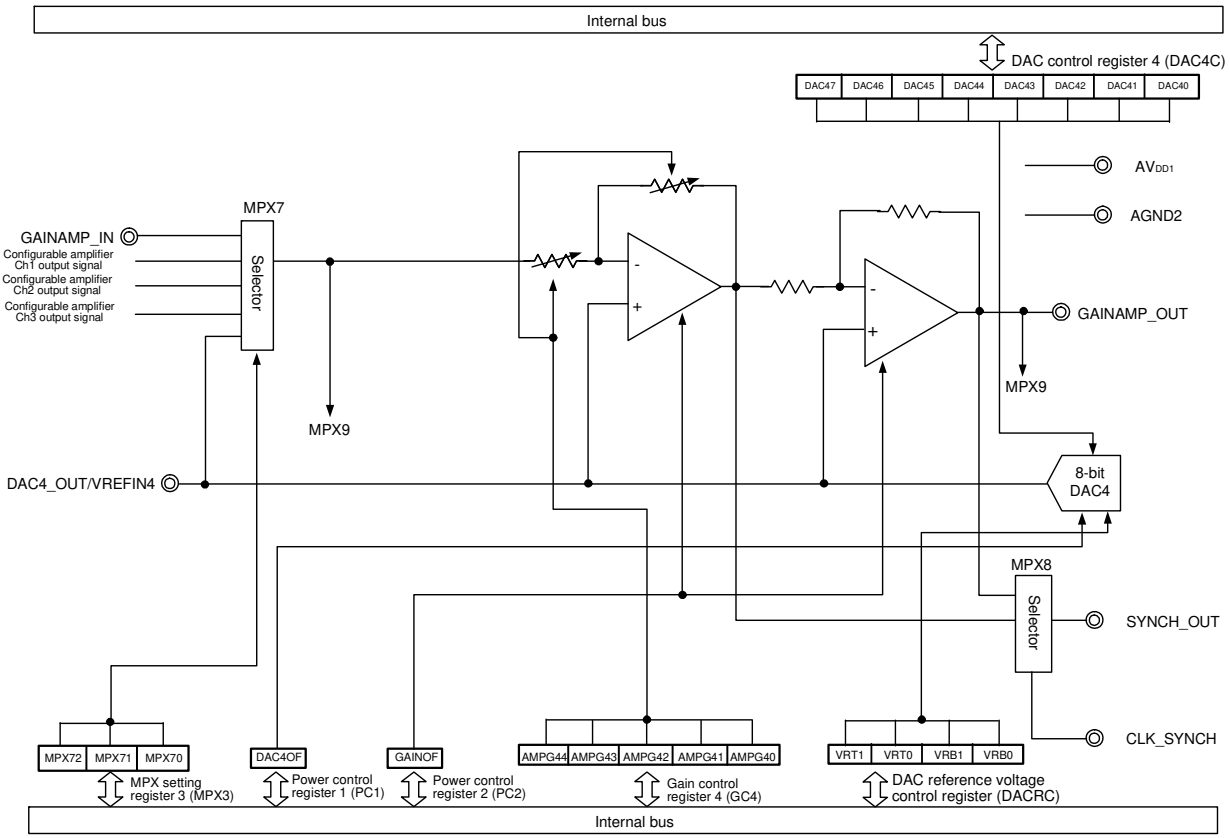
And also, the DAC4_OUT output signals can be used as the reference voltage for gain adjustment amplifier.
If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.
For details about use of D/A converter, see **4. 3 D/A Converter**.

4. 2. 2 Block diagram

- **64-pin products**



- **80-pin products**



4. 2. 3 Registers controlling the gain adjustment amplifier

The gain adjustment amplifier is controlled by the following 3 registers:

- MPX setting register 3 (MPX3)
- Gain control register 4 (GC4)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the gain adjustment amplifier, use bits 2 to 0.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	–
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

MPX72	MPX71	MPX70	Source of gain adjustment amplifier input
0	0	0	GAINAMP_IN pin
0	0	1	Configurable amplifier Ch1 output signal
0	1	0	Configurable amplifier Ch2 output signal
0	1	1	Configurable amplifier Ch3 output signal
1	0	0	D/A converter Ch4 output signal or VREFIN4 pin
Other than above			Setting prohibited

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

(2) Gain control register 4 (GC4)

This register is used to specify the gain of the gain adjustment amplifier.

Reset signal input clears this register to 00H.

Address: 0AH After reset: 00H R/W

	7	6	5	4	3	2	1	0
GC4	0	0	0	AMP44	AMP43	AMP42	AMP41	AMP40

AMP44	AMP43	AMP42	AMP41	AMP40	Gain
0	0	0	0	0	6 dB
0	0	0	0	1	8 dB
0	0	0	1	0	10 dB
0	0	0	1	1	12 dB
0	0	1	0	0	14 dB
0	0	1	0	1	16 dB
0	0	1	1	0	18 dB
0	0	1	1	1	20 dB
0	1	0	0	0	22 dB
0	1	0	0	1	24 dB
0	1	0	1	0	26 dB
0	1	0	1	1	28 dB
0	1	1	0	0	30 dB
0	1	1	0	1	32 dB
0	1	1	1	0	34 dB
0	1	1	1	1	36 dB
1	0	0	0	0	38 dB
1	0	0	0	1	40 dB
Other than above					Setting prohibited

<R> **Remark** Bits 7 to 5 are fixed at 0 of read only.

(3) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the gain adjustment amplifier, be sure to set bit 4 to 1.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

GAINOF	Operation of gain adjustment amplifier
0	Stop operation of the gain adjustment amplifier.
1	Enable operation of the gain adjustment amplifier.

Caution Be sure to clear bit 2 to "0".

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

- **80-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

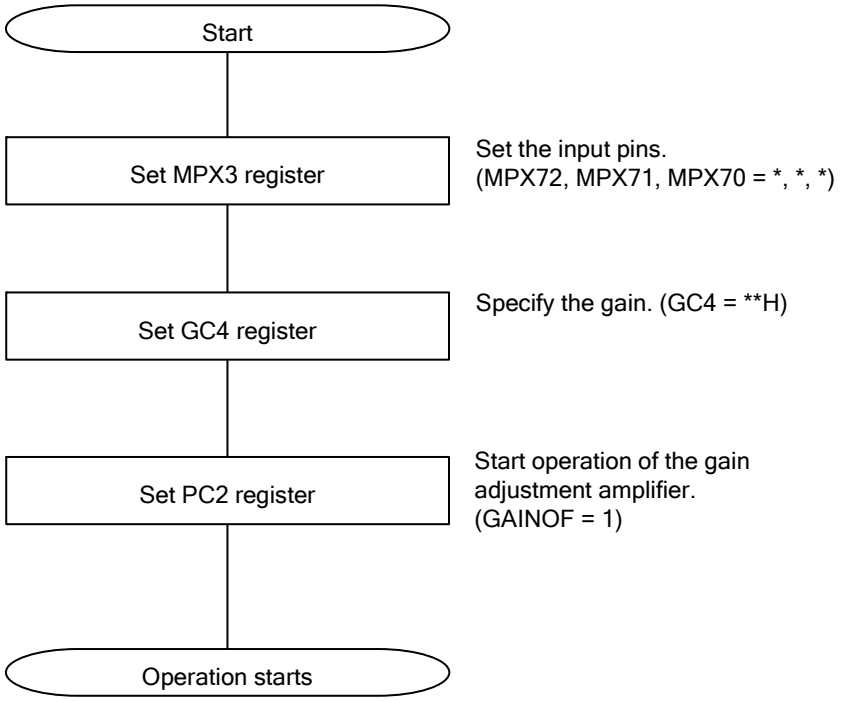
GAINOF	Operation of gain adjustment amplifier
0	Stop operation of the gain adjustment amplifier.
1	Enable operation of the gain adjustment amplifier.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

4. 2. 4 Procedure for operating the gain adjustment amplifier

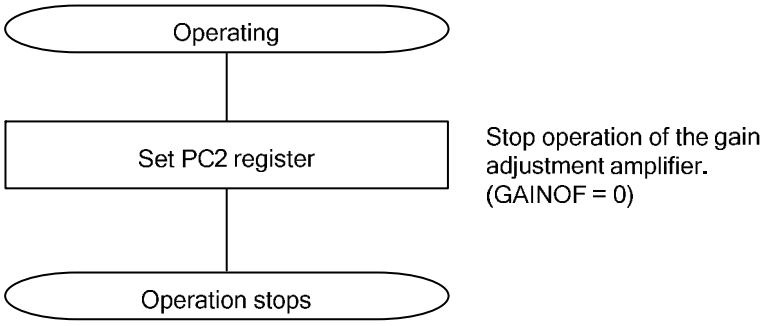
Follow the procedures below to start and stop the gain adjustment amplifier.

Example of procedure for starting the gain adjustment amplifier



Remark *: don't care

Example of procedure for stopping the gain adjustment amplifier



4. 3 D/A Converter

The RL78/G1E (64-pin products, 80-pin products) has four on-chip D/A converter channels.

4. 3. 1 Overview of D/A converter features

The D/A converters are 8-bit resolution converters that convert digital input signals into analog signals.

The D/A converters have the following features:

- 8-bit resolution (× 4 ch: Ch1 to Ch4)
- R-2R ladder method

<R>

- Analog output voltage: Output voltage can be calculated with the equation shown below.

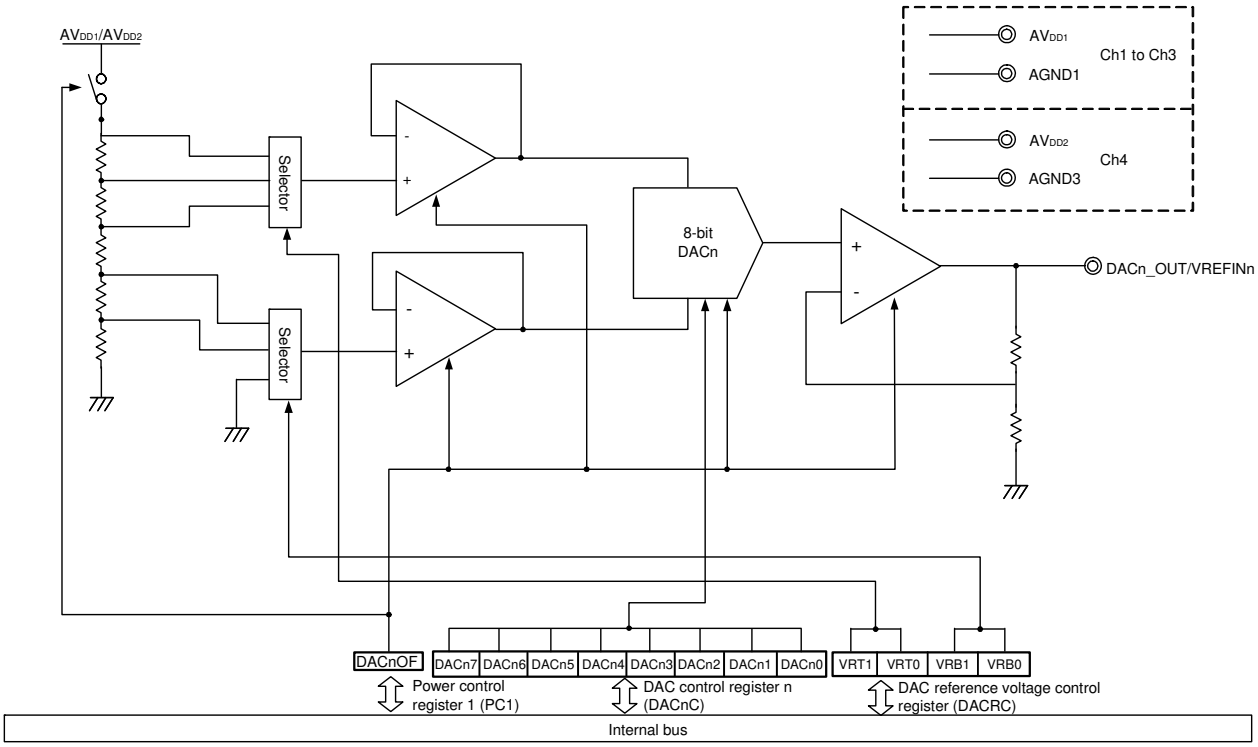
Output voltage = {(Reference voltage upper limit – Reference voltage lower limit) × m/256}
+ Reference voltage lower limit
(m = 0 to 255: Value set to DACnC register)

- Controls the reference voltage for the configurable amplifiers, gain adjustment amplifiers, low-pass filter, and high-pass filter **Note**
- Includes a power-off function.

Note 80-pin products only.

Remark n = 1 to 4

4. 3. 2 Block diagram



Remark: n = 1 to 4

4. 3. 3 Registers controlling the D/A converters

The D/A converters are controlled by the following 3 registers:

- DAC reference voltage control register (DACRC)
- DAC control registers 1, 2, 3, 4 (DAC1C, DAC2C, DAC3C, DAC4C)
- Power control register 1 (PC1)

(1) DAC reference voltage control register (DACRC)

This register is used to specify the upper (VRT) and lower (VRB) limits of the reference voltage for D/A converter channels Ch1 to Ch4.

When selecting the upper limit of the reference voltage, use bits 3 and 2. When selecting the lower limit of the reference voltage, use bits 1 and 0.

Reset signal input clears this register to 00H.

Address: 0CH After reset: 00H R/W

	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	VRT1	VRT0	VRB1	VRB0

<R>

VRT1	VRT0	Reference voltage upper limit (Typ.)
0	0	AV_{DD1}
0	1	$AV_{DD1} \times 4/5$
1	0	$AV_{DD1} \times 3/5$
1	1	AV_{DD1}

<R>

VRB1	VRB0	Reference voltage lower limit (Typ.)
0	0	AGND1
0	1	$AV_{DD1} \times 1/5$
1	0	$AV_{DD1} \times 2/5$
1	1	AGND1

Remarks 1. Bits 7 to 4 are fixed at 0 of read only.

2. To calculate the output voltage, see **4. 3. 1 Overview of D/A converter features**.

(2) DAC control registers 1, 2, 3, 4 (DAC1C, DAC2C, DAC3C, DAC4C)

This register is used to specify the analog voltage to be output to the DACn_OUT pin. The DACn_OUT output signal can be used as the reference voltage for the configurable amplifiers, gain adjustment amplifier, low-pass filter, and high-pass filter.

Reset signal input sets this register to 80H.

Address: 0DH (n = 1), 0EH (n = 2), 0FH (n = 3), 10H (n = 4) After reset: 80H R/W

	7	6	5	4	3	2	1	0
DACnC	DACn7	DACn6	DACn5	DACn4	DACn3	DACn2	DACn1	DACn0

Remarks 1. n = 1 to 4

2. To calculate the output voltage, see **4. 3. 1 Overview of D/A converter features**.

(3) Power control register 1 (PC1)

This register is used to enable or disable operation of the configurable amplifiers and the D/A converters. Use this register to stop unused functions to reduce power consumption and noise.

When using one of D/A converter channels Ch1 to Ch4, be sure to set the control bit that corresponds to the channel (bits 7 to 4) to 1.

Reset signal input clears this register to 00H.

Address: 11H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC1	DAC4OF	DAC3OF	DAC2OF	DAC1OF	0	AMP3OF	AMP2OF	AMP1OF

DAC4OF	Operation of D/A converter Ch4
0	Stop operation of D/A converter Ch4.
1	Enable operation of D/A converter Ch4.

DAC3OF	Operation of D/A converter Ch3
0	Stop operation of D/A converter Ch3.
1	Enable operation of D/A converter Ch3.

DAC2OF	Operation of D/A converter Ch2
0	Stop operation of D/A converter Ch2.
1	Enable operation of D/A converter Ch2.

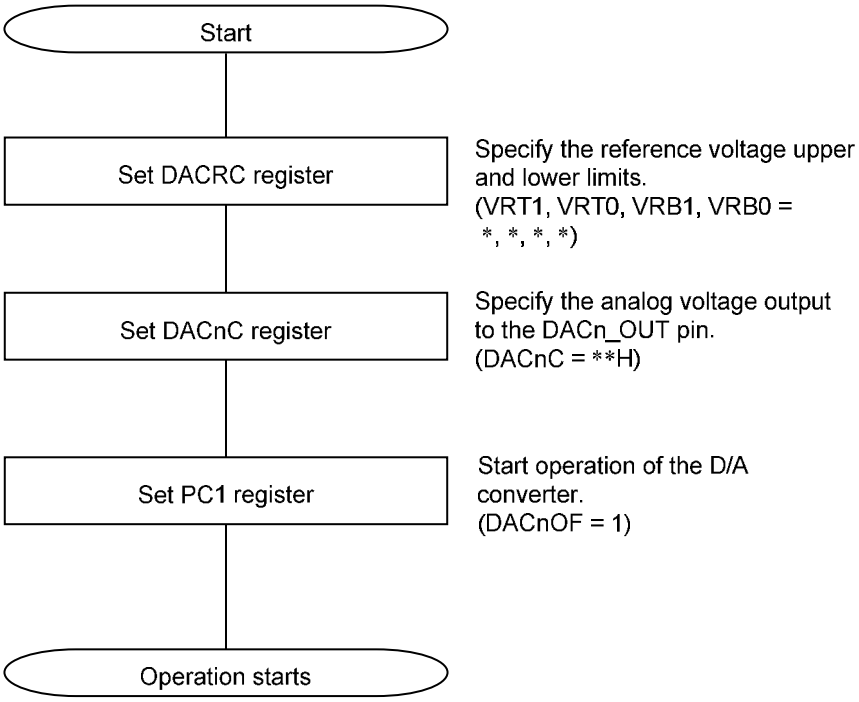
DAC1OF	Operation of D/A converter Ch1
0	Stop operation of D/A converter Ch1.
1	Enable operation of D/A converter Ch1.

Caution Be sure to clear bit 3 to "0".

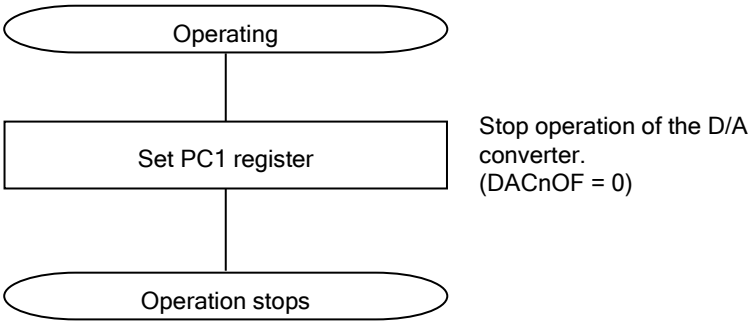
4. 3. 4 Procedure for operating the D/A converters

Follow the procedures below to start and stop the D/A converters.

Example of procedure for starting the D/A converters



Example of procedure for stopping the D/A converters



Remark *: don't care
n = 1 to 4

4. 3. 5 Notes on using D/A converters

Observe the following points when using the D/A converters:

(1) Only a very small current can flow from the DACn_OUT pin because the output impedance of the D/A converters is high. If the load input impedance is low, insert a follower amplifier between the load and the DACn_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

(2) If inputting an external reference power supply to the VREFINn pin, be sure to set the DACnOF bit to 0.

Remark n = 1 to 4

4. 4 Low-Pass Filter

The RL78/G1E (64-pin products, 80-pin products) has one on-chip switched-capacitor low-pass filter channel.

4. 4. 1 Overview of low-pass filter features

The features of low-pass filter are described below.

- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (f_C) range: 9 Hz to 4.5 kHz
- External input clock frequency (f_{CLK_LPF}) range: $f_C \times 2 / 0.009$ = 2 kHz to 1 MHz
<R> - Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for low-pass filter.

If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.

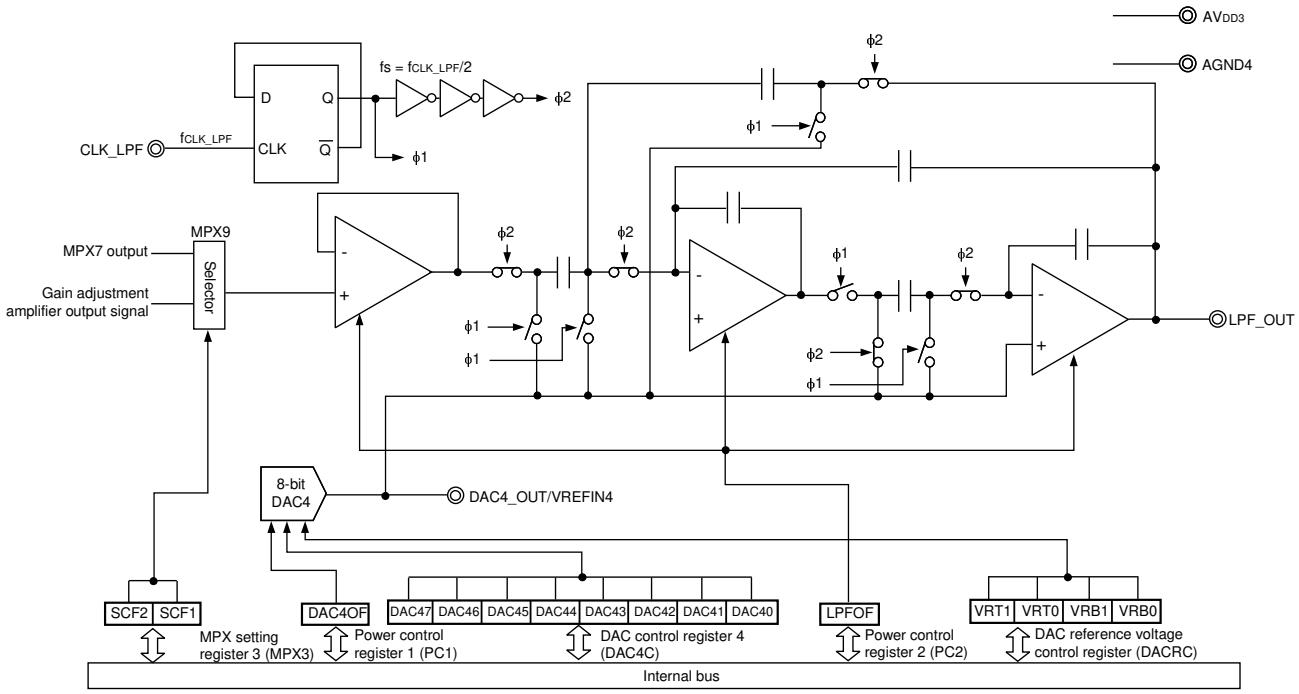
For details about use of D/A converter, see **4. 3 D/A Converter**.

Remarks 1. The internal control clock (f_S) of the low-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (f_S) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_LPF pin.

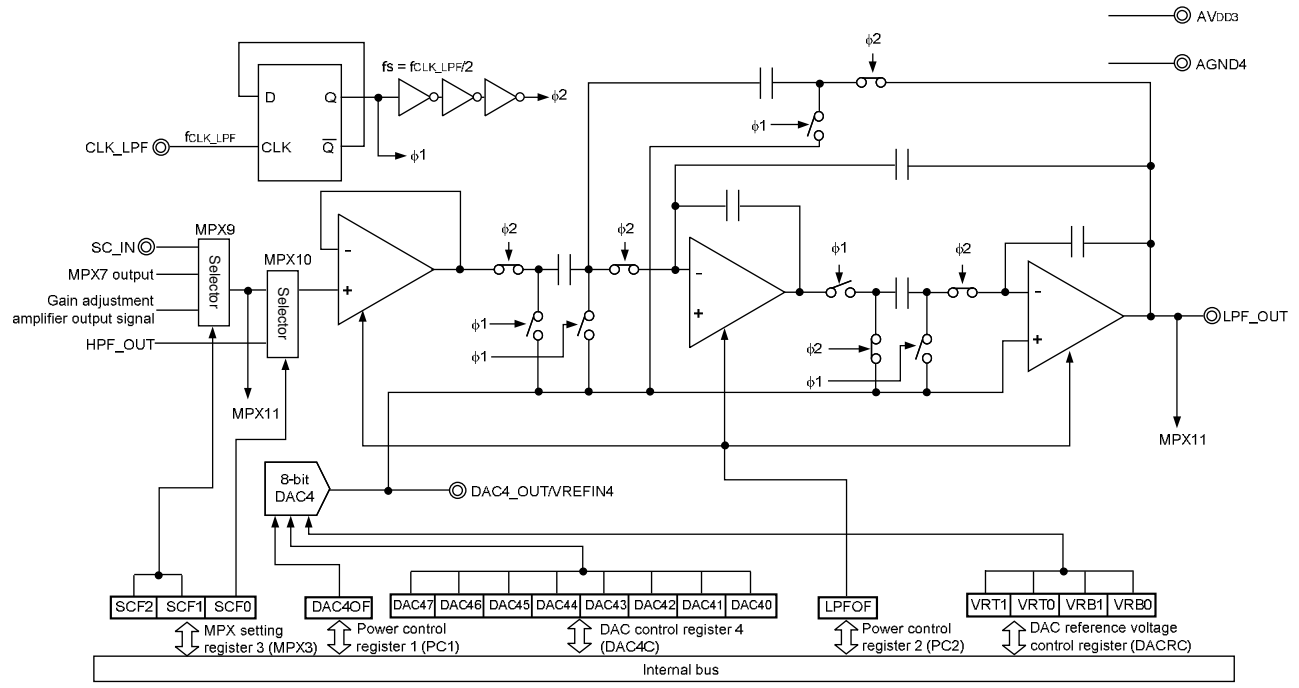
2. The phase of the signal input to the low-pass filter inverts after passing the low-pass filter.

4. 4. 2 Block diagram

- **64-pin products**



- **80-pin products**



<R> 4. 4. 3 Registers controlling the low-pass filter

The low-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

<R> This register is used to control MPX7, MPX9, MPX10, and MPX11.

When selecting the signal to be input to the filter circuits, use bits 5 and 4. When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	–
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

Caution Be sure to clear bit 3 to "0".

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

- **80-pin products**

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

<R> **Remark** Bits 7 and 6 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the low-pass filter, be sure to set bit 3 to 1.

Reset signal input clears this register to 00H.

- **64-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

LPFOF	Operation of low-pass filter
0	Stop operation of the low-pass filter.
1	Enable operation of the low-pass filter.

Caution Be sure to clear bit 2 to "0".

<R> **Remark** Bits 7 to 5 can be set to 1, but this has no effect on the function.

- **80-pin products**

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

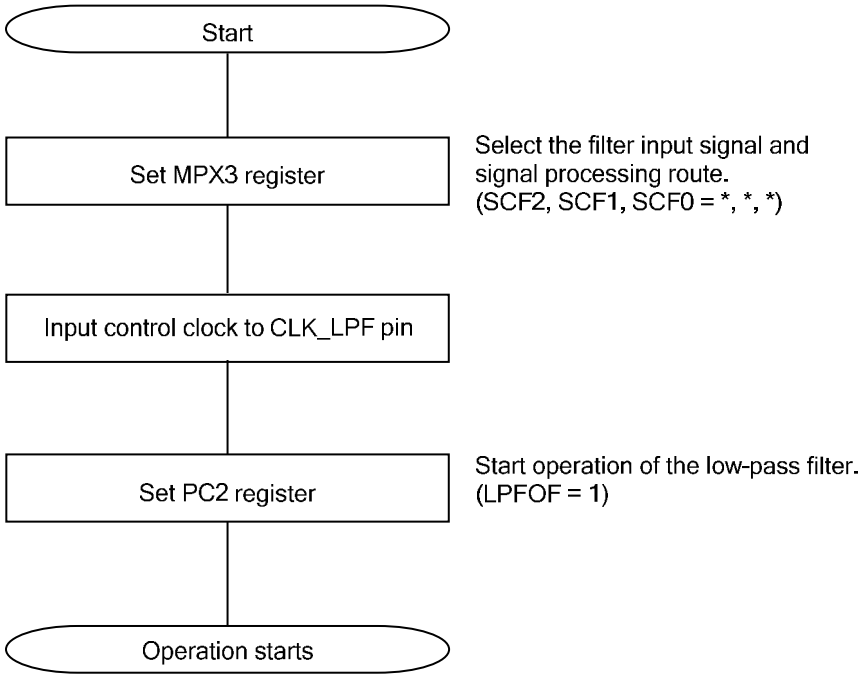
LPFOF	Operation of low-pass filter
0	Stop operation of the low-pass filter.
1	Enable operation of the low-pass filter.

<R> **Remark** Bits 7 to 5 can be set to 1, but this has no effect on the function.

4. 4. 4 Procedure for operating the low-pass filter

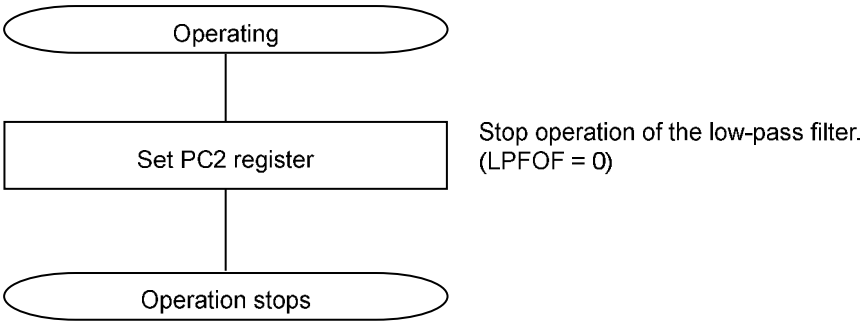
Follow the procedures below to start and stop the low-pass filter.

Example of procedure for starting the low-pass filter



Remark *: don't care

Example of procedure for stopping the low-pass filter



4. 5 High-Pass Filter

The RL78/G1E (80-pin products) has one on-chip switched-capacitor high-pass filter channel [Note].

Note The high-pass filter is not provided in the RL78/G1E (64-pin products).

4. 5. 1 Overview of high-pass filter features

The features of high-pass filter are described below.

- Butterworth characteristics (Q value = 0.702)
- Cutoff frequency (f_C) range: 8 Hz to 800 Hz
- External input clock frequency (f_{CLK_HPF}) range: $f_C \times 2 / 0.008$ = 2 kHz to 200 kHz
<R> - Includes a power-off function.

And also, the DAC4_OUT output signals can be used as the reference voltage for high-pass filter.

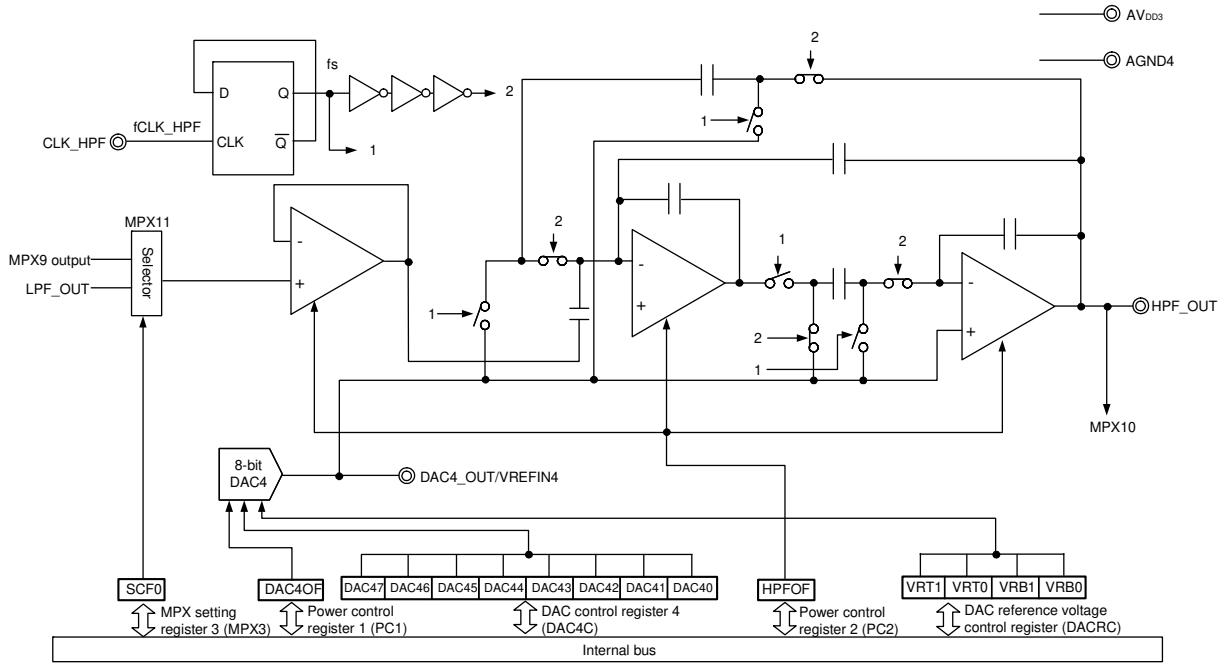
If D/A converter is powered off, the external reference voltage is to be input to DAC4_OUT/VREFIN4 pin.

For details about use of D/A converter, see **4. 3 D/A Converter**.

Remarks 1. The internal control clock (f_S) of the high-pass filter has a duty of 50%, so the external input clock is divided by two at the internal D flip-flop before being used for the low-pass filter. If the internal control clock frequency (f_S) is 100 kHz, therefore, input a 200 kHz clock signal to the CLK_HPF pin.

2. The phase of the signal input to the high-pass filter inverts after passing the high-pass filter.

4. 5. 2 Block diagram



4. 5. 3 Registers controlling the high-pass filter

<R> The high-pass filter is controlled by the following 2 registers:

- MPX setting register 3 (MPX3)
- Power control register 2 (PC2)

(1) MPX setting register 3 (MPX3)

This register is used to control MPX7, MPX9, MPX10, and MPX11.

<R> When selecting the signal to be input to the filter circuits, use bits 5 and 4. When switching the order in which signals are processed by the low-pass and high-pass filters, use bit 3.

- 80-pin products

Address: 05H After reset: 00H R/W

	7	6	5	4	3	2	1	0
MPX3	0	0	SCF2	SCF1	SCF0	MPX72	MPX71	MPX70

<R>

SCF2	SCF1	Source of input to filter circuits
0	0	SC_IN pin
0	1	MPX7 output signal
1	0	Gain adjustment amplifier output signal
1	1	Setting prohibited

SCF0	Specification of the order of filter signal processing
0	The MPX9 output signal passes the low-pass filter and then is input to the high-pass filter.
1	The MPX9 output signal passes the high-pass filter and then is input to the low-pass filter.

Remark Bits 7 and 6 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the high-pass filter, be sure to set bit 2 to 1.

Reset signal input clears this register to 00H.

- 80-pin products

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

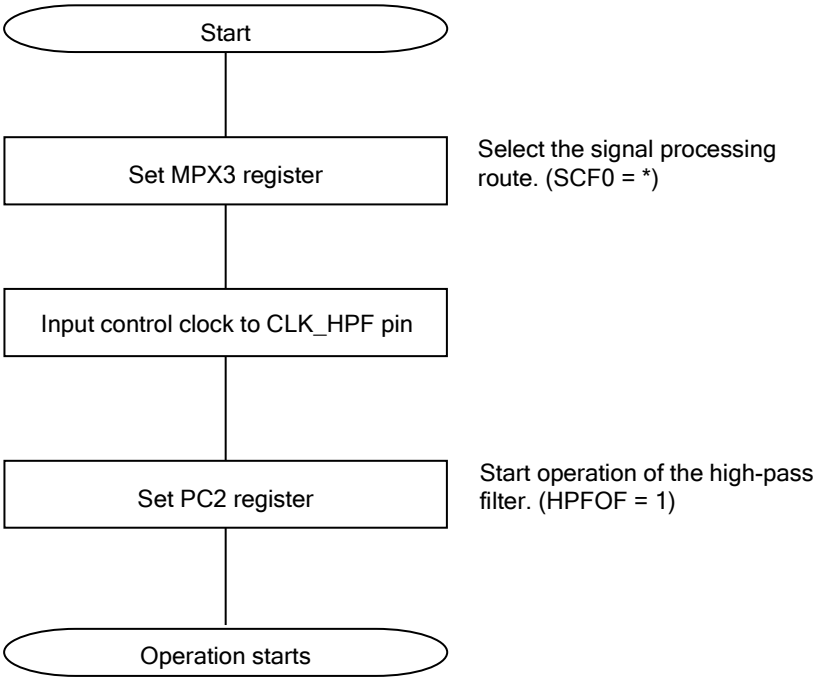
HPFOF	Operation of high-pass filter
0	Stop operation of the high-pass filter.
1	Enable operation of the high-pass filter.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

4. 5. 4 Procedure for operating the high-pass filter

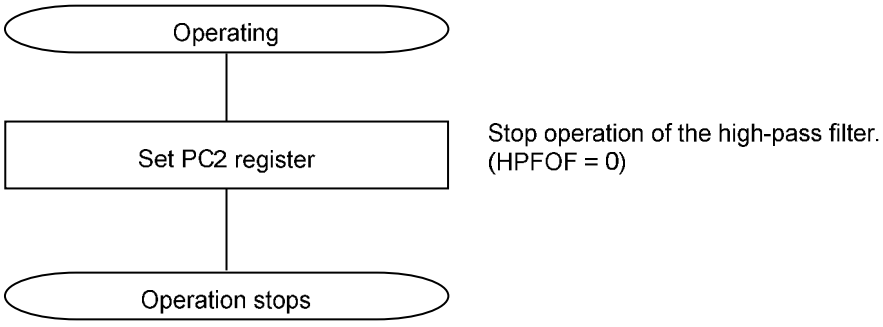
Follow the procedures below to start and stop the high-pass filter.

Example of procedure for starting the high-pass filter



Remark *: don't care

Example of procedure for stopping the high-pass filter



4 .6 Temperature Sensor

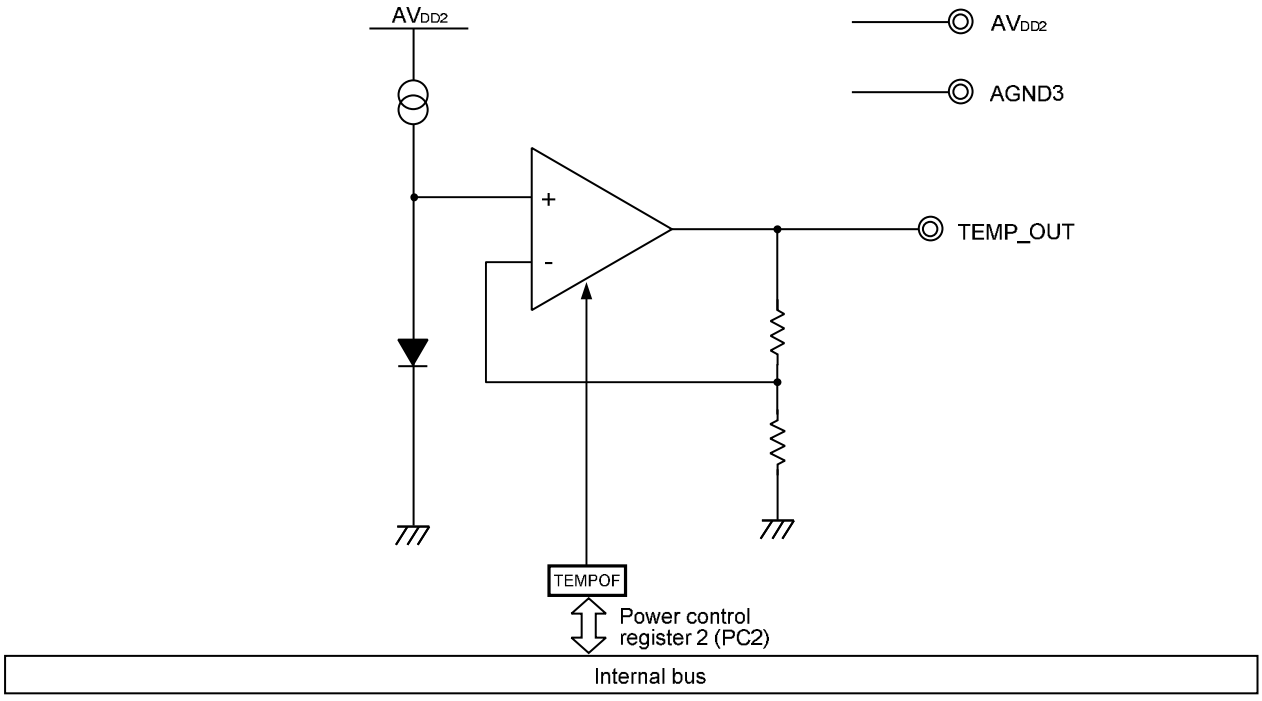
The RL78/G1E (64-pin products, 80-pin products) has one on-chip temperature sensor channel.

4. 6. 1 Overview of temperature sensor features

The features of temperature sensor are described below.

- Output voltage temperature coefficient: –5 mV/°C (Typ.)
- Includes a power-off function.

4. 6. 2 Block diagram



4. 6. 3 Registers controlling the temperature sensor

The temperature sensor is controlled by power control register 2 (PC2).

(1) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.

Reset signal input clears this register to 00H.

- 64-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Caution Be sure to clear bit 2 to "0".

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

- 80-pin products

Address: 12H After reset: 00 R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

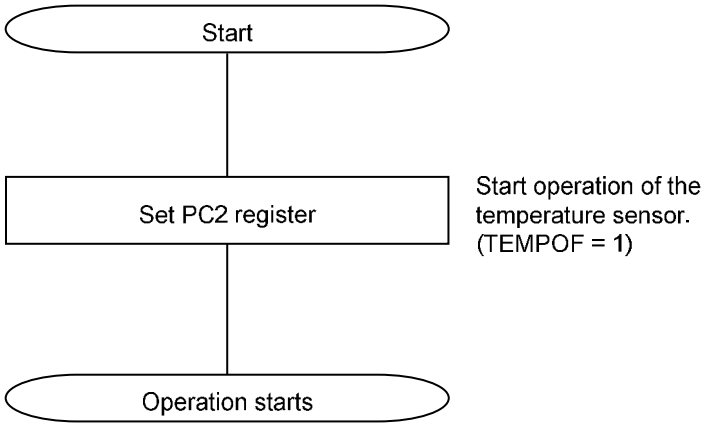
TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 7 to 5 can be set to 1, but this has no effect on the function.

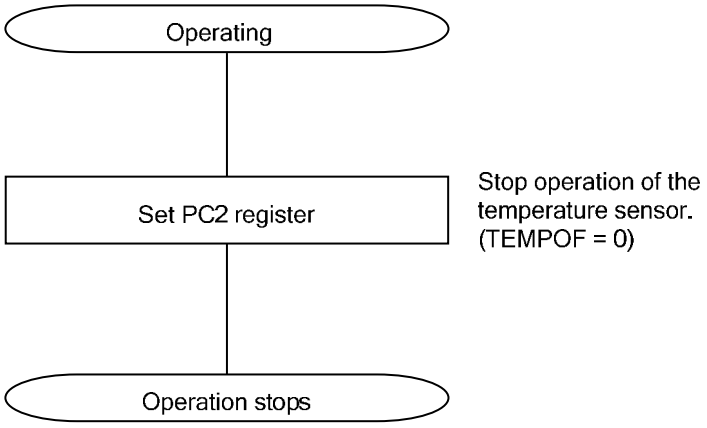
4. 6. 4 Procedure for operating the temperature sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor



Example of procedure for stopping the temperature sensor



4. 7 Variable Output Voltage Regulator

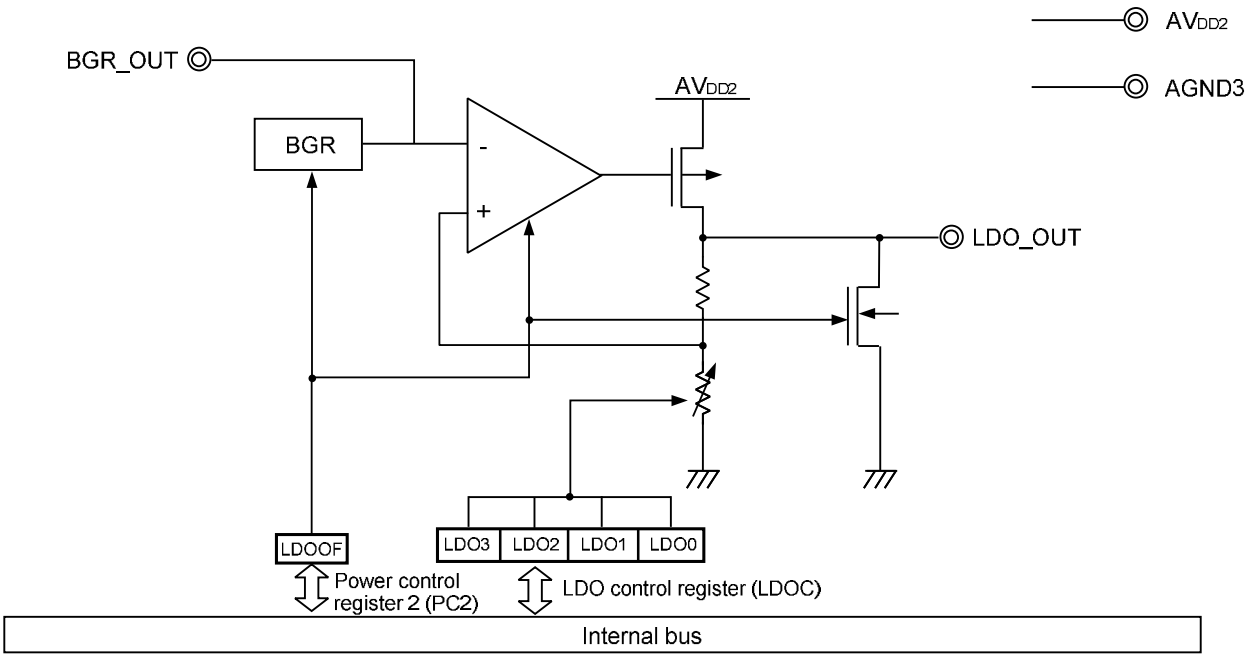
The RL78/G1E (64-pin products, 80-pin products) has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 3.3 V (default) from a supplied voltage of 5 V.

4. 7. 1 Overview of variable output voltage regulator features

The features of variable output voltage regulator are described below.

- Output voltage range: 2.0 to 3.3 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

4. 7. 2 Block diagram



4. 7. 3 Registers controlling the variable output voltage regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- Power control register 2 (PC2)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.

Reset signal input sets this register to 0DH.

Address: 0BH After reset: 0DH R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output Voltage of Variable Output Voltage Regulator (Typ.)
0	0	0	0	2.0 V
0	0	0	1	2.1 V
0	0	1	0	2.2 V
0	0	1	1	2.3 V
0	1	0	0	2.4 V
0	1	0	1	2.5 V
0	1	1	0	2.6 V
0	1	1	1	2.7 V
1	0	0	0	2.8 V
1	0	0	1	2.9 V
1	0	1	0	3.0 V
1	0	1	1	3.1 V
1	1	0	0	3.2 V
1	1	0	1	3.3 V Note
Other than above				Setting prohibited

Note Output voltage of 3.3 V is available when the power supply voltage is more than 4 V.

<R> **Remark** Bits 7 to 4 are fixed at 0 of read only.

(2) Power control register 2 (PC2)

This register is used to enable or disable operation of the gain adjustment amplifier, the low-pass filter, the high-pass filter, the variable output voltage regulator, the reference voltage generator, and the temperature sensor. Use this register to stop unused functions to reduce power consumption and noise.

When using the variable output voltage regulator and reference voltage generator, be sure to set bit 1 to 1.

Reset signal input clears this register to 00H.

- 64-pin products

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	0	LDOOF	TEMPOF

LDOOF	Operation of variable output voltage regulator and reference voltage generator
0	Stop operation of the variable output voltage regulator and reference voltage generator.
1	Enable operation of the variable output voltage regulator and reference voltage generator.

Caution Be sure to clear bit 2 to "0".

<R> **Remark** Bits 7 to 5 can be set to 1, but this has no effect on the function.

- 80-pin products

Address: 12H After reset: 00H R/W

	7	6	5	4	3	2	1	0
PC2	0	0	0	GAINOF	LPFOF	HPFOF	LDOOF	TEMPOF

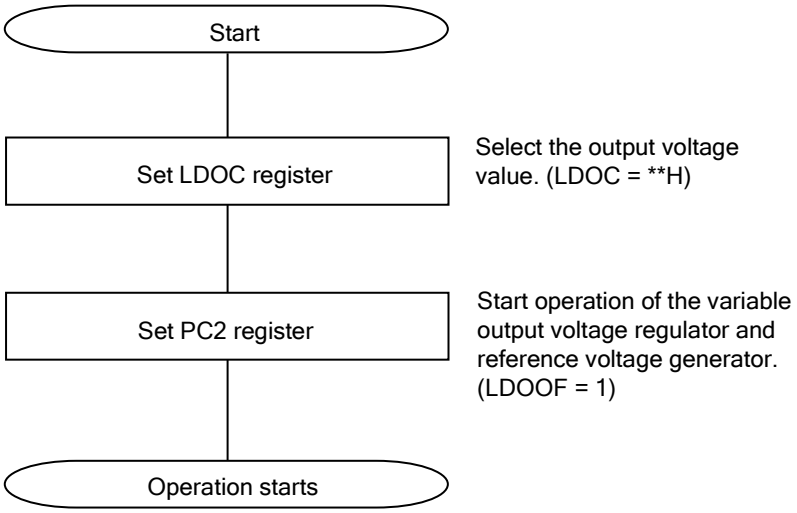
LDOOF	Operation of variable output voltage regulator and reference voltage generator
0	Stop operation of the variable output voltage regulator and reference voltage generator.
1	Enable operation of the variable output voltage regulator and reference voltage generator.

<R> **Remark** Bits 7 to 5 can be set to 1, but this has no effect on the function.

4. 7. 4 Procedure for operating the variable output voltage regulator

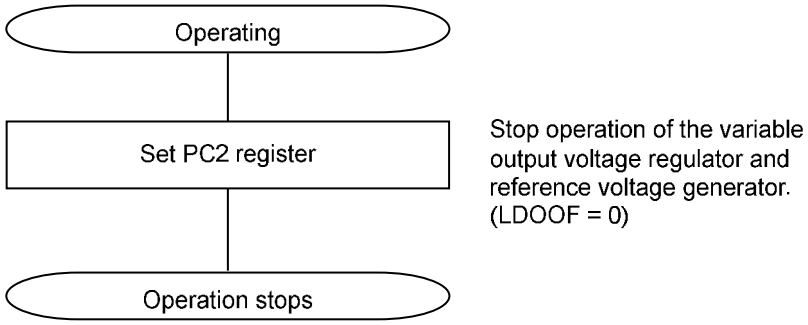
Follow the procedures below to start and stop the variable output voltage regulator and reference voltage generator.

Example of procedure for starting the variable output voltage regulator and reference voltage generator



Remark *: don't care

Example of procedure for stopping the variable output voltage regulator and reference voltage generator



4. 8 Reference Voltage Generator

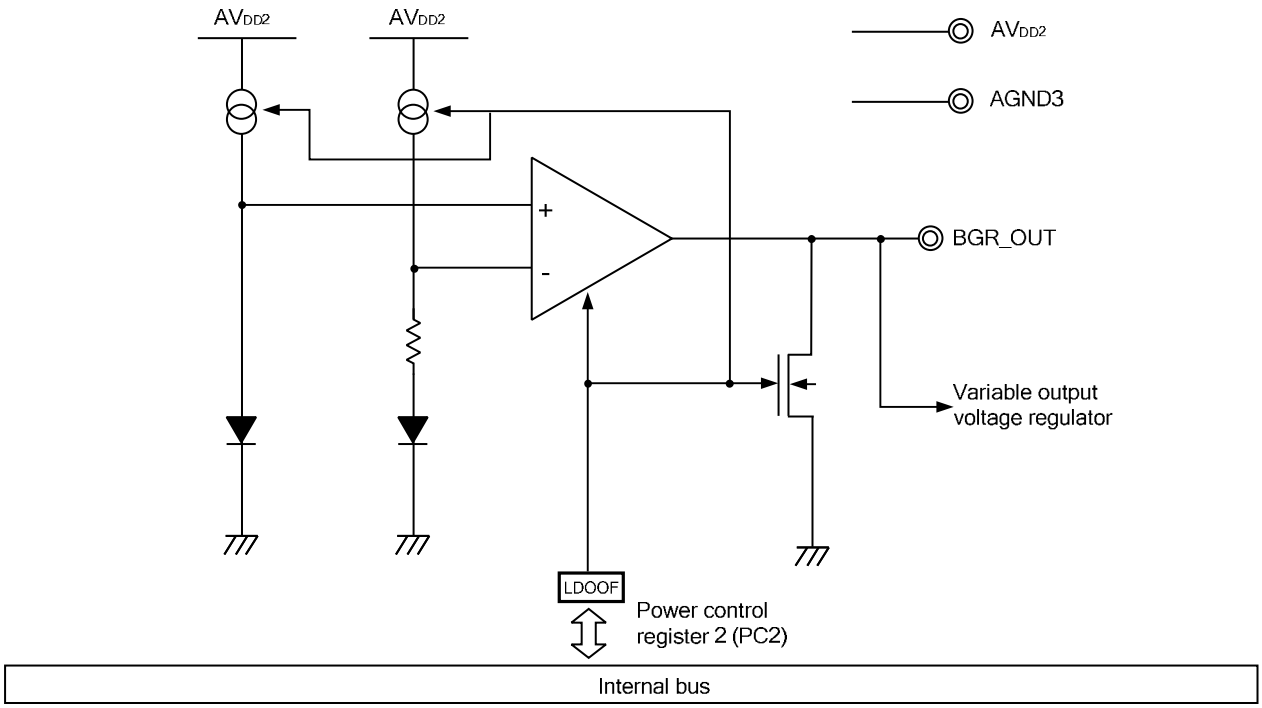
The RL78/G1E (64-pin products, 80-pin products) has one on-chip reference voltage generator channel.

4. 8. 1 Overview of reference voltage generator features

<R> The features of reference voltage generator are described below.

- Output reference voltage: 1.21 V (Typ.)
- Includes a power-off function.

4. 8. 2 Block diagram



4. 8. 3 Registers controlling the reference voltage generator

The reference voltage generator is controlled by power control register 2 (PC2).

For details about the setting of power control register 2, see **4. 7. 3 (2) Power control register 2 (PC2)**.

4. 8. 4 Procedure for operating the reference voltage generator

For details about the procedures to start and stop the reference voltage generator, see **4. 7. 4 Procedure for operating the variable output voltage regulator**.

4. 8. 5 Notes on using the reference voltage generator

Observe the following points when using the reference voltage generator:

(1) Only a very small current can flow from the BGR_OUT pin because the output impedance of the reference voltage generator is high. If the load input impedance is low, insert a follower amplifier between the load and the BGR_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

4. 9 SPI

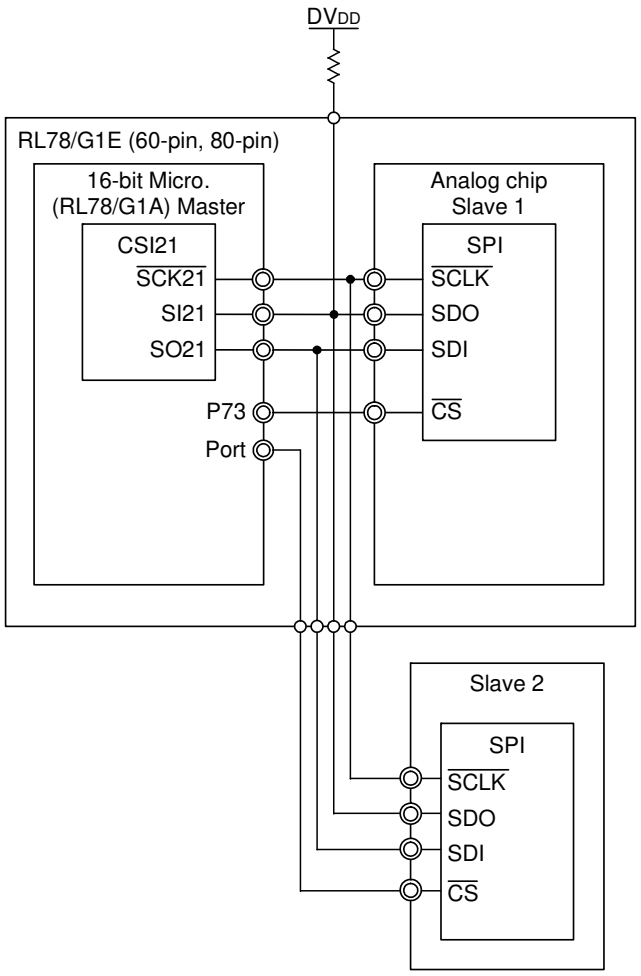
4. 9. 1 Overview of SPI features

The SPI interface is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{SCLK}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{CS}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 4-4. SPI Configuration Example



Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{RESET}$ pin before starting SPI communication. For details, see 4.10 Analog Reset.

4. 9. 2 SPI communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{CS}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{SCLK}$ has been detected following the fall of $\overline{CS}$, and the operation specified by the data is executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{SCLK}$ following the fall of $\overline{CS}$.

Figure 4-5. SPI Communication Timing

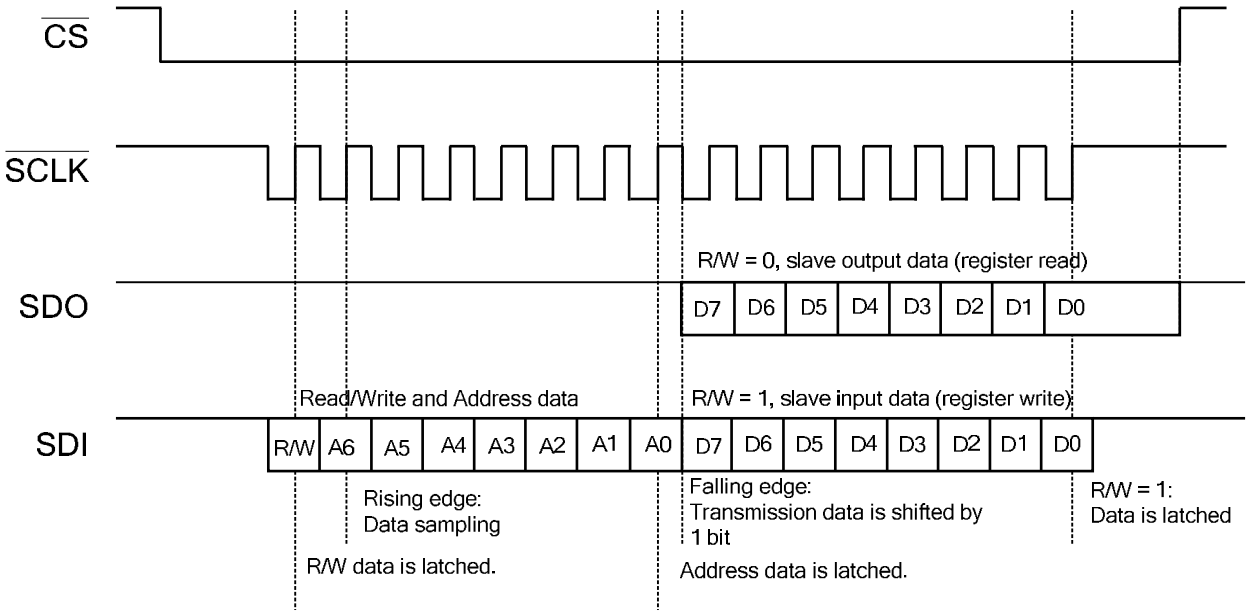


Table 4-11. SPI Control Registers

Address	SPI Control Register	R/W	After Reset
00H	Configuration register 1 (CONFIG1)	R/W	00H
01H	Configuration register 2 (CONFIG2)	R/W	00H
03H	MPX setting register 1 (MPX1)	R/W	00H
04H	MPX setting register 2 (MPX2)	R/W	00H
05H	MPX setting register 3 (MPX3)	R/W	00H
06H	Gain control register 1 (GC1)	R/W	00H
07H	Gain control register 2 (GC2)	R/W	00H
08H	Gain control register 3 (GC3)	R/W	00H
09H	AMP operation mode control register (AOMC)	R/W	00H
0AH	Gain control register 4 (GC4)	R/W	00H
0BH	LDO control register (LDOC)	R/W	0DH
0CH	DAC reference voltage control register (DACRC)	R/W	00H
0DH	DAC control register 1 (DAC1C)	R/W	80H
0EH	DAC control register 2 (DAC2C)	R/W	80H
0FH	DAC control register 3 (DAC3C)	R/W	80H
10H	DAC control register 4 (DAC4C)	R/W	80H
11H	Power control register 1 (PC1)	R/W	00H
12H	Power control register 2 (PC2)	R/W	00H
13H	Reset control register (RC)	R/W	00H[Note]

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register. For details, see **4. 10 Analog Reset.**

4. 10 Analog Reset

4. 10. 1 Overview of analog reset feature

The RL78/G1E (64-pin products, 80-pin products) has an on-chip analog reset function. The SPI control registers of analog block are initialized by analog reset. Reset can be generated in the following two ways:

- External reset by inputting an external reset signal to the $\overline{\text{ARESET}}$ pin
- Internal reset by writing 1 to the RESET bit of the reset control register (RC)

The functions of the external reset and the internal reset are described below.

- After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{ARESET}}$ pin before starting SPI communication. For the details of $\overline{\text{ARESET}}$ pin, see **2. 5. 31 $\overline{\text{ARESET}}$**.
- During analog reset, each function of analog block is shifted to the status shown in Table 4-12. The status of each SPI control register after analog reset has been acknowledged is shown in Table 4-13. After analog reset, the status of each pin is shown in Table 4-14.
- External reset is generated when a low-level signal is input to the $\overline{\text{ARESET}}$ pin. On the other hand, internal reset is generated when 1 is written to the RESET bit of the reset control register (RC).
- External reset is subsequently cancelled by inputting a high-level signal to $\overline{\text{ARESET}}$ pin after a low-level signal is input to this pin. On the other hand, internal reset is subsequently cancelled by writing 0 to the RESET bit of the reset control register (RC) after 1 is written to the same bit of this register.

<R> **Cautions When generating an external reset, input a low-level signal to the $\overline{\text{ARESET}}$ pin for at least 10 μs.**

Table 4-12. Statuses during Analog Reset

Function Block	External Reset from $\overline{\text{ARESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Configurable amplifier	Operation stops.	
Gain adjustment amplifier	Operation stops.	
D/A converter	Operation stops.	
Low-pass filter	Operation stops.	
High-pass filter Note	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
Reference voltage generator	Operation stops.	
SPI	Operation stops.	Operation enabled.

Note 80-pin products only.

Table 4-13. Statuses of SPI Control Registers after Analog Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	Configuration register 1 (CONFIG1)	00H	00H
01H	Configuration register 2 (CONFIG2)	00H	00H
03H	MPX setting register 1 (MPX1)	00H	00H
04H	MPX setting register 2 (MPX2)	00H	00H
05H	MPX setting register 3 (MPX3)	00H	00H
06H	Gain control register 1 (GC1)	00H	00H
07H	Gain control register 2 (GC2)	00H	00H
08H	Gain control register 3 (GC3)	00H	00H
09H	AMP operation mode control register (AOMC)	00H	00H
0AH	Gain control register 4 (GC4)	00H	00H
0BH	LDO control register (LDOC)	0DH	0DH
0CH	DAC reference voltage control register (DACRC)	00H	00H
0DH	DAC control register 1 (DAC1C)	80H	80H
0EH	DAC control register 2 (DAC2C)	80H	80H
0FH	DAC control register 3 (DAC3C)	80H	80H
10H	DAC control register 4 (DAC4C)	80H	80H
11H	Power control register 1 (PC1)	00H	00H
12H	Power control register 2 (PC2)	00H	00H
13H	Reset control register (RC)	00H	01H Note

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or writing 0 to the RESET bit of the reset control register (RC)..

Table 4-14. Pin Statuses after Analog Reset

Pin Name	External Reset from $\overline{\text{ARESET}}$ Pin	Internal Reset by Reset Control Register (RC)
SC_IN	Hi-Z	Hi-Z
CLK_SYNCH	Pull-down input	Pull-down input
SYNCH_OUT	Hi-Z	Hi-Z
GAINAMP_OUT	Hi-Z	Hi-Z
GAINAMP_IN	Hi-Z	Hi-Z
MPXIN61	Hi-Z	Hi-Z
MPXIN51	Hi-Z	Hi-Z
MPXIN60	Hi-Z	Hi-Z
MPXIN50	Hi-Z	Hi-Z
AMP3_OUT	Hi-Z	Hi-Z
DAC3_OUT/VREFIN3	Pull-down input	Pull-down input
AMP2_OUT	Hi-Z	Hi-Z
AMP1_OUT	Hi-Z	Hi-Z
DAC2_OUT/VREFIN2	Pull-down input	Pull-down input
DAC1_OUT/VREFIN1	Pull-down input	Pull-down input
MPXIN41	Hi-Z	Hi-Z
MPXIN31	Hi-Z	Hi-Z
MPXIN40	Hi-Z	Hi-Z
MPXIN30	Hi-Z	Hi-Z
MPXIN21	Hi-Z	Hi-Z
MPXIN11	Hi-Z	Hi-Z
MPXIN20	Hi-Z	Hi-Z
MPXIN10	Hi-Z	Hi-Z
BGR_OUT	Pull down	Pull down
LDO_OUT	Pull down	Pull down
TEMP_OUT	Pull down	Pull down
$\overline{\text{SCLK}}$	Hi-Z	Pull-up input
SDO	Hi-Z (open drain)	Hi-Z (open drain)
SDI	Hi-Z	Pull-up input
$\overline{\text{CS}}$	Hi-Z	Pull-up input
<R> DAC4_OUT/VREFIN4	Pull-down input	Pull-down input
HPF_OUT	Hi-Z	Hi-Z
CLK_HPF	Pull-down input	Pull-down input
CLK_LPF	Pull-down input	Pull-down input
LPF_OUT	Hi-Z	Hi-Z

4. 10. 2 Registers controlling the analog reset

(1) Reset control register (RC)

This register is used to control the reset feature in the analog block.

<R> An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is not initialized by generating internal reset of the reset control register, but it can be done by generating external reset from $\overline{\text{ARESET}}$ pin. External reset from $\overline{\text{ARESET}}$ pin clears this register to 00H.

Address: 13H After reset: 00H Note R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

<R> **Note** The reset control register is not initialized by generating internal reset of the reset control register, but it can be done to 00H by generating external reset from $\overline{\text{ARESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enables writing to all the registers.

<R> **Remark** Bits 7 to 1 are fixed at 0 of read only.

CHAPTER 5 ELECTRICAL SPECIFICATIONS

In this capter, the electrical specification is described for the target products shown below.

Target products A: Consumer applications T_A = −40 to +85°C
R5F10FLCANA, R5F10FLCANA, R5F10FLDANA, R5F10FLDANA,
R5F10FLEANA, R5F10FLEANA, R5F10FMCAFB, R5F10FMCAFB,
R5F10FMDAFB, R5F10FMDAFB, R5F10FMEAFB, R5F10FMEAFB

Target products D: Industrial applications T_A = −40 to +85°C
R5F10FLCDNA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLDDNA,
R5F10FLEDNA, R5F10FLEDNA, R5F10FMCDFB, R5F10FMCDFB,
R5F10FMDDFB, R5F10FMDDFB, R5F10FMEDFB, R5F10FMEDFB

Cautions 1. The RL78/G1E microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product, so that refer to CHAPTER 2 PIN FUNCTIONS. In this Chapter, most of the descriptions use the case of 80-pin products as an example.

5. 1 Absolute Maximum Ratings

5. 1. 1 Absolute maximum ratings of microcontroller block

Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.5 to +6.5	V
	AV_{DD}			−0.5 to +4.6	V
	AV_{REFP}			−0.3 to AV_{DD} +0.3 Note 3	V
	AV_{SS}			−0.5 to +0.3	V
	AV_{REFM}			−0.3 to AV_{DD} +0.3 Note 3 and $AV_{REFM} \leq AV_{REFP}$	V
REGC pin input voltage	V_{IREGC}	REGC		−0.3 to 2.8 and −0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140		−0.3 to V_{DD} + 0.3 Note 2	V
	V_{I3}	P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		−0.3 to V_{DD} + 0.3 Note 2	V
	V_{I4}	P20 to P24		−0.3 to AV_{DD} + 0.3 Note 3	V
	V_{I5}	I.C pin		−0.5 to +0.3	V
Output voltage	V_{O1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P130, P140		−0.3 to V_{DD} + 0.3 Note 2	V
	V_{O2}	P20 to P24		−0.3 to AV_{DD} + 0.3 Note 3	V
Analog input voltage	V_{AI1}	ANI16 to ANI18, ANI20 to ANI26, ANI28, ANI30		−0.3 to V_{DD} + 0.3 and -0.3 to $AV_{REF(+)}$ + 0.3 Note 2, 4	V
	V_{AI2}	ANI0 to ANI4		−0.3 to AV_{DD} + 0.3 and -0.3 to $AV_{REF(+)}$ + 0.3 Note 3, 4	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins: −170 mA	P00 to P04, P40 to P42, P130, P140	−70	mA
			P10 to P15, P50, P51, P70 to P73	−100	mA
	I_{OH2}	Per pin	ANI0 to ANI4	−0.1	mA
		Total of all pins		−1.3	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins: 170 mA	P00 to P04, P40 to P42, P130, P140	70	mA
			P10 to P15, P50, P51, P70 to P73	100	mA
	I_{OL2}	Per pin	ANI0 to ANI4	0.4	mA
		Total of all pins		6.4	mA

(**Notes**, **Causion** and **Remarks** are listed on the next page.)

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not apply any external voltage to this pin.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

4. Do not exceed $AV_{REF(+)}$+0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D Conveter.

3. V_{SS} is reference voltage.

5. 1. 2 Absolute maximum ratings of analog block

Absolute maximum ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	AV_{DDA}	AV_{DD1}, AV_{DD2}, AV_{DD3}	−0.3 to +6.0	V
	DV_{DD}	DV_{DD}	−0.3 to +6.0	V
	AGND	AGND1, AGND2, AGND3, AGND4	−0.3 to +0.3	V
	DGND	DGND	−0.3 to +0.3	V
Input voltage	V_{I1}	MPXIN10, MPXIN11, MPXIN20, MPXIN21, MPXIN30, MPXIN31, MPXIN40, MPXIN41, MPXIN50, MPXIN51, MPXIN60, MPXIN61, SC_IN, CLK_SYNCH, VREFIN1, VREFIN2, VREFIN3, VREFIN4, CLK_LPF, CLK_HPF, $\overline{\text{RESET}}$	−0.3 to AV_{DDA} + 0.3[Note]	V
	V_{I2}	$\overline{\text{SCLK}}$, SDI, $\overline{\text{CS}}$	−0.3 to DV_{DD} + 0.3[Note]	V
Output voltage	V_{O1}	LDO_OUT, BGR_OUT, AMP1_OUT, AMP2_OUT, AMP3_OUT, GAINAMP_OUT, SYNCH_OUT, LPF_OUT, HPF_OUT, DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	−0.3 to AV_{DDA} + 0.3[Note]	V
	V_{O2}	SDO	−0.3 to DV_{DD} + 0.3[Note]	V
Output current	I_{O1}	AMP1_OUT, AMP2_OUT, AMP3_OUT, GAINAMP_OUT, SYNCH_OUT LPF_OUT, HPF_OUT DAC1_OUT, DAC2_OUT, DAC3_OUT, DAC4_OUT, TEMP_OUT	1	mA
	I_{O2}	SDO	−10	mA
	I_{LDOOUT}	LDO_OUT	15	mA

Note Must be 6.0 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> **5. 1. 3 Absolute maximum ratings (common to microcontroller block and analog block)**

Absolute maximum ratings

Parameter	Symbol	Conditions	Ratings	Unit
Operating ambient temperature	T_A	In normal operation mode	−40 to +85	°C
		In flash memory programming mode	−40 to +85	°C
Storage temperature	T_{stg}		−40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

5. 2 Electrical Specifications of Microcontroller Block

5. 2. 1 Oscillator characteristics

5. 2. 1. 1 X1 oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

<R>

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator / Crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	

<R> **Note** Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time. Also, be sure to apply to the resonator manufacturer for evaluation on the actual circuit so as to confirm the oscillation characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

<R> **Remark** When using the X1 oscillator, see **3. 5. 4 System clock oscillator**.

<R> 5. 2. 1. 2 On-chip oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to + 85 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	− 1.0		+ 1.0	%
			1.6 V ≤ V_{DD} ≤ 1.8 V	− 5.0		+ 5.0	%
		−40 to − 20 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	− 1.5		+ 1.5	%
			1.6 V ≤ V_{DD} ≤ 1.8 V	− 5.5		+ 5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				− 15		+ 15	%

Notes 1. Frequency can be selected in a high-speed on-chip oscillator. Selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. Indicates only permissible frequency level. Refer to AC Characteristics for instruction execution time.

5. 2. 2 DC characteristics

5. 2. 2. 1 Pin characteristics

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P04, P10 to P15, P40 to P42, P50, P51, P130, P140	1.6 V ≤ V_{DD} ≤ 5.5 V			−10.0[Note 2]	mA
		Per pin for P70 to P73	1.6 V ≤ V_{DD} ≤ 5.5 V			−3.0[Note 2]	mA
		Total of P00 to P04, P40 to P42, P130, P140 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−55.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−10.0	
			1.8 V ≤ V_{DD} < 2.7 V			−5.0	
			1.6 V ≤ V_{DD} < 1.8 V			−2.5	
		Total of P10 to P15, P50, P51, P70 to P73 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			−80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			−19.0	
			1.8 V ≤ V_{DD} < 2.7 V			−10.0	
			1.6 V ≤ V_{DD} < 1.8 V			−5.0	
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ V_{DD} ≤ 5.5 V			−100.0	mA
	I_{OH2}	Per pin for P20 to P24	1.6 V ≤ AV_{DD} ≤ 3.6 V			−0.1[Note 2]	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ AV_{DD} ≤ 3.6 V			−1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty ≤ 70%.
The output current value that has changed the duty ratio > 70% can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7) / (n × 0.01)

<Example> When I_{OH} = −10.0 mA and n = 80%

Total output current of pins = (-10.0 × 0.7) / (80 × 0.01) ≅ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15 and P50 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P04, P10 to P15, P40 to P42, P50 to P51, P130, P140	1.6 V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Per pin for P70 to P73	1.6 V ≤ V_{DD} ≤ 5.5 V			3.0[Note 2]	mA
		Total of P00 to P04, P40 to P42, P130, P140 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	
			1.8 V ≤ V_{DD} < 2.7 V			9.0	
			1.6 V ≤ V_{DD} < 1.8 V			4.5	
		Total of P10 to P15, P50, P51, P70 to P73 (When duty = 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	
			1.8 V ≤ V_{DD} < 2.7 V			20.0	
			1.6 V ≤ V_{DD} < 1.8 V			10.0	
		Total of all pins[Note 3]	1.6 V ≤ V_{DD} ≤ 5.5 V			150.0	mA
	I_{OL2}	Per pin for P20 to P24	1.6 V ≤ AV_{DD} ≤ 3.6 V			0.4[Note 2]	mA
		Total of all pins[Note 3]	1.6 V ≤ AV_{DD} ≤ 3.6 V			5.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{SS} pin to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty ≤ 70%.
The output current value that has changed the duty ratio > 70 % can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7) / (n × 0.01)
  <Example> When I_{OL} = 10.0 mA and n = 80%
  Total output current of pins = (10.0 × 0.7) / (80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140	Normal input buffer	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P15	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}	V
			TTL input buffer 3.3V ≤ V_{DD} < 4.0 V	2.0		V_{DD}	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	1.5		V_{DD}	V
	V_{IH3}	P20 to P24		0.7AV_{DD}		AV_{DD}	V
	V_{IH5}	P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140	Normal input buffer	0		0.2V_{DD}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P15	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ V_{DD} ≤ 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ V_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P24		0		0.3AV_{DD}	V
	V_{IL5}	P121, P122, P137, EXCLK, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, and P50 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −10.0 mA	V_{DD} − 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −3.0 mA	V_{DD} − 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −2.0 mA	V_{DD} − 0.6			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −1.5 mA	V_{DD} − 0.5			V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = −1.0 mA	V_{DD} − 0.5			V
	V_{OH2}	P20 to P24	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OH2} = −100 μA	AV_{DD} − 0.5			V
	V_{OH4}	P70 to P73	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH4} = −3.0 mA	V_{DD} − 1.1			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH4} = −2.0 mA	V_{DD} − 0.9			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH4} = −1.5 mA	V_{DD} − 0.7			V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH4} = −1.0 mA	V_{DD} − 0.7			V

Caution P00, P02 to P04, P10 to P15 and P50 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.5	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ V_{DD} < 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P24	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL4}	P70 to P73	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -3.0 mA			1.0	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -1.5 mA			0.6	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -0.6 mA			0.5	V
			1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL4} = -0.3 mA			0.5	V

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P137, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH3}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{DD}$	Input port or external clock input selected			1	μA
				Resonator connected			10	μA
	I_{LIH4}	P20 to P24	$V_I = AV_{DD}$				1	μA
Input leakage current, low	I_{LIL1}	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140	$V_I = V_{SS}$				−1	μA
	I_{LIL2}	P121, P122, P137, $\overline{\text{RESET}}$	$V_I = V_{SS}$				−1	μA
	I_{LIL3}	P121, P122 (X1, X2, EXCLK)	$V_I = V_{SS}$	Input port or external clock input selected			−1	μA
				Resonator connected			−10	μA
	I_{LIL4}	P20 to P24	$V_I = AV_{SS}$				−1	μA
On-chip pull-up resistance	R_U	P00 to P04, P10 to P15, P40 to P42, P50, P51, P70 to P73, P140	$V_I = V_{SS}$, input port selected		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

5. 2. 2. 2 Supply current characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/3)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS(High-speed main) mode Note 4	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		mA
						V_{DD} = 3.0 V		2.1		
					Normal operation	V_{DD} = 5.0 V		4.6	7.0	mA
						V_{DD} = 3.0 V		4.6	7.0	
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	
			LS (Low-speed main) mode Note 4	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	
			LV (Low-voltage main) mode Note 4	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	
			HS (High-speed main) mode Note 4	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	
						Resonator connection		3.2	4.8	
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	
						Resonator connection		1.9	2.7	
			LS (Low-speed main) mode Note 4	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	
						Resonator connection		1.1	1.7	

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pullup/pull-down resistors, and data flash rewriting.

2. When the high-speed on-chip oscillator is stopped.

3. When the high-speed system clock is stopped.

4. The relationship between the operation voltage range, CPU operating frequency, and operating mode is as below.

HS (High-speed main) mode: V_{DD} = 2.7 to 5.5 V @ 1 MHz to 32 MHz
V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz

LS (Low-speed main) mode: V_{DD} = 1.8 to 5.5 V @ 1 MHz to 8 MHz

LV (Low-voltage main) mode: V_{DD} = 1.6 to 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (High-speed main) mode[Note 6]	f_{IH} = 32 MHz[Note 4]	V_{DD} = 5.0 V		0.54	1.63	mA
					V_{DD} = 3.0 V		0.54	1.63	
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		0.44	1.28	mA
					V_{DD} = 3.0 V		0.44	1.28	
				f_{IH} = 16 MHz[Note 4]	V_{DD} = 5.0 V		0.40	1.00	mA
					V_{DD} = 3.0 V		0.40	1.00	
			LS (Low-speed main) mode[Note 6]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	
			LV (Low-voltage main) mode[Note 6]	f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	
			HS (High-speed main) mode[Note 6]	f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	
				f_{MX} = 20 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.28	1.00	
					Resonator connection		0.45	1.17	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	
				f_{MX} = 10 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		0.19	0.60	
					Resonator connection		0.26	0.67	
			LS (Low-speed main) mode[Note 6]	f_{MX} = 8 MHz[Note 3], V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	
				f_{MX} = 8 MHz[Note 3], V_{DD} = 2.0 V	Square wave input		95	330	
					Resonator connection		145	380	
	I_{DD3}[Note 5]	STOP mode	T_A = −40°C				0.15	0.50	μA
			T_A = +25°C				0.22	0.50	
			T_A = +50°C				0.34	1.10	
			T_A = +70°C				0.46	1.90	
			T_A = +85°C				0.75	3.30	

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, on-chip pullup/pull-down resistors, and data flash rewriting.

2. When the HALT instruction is executed for the flash memory.

3. When the high-speed on-chip oscillator is stopped.

4. When the high-speed system clock is stopped.

5. Not including the current flowing into 12-bit interval timer, watchdog timer.

6. The relationship between the operation voltage range, CPU operating frequency, and operating mode is as below.

HS (High-speed main) mode:	V_{DD} = 2.7 to 5.5 V @ 1 MHz to 32 MHz
	V_{DD} = 2.4 to 5.5 V @ 1 MHz to 16 MHz
LS (Low-speed main) mode:	V_{DD} = 1.8 to 5.5 V @ 1 MHz to 8 MHz
LV (Low-voltage main) mode:	V_{DD} = 1.6 to 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. The TYP. temperature condition in modes other than STOP mode is T_A = 25°C.

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (3/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
<R> Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
12-bit Interval timer operating current	I_{IT} Note 1, 2, 3				0.02 Note 3		μA
Watchdog timer operating current	I_{WDT} Note 1, 2, 4	f_{IL} = 15 kHz, f_{MAIN} is stopped			0.22		μA
A/D converter operating current	I_{ADC} Note 5, 6	AV_{DD} = 3.0 V, When conversion at maximum speed			420	720	μA
$AV_{REF(+)}$ current	I_{AVREF} Note 7	AV_{DD} = 3.0 V, ADREFP1 = 0, ADREFP0 = 0 Note 6			14.0	25.0	μA
		AV_{REFP} = 3.0 V, ADREFP1 = 0, ADREFP0 = 1 Note 9			14.0	25.0	μA
		ADREFP1 = 1, ADREFP0 = 0 Note 1			14.0	25.0	μA
A/D converter reference voltage current	I_{ADREF} Note 1, 8	V_{DD} = 3.0 V			75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1	V_{DD} = 3.0 V			75.0		μA
LVD operating current	I_{LVD} Note 1, 10				0.08		μA
BGO operating current	I_{BGO} Note 1, 11				2.5	12.2	mA
Selfprogramming operating current	I_{FSP} Note 1, 12				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ}	A/D converter operation (AV_{DD} = 3.0 V)	The mode is performed Note 1, 13		0.50	0.60	mA
			During A/D conversion Note 1		0.60	0.75	mA
			During A/D conversion Note 6		420	720	μA
		CSI/UART operation Note 1			0.70	0.84	mA

(**Notes** and **Remarks** are listed on the next page.)

<R> **Notes 1.** Current flowing to V_{DD}.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip ocsillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and IIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and IWDT when the watchdog timer is in operation.

5. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC}, I_{AVREF}, I_{ADREF} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing to the AV_{DD}.

7. Current flowing from the reference voltage source of A/D converter.

8. Operation current flowing to the internal reference voltage.

9. Current flowing to the AV_{REFP}.

10. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.

11. Current flowing only during data flash rewrite.

12. Current flowing only during self programming.

13. For shift time to the SNOOZE mode, see **3. 18 Standby Function**.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{CLK}: CPU/peripheral hardware clock frequency

3. The TYP. temperature condition is T_A = 25°C.

5. 2. 3 AC characteristics

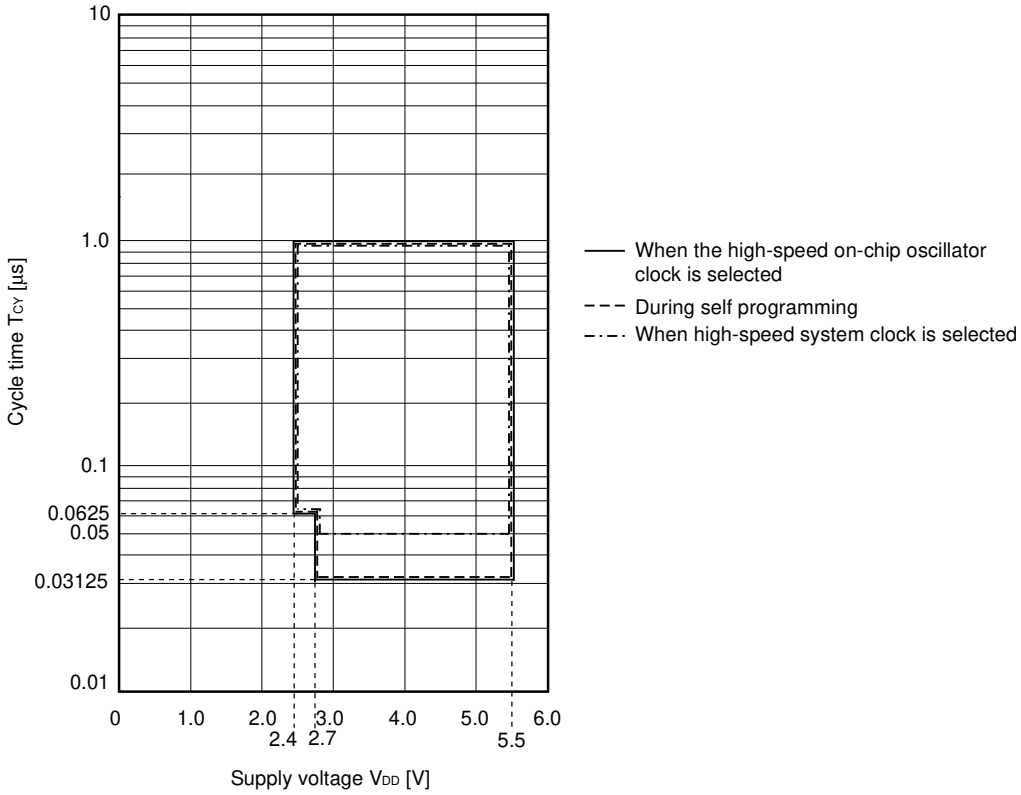
(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (Low-voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (Low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	
		1.8 V ≤ V_{DD} < 2.4 V			1.0		8.0	
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			
		1.8 V ≤ V_{DD} < 2.4 V			60			
		1.6 V ≤ V_{DD} < 1.8 V			120			
TI00, TI04, TI07 input high/low level width	t_{TIH}, t_{TIL}				1/f_{MCK} + 10			ns
TO00, TO04, TO07 output frequency	f_{TO}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.6 V ≤ V_{DD} < 5.5 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
PCLBUZ0 output frequency	f_{PCL}	HS (high-speed main) mode		4.0 V ≤ V_{DD} ≤ 5.5 V			16	MHz
				2.7 V ≤ V_{DD} < 4.0 V			8	
				1.8 V ≤ V_{DD} < 2.7 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LV (Low-voltage main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
		LS (Low-speed main) mode		1.8 V ≤ V_{DD} ≤ 5.5 V			4	
				1.6 V ≤ V_{DD} < 1.8 V			2	
Interrupt input high level width, low level width	t_{INIH}, t_{INIL}	INTP0, INTP1, INTP2, INTP6		1.6 V ≤ V_{DD} ≤ 5.5 V	1			μs
<R> Key interrupt input high level width, low level width	t_{KR}	KR0 to KR7		1.8 V ≤ V_{DD} ≤ 5.5 V 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
				1.6 V ≤ V_{DD} < 1.8 V 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}				10			μs

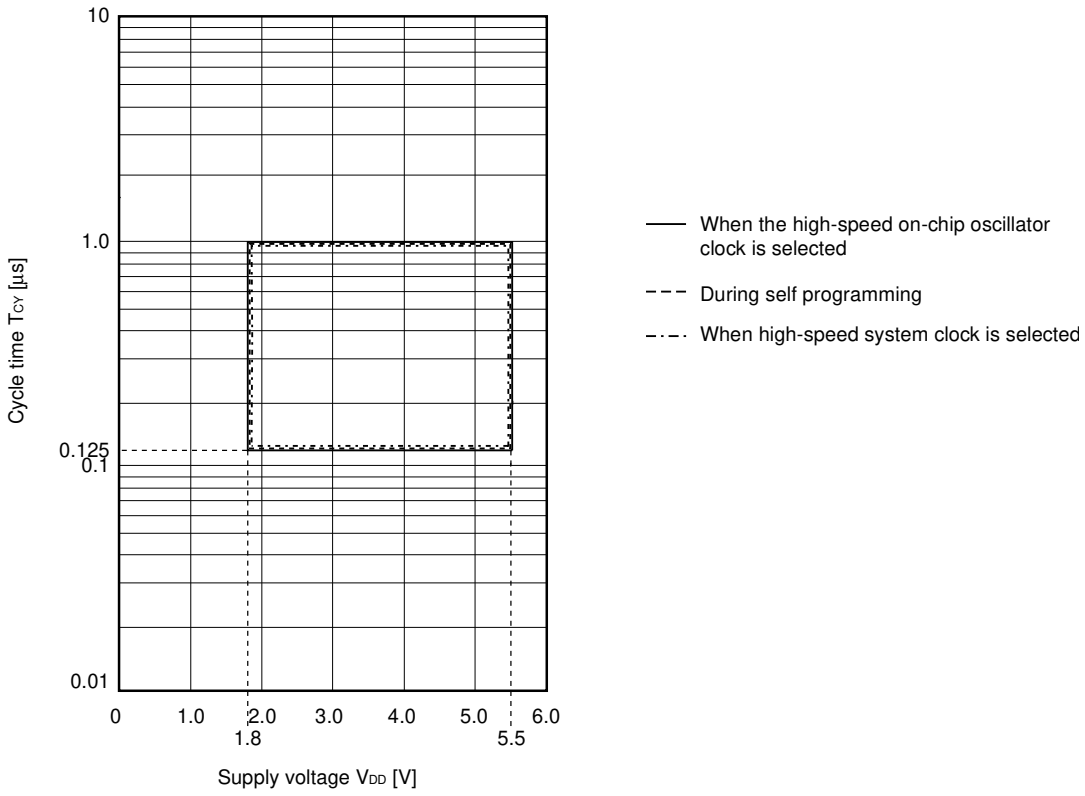
Remark f_{MCK}: Timer array unit operation clock frequency. (Operation clock to be set by the timer clock select register 0 (TPS0) and CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

<R> **Minimum Instruction Execution Time during Main System Clock Operation**

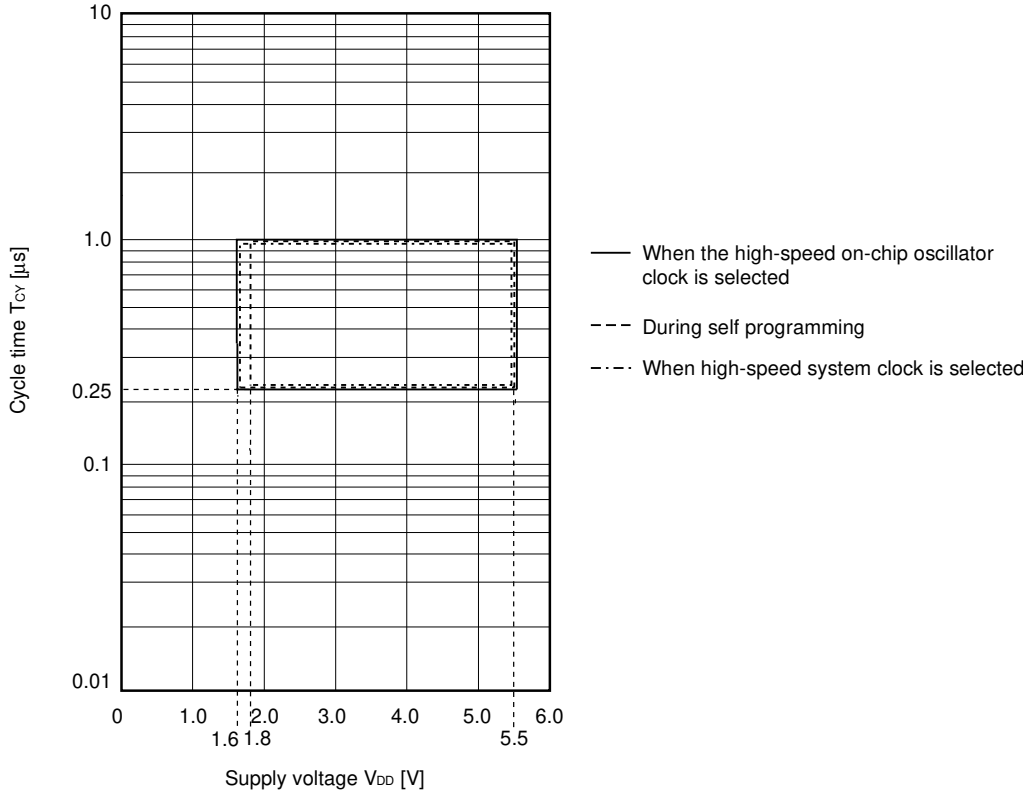
T_{CY} vs V_{DD} (HS (high-speed main) mode)



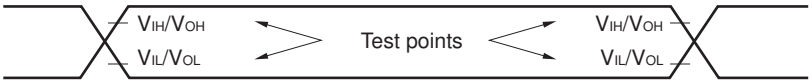
T_{CY} vs V_{DD} (LS (low-speed main) mode)



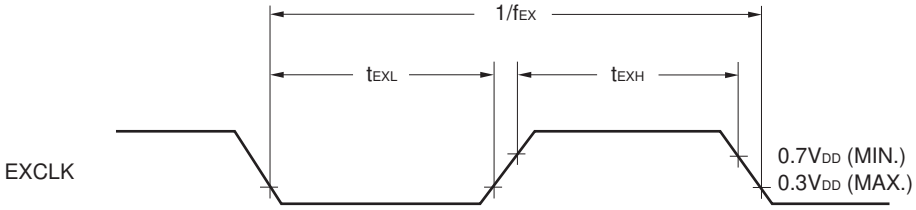
T_{CY} vs V_{DD} (LV (low-voltage main) mode)



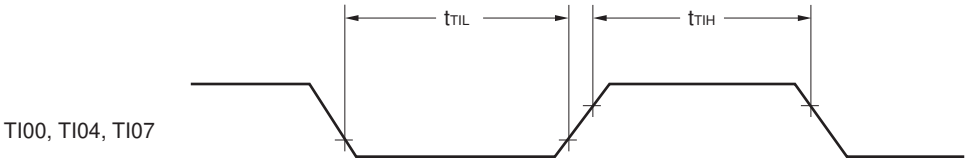
<R> **AC Timing Test Points**

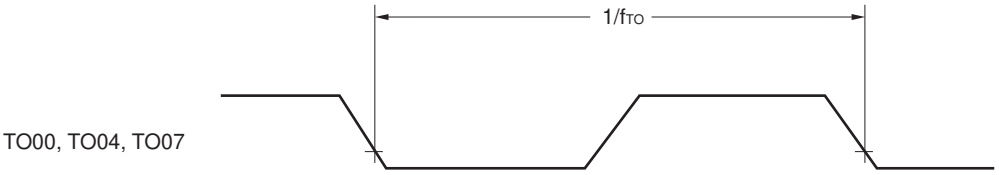


External System Clock Timing

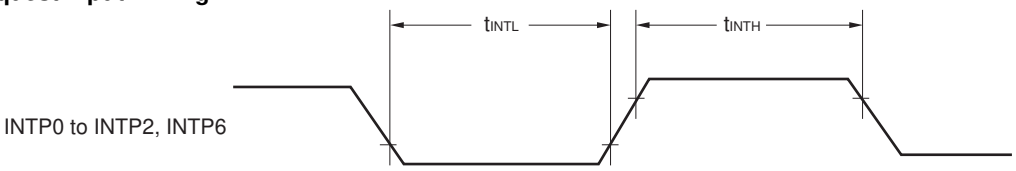


TI/TO Timing

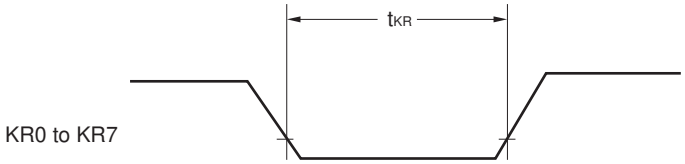




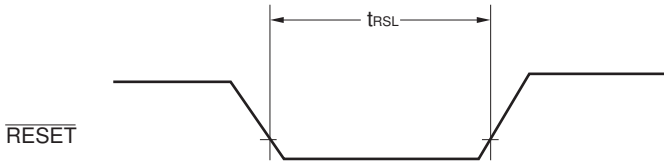
Interrupt Request Input Timing



Key Interrupt Input Timing

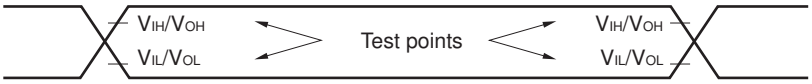


$\overline{\text{RESET}}$ Input Timing



<R> 5. 2. 4 Peripheral functions characteristics

AC Timing Test Points



<R> 5. 2. 4. 1 Serial array unit

(1) Communication between devices at same potential (UART mode) (dedicated baud rate generator output)

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 4		2.4 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3		0.6	Mbps
		1.8 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3		0.6	Mbps
		1.7 V ≤ V_{DD} ≤ 5.5 V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		5.3 Note 5		1.3 Note 5		0.6	Mbps
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		f_{MCK}/6		f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 6		—		1.3 Note 5		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

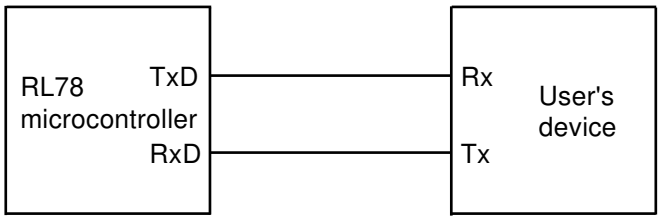
4. Transfer rate in the SNOOZE mode is 4800 bps.

5. The following conditions are required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: 2.6 Mbps max.
1.8 V ≤ V_{DD} < 2.4 V: 1.3 Mbps max.
1.6 V ≤ V_{DD} < 1.8 V: 0.6 Mbps max.

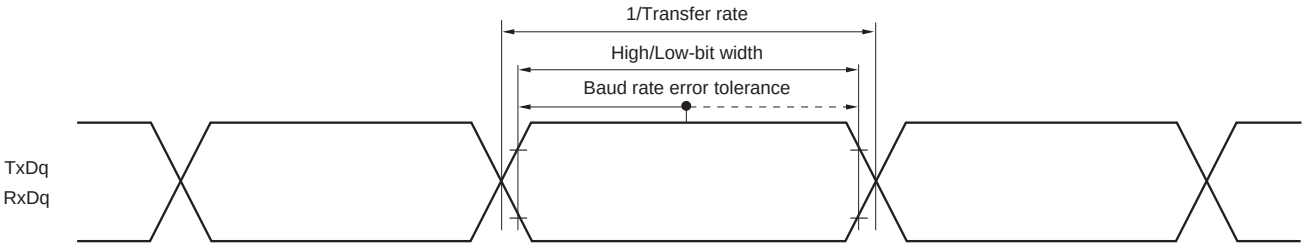
6. f_{CLK} in each operating mode is as below.
HS (high-speed main) mode : f_{CLK} = 32 MHz
LS (low-speed main) mode : f_{CLK} = 8 MHz
LV (low-voltage main) mode : f_{CLK} = 4 MHz

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication between devices at same potential)



UART mode bit width (during communication between devices at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 2), g: PIM, POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

<R> **(2) Communication between devices at same potential (CSI mode) (master mode, SCKp ... internal clock output corresponding CSI00 only)**

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 2/f_{CLK}	83.3 Note 4		250		500		ns
SCKp high-level width, low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -7		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -10		t_{KCY1}/2 -50		t_{KCY1}/2 -50		
Slp setup time (to SCKp↑) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	23		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	33		110		110		
Slp hold time (from SCKp↑) Note 5	t_{KSI1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 6	t_{KSO1}	C = 20 pF Note 7		10		10		10	ns

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. f_{MCK} must be 24 MHz or less.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

6. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

7. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

<R> **(3) Communication between devices at same potenntial (CSI mode) (master mode, SCKp ... internal clock output)**

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	125		500		1000		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	250		500		1000		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	500		500		1000		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	1000		1000		1000		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V t_{KCY1} ≥ 4/f_{CLK}	−		1000		1000		ns
SCKp high-level width low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -12		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -18		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -38		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY1}/2 -100		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	−		t_{KCY1}/2 -100		t_{KCY1}/2 -100		ns
<R> Slp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V	44		110		110		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V	75		110		110		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V	110		110		110		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V	220		220		220		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	−		220		220		ns
Slp hold time (from SCKp↑) Note 4	t_{KSI1}	1.7 V ≤ V_{DD} ≤ 5.5 V	19		19		19		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V	−		19		19		
Slp hold time (from SCKp↑) Note 5	t_{KSO1}	1.7 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		25		25		25	ns
		1.6 V ≤ V_{DD} ≤ 5.5 V C = 30 pF Note 6		−		25		25	

(**Notes Caution** and **Remark** are listed on the next page.)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

6. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

<R> **(4) Communication between devices at same potential (CSI mode)**
(slave mode, SCKp ... External clock input) (1/2)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 20MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < f_{MCK}	8/f_{MCK}		–		–		ns
			f_{MCK} ≤ 16MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		6/f_{MCK} and 500ns		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		6/f_{MCK} and 750ns		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		6/f_{MCK} and 1500ns		6/f_{MCK} and 1500ns		ns
SCKp high-level width low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -7		t_{KCY2}/2 -7		t_{KCY2}/2 -7		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -8		t_{KCY2}/2 -8		t_{KCY2}/2 -8		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -18		t_{KCY2}/2 -18		t_{KCY2}/2 -18		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 -66		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		–		t_{KCY2}/2 -66		t_{KCY2}/2 -66		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

<R> **(4) Communication between devices at same potential (CSI mode) (slave mode, SCKp ... External clock input) (2/2)**

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 4	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ +20		$1/f_{MCK}$ +30		$1/f_{MCK}$ +30		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ +30		$1/f_{MCK}$ +30		$1/f_{MCK}$ +30		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ +40		$1/f_{MCK}$ +40		$1/f_{MCK}$ +40		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		$1/f_{MCK}$ +40		$1/f_{MCK}$ +40		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}	1.8 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ +31		$1/f_{MCK}$ +31		$1/f_{MCK}$ +31		ns
		1.7 V ≤ V_{DD} ≤ 5.5 V		$1/f_{MCK}$ +250		$1/f_{MCK}$ +250		$1/f_{MCK}$ +250		ns
		1.6 V ≤ V_{DD} ≤ 5.5 V		—		$1/f_{MCK}$ +250		$1/f_{MCK}$ +250		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	C = 30 pF Note 6	2.7V ≤ V_{DD} ≤ 5.5V		$2/f_{MCK}$ +44		$2/f_{MCK}$ +110		$2/f_{MCK}$ +110	ns
			2.4V ≤ V_{DD} ≤ 5.5V		$2/f_{MCK}$ +75		$2/f_{MCK}$ +110		$2/f_{MCK}$ +110	ns
			1.8V ≤ V_{DD} ≤ 5.5V		$2/f_{MCK}$ +110		$2/f_{MCK}$ +110		$2/f_{MCK}$ +110	ns
			1.7V ≤ V_{DD} ≤ 5.5V		$2/f_{MCK}$ +220		$2/f_{MCK}$ +220		$2/f_{MCK}$ +220	ns
			1.6V ≤ V_{DD} ≤ 5.5V		—		$2/f_{MCK}$ +220		$2/f_{MCK}$ +220	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

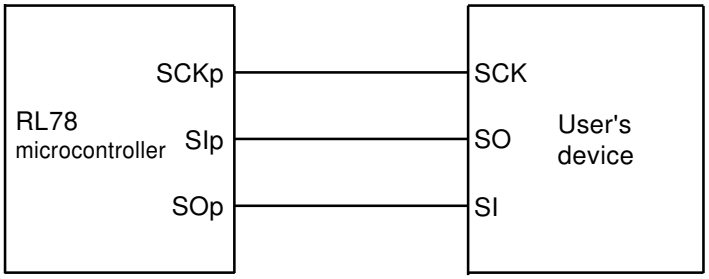
6. C is the load capacitance of the SOp output line.

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

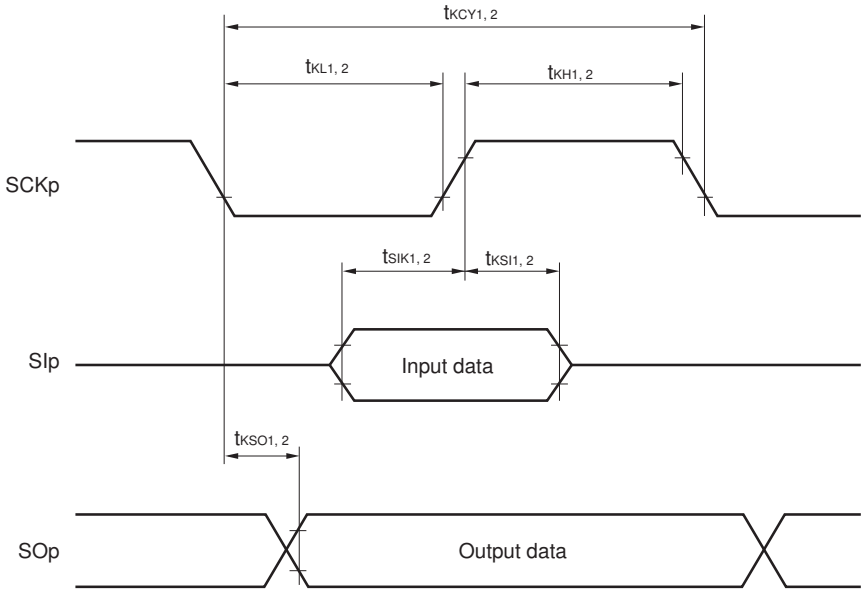
Remarks 1. p: CSI number (p = 00, 10, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

2. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

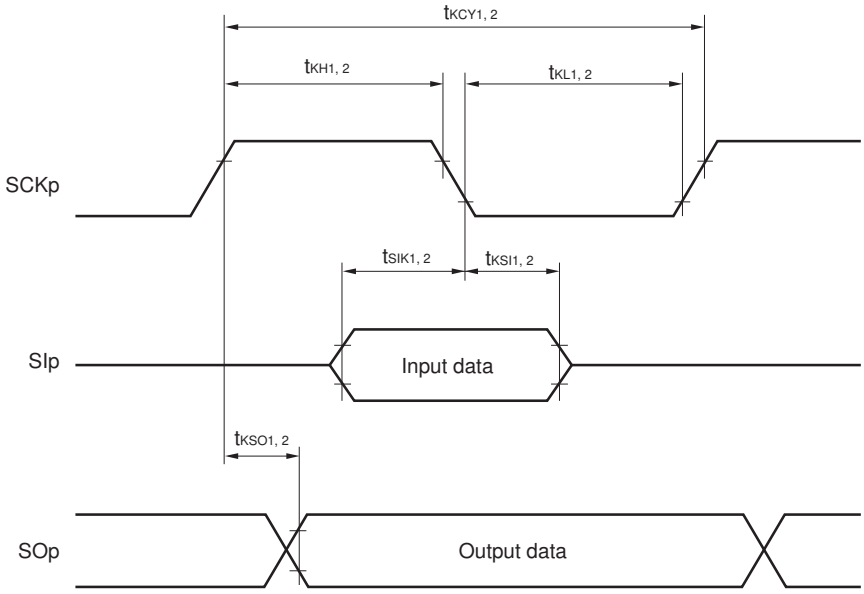
CSI mode connection diagram (during communication between devices with the same voltage)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing (during communication between devices with the same voltage)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

<R> **(5) Communication between devices at same potential (simplified I^2C mode) (1/2)**

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 4		400 Note 4		400 Note 4	kHz
		1.8 V ≤ V_{DD} ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 4		400 Note 4		400 Note 4	kHz
		1.8 V ≤ V_{DD} < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 4		300 Note 4		300 Note 4	kHz
		1.7 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250 Note 4		250 Note 4		250 Note 4	kHz
		1.6 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		−		250 Note 4		250 Note 4	kHz
Hold time when SCLr = L	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	−		1850		1850		ns
Hold time when SCLr = H	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ V_{DD} < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	−		1850		1850		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The value must also be f_{CLK}/4 or lower.

(**Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

<R> **(5) Communication between devices at same potential (simplified I^2C mode) (2/2)**

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (for reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	$1/f_{MCK}$ +85 Note 4		$1/f_{MCK}$ +145 Note 4		$1/f_{MCK}$ +145 Note 4		ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	$1/f_{MCK}$ +145 Note 4		$1/f_{MCK}$ +145 Note 4		$1/f_{MCK}$ +145 Note 4		ns
		1.8 V ≤ V_{DD} < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	$1/f_{MCK}$ +230 Note 4		$1/f_{MCK}$ +230 Note 4		$1/f_{MCK}$ +230 Note 4		ns
		1.7 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	$1/f_{MCK}$ +290 Note 4		$1/f_{MCK}$ +290 Note 4		$1/f_{MCK}$ +290 Note 4		ns
		1.6 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	−		$1/f_{MCK}$ +290 Note 4		$1/f_{MCK}$ +290 Note 4		ns
Data hold time (for transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ V_{DD} ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ V_{DD} < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	−	−	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

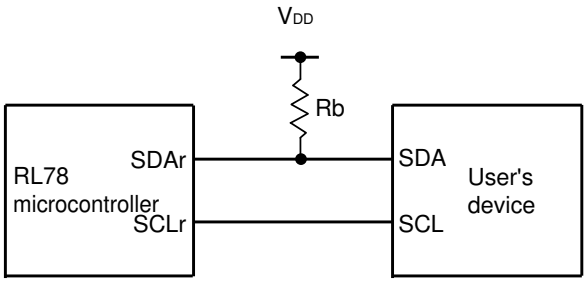
3. LV is condition of LV (low-voltage main) mode.

4. Set the f_{MCK} value so as not to exceed the hold time when SCLr = "L" and SCLr = "H".

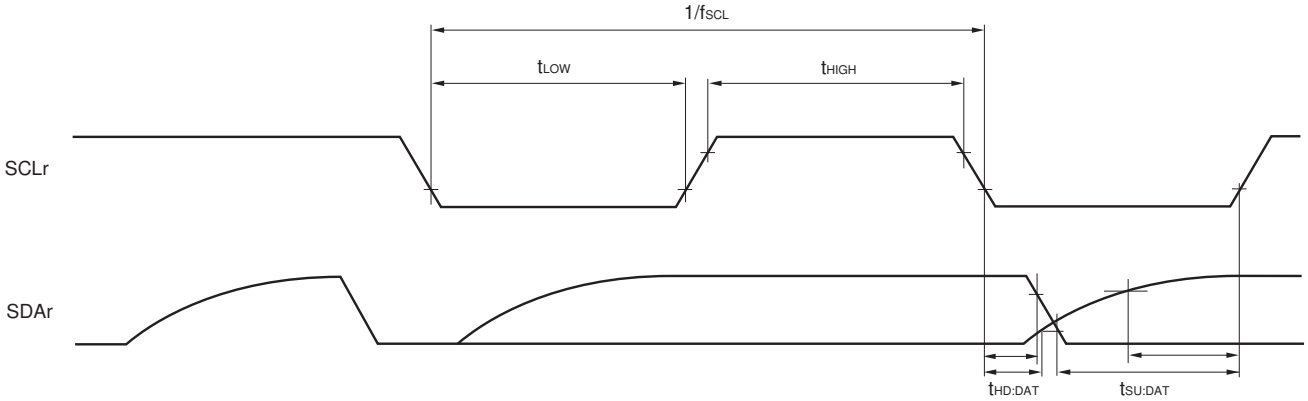
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I^2C connection diagram (during communication between devices at same potential)



Simplified I^2C mode serial transfer timing (during communication between devices at same potential)



Remarks 1. Rb [Ω]: Communication line (SDAr) pull-up resistance,
Cb [F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 10, 20), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00 to 03, 10, 11)

<R> **(6) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (UART mode) (output from dedicated baud rate generator) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 4		Reception	4.0V ≤ V_{DD} ≤ 5.5V, 2.7V ≤ Vb ≤ 4.0V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3		1.3		0.6	Mbps
			2.7V ≤ V_{DD} < 4.0V, 2.3V ≤ Vb ≤ 2.7V		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3		1.3		0.6	Mbps
			1.8V ≤ V_{DD} < 3.3V, 1.6V ≤ Vb ≤ 2.0V Note 5		f_{MCK}/6		f_{MCK}/6		f_{MCK}/6	bps
			Theoretical value of the maximum transfer rate: f_{MCK} = f_{CLK} Note 7		5.3 Note 6		1.3		0.6	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode is 4,800 bps.

5. Specify a value so as to satisfy V_{DD} ≥ Vb.

6. The following conditions are also required for low voltage interface.
2.4 V ≤ V_{DD} < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ V_{DD} < 2.4 V: MAX. 1.3 Mbps

7. f_{CLK} in each operating mode is as below.
HS (high-speed main) mode: f_{CLK} = 32 MHz
LS (low-speed main) mode: f_{CLK} = 8 MHz
LV (low-voltage main) mode: f_{CLK} = 4 MHz

(**Caution** and **Remarks** are listed on the next page.)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remarks 1. Vb [V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

4. The AC characteristics of serial array units communicating with a device at different potential in UART mode is observed at V_{IH} and V_{IL} below.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V
1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

5. UART2 cannot communicate with a device at different potential when bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

<R> **(6) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (UART mode) (output from dedicated baud rate generator) (2/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0V ≤ V_{DD} ≤ 5.5V, 2.7V ≤ Vb ≤ 4.0V		**Note 4**		**Note 4**		**Note 4**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 5		2.8 Note 5		2.8 Note 5	Mbps
			2.7V ≤ V_{DD} < 4.0V, 2.3V ≤ Vb ≤ 2.7V		**Note 7**		**Note 7**		**Note 7**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 8		1.2 Note 8		1.2 Note 8	Mbps
			1.8V ≤ V_{DD} < 3.3V, 1.6V ≤ Vb ≤ 2.0V Note 5		**Note 9**		**Note 9**		**Note 9**	bps
			Theoretical value of the maximum transfer rate: Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 10		0.43 Note 10		0.43 Note 10	Mbps

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The smaller value derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.2}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

(Other **Notes** and **Caution** are listed on the next page.)

5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 4** above to calculate the maximum transfer rate under conditions of the customer.

6. Specify a value so as to satisfy $V_{DD} \geq Vb$.

7. The smaller value derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\ V \leq V_{DD} < 4.0\ V$, $2.3\ V \leq Vb \leq 2.7\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{2.0}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{2.0}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100[\%]$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 7** above to calculate the maximum transfer rate under conditions of the customer.

9. The smaller value derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\ V \leq V_{DD} \leq 3.3\ V$, $1.6\ V \leq Vb \leq 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-Cb \times Rb \times \ln(1 - \frac{1.5}{Vb})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-Cb \times Rb \times \ln(1 - \frac{1.5}{Vb})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100[\%]$$

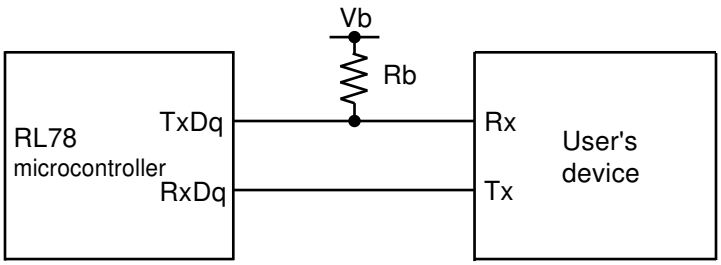
* This value is the theoretical value of the relative difference between the transmission and reception sides.

10. This value as an example is calculated when the conditions described in the Conditions column are met. See **Note 9** above to calculate the maximum transfer rate under conditions of the customer.

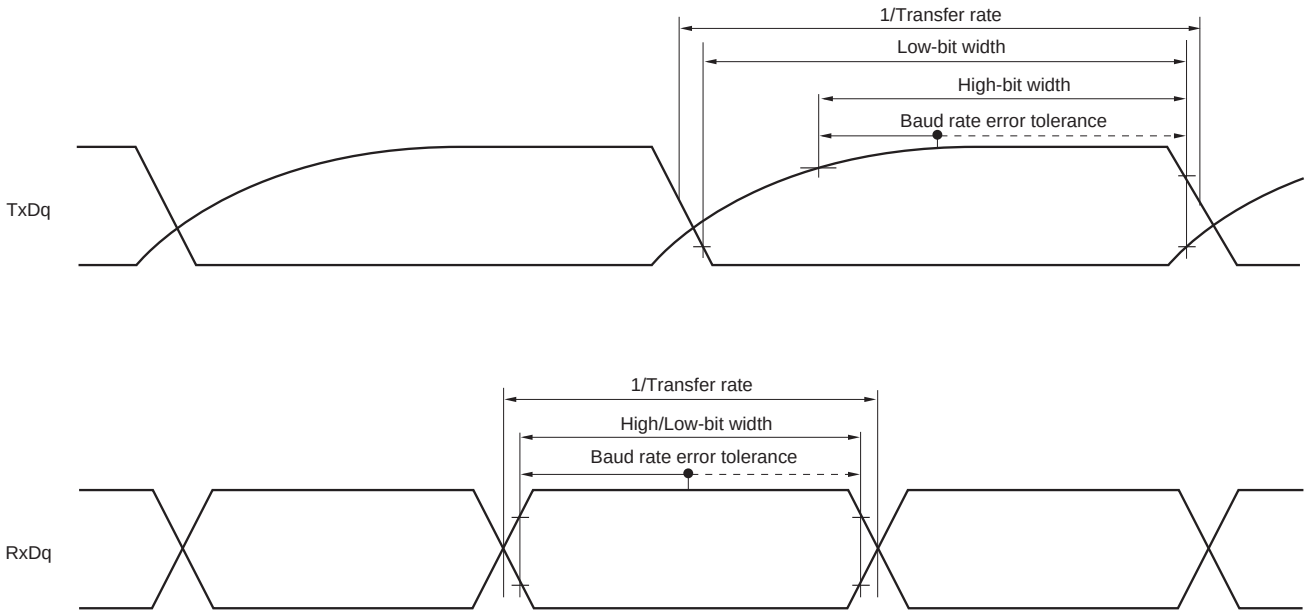
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

UART mode connection diagram (during communication between devices at different potential)



UART mode bit width (during communication between devices at different potential) (reference)



Remarks 1. Rb [Ω]: Communication line (TxDq) pull-up resistance, Cb [F]: Communication line (TxDq) load capacitance, Vb [V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

4. The AC characteristics of serial array units communicating with a device at different potential in UART mode is observed at V_{IH} and V_{IL} below.

4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

5. UART2 cannot communicate with a device at different potential when bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

<R> **(7) Communication between devices at different potential (2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output corresponding CSI00 only) (1/2)**

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ, t_{KCY1} ≥ 2/f_{CLK}	200		1150		1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ, t_{KCY1} ≥ 2/f_{CLK}	300		1150		1150		
SCKp high level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -120		t_{KCY1}/2 -120		t_{KCY1}/2 -120		
SCKp low level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -7		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -10		t_{KCY1}/2 -50		t_{KCY1}/2 -50		
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		479		479		
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130		130	

(**Notes** are listed on the next page.)

<R> **(7) Communication between devices at different potential (2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output corresponding CSI00 only) (2/2)**

(T_A = −40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		110		110		
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		10	

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. This indicates the time when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. Rb [Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb [F]: Communication line (SCKp, SOp) load capacitance, Vb [V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

3. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.

4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

<R> **(8) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output) (1/2)**

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ, t_{KCY1} ≥ 4/f_{CLK}	300		1150		1150		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ, t_{KCY1} ≥ 4/f_{CLK}	500		1150		1150		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ, t_{KCY1} ≥ 4/f_{CLK}	1150		1150		1150		
SCKp high level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -75		t_{KCY1}/2 -75		t_{KCY1}/2 -75		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -170		t_{KCY1}/2 -170		t_{KCY1}/2 -170		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ	t_{KCY1}/2 -458		t_{KCY1}/2 -458		t_{KCY1}/2 -458		
SCKp low level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	t_{KCY1}/2 -12		t_{KCY1}/2 -50		t_{KCY1}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	t_{KCY1}/2 -18		t_{KCY1}/2 -50		t_{KCY1}/2 -50		
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 4 Cb = 30 pF, Rb = 5.5 kΩ	t_{KCY1}/2 -50		t_{KCY1}/2 -50		t_{KCY1}/2 -50		

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Specify a value so as to satisfy $V_{DD} \geq Vb$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. Rb [Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb [F]: Communication line (SCKp, SOp) load capacitance, Vb [V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

3. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.

$4.0\ V \leq V_{DD} \leq 5.5\ V$, $2.7\ V \leq Vb \leq 4.0\ V$: $V_{IH} = 2.2\ V$, $V_{IL} = 0.8\ V$

$2.7\ V \leq V_{DD} < 4.0\ V$, $2.3\ V \leq Vb \leq 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

$1.8\ V \leq V_{DD} < 3.3\ V$, $1.6\ V \leq Vb \leq 2.0\ V$: $V_{IH} = 1.5\ V$, $V_{IL} = 0.32\ V$

4. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

<R> **(8) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (master mode, SCKp ... internal clock output) (2/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
SIp setup time (to SCKp↑) Note 4	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 4	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns
SIp setup time (to SCKp↓) Note 5	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 5	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ V_{DD} < 4.0 V, 1.6 V ≤ Vb ≤ 2.0 V, Note 6 Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

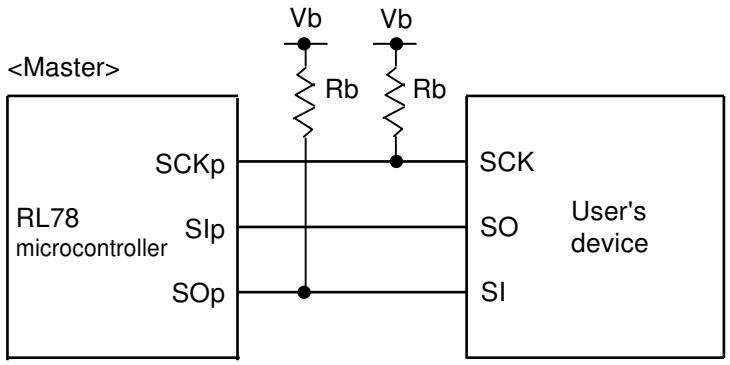
4. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. This indicates the time when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0.

6. Specify a value so as to satisfy $V_{DD} \geq Vb$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication between devices at different potential)



Remarks 1. Rb [Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb [F]: Communication line (SCKp, SOp) load capacitance, Vb [V]: Communication line voltage

2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

3. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.

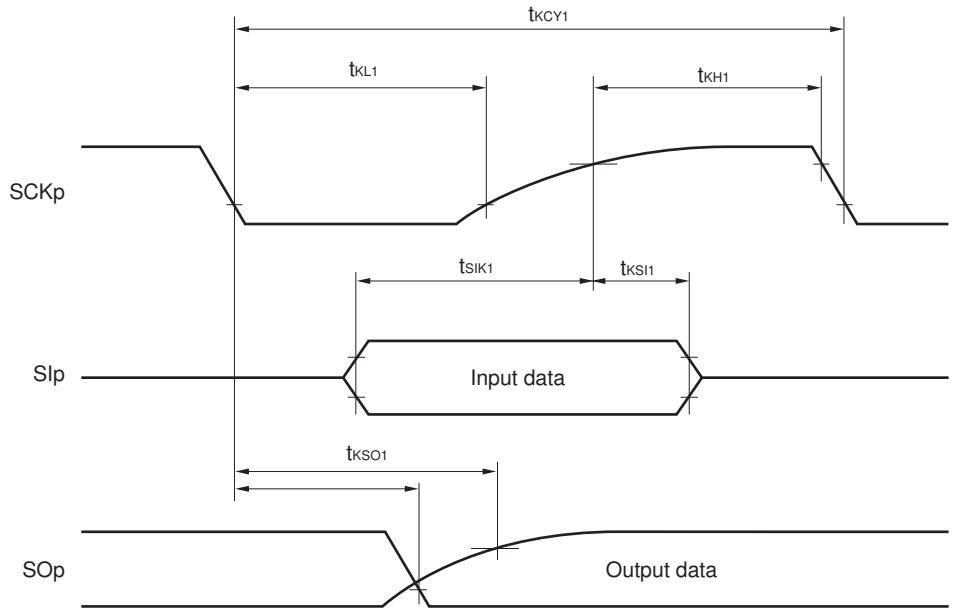
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

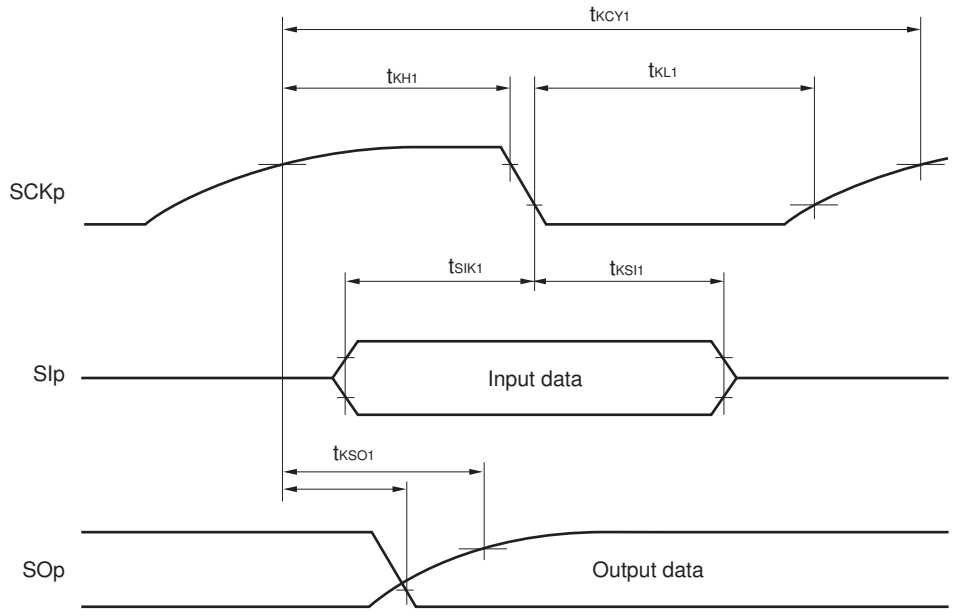
1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

4. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing: master mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

2. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

<R> **(9) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (slave mode, SCKp ... External clock input) (1/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 4	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V							
		24 MHz < f_{MCK}	14/f_{MCK}		−		−		ns
		20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		−		−		ns
		8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		−		−		ns
		4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		−		ns
		f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V							
		24 MHz < f_{MCK}	20/f_{MCK}		−		−		ns
		20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		−		−		ns
		16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		−		−		ns
		8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		−		−		ns
		4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		−		ns
		f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5							
		24 MHz < f_{MCK}	48/f_{MCK}		−		−		ns
		20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		−		−		ns
		16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		−		−		ns
		8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		−		−		ns
		4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		−		ns
		f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

5. Specify a value so as to satisfy V_{DD} ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

<R> **(9) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (CSI mode) (slave mode, SCKp ... External clock input) (2/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-level width SCKp low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	t_{KCY2}/2 -12		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	t_{KCY2}/2 -18		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4	t_{KCY2}/2 -50		t_{KCY2}/2 -50		t_{KCY2}/2 -50		ns
SIp setup time (to SCKp↑) Note 5	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4	1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		ns
SIp hold time (from SCKp↑) Note 5	t_{KSI2}		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
Delay time from SCKp↓ to SOp output Note 6	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/f_{MCK} +120		2/f_{MCK} +573		2/f_{MCK} +573	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/f_{MCK} +214		2/f_{MCK} +573		2/f_{MCK} +573	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 4, Cb = 30 pF, Rb = 5.5 kΩ		2/f_{MCK} +573		2/f_{MCK} +573		2/f_{MCK} +573	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. Specify a value so as to satisfy V_{DD} ≥ Vb.

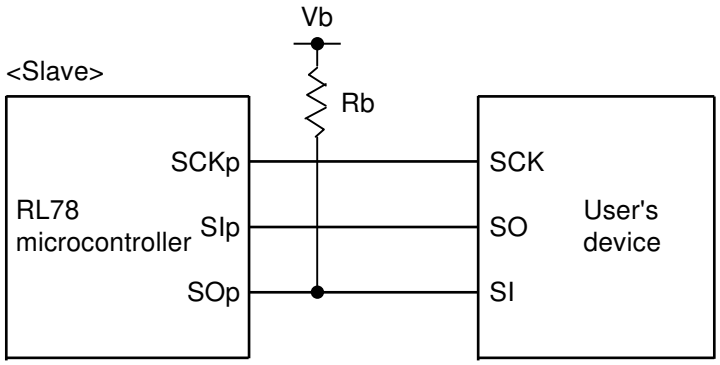
5. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↓.

6. This indicates the time when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. When DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0, this specification refers to SCKp↑.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

CSI mode connection diagram (during communication between devices at different potential)



Remarks 1. Rb [Ω]: Communication line (SOp) pull-up resistance, Cb [F]: Communication line (SOp) load capacitance, Vb [V]: Communication line voltage

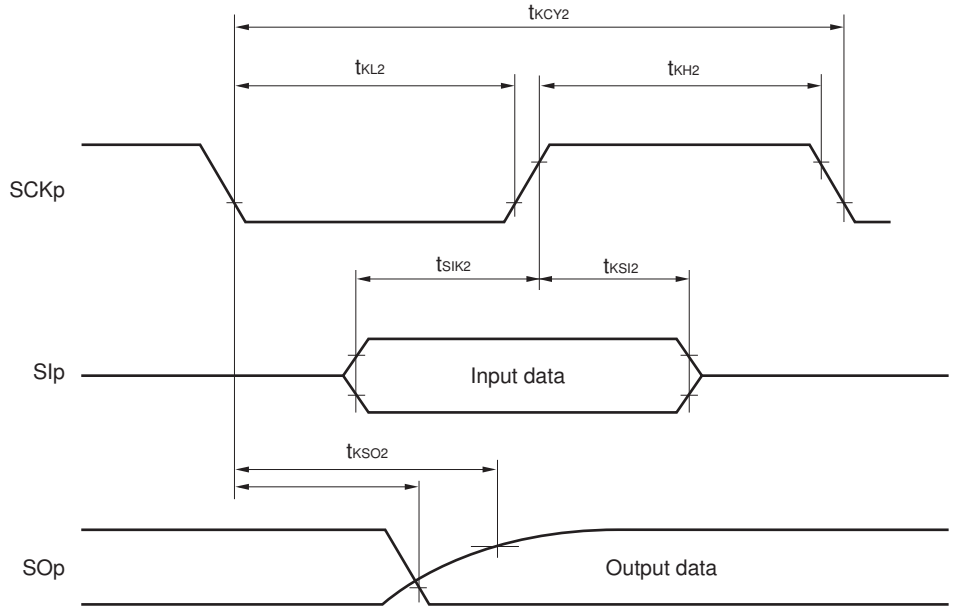
2. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 10, 20))

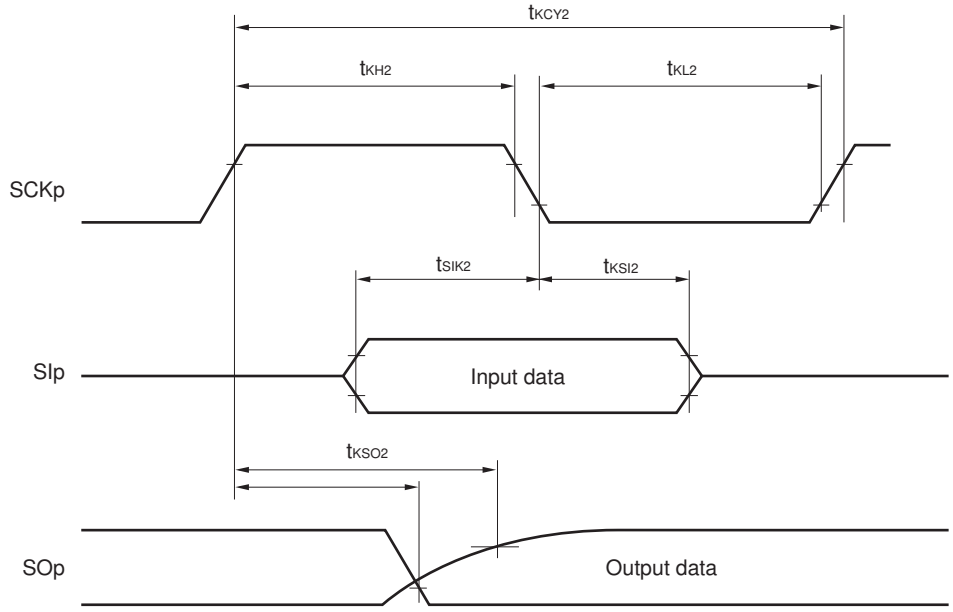
4. The AC characteristics of serial array units communicating with a device at different potential in CSI mode is observed at V_{IH} and V_{IL} below.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V
1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

5. CSI01, CSI11, and CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

CSI mode serial transfer timing: slave mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 0 or DAPmn = 1 and CKPmn = 1)



CSI mode serial transfer timing: slave mode (during communication between devices at different potential)
(when DAPmn = 0 and CKPmn = 1 or DAPmn = 1 and CKPmn = 0)



Remarks 1. p: CSI number (p = 00, 10, 20), m: Unit number, n: Channel number (mn = 00, 10, 20),
g: PIM and POM numbers (g = 0, 1)

2. CSI21 cannot communicate with a device at different potential. Use other CSI channels for communication between devices at different potential.

<R> **(10) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (simplified I^2C mode) (1/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 4		300 Note 4		300 Note 4	kHz
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 4		300 Note 4		300 Note 4	kHz
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 4		300 Note 4		300 Note 4	kHz
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 4		300 Note 4		300 Note 4	kHz
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ		300 Note 4		300 Note 4		300 Note 4	kHz
Hold time when SCLr = L	t_{LOW}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = H	t_{HIGH}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	610		610		610		ns

(**Notes** are listed on the next page.)

<R> **(10) Communication between devices at different potential (1.8 V, 2.5 V or 3 V) (simplified I^2C mode) (2/2)**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (for reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1/f_{MCK} +135 Note 6		1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/f_{MCK} +135 Note 6		1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		1/f_{MCK} +190 Note 6		ns
Data hold time (for transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ V_{DD} ≤ 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 5, Cb = 100 pF, Rb = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. HS is condition of HS (high-speed main) mode.

2. LS is condition of LS (low-speed main) mode.

3. LV is condition of LV (low-voltage main) mode.

4. The value must also be f_{CLK}/4 or lower.

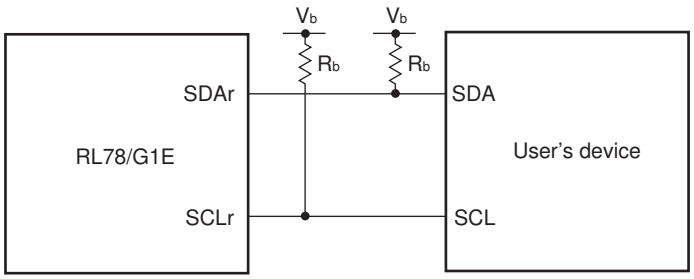
5. Specify a value so as to satisfy V_{DD} ≥ Vb.

6. Set the f_{MCK} value so as not to exceed the hold time when SCLr = “L” and SCLr = “H”.

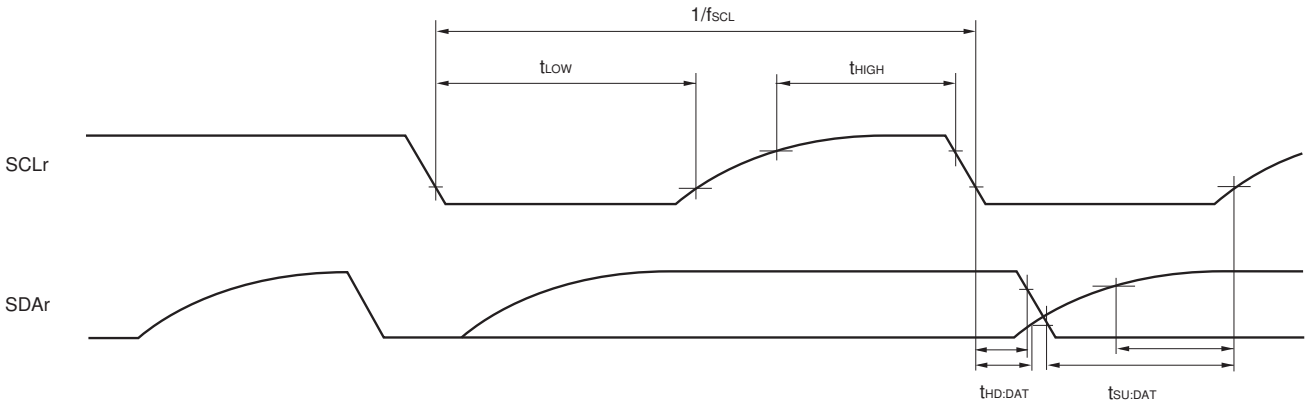
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication between devices at different potential)



Simplified I²C mode serial transfer timing (during communication between devices at different potential)



Remarks 1. Rb [Ω]: Communication line (SDAr, SCLr) pull-up resistance, Cb [F]: Communication line (SDAr, SCLr) load capacitance, Vb [V]: Communication line voltage

2. r: IIC number (r = 00, 10, 20), g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operating clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 02, 10))

5. 2. 5 Analog block characteristics

5. 2. 5. 1 A/D converter characteristics

<R> **Division of A/D Converter Characteristics**

Reference voltage / Input channel	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = AV_{DD} Reference voltage (-) = AV_{SS}	Reference voltage (+) = Internal refrence voltage Reference voltage (-) = AV_{SS}
High-accuracy channe; ANI0 to ANI4 (input buffer power supply: AV_{DD})	See 5. 2. 5. 1 (1) See 5. 2. 5. 1 (2)	See 5. 2. 5. 1 (3)	See 5. 2. 5. 1 (6)
Normal channel; ANI16 to ANI18, ANI20 to ANI26, ANI28, ANI30 (input buffer power supply: V_{DD})	See 5. 2. 5. 1 (4)	See 5. 2. 5. 1 (5)	
Internal reference voltage, temperature sensor output	See 5. 2. 5. 1 (4)	See 5. 2. 5. 1 (5)	–

See the section shown above for the electrical specifications depending on both input channel and reference voltage.

<R> (1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI4

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V, HALT mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				12	bit
Overall error[Notes 1, 2, 3]	AINL	12-bit resolution		±1.7	±3.3	LSB
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	3.375			μs
Zero-scale error[Notes 1, 2, 3]	E_{ZS}	12-bit resolution		±1.3	±3.2	LSB
Full-scale error[Notes 1, 2, 3]	E_{FS}	12-bit resolution		±0.7	±2.9	LSB
Integral linearity error[Notes 1, 2, 3]	ILE	12-bit resolution		±1.0	±1.4	LSB
Differential linearity error[Notes 1, 2, 3]	DLE	12-bit resolution		±0.9	±1.2	LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

<R> **Notes 1.** TYP. Value is the average value at AV_{DD} = AV_{REFP} = 3 V and T_A = 25°C. MAX. value is the average value ±3σ at normalized distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

<R> **Cautions 1. Route the wiring so that noise will not be superimposed on each power line and ground line, and insert a capacitor to suppress noise.**
In addition, separate the reference voltage line of AV_{REFP} from the other power lines to keep it free from the influences of noise.

2. During A/D conversion, keep a pulse, such as a digital signal, that abruptly changes its level from being input to or output from the pins adjacent to the converter pins and P20 to P27.

<R> (2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI2 to ANI4 (ANI pins that use AV_{DD} as their power source)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, AV_{REFP} ≤ AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±4.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.0	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.0	
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

<R> (3) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI4 (ANI pins that use AV_{DD} as their power source)

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±7.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{DD}	V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

<R> (4) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target for conversion: ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 (ANI pins that use V_{DD} as their power source), interanal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V, AV_{REFP} ≤ AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{REFP}, reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±7.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±3.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	LSB
		10-bit resolution	1.8 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±2.0	
		8-bit resolution	1.6 V ≤ AV_{REFP} ≤ AV_{DD} ≤ 3.6 V			±1.5	
Analog input voltage	V_{AIN}			0		AV_{REFP} and V_{DD}	V
		Intenal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

4. Refer to **5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics**.

<R> (5) When reference voltage (+) = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30 (ANI pins that use V_{DD} as their power source), interanal reference voltage, temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = AV_{DD}, reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±6.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ AV_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ AV_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ AV_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ AV_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3	EZS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Full-scale error Notes 3	EFS	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±8.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±3.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.5	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±2.5	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.0	
Analog input voltage	V_{AIN}			0		AV_{DD} and V_{DD}	V
		Intenal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 4			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 4			V

Notes 1. The lower 2 bits of the ADCR register cannot be used.

2. The lower 4 bits of the ADCR register cannot be used.

3. Excludes quantization error (±1/2 LSB).

4. Refer to **5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics**.

<R> (6) When reference voltage (+) = internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{SS} (ADREFM = 0), target for conversion: ANI0 to ANI4, ANI16 to ANI18, ANI20 to ANI26, ANI28, and ANI30

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, AV_{DD} ≤ V_{DD}, V_{SS} = 0 V, AV_{SS} = 0 V, reference voltage (+) = internal reference voltage, reference voltage (–) = AV_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error[Notes]	EZS	8-bit resolution			±4.0	LSB
Integral linearity error[Note]	ILE	8-bit resolution			±2.0	LSB
Differential linearity error[Note]	DLE	8-bit resolution			±2.5	LSB
Reference voltage (+)	$AV_{REF}(+)$	= internal reference voltage (V_{BGR})	1.38	1.45	1.5	V
Analog input voltage	V_{AIN}		0		V_{BGR}	V

Note Excludes quantization error (±1/2 LSB).

5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics

(T_A = −40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

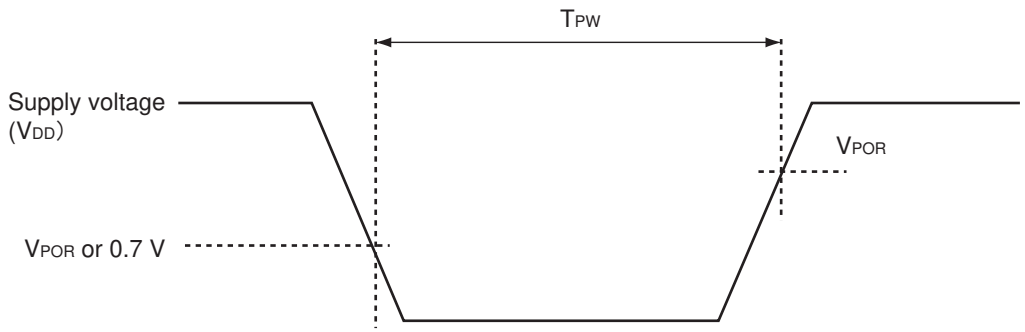
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor output voltage that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t_{AMP}		10			μs

5. 2. 5. 3 POR circuit characteristics

(T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	When power supply voltage is rising	1.47	1.51	1.55	V
	V_{PDR}	When power supply voltage is falling	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note This is the time required for the POR circuit to execute a reset when V_{DD} falls below V_{PDR}. When the microcontroller enters STOP mode or if the main system clock (f_{MAIN}) has been stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), this is the time required for the POR circuit to execute a reset before V_{DD} rises to V_{POR} after having fallen below 0.7 V.



5. 2. 5. 4 LVD circuit characteristics

• LVD detection voltage of reset mode and interrupt mode

(T_A = −40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD10}	When power supply voltage is rising	3.98	4.06	4.14	V
			When power supply voltage is falling	3.90	3.98	4.06	V
		V_{LVD11}	When power supply voltage is rising	3.68	3.75	3.82	V
			When power supply voltage is falling	3.60	3.67	3.74	V
		V_{LVD12}	When power supply voltage is rising	3.07	3.13	3.19	V
			When power supply voltage is falling	3.00	3.06	3.12	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

• LVD detection voltage of interrupt & reset mode

(T_A = −40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDB0}	VPOC2, VPOC1, VPOC0 = 0, 0, 1 reset release when power supply voltage is falling			1.80	1.84	1.87	V
	V_{LVDB3}		LVIS1, LVIS0 = 0, 0	Reset release voltage when power supply voltage is rising	3.07	3.13	3.19	V
				Interrupt generating voltage when power supply voltage is falling	3.00	3.06	3.12	V
	V_{LVDC0}	VPOC2, VPOC1, VPOC0 = 0, 1, 0 reset release when power supply voltage is falling			2.40	2.45	2.50	V
	V_{LVDC3}		LVIS1, LVIS0 = 0, 0	Reset release voltage when power supply voltage is rising	3.68	3.75	3.82	V
				Interrupt generating voltage when power supply voltage is falling	3.60	3.67	3.74	V
	V_{LVDD0}	VPOC2, VPOC1, VPOC0 = 0, 1, 1 reset release when power supply voltage is falling			2.70	2.75	2.81	V
	V_{LVDD3}		LVIS1, LVIS0 = 0, 0	Reset release voltage when power supply voltage is rising	3.98	4.06	4.14	V
				Interrupt generating voltage when power supply voltage is falling	3.90	3.98	4.06	V

<R>

Caution Set the detection voltage (V_{LVD}) to be within the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H/010C2H). The following shows the operating voltage range.

HS (high-speed main) mode: V_{DD} = 2.7 to 5.5 V@1 MHz to 32 MHz

V_{DD} = 2.4 to 5.5 V@1 MHz to 16 MHz

LS (low-speed main) mode: V_{DD} = 1.8 to 5.5 V@1 MHz to 8 MHz

LV (low voltage main) mode: V_{DD} = 1.6 to 5.5 V@1 MHz to 4 MHz

5. 2. 5. 5 Supply voltage rise slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage rise	SVDD				54	V/ms

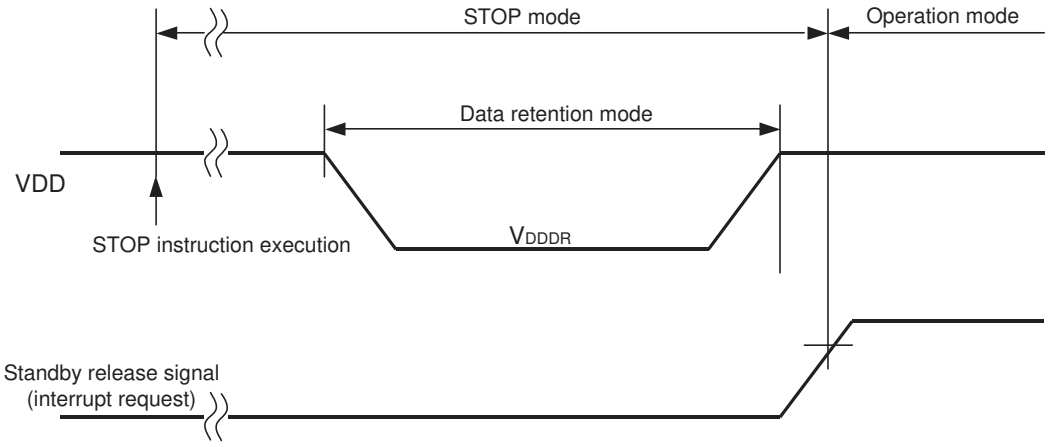
Caution Be sure to maintain the internal reset state until V_{DD} reaches the operating voltage range specified in 5. 2. 3 AC Characteristics, by using the LVD circuit or external reset pin.

5. 2. 6 Data memory STOP mode low supply voltage data retention characteristics

<R> (T_A = −40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effective, but data is not retained when a POR reset is effective.



5. 2. 7 Flash memory programming characteristics

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		32	MHz
Number of code flash rewrites Note 1, 2	C_{erwr}	Retained for 20 years	T_A = 85°C Note 3	1,000			times
Number of data flash rewrites Note 1, 2		Retained for 1 year	T_A = 25°C Note 3		1,000,000		
		Retained for 5 years	T_A = 85°C Note 3	100,000			
		Retained for 20 years	T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using a flash memory programmer and a Renesas Electronics self programming library.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

<R> 5. 2. 8 Dedicated flash memory programmer communication (UART)

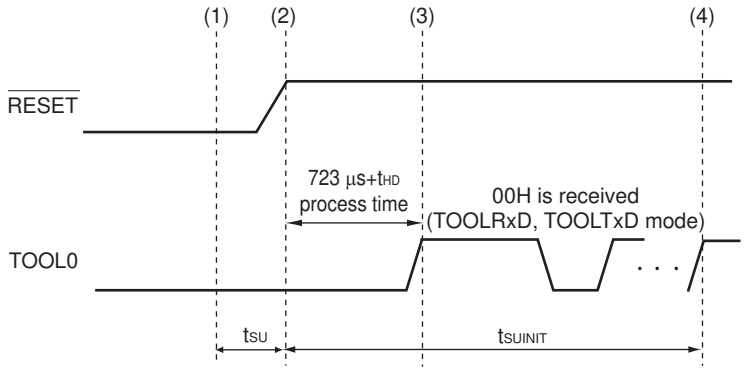
(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		When programming for flash memory	115.2 k		1 M	bps

<R> **5. 2. 9 Timing specs for switching flash memory programming modes**

(T_A = −40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD resets must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a external reset ends	t_{SU}	POR and LVD resets must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except flash firmware processing time)	t_{HD}	POR and LVD resets must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD resets must end before the external reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> The flash memory programming mode is set by UART reception and the baud rate setting completes.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a external reset ends.

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external or internal resets end (except flash firmware processing time).

5. 3 Electrical Specifications of Analog Block

<R> 5. 3. 1 Operating conditions of analog block

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP.	MAX.	
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, AV_{DD3}, DV_{DD}	3.0	–	5.5	V

5. 3. 2 Supply current characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V)

Parameter	Symbol	Conditions		Ratings			Unit
				MIN	TYP	MAX	
Supply current	Istby11[Note]	PC1 = 00H, PC2 = 00H	T_A = -40°C	–	100	150	nA
			T_A = +25°C	–	140	210	nA
			T_A = +50°C	–	290	550	nA
			T_A = +85°C	–	850	1850	nA
	Im111[Note]	PC1 = 47H (configurable amplifiers Ch1 to Ch3 and D/A converters Ch3 are operating) PC2 = 00H, CC1, CC0 = 0, 0, DACRC = 00H		–	1.55	3.6	mA
	Im112[Note]	PC1 = F7H, PC2 = 13H (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, gain adjustment amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	3.4	7.6	mA
	Im113[Note]	PC1 = 7FH, PC2 = 0FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, low-pass filter, high-pass filter, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	4.5	11.0	mA
	Im114[Note]	PC1 = F7H, PC2 = 1FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, general operational amplifier, low-pass filter, high-pass filter, gain adjustment amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 0, 0, DACRC = 00H		–	4.5	11.3	mA
	Im121[Note]	PC1 = 47H (configurable amplifiers Ch1 to Ch3 and D/A converters Ch1 to Ch3 are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	0.73	1.8	mA
	Im122[Note]	PC1 = F7H, PC2 = 13H (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, gain adjustment amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	2.6	5.8	mA
	Im123[Note]	PC1 = F7H, PC2 = 0FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, low-pass filter, high-pass filter, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	3.7	9.2	mA
	Im124[Note]	PC1 = F7H, PC2 = 1FH (configurable amplifiers Ch1 to Ch3, D/A converters Ch1 to Ch4, low-pass filter, high-pass filter, gain adjustment amplifier, variable output voltage regulator, reference voltage generator, and temperature sensor are operating), CC1, CC0 = 1, 1, DACRC = 00H		–	3.9	9.5	mA

(**Note** is listed on the next page.)

Note Total current flowing to internal power supply pins AV_{DD1}, AV_{DD2}, AV_{DD3}, and DV_{DD}. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to AV_{DD1}, AV_{DD2}, AV_{DD3} or DV_{DD}, or AGND1, AGND2, AGND3, AGND4, or DGND is included. See the table below to check the definition of those symbols of the current flowing.

Parameter	Symbol	Analog function with power on											
		Configurable amplifier			Gain adjustment amplifier	D/A converter				Low-pass filter	High-pass filter	Temperature sensor	Variable output voltage regulator
		Ch1	Ch2	Ch3		Ch1	Ch2	Ch3	Ch4				
Supply current	Im111 Note 1	ON	ON	ON	–	–	–	ON	–	–	–	–	–
	Im112 Note 1	ON	ON	ON	ON	ON	ON	ON	ON	–	–	ON	ON
	Im113 Note 1	ON	ON	ON	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im114 Note1	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
	Im121 Note 2	ON	ON	ON	–	–	–	ON	–	–	–	–	–
	Im122 Note 2	ON	ON	ON	ON	ON	ON	ON	ON	–	–	ON	ON
	Im123 Note 2	ON	ON	ON	–	ON	ON	ON	ON	ON	ON	ON	ON
	Im124 Note 2	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON

Notes 1. CC1, CC0 = 0, 0

2. CC1, CC0 = 1, 1

5. 3. 3 Electrical specifications of each block

5. 3. 3. 1 Configurable amplifier characteristics

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, non-inverting amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	μA
	Icc01	CC1, CC0 = 0, 1	–	175	390	μA
	Icc10	CC1, CC0 = 1, 0	–	125	275	μA
	Icc11	CC1, CC0 = 1, 1	–	55	120	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Setting time	t_{SET_AMP00}	GCn = 00H (9.5 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GCn = 00H (9.5 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GCn = 00H (9.5 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GCn = 00H (9.5 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF, CC1, CC0 = 0, 0 GCn = 11H (40.1 dB)	–	2.3		MHz
	GBW01	CL = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40.1 dB)	–	1.1		MHz
	GBW10	CL = 30 pF, CC1, CC0 = 1, 0 GCn = 11H (40.1 dB)	–	0.71		MHz
	GBW11	CL = 30 pF, CC1, CC0 = 1, 1 GCn = 11H (40.1 dB)	–	0.22		MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	64	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40.1 dB)	–	107	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40.1 dB)	–	159	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, non-inverting amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20.8 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20.8 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20.8 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (9.5 dB)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (9.5 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (9.5 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	μA
	Icc01	CC1, CC0 = 0, 1	–	175	390	μA
	Icc10	CC1, CC0 = 1, 0	–	125	275	μA
	Icc11	CC1, CC0 = 1, 1	–	55	120	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1} - 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF,CC1, CC0 = 0, 0 GCn = 11H (40 dB)	–	1.5		MHz
	GBW01	CL = 30 pF,CC1, CC0 = 0, 1 GCn = 11H (40 dB)	–	0.9		MHz
	GBW10	CL = 30 pF,CC1, CC0 = 1, 0 GCn = 11H (40 dB)	–	0.67		MHz
	GBW11	CL = 30 pF,CC1, CC0 = 1, 1 GCn = 11H (40 dB)	–	0.22		MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	63	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	105	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	150	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, inverting amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GCn = 00H (6 dB), f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GCn = 00H (6 dB), f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1 GCn = 00H (6 dB), f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, differential amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	μA
	Icc01	CC1, CC0 = 0, 1	–	175	390	μA
	Icc10	CC1, CC0 = 1, 0	–	125	275	μA
	Icc11	CC1, CC0 = 1, 1	–	55	120	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1+ 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GCn = 00H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GCn = 00H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GCn = 00H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF, CC1, CC0 = 0, 0, GCn = 11H (40 dB)	–	1.5	–	MHz
	GBW01	CL = 30 pF, CC1, CC0 = 0, 1, GCn = 11H (40 dB)	–	1.0	–	MHz
	GBW10	CL = 30 pF, CC1, CC0 = 1, 0, GCn = 11H (40 dB)	–	0.67	–	MHz
	GBW11	CL = 30 pF, CC1, CC0 = 1, 1, GCn = 11H (40 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 11H (40 dB)	–	63	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 11H (40 dB)	–	85	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 11H (40 dB)	–	106	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 11H (40 dB)	–	160	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, differential amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C GCn = 07H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C GCn = 07H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C GCn = 07H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
<R> Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (6 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0 CL = 30 pF, GCn = 00H (6 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (6 dB)	–	0.09	–	V/μs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0, GCn = 11H (40 dB), f = 1 kHz	–	84	–	dB
	CMRR01	CC1, CC0 = 0, 1, GCn = 11H (40 dB) f = 1 kHz	–	82	–	dB
	CMRR10	CC1, CC0 = 1, 0, GCn = 11H (40 dB) f = 1 kHz	–	80	–	dB
	CMRR11	CC1, CC0 = 1, 1, GCn = 11H (40 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (6 dB), f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (6 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (6 dB) f = 1 kHz	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (6 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

Remark n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, transimpedance amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption Note	Icc00	CC1, CC0 = 0, 0	–	330	720	μA
	Icc01	CC1, CC0 = 0, 1	–	175	390	μA
	Icc10	CC1, CC0 = 1, 0	–	125	275	μA
	Icc11	CC1, CC0 = 1, 1	–	55	120	μA
Input current	IINL	GCn = 0FH (Rfb = 640 kΩ)	(10)	–	–	nA
Output voltage	VOUTL	IOL= -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GCn = 00H (20 kΩ), CC1, CC0 = 0, 0 CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GCn = 00H (20 kΩ), CC1, CC0 = 0, 1 CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GCn = 00H (20 kΩ), CC1, CC0 = 1, 0 CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GCn = 00H (20 kΩ), CC1, CC0 = 1, 1 CL = 30 pF, output voltage = 1V_{PP}, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Current-to-voltage conversion gain bandwidth	GBW00_0	CL = 30 pF, CC1, CC0 = 0, 0 GCn = 00H (Rfb = 20 kΩ)	–	1.3	–	MHz
	GBW00_1	CL = 30 pF, CC1, CC0 = 0, 0 GCn = 0FH (Rfb = 640 kΩ)	–	1.0	–	MHz
	GBW01_0	CL = 30 pF, CC1, CC0 = 0, 1 GCn = 00H (Rfb = 20 kΩ)	–	0.79	–	MHz
	GBW01_1	CL = 30 pF, CC1, CC0 = 0, 1 GCn = 0FH (Rfb = 640 kΩ)	–	0.51	–	MHz
	GBW10_0	CL = 30 pF, CC1, CC0 = 1, 0 GCn = 00H (Rfb = 20 kΩ)	–	0.58	–	MHz
	GBW10_1	CL = 30 pF, CC1, CC0 = 1, 0 GCn = 0FH (Rfb = 640 kΩ)	–	0.31	–	MHz
	GBW11_0	CL = 30 pF, CC1, CC0 = 1, 1 GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	MHz
	GBW11_1	CL = 30 pF, CC1, CC0 = 1, 1 GCn = 0FH (Rfb = 640 kΩ)	–	0.09	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	66	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	90	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	116	–	nV/√ Hz
	En11	CC1, CC0 = 1, 1 f = 1 kHz, GCn = 00H (Rfb = 20 kΩ)	–	193	–	nV/√ Hz

Note These are the values for one channel of configurable amplifier.

Remark 1. In the ratings column, values in parentheses are the target design values and therefore are not tested for shipment.

2. n = 1 to 3

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, transimpedance amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GCn = 07H (Rfb = 80 kΩ)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GCn = 00H (Rfb = 20 kΩ)	–	0.09	–	V/μs
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0, GCn = 00H (Rfb = 20 kΩ)	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1, GCn = 00H (Rfb = 20 kΩ)	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0, GCn = 00H (Rfb = 20 kΩ)	–	62	–	dB
	PSRR11	CC1, CC0 = 1, 1, GCn = 00H (Rfb = 20 kΩ)	–	50	–	dB
Rfb setting error	Rfb_Accu1	T_A = 25°C	-25	–	25	%
	Rfb_Accu2	T_A = –40 to 85°C	-35	–	35	%

Remark n = 1 to 3

($-40°C \leq T_A \leq 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier) (1/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 0	–	970	2,150	μA
	Icc01	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 0, 1	–	510	1,150	μA
	Icc10	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 0	–	350	780	μA
	Icc11	AMP1OF = AMP2OF = AMP3OF = 1, CC1, CC0 = 1, 1	–	140	330	μA
Input voltage	VINL		AGND1 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 1.5	V
Output voltage	VOUTL	IOL = -200 μA	–	AGND1 + 0.02	AGND1 + 0.06	V
	VOUTH	IOH = 200 μA	AV_{DD1}- 0.06	AV_{DD1} - 0.02	–	V
Settling time	t_{SET_AMP00}	GC3 = 00H (20 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	9	μs
	t_{SET_AMP01}	GC3 = 00H (20 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	GC3 = 00H (20 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	28	μs
	t_{SET_AMP11}	GC3 = 00H (20 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	71	μs
Gain bandwidth	GBW00	CL = 30 pF, CC1, CC0 = 0, 0 GC3 = 11H (54 dB)	–	1.82	–	MHz
	GBW01	CL = 30 pF, CC1, CC0 = 0, 1 GC3 = 11H (54 dB)	–	1.03	–	MHz
	GBW10	CL = 30 pF, CC1, CC0 = 1, 0 GC3 = 11H (54 dB)	–	0.69	–	MHz
	GBW11	CL = 30 pF, CC1, CC0 = 1, 1 GC3 = 11H (54 dB)	–	0.22	–	MHz
Equivalent input noise	En00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	90	–	nV/√ Hz
	En01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	119	–	nV/√ Hz
	En10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	150	–	nV/√ Hz
<R>	En11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	260	–	nV/√ Hz

(-40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN1 = VREFIN2 = VREFIN3 = 1.7 V, AMP1OF = AMP2OF = AMP3OF = 1, DAC1OF = DAC2OF = DAC3OF = 0, GC1 = GC2 = 03H, instrumentation amplifier) (2/2)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	CC1, CC0 = 0, 0, T_A = 25°C, GC3 = 00H (20 dB)	-7	–	7	mV
	VOFF01	CC1, CC0 = 0, 1, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF10	CC1, CC0 = 1, 0, T_A = 25°C, GC3 = 00H (20 dB)	-10	–	10	mV
	VOFF11	CC1, CC0 = 1, 1, T_A = 25°C, GC3 = 00H (20 dB)	-12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC		–	±6.0	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.68	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.35	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF, GC3 = 00H (20 dB)	–	0.25	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF, GC3 = 00H (20 dB)	–	0.09	–	V/μs
Common mode rejection ratio	CMRR00	CC1, CC0 = 0, 0 GC3 = 11H (54 dB) f = 1 kHz	–	86	–	dB
	CMRR01	CC1, CC0 = 0, 1 GC3 = 11H (54 dB) f = 1 kHz	–	84	–	dB
	CMRR10	CC1, CC0 = 1, 0 GC3 = 11H (54 dB) f = 1 kHz	–	82	–	dB
<R>	CMRR11	CC1, CC0 = 1, 1 GC3 = 11H (54 dB) f = 1 kHz	–	76	–	dB
Power supply rejection ratio	PSRR00	CC1, CC0 = 0, 0 GC3 = 00H (20 dB) f = 1 kHz	–	70	–	dB
	PSRR01	CC1, CC0 = 0, 1 GC3 = 00H (20 dB) f = 1 kHz	–	68	–	dB
	PSRR10	CC1, CC0 = 1, 0 GC3 = 00H (20 dB) f = 1 kHz	–	62	–	dB
<R>	PSRR11	CC1, CC0 = 1, 1 GC3 = 00H (20 dB) f = 1 kHz	–	50	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

5. 3. 3. 2 Gain adjustment amplifier characteristics

(1) 64-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
Gain bandwidth	GBW2	CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB)	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR2	f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB

(2) 80-pin products

(–40°C ≤ T_A ≤ 85°C, AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0 V, VREFIN4 = 1.7 V, GAINOF = 1, DAC4OF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	530	1,300	μA
Input voltage	VINL		AGND2 - 0.1	–	–	V
	VINH		–	–	AV_{DD1} - 0.05	V
Output voltage	VOUTL1	IOL = -100 μA, GAINAMP_OUT pin	–	AGND2 + 0.02	AGND2 + 0.05	V
	VOUTH1	IOH = 100 μA, GAINAMP_OUT pin	AV_{DD1} - 0.05	AV_{DD1} - 0.02	–	V
	VOUTL2	IOL = -100 μA, SYNCH_OUT pin	–	AGND2 + 0.03	AGND2 + 0.06	V
	VOUTH2	IOH = 100 μA, SYNCH_OUT pin	AV_{DD1} - 0.06	AV_{DD1} - 0.03	–	V
Gain bandwidth	GBW1	CLK_SYNCH = H, SYNCH_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	1.38	–	MHz
	GBW2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin CL = 30 pF, GC4 = 11H (40 dB)	–	0.86	–	MHz
Input conversion offset voltage	VOFF	GC4 = 00H (6 dB), T_A = 25°C, GAINAMP_IN = 2.5 V	-30	–	30	mV
Input conversion offset voltage temperature coefficient	VOTC1	CLK_SYNCH = H, SYNCH_OUT pin	–	±6	–	μV/°C
	VOTC2	CLK_SYNCH = L, GAINAMP_OUT pin	–	±18	–	μV/°C
Slew rate	SR	CL = 30 pF	–	0.9	–	V/μs
Equivalent input noise	En_Gain	f = 1 kHz, GC4 = 11H (40 dB) GAINAMP_OUT pin	–	700	–	nV/√ Hz
Power supply rejection ratio	PSRR1	CLK_SYNCH = H, SYNCH_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	60	–	dB
	PSRR2	CLK_SYNCH = L, SYNCH_OUT or GAINAMP_OUT pin, f = 1 kHz, GC4 = 00H (6 dB)	–	45	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	-0.6	–	0.6	dB
	GAIN_Accu2	T_A = –40 to 85°C	-1.0	–	1.0	dB
CLK_SYNCH low-level input voltage	V_{ILCLK_SYNCH}				0.3 × AV_{DD1}	V
CLK_SYNCH high-level input voltage	V_{IHCLK_SYNCH}		0.7 × AV_{DD1}			V

5. 3. 3. 3 D/A converter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = DV_{DD} = 5.0$ V, DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
DAC ALL ON current consumption 1	I_{DAC_ON1}	DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1, VRB1, VRB0 = 0, 0	–	1400	2950	μA
DAC ALL ON current consumption 2	I_{DAC_ON2}	DAC1OF = DAC2OF = DAC3OF = DAC4OF = 1, VRB1, VRB0 ≠ 0, 0	–	1620	3360	μA
Buffer AMP ON current consumption 1 Note 1	I_{DAC_Buff1}	DACxOF = 1, VRB1, VRB0 = 0, 0 (x = 1, 2, 3, 4)	–	390	820	μA
Buffer AMP ON current consumption 2 Note 1	I_{DAC_Buff2}	DACxOF = 1, VRB1, VRB0 ≠ 0, 0 (x = 1, 2, 3, 4)	–	610	1320	μA
DAC1 GAMP ON current consumption	I_{DAC_AMP1}	DAC1OF = 1	–	140	320	μA
DAC2 GAMP ON current consumption	I_{DAC_AMP2}	DAC2OF = 1	–	120	265	μA
DAC3 GAMP ON current consumption	I_{DAC_AMP3}	DAC3OF = 1	–	120	265	μA
DAC4 GAMP ON current consumption	I_{DAC_AMP4}	DAC4OF = 1	–	630	1370	μA
Resolution	RES		–	–	8	bit
<R> Settling time	tSET	output voltage = 1 Vpp output convergence voltage Vpp = 990 mV	–	–	100	μs
Differential non-linearity error Note 2	DNL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	–2	–	2	LSB
Integral non-linearity error	INL	VRT1 = VRT0 = 0, VRB1 = VRB0 = 0	–2	–	2	LSB

Notes 1. Buffer amplifier is powered on when one of DACx (x = 1, 2, 3, 4) is powered on at least. For example, the current consumption ($I_{_EXAMPLE}$) is shown as a following equation when "DAC1OF=DAC2OF=1", and "VRB1, VRB0=0, 0". $I_{EXAMPLE} = I_{DAC_Buff1} + I_{DAC_AMP1} + I_{DAC_AMP2}$

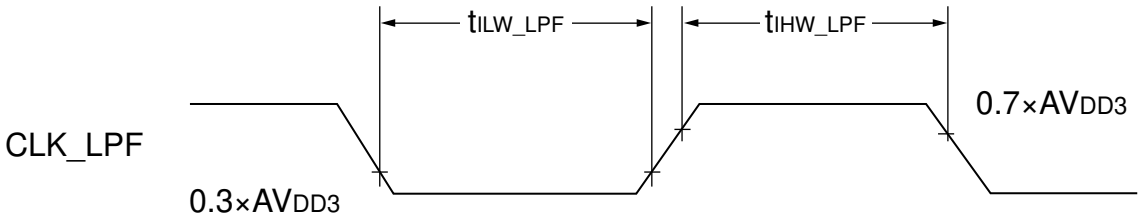
2. Guaranteed monotonic.

5. 3. 3. 4 Low-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, LPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILLPF}		AGND4 +0.2	–	–	V
	V_{IHLPF}		–	–	AV_{DD3} -1.5	V
Output voltage	V_{OLLPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHLPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_LPF} = 2 kHz	–	9	–	Hz
	fc2	f_{CLK_LPF} = 1 MHz	–	4.5	–	kHz
CLK_LPF low-level input voltage	V_{ILCLK_LPF}				$0.3 \times AV_{DD3}$	V
CLK_LPF high-level input voltage	V_{IHCLK_LPF}		$0.7 \times AV_{DD3}$			V
CLK_LPF Input frequency	f_{CLK_LPF}		2	–	1000	kHz
<R> CLK_LPF Input low-level-width Input high-level-width	t_{ILW_LPF} t_{IHW_LPF}		200	–	–	ns

Clock Timing

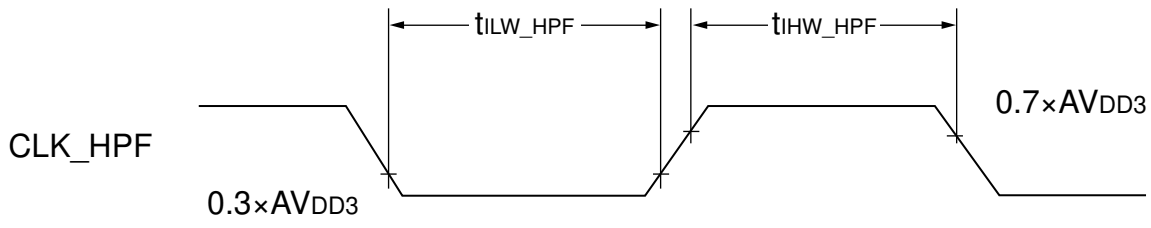


5. 3. 3. 5 High-pass filter characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, HPFOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	800	1800	μA
Input voltage	V_{ILHPF}		AGND4 +0.2	–	–	V
	V_{IHHPF}		–	–	AV_{DD3} - 1.5	V
<R> Output voltage	V_{OLHPF}	IOL = –200 μA	–	AGND4 +0.22	AGND4 +0.25	V
	V_{OHHPF}	IOH = 200 μA	AV_{DD3} -1.55	AV_{DD3} -1.52	–	V
Cutoff frequency	fc1	f_{CLK_HPF} = 2 kHz	–	8	–	Hz
	fc2	f_{CLK_HPF} = 200 kHz	–	800	–	Hz
CLK_HPF low-level input voltage	V_{ILCLK_HPF}				$0.3 \times AV_{DD3}$	V
CLK_HPF high-level input voltage	V_{IHCLK_HPF}		$0.7 \times AV_{DD3}$			V
CLK_HPF Input frequency	f_{CLK_HPF}		2	–	200	kHz
CLK_HPF Input low-level-width Input high-level-width	t_{ILW_HPF} t_{IHW_HPF}		200	–	–	ns

Clock Timing



5. 3. 3. 6 Temperature sensor characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, TEMPOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Current consumption	IccA		–	105	220	μA
Output voltage	V_O	$T_A = 25°C$	–	1.67	–	V
Temperature sensitivity	T_{SE}		–	–5.0	–	mV/°C

5. 3. 3. 7 Variable output voltage regulator characteristics

(-40°C ≤ T_A ≤ 85°C, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccON	Iout = 0 mA	–	150	320	μA
Output voltage accuracy	V_Accu	Iout = 0 mA	-10	–	10	%
Load current characteristics	Vout_load	Iout = 0 to 5 mA	–	15	30	mV
Output current	Io		–	–	15	mA
Dropout voltage [Note]	Vd	Iout = 15 mA	–	–	0.4	V
Power supply rejection ratio	PSRR	f = 1 kHz, CL = 4.7 μF, Io = 5 mA, AV_{DD2} = 5.0 V, LDOC = 0DH (3.3 V)	–	60	–	dB
Discharge resistance	Rs	LDOOF = 0	540	715	1200	Ω
Settling time	Tset_rise	CL = 4.7 μF, CBGR_OUT = 0.1 μF	–	–	5.0	ms
	Tset_fall	CL = 4.7 μF, CBGR_OUT = 0.1 μF	–	–	45	ms

Note The output voltage range is determined not only by dropout voltage but also by output voltage accuracy.

5. 3. 3. 8 Reference voltage generator characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN.	TYP.	MAX.	
Output voltage	V_{BGR}		–	1.21	–	V

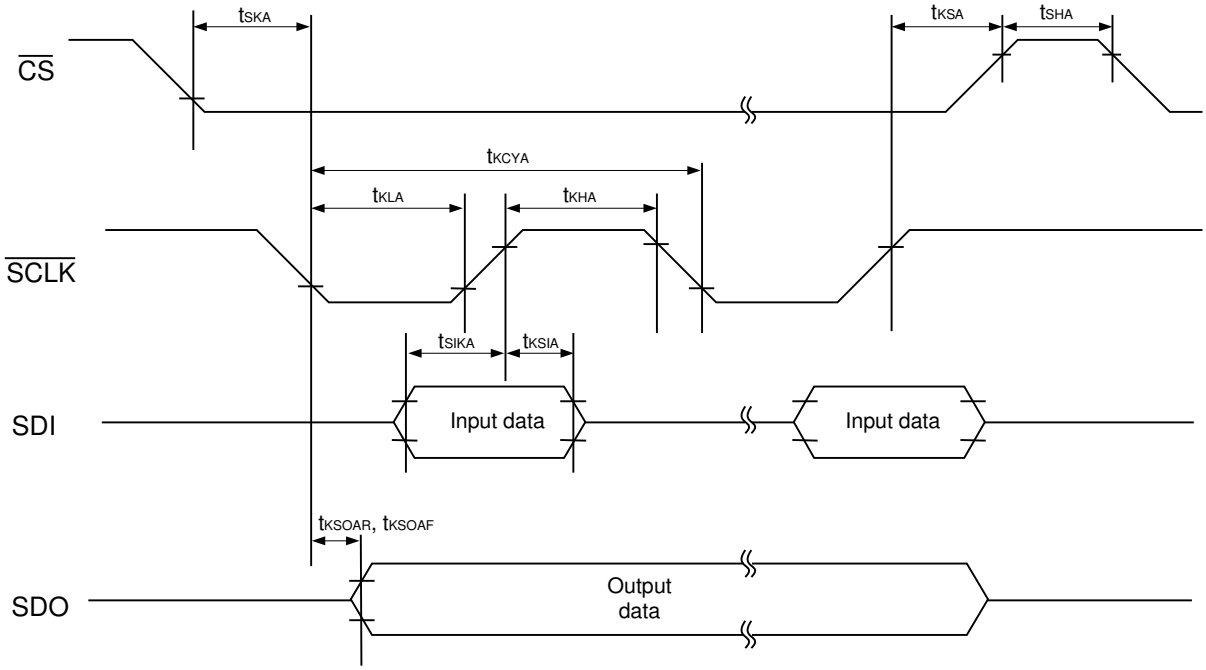
<R> 5. 3. 3. 9 SPI characteristics

($-40°C \le T_A \le 85°C$, $AV_{DD1} = AV_{DD2} = AV_{DD3} = AV_{DD4} = DV_{DD} = 5.0$ V)

	Parameter	Symbol	Conditions	Ratings			Unit
				MIN.	TYP.	MAX.	
	Input voltage, high	V_{IH}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	2.0	DV_{DD}	DV_{DD} + 0.1	V
	Input voltage, low	V_{IL}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin, $\overline{RESET}$ pin	–0.1	DGND	0.7	V
	Leakage current during high level input	I_{leak_Hi1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	–1	–	2	μA
		I_{leak_Hi2}	$\overline{RESET}$ pin	–1	–	2	μA
	Leakage current during low level input Note	I_{leak_Lo1}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	50	100	200	μA
		I_{leak_Lo2}	$\overline{RESET}$ pin	–1	–	2	μA
	Low-level output voltage at SDO pin	V_{SDO_Lo}	IO = -5 mA	–	400	830	mV
	Leakage current when SDO pin is off	I_{leak_SDO}		–1	–	2	μA
<R>	Pull-up resistance	R_{SPI}	$\overline{CS}$ pin, SDI pin, $\overline{SCLK}$ pin	32.5	50	67.5	kΩ
	$\overline{SCLK}$ cycle time	t_{KCYA}		100	–	–	ns
	$\overline{SCLK}$ high-level width low-level width	t_{KHA}, t_{KLA}		$0.9t_{KCYA}/2$	–	–	ns
	SDI setup time (to $\overline{SCLK}$↑)	t_{SIKA}		40	–	–	ns
	SDI hold time (from $\overline{SCLK}$↑)	t_{KSIA}		20	–	–	ns
	Delay time from $\overline{SCLK}$↓ to SDO output	t_{KSOAR}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5 V	–	250	300	ns
		t_{KSOAF}	Pull-up resistance = 10 kΩ, CL = 5 pF, VSDO = 5 V	–	–	20	ns
	$\overline{CS}$ high-level width	t_{SHA}		200	–	–	ns
	Delay time from $\overline{CS}$↓to $\overline{SCLK}$↓ output	t_{SKA}		200	–	–	ns
	Delay time from $\overline{SCLK}$↑ to $\overline{CS}$ ↑ output	t_{KSA}		200	–	–	ns

Note Including the current flowing into each pull-up resistor

SPI transfer clock timing

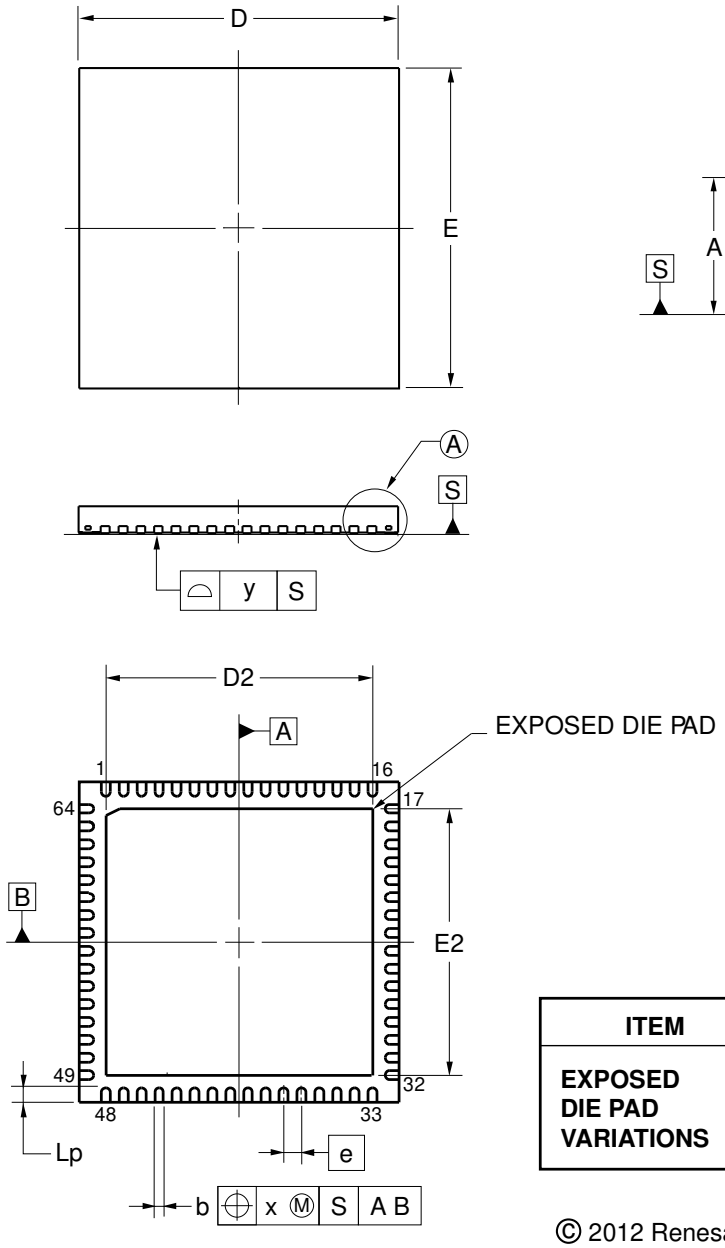


CHAPTER 6 PACKAGE DRAWINGS

R5F10FLCANA, R5F10FLDANA, R5F10FLEANA, R5F10FLCDNA, R5F10FLDDNA, R5F10FLEDNA

64-PIN PLASTIC WQFN (9 x 9)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN64-9x9-0.50	PWQN0064KD-A	P64K8-50-6BA-1	0.21



(UNIT: mm)

ITEM	DIMENSIONS
D	9.00±0.05
E	9.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.50
y	0.50

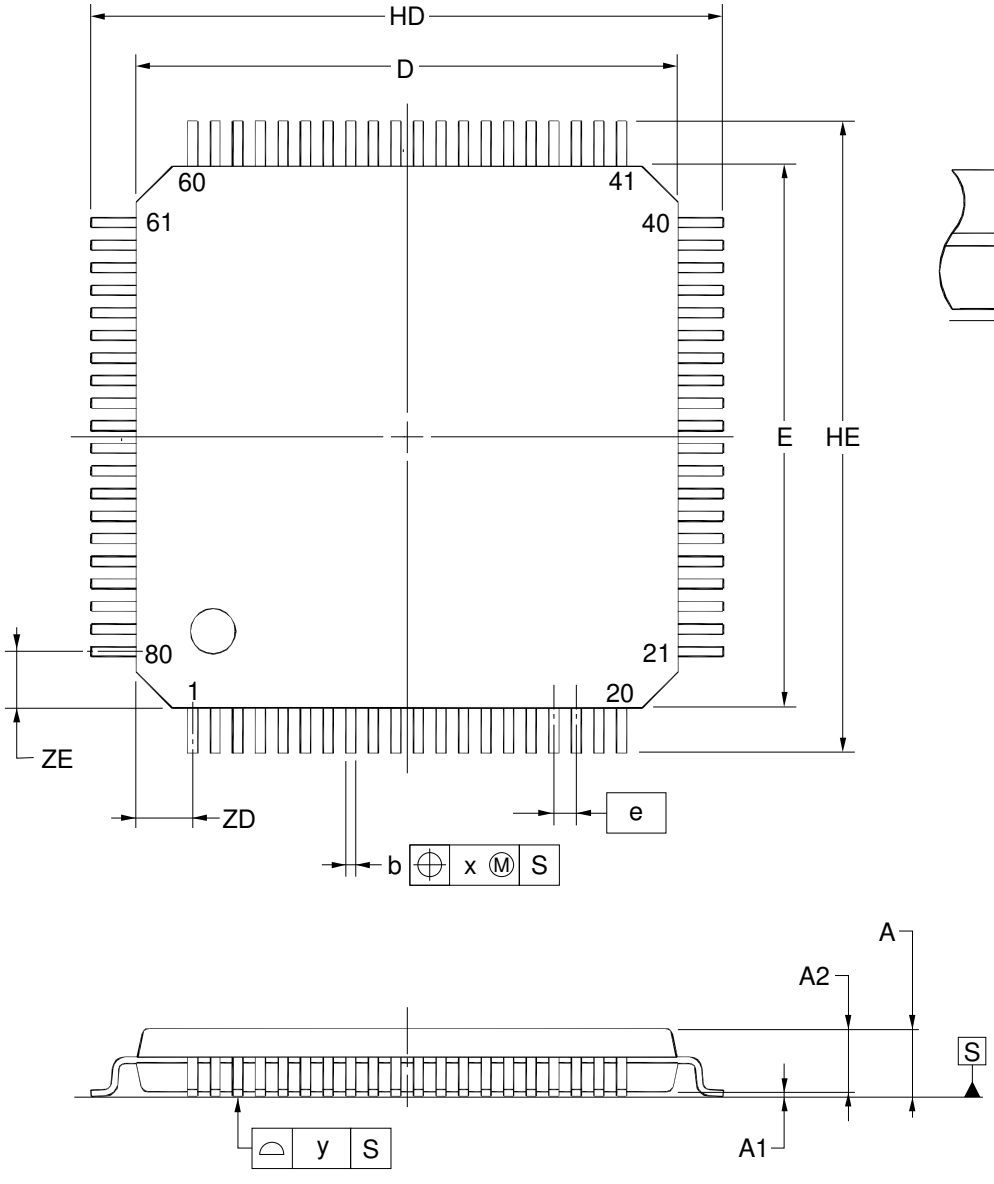
ITEM		D2			E2		
EXPOSED DIE PAD VARIATIONS	A	MIN	NOM	MAX	MIN	NOM	MAX
		7.45	7.50	7.55	7.45	7.50	7.55

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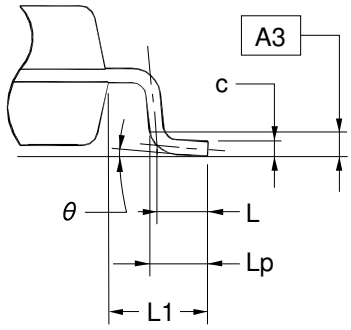
R5F10FMCAFB, R5F10FMDAFB, R5F10FMEAFB, R5F10FMCDFB, R5F10FMDDFB, R5F10FMEDFB

80-PIN PLASTIC LQFP (FINE PITCH) (12 × 12)

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-B	P80GK-50-GAK-2	0.53



detail of lead end



(UNIT:mm)

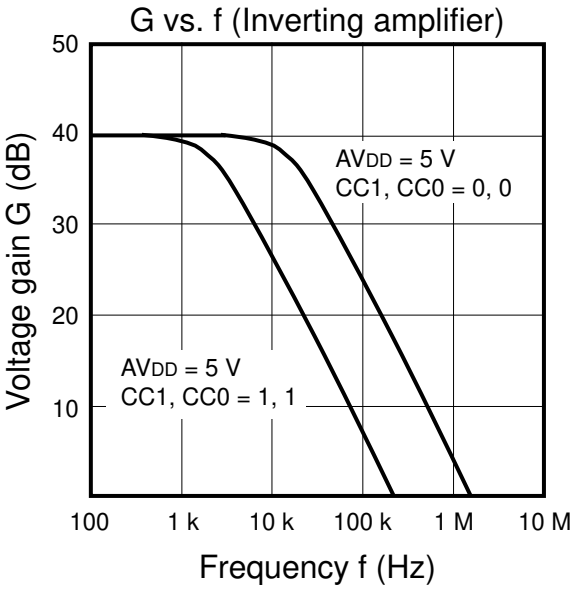
ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

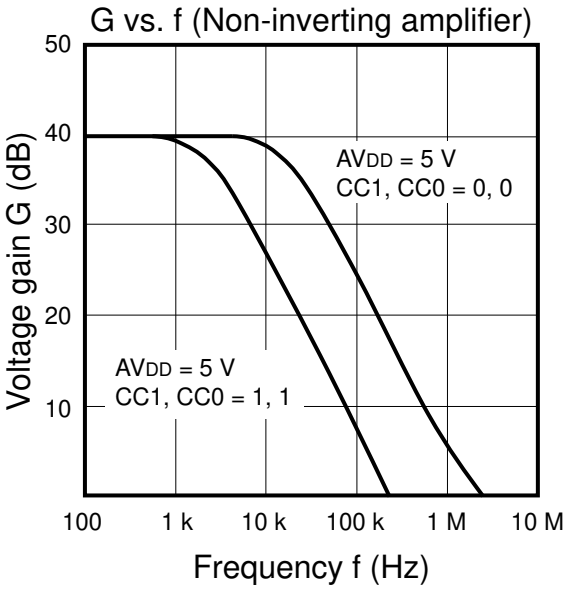
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

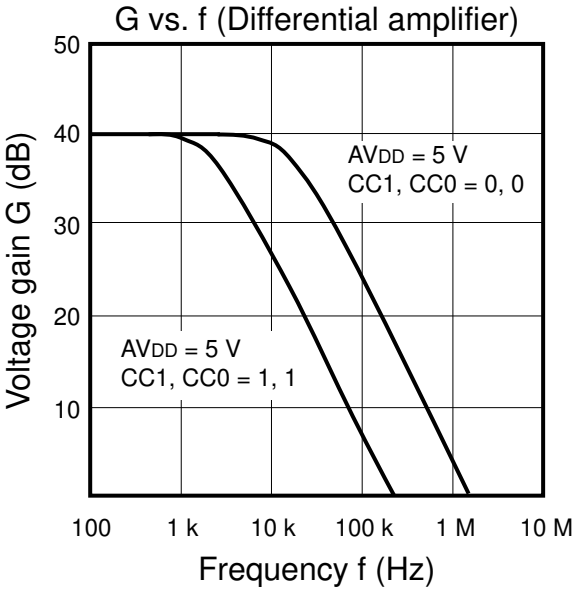
© 2012 Renesas Electronics Corporation. All rights reserved.

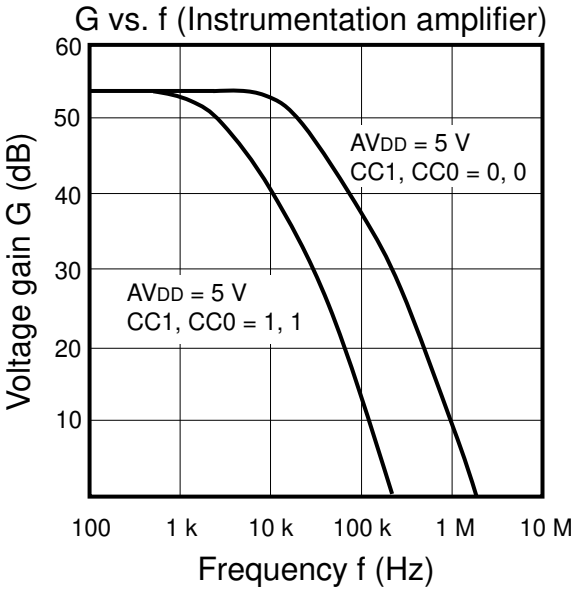
APPENDIX A CHARACTERISTICS CURVE (T_A = 25°C, TYP.) (REFERENCE VALUE)

• Configurable amplifier

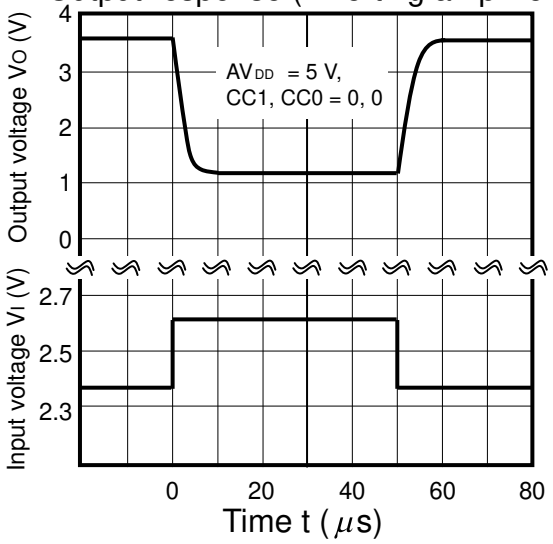




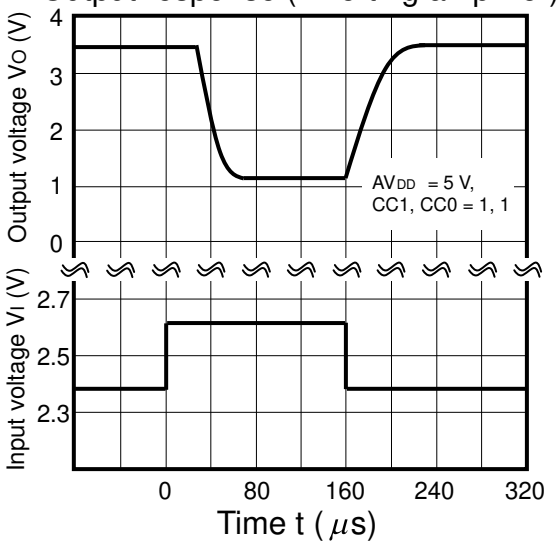




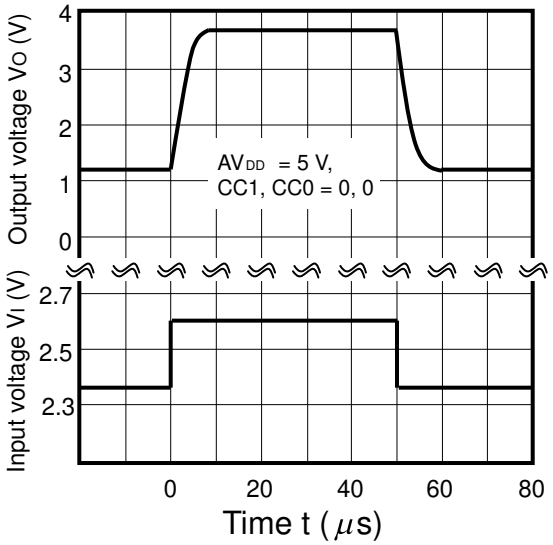
Output response (Inverting amplifier)



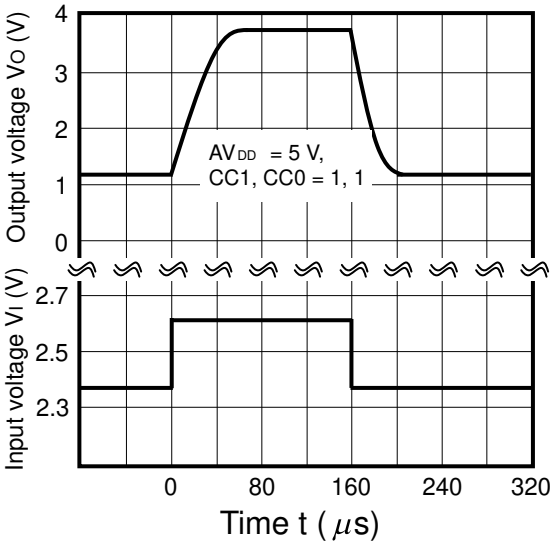
Output response (Inverting amplifier)



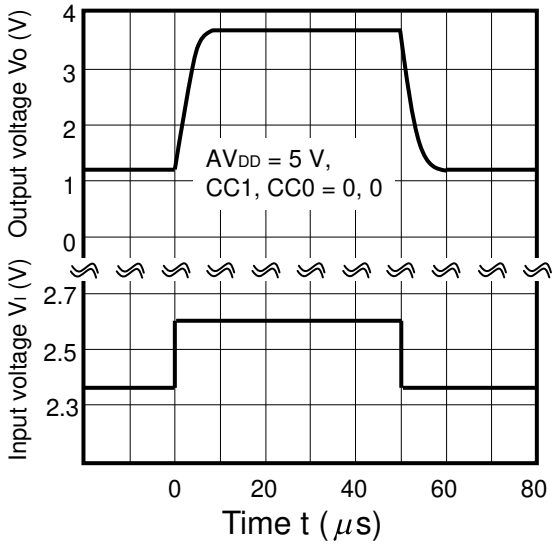
Output response (Non-inverting amplifier)



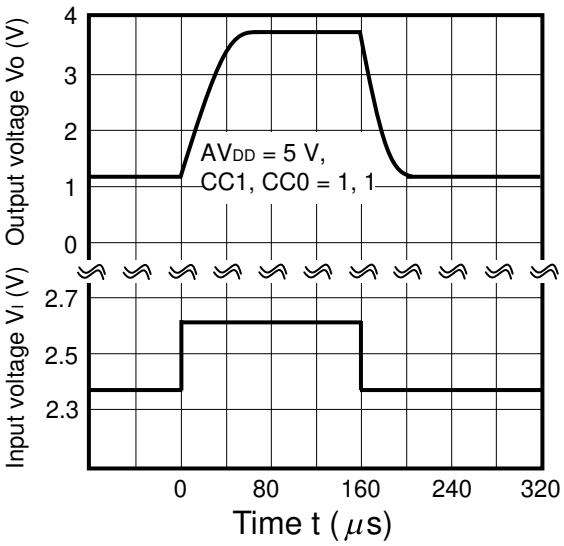
Output response (Non-inverting amplifier)



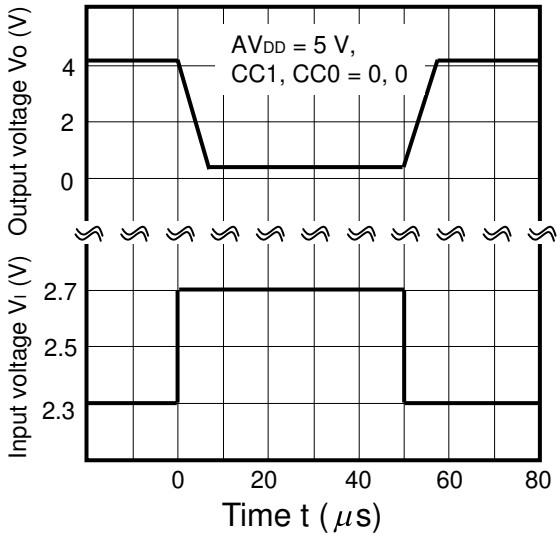
Output response (Differential amplifier)



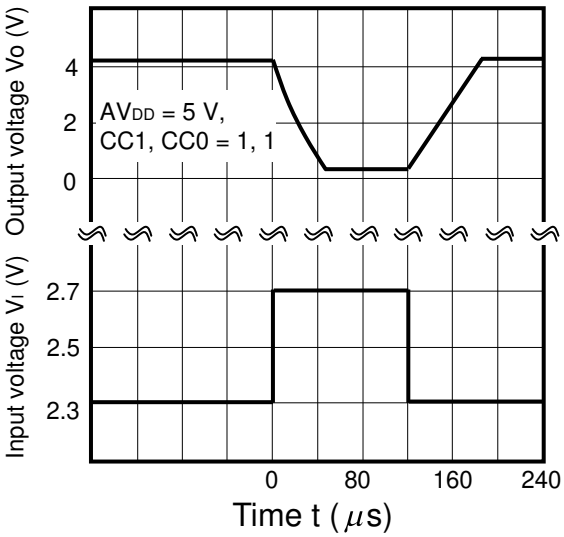
Output response (Differential amplifier)



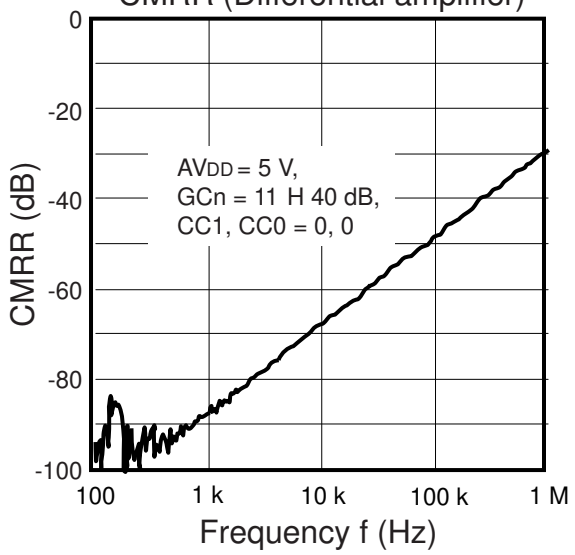
Output response (Instrumentation amplifier)



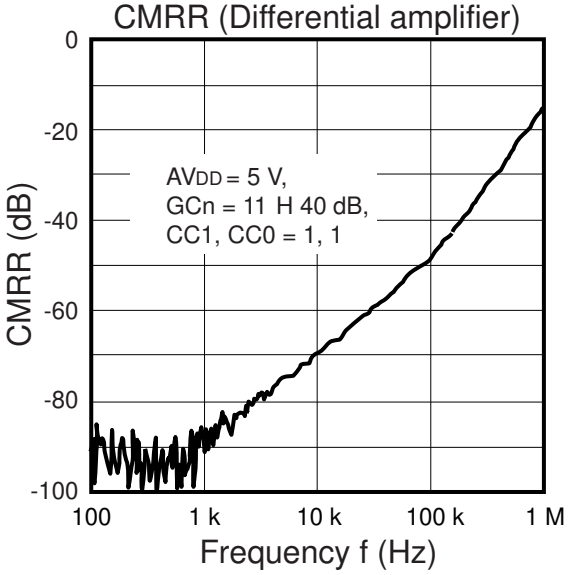
Output response (Instrumentation amplifier)



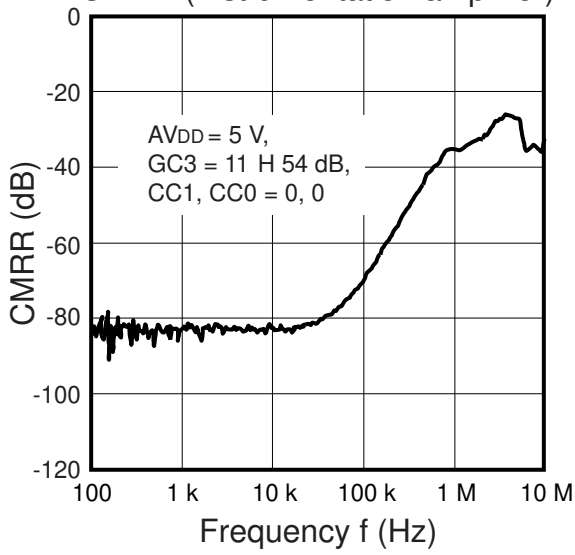
CMRR (Differential amplifier)



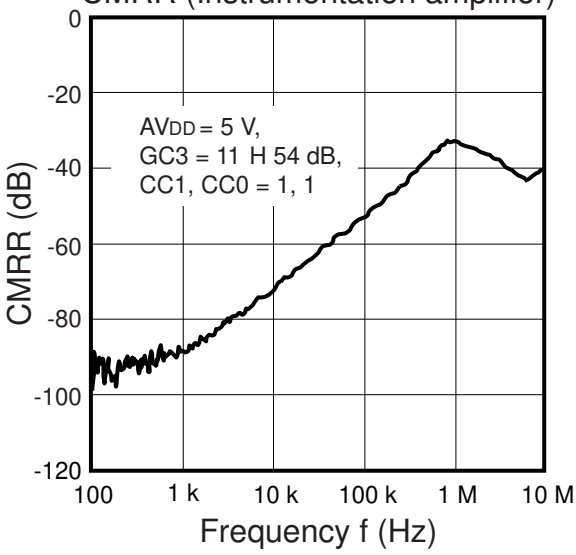
CMRR (Differential amplifier)

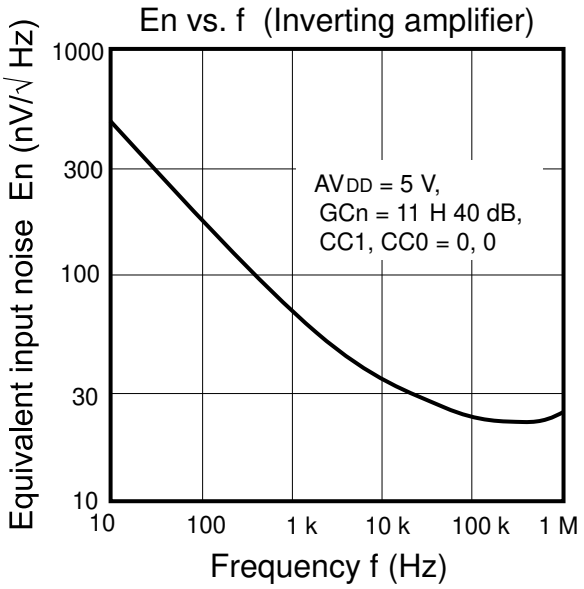


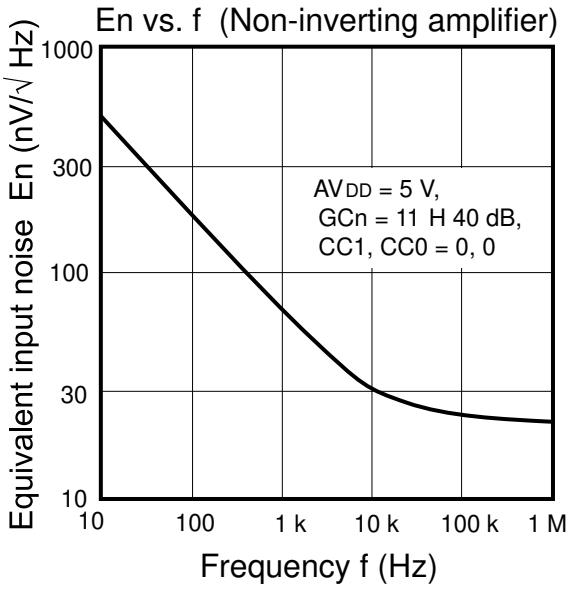
CMRR (Instrumentation amplifier)

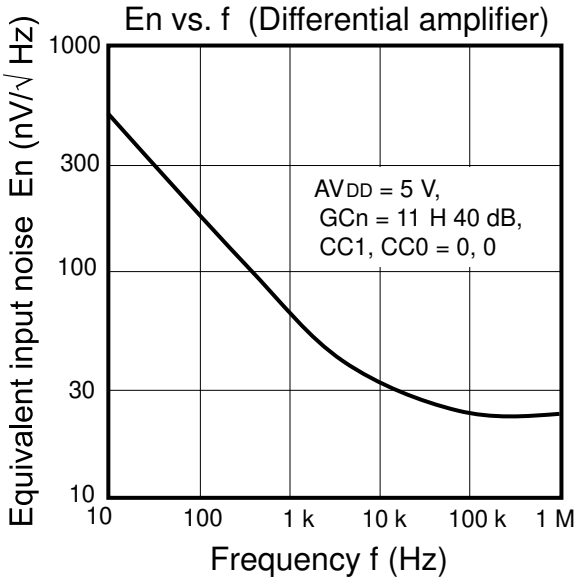


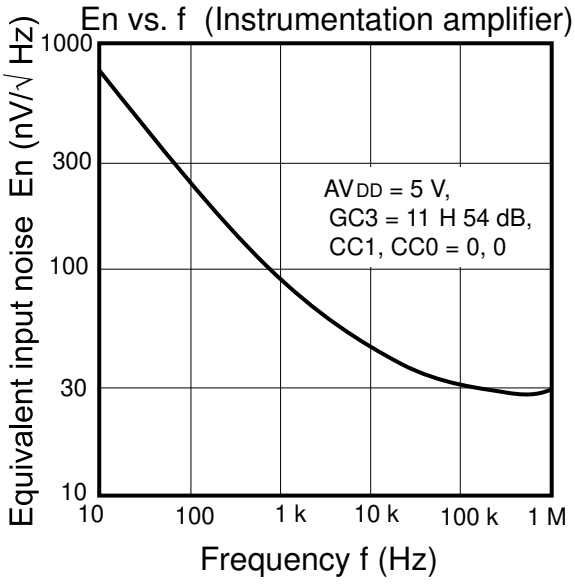
CMRR (Instrumentation amplifier)



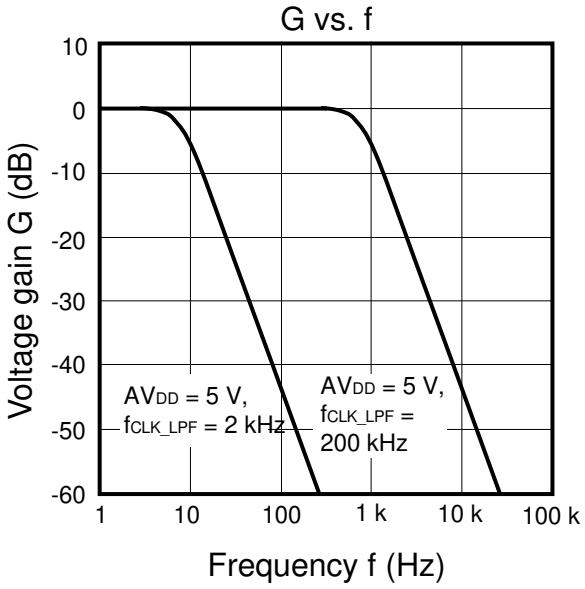

En vs. f (Inverting amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1 k
10 k
100 k
1 M
Frequency f (Hz)

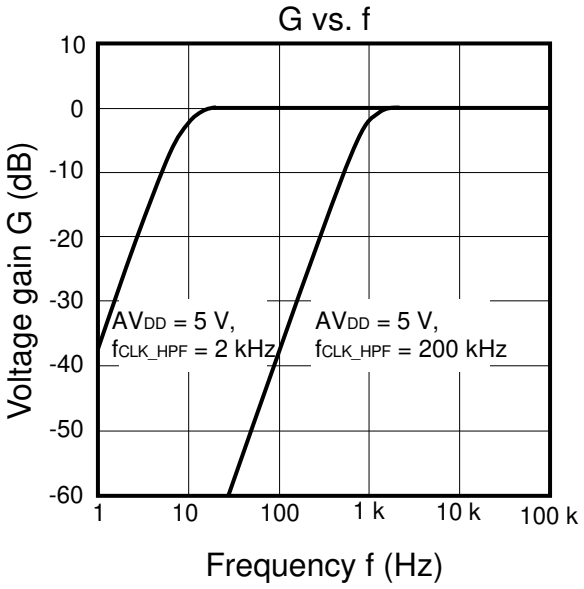

En vs. f (Non-inverting amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1 k
10 k
100 k
1 M
Frequency f (Hz)


En vs. f (Differential amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GCn = 11 H 40 dB,
CC1, CC0 = 0, 0
10
100
1 k
10 k
100 k
1 M
Frequency f (Hz)

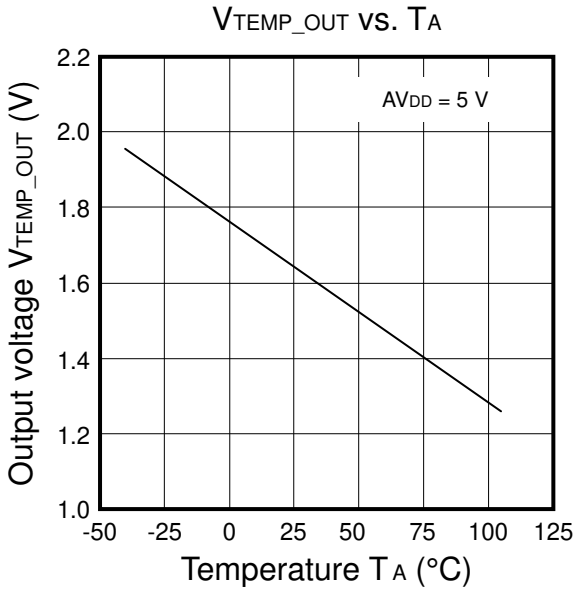

En vs. f (Instrumentation amplifier)
Equivalent input noise En (nV/√ Hz)
1000
300
100
30
10
AVDD = 5 V,
GC3 = 11 H 54 dB,
CC1, CC0 = 0, 0
10
100
1 k
10 k
100 k
1 M
Frequency f (Hz)

• Low-pass filter and high-pass filter



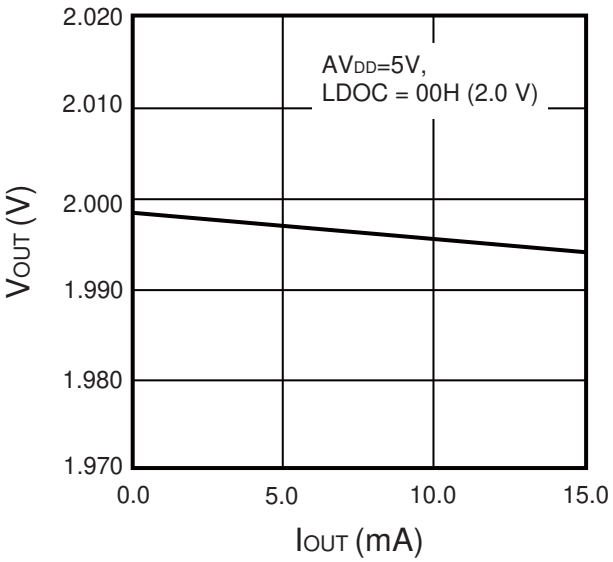


• Temperature sensor

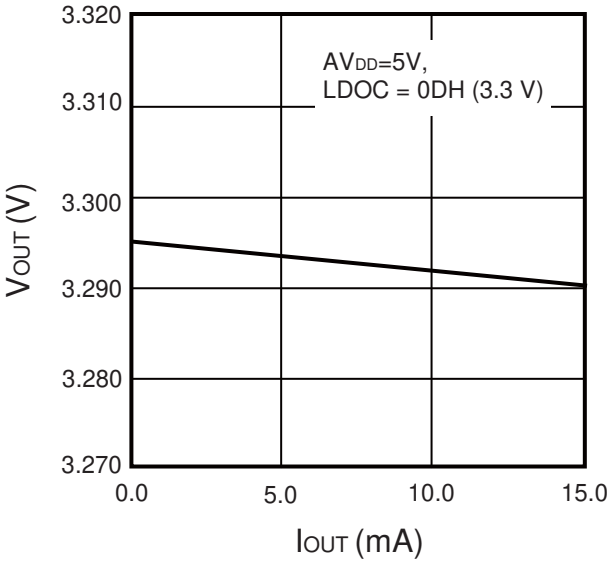


• Variable output voltage regulator

Output voltage vs. Load current



Output voltage vs. Load current



APPENDIX B REVISION HISTORY

B. 1 Major Revisions in This Edition

(1/4)

Page	Description	Classification
R01UH0353EJ0100 → R01UH0353EJ0200		
CHAPTER 1 OUTLINE		
p.1	Modification of **1. 1 Features**	(c)
p.4	Deletion of **Note** form **1. 2 List of Part Numbers**	(c)
p.5-14	Modification of SCK00, SCK10, SCK20, SCK21 in **1. 3 Pin Configuration (Top View)**, in **1. 4 Pin Identification** and **1. 5 Block Diagram**	(a)
p.15-17	Modification of **1. 6 Outline of Functions**	(c)
CHAPTER 2 PIN FUNCTIONS		
p.18-21	Modification of the alternative function and **Remark** in **2. 1 Pin Functions in Microcontroller Block (1) (2)**	(c)
p.23, 24	Modification of the table structure, **Caution** and **Remark** in **2. 1. 1. 1 64-pin products**	(c)
p.25, 26	Modification of the table structure, **Caution** and **Remark** in **2. 1. 1. 2 80-pin products**	(c)
p.28	Modification of the function name and **Remark** in **2. 1. 2. 1 Functions available for each product**	(c)
p.30, 31	Modification of the function name, **Caution** and **Remark** in **2. 1. 2. 2 Description of each function**	(c)
p.32	Modification of the description in **2. 2 Pin Functions in Analog Block**	(c)
p.32	Modification of the table structure in **2. 2. 1 64-pin products**	(c)
p.33	Modification of the table structure in **2. 2. 2 80-pin products**	(c)
p.34, 35	Modification of **Table 2-3. Connections of Unused Pins**	(c)
p.36-46	Modification of **2. 4 Block Diagram of Pins**	(c)
p.50	Modification of **2. 5. 2 Port 1 (P10 to P15)**	(a)
p.54	Modification of **2. 5. 6 Port 7 (P70 to P73)**	(a)
CHAPTER 3 MICROCONTROLLER BLOCK		
p.77	Change of the register name of OSMC to “Subsystem clock supply mode control register” in **Table 3-3.**	(c)
p.83	Change of the register name of OSMC to “Subsystem clock supply mode control register” in **Table 3-4.**	(c)
p.90	Modification of the descriptions in **3. 4. 2. 1 Port 0**	(c)
p.90	Modification of the descriptions in **3. 4. 2. 2 Port 1**	(c)
p.91	Modification of the descriptions in **3. 4. 2. 5 Port 4**	(c)
p.91	Modification of the descriptions in **3. 4. 2. 6 Port 5**	(c)
p.91	Modification of the descriptions in **3. 4. 2. 8 Port 7**	(c)
p.93, 94	Addition of **3. 4. 3 Registers controlling port function**	(c)
p.93, 94	Modification of **Caution** and **Remark** in **3. 4. 3 Registers controlling port function**	(c)
p.95	Modification of **3. 4. 3. 1 Port mode register (PMxx)**	(c)
p.96	Modification of **3. 4. 3. 2 Port register (Pxx)**	(c)
p.97	Modification of **3. 4. 3. 3 Pull-up resistor option register (PUxx)**	(c)

Remark “Classification” in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

(2/4)

Page	Description	Classification
p.97	Modification of **3. 4. 3. 4 Port input mode register (PIMxx)**	(c)
p.98	Modification of **3. 4. 3. 5 Port output mode register (POMxx)**	(c)
p.98	Modification of **3. 4. 3. 6 Port mode control register (PMCxx)**	(c)
p.101	Addition of **Remark** in **3. 4. 3. 8 Peripheral I/O redirection register (PIOR)**	(c)
p.102	Addition of **3. 4. 4. 4 Handling different potential (1.8 V,2.5 V or 3 V) by using EVDD ≤ VDD**	(c)
p.103, 104	Modification of **3. 4. 4. 5 Handling different potential (1.8 V,2.5 V or 3 V) by using I/O buffers**	(c)
p.105	Modification of **3. 4. 5 Register settings when using alternate function**	(c)
p.106, 107	Modification of **3. 5. 1 Functions of clock generator**	(c)
p.108	Modification of **Table 3-6. Configuration of Clock Generator**	(c)
p.109	Modification of **Figure 3-1. Block Diagram of Clock Generator**	(c)
p.111	Modification of **3. 5. 3. 1 Clock operation mode control register (CMC)**	(c)
p.116	Modification of **3. 5. 3. 7 Subsystem clock supply mode control register (OSMC)**	(c)
p.118-121	Modification of **3. 5. 7 Resonator and oscillator constants**	(c)
p.126	Modification of **3. 6. 1. 2 <1> One-shot pulse output**	(c)
p.134	Modification of **3. 6. 3. 1 Peripheral enable register 0 (PER0)**	(c)
p.135-139	Modification of **3. 6. 3. 3 Timer mode register mn (TMRmn)**	(c)
p.144	Modification of **3. 6. 3. 15 Registers controlling port functions of pins to be used for timer I/O**	(c)
p.147	Modification of **3. 8. 2 Configuration of 12-bit interval timer**	(a)
p.148	Modification of **3. 8. 3. 2 Subsystem clock supply mode control register (OSMC)**	(c)
p.153	Modification of **3. 9. 3. 2 Registers controlling port functions of pins used for clock or buzzer output**	(c)
p.155, 156	Modification of **3. 11. 1 Function of A/D converter**	(c)
p.157	Modification of **Figure 3-8. Block Diagram of A/D converter**	(c)
p.160	Modification of **3. 11. 3. 1 Peripheral enable register 0 (PER0)**	(c)
p.161	Modification of **3. 11. 3. 3 A/D converter mode register 1 (ADM1)**	(c)
p.167	Modification of **3. 11. 3. 11 Registers controlling port function of analog input pins**	(c)
p.173	Modification of **Table 3-12. Configuration of Serial Array Unit**	(c)
p.175	Modification of **Figure 3-9. Block Diagram of Serial Array Unit 0**	(a)
p.176	Modification of **Figure 3-10. Block Diagram of Serial Array Unit 1**	(c)
p.177	Modification of **3. 12. 2. 1 Shift register**	(c)
p.177, 178	Modification of **3. 12. 2. 2 Lower 8/9 bits of the serial data register mn (SDRmn)**	(c)
p.179	Modification of **3. 12. 3. 1 Peripheral enable register 0 (PER0)**	(c)
p.180, 181	Modification of **3. 12. 3. 3 Serial mode register mn (SMRmn)**	(c)
p.182-184	Modification of **3. 12. 3. 4 Serial communication operation setting register mn (SCRmn)**	(c)
p.188	Modification of **3. 12. 3. 17 Registers controlling port functions of serial input/output pins**	(c)
p.194-196	Modification of **Table 3-13. Interrupt Source List**	(c)
p.200, 202	Modification of **Table 3-14. Flags Corresponding to Interrupt Request Sources**	(a)

Remark "Classification" in the above table classifies revisions as follows.

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Page	Description	Classification
p.215	Modification of **Table 3-17. Configuration of Key Interrupt**	(c)
p.216	Modification of **Figure 3-14. Block Diagram of Key Interrupt**	(c)
p.217	Modification Addition of **3. 17. 3. 2 Key return mode registers 0 (KRM0)**	(c)
p.223, 224	Modification of **3. 21. 1 Functions of voltage detector**	(c)
p.224	Modification of **Figure 3-15. Block Diagram of Voltage Detector**	(c)
p.226, 227	Modification of **Format of User Option Byte (000C1H/010C1H) (1/2) (2/2)**	(c)
p.229	Modification of **3. 22. 1 Overview of safety functions**	(c)
p.233, 234	Modification of **3. 24. 1. 1 User option byte (000C0H to 000C2H/010C0H to 010C2H)**	(c)
p.235-237	Modification of **3. 24. 2 Format of user option byte**	(c)
p.239	Modification of **3. 25. 1 Serial Programming Using Flash Memory Programmer**	(c)
p.240	Modification of **Table 3-18. Wiring Between RL78/G1E and Dedicated Flash Memory Programmer**	(c)
p.241	Modification of **3. 25. 2 Serial programming using external device (that Incorporates UART)**	(c)
p.241	Modification of **3. 25. 4 Serial programming method**	(c)
p.241	Modification of **3. 25. 5 Processing time for each command when PG-FP5 Is in use (Reference value)**	(c)
p.241	Modification of **3. 25. 6 Self-programming**	(c)
p.241	Modification of **3. 25. 7 Security Settings**	(c)
p.241	Modification of **3. 25. 8 Data flash**	(c)
p.242	Modification of **Figure 3-16. Connection Example of E1 On-chip Debugging Emulator and RL78/G1E**	(c)
CHAPTER 4 ANALOG BLOCK		
p.256	Addition of **Remark** to **4. 1. 3 (5) Gain control register 1 (GC1)**	(c)
p.259	Addition of **Remark** to **4. 1. 3 (6) Gain control register 2 (GC2)**	(c)
p.262	Addition of **Remark** to **4. 1. 3 (7) Gain control register 3 (GC3)**	(c)
p.266	Addition of **Remark** to **4. 1. 3 (8) AMP operation mode control register (AOMC)**	(c)
p.282	Modification of **4. 2. 1 Overview of gain adjustment amplifier features**	(c)
p.284, 285	Modification of **4. 2. 3 Registers controlling the gain adjustment amplifier**	(c)
p.288	Modification of **4. 3. 1 Overview of D/A converter features**	(c)
p.289	Modification of **4. 3. 3 Registers controlling the D/A converters**	(c)
p.289	Modification of **4. 3. 3 (1) DAC reference voltage control register (DACRC)**	(c)
p.293	Modification of **4. 4. 1 Overview of low-pass filter features**	(c)
p.295, 296	Modification of **4. 4. 3 Registers controlling the low-pass filter**	(c)
p.298	Modification of **4. 5. 1 Overview of low-pass filter features**	(c)
p.300	Modification of **4. 5. 3 Registers controlling the high-pass filter**	(c)
p.307	Addition of **Remark** to **4. 7. 3 (1) LDO control register (LDOC)**	(c)
p.308	Addition of **Remark** to **4. 7. 3 (2) Power control register 2 (PC2)**	(c)
p.314	Modification of **Note** in **Table 4-11. SPI Control Registers**	(c)

Remark "Classification" in the above table classifies revisions as follows.
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(d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

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Page	Description	Classification
p.315	Modification of **Caution** in **4. 10. 1 Overview of analog reset feature**	(c)
p.316	Modification of **Note** in **Table 4-13. Statuses of SPI Control Registers after Analog Reset Is Acknowledged**	(c)
p.317	Modification of **Table 4-14. Pin Statuses after Analog Reset**	(c)
p.318	Modification of **4. 10. 2 Registers controlling the analog reset**	(c)
CHAPTER 5 ELECTRICAL SPECIFICATIONS		
p.323	Modification of **5. 1. 3 Absolute maximum ratings (common to microcontroller block and analog block)**	(c)
p.324	Modification of **5. 2. 1. 1 X1 oscillator characteristics**	(c)
p.325	Modification of **5. 2. 1. 2 On-chip oscillator characteristics**	(c)
p.335, 336	Modification of **5. 2. 2. 2 Supply current characteristics**	(c)
p.337	Modification of **5. 2. 3 AC characteristics**	(a)
p.338-340	Modification of two figures about **Minimum Instruction Execution Time during Main System Clock Operation** and **AC Timing Test Points**	(c)
p.342	Addition of **AC Timing Test Points** to **5. 2. 4 Peripheral functions characteristics**	(c)
p.342	Modification of **5. 2. 4. 1 Serial array unit (1)**	(c)
p.344	Modification of **5. 2. 4. 1 Serial array unit (2)**	(c)
p.345	Modification of **5. 2. 4. 1 Serial array unit (3)**	(c)
p.347, 348	Modification of **5. 2. 4. 1 Serial array unit (4)**	(c)
p.350, 351	Modification of **5. 2. 4. 1 Serial array unit (5)**	(c)
p.353, 355	Modification of **5. 2. 4. 1 Serial array unit (6)**	(c)
p.358, 359	Modification of **5. 2. 4. 1 Serial array unit (7)**	(c)
p.360, 362	Modification of **5. 2. 4. 1 Serial array unit (8)**	(c)
p.365, 366	Modification of **5. 2. 4. 1 Serial array unit (9)**	(c)
p.369, 370	Modification of **5. 2. 4. 1 Serial array unit (10)**	(c)
p.372-377	Modification of **5. 2. 5. 1 A/D converter characteristics**	(c)
p.379	Correction of the **Caution** in **5. 2. 5. 4 LVD circuit characteristics**	(a)
p.381	Modification of **5. 2. 6 Data memory STOP mode low supply voltage data retention characteristics**	(c)
p.382	Addition of **5. 2. 8 Dedicated flash memory programmer communication (UART)**	(c)
p.383	Modification of **5. 2. 9 Timing specs for switching flash memory programming modes**	(c)
p.384	Change of the title to **5. 3. 1 "Operating conditions of analog block"**	(c)
p.392, 395, 396	Modification of **5. 3. 3. 1 Configurable amplifier characteristics**	(c)
p.399	Modification of **5. 3. 3. 3 D/A converter characteristics**	(c)
p.400	Modification of **5. 3. 3. 4 Low-pass filter characteristics**	(c)
p.401	Modification of **5. 3. 3. 5 High-pass filter characteristics**	(c)
p.403	Modification of **5. 3. 3. 9 SPI characteristics**	(c)

Remark "Classification" in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents

B. 2 Revision History of Preceding Editions

Here is the revision history of the preceding editions. Chapter indicates the chapter of each edition.

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Edition	Description	Chapter
Rev.1.00	The structure of **CHAPTERS** and **Sessions** are drastically changed.	Whole pages
	Modification of **1. 1 Features**	**CHAPTER 1 OUTLINE**
	Addition of Packaging, modification of Part Numbers and addition of **Cautions** in **1. 2 List of Part Numbers**	
	Modification of **Note 7.** for 64-pin products in **1. 3 Pin Configuration**	
	Modification of **Note 6.** for 80-pin products in **1. 3 Pin Configuration**	
	Addition of Items and **Notes** in **1. 6 Outline of Functions**	
	Error correction of the descriptions in **1. 6 Outline of Functions**	
	Modification of the tables for **Comparison of port functions with RL78/G1A** in **2. 1 Pin Functions in Microcontroller Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the descriptions in **2. 1. 1 Port functions**	
	Addition of the descriptions in **2. 1. 2 Functions other than port Functions**	
	Error correction of the descriptions in **2. 2 Pin Functions in Analog Block**	
	Addition of **Notes** about the pin of $\overline{\text{ARESET}}$ in **2. 3 Recommended Connection of Unused Pins**	
	Addition of the descriptions for the pin of $\overline{\text{RESET}}$ and the pin of $\overline{\text{ARESET}}$ in **2. 5 Instruction of Pin Functions**	
	Addition of the items listed on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	**CHAPTER 3 MICROCONTROLLER BLOCK**
	Error correction of the descriptions on the tables in **3. 2 Comparison of Each Function with RL78/G1A (64-pin products)**	
	Modification of the tables for **List of Differences in Special Function Registers (SFRs)** in **3. 3. 2. 4 Special function registers (SFRs)**	
	Modification of the tables for **List of Differences in Expanded Special Function Registers (2nd SFRs)** in **3. 3. 2. 5 Expanded special function registers (2nd SFRs)**	
	Addition of the descriptions for each port in **3. 4. 2 Port configuration**	
	Error correction of the descriptions for each port in **3. 4. 2 Port configuration**	
	Addition of registers listed in **3. 4. 3 Registers controlling port functions**	
	Modification of the frequency for oscillation about the function of high-speed on-chip oscillator and addition of the table about the frequency for oscillation in **3. 5. 1 Functions of clock generator**	
	Addition of the registers listed in **3. 5. 3 Registers controlling clock generator**	
	Error correction of the descriptions about a crystal resonator in **3. 5. 7 Resonator and oscillator constants**	
	Addition of “Port mode control register” to **Table 3-8.**	
	Modification of the figures for Block Diagram on **Figure 3-4.** and **Figure 3-5.** in **3. 6. 2 Configuration of timer array unit**	
	Addition of the registers listed in **3. 6. 3 Registers controlling timer array unit**	
	Addition of the registers listed in **3. 8. 3 Registers controlling 12-bit interval timer**	

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Edition	Description	Chapter
Rev.1.00	Addition of the registers listed in **3. 9. 3 Registers controlling clock output/buzzer output controller**	**CHAPTER 3 MICROCONTROLLER BLOCK**
	Addition of the registers listed in **3. 11. 3 Registers used in A/D converters**	
	Addition and Modification of **Cautions** in **3. 11. 3. 7 Analog input channel specification register (ADS)**	
	Addition of the registers listed in **3. 12. 3 Registers controlling serial array unit**	
	Error correction of the number of maskable interrupts (internal) in **3. 16 Interrupt Functions**	
	Addition of the registers listed in **3. 16. 3 Registers controlling interrupt functions**	
	Error correction of the number of key interrupt input channels for 64-pin products in **3. 17 Key Interrupt Function**	
	Addition of the registers listed in **3. 17. 3 Registers controlling key interrupt**	
	Addition of **Caution** in **3. 17. 3. 2 Key return mode registers 0 (KRM0)**	
	Error correction of the descriptions in **3. 21. Voltage Detector**	
	Addition of the registers listed in **3. 21. 3 Registers controlling voltage detector**	
	Error correction of the descriptions about user option byte (000C1H/010C1H) in **3. 21. 3 Registers controlling voltage detector**	
	Addition of the registers listed in **3. 22. 3 Operation of safety functions**	
	Error correction of the descriptions about user option byte (000C1H/010C1H) in **3. 24. 2 Format of user option byte**	
	Addition of **3. 25 Flash Memory**	
	Addition of **3. 26. 1 Connecting E1 on-chip debugging emulator to RL78/G1E**	
	Addition of the descriptions about the reference voltage in **4. 1. 1 Overview of configurable amplifier features**	**CHAPTER 4 ANALOG BLOCK**
	Modification of the registers listed in **4. 1. 3 Registers controlling the configurable amplifiers**	
	Addition of the descriptions about the reference voltage in **4. 2. 1 Overview of gain adjustment amplifier features**	
	Modification of the registers listed in **4. 2. 3 Registers controlling the gain adjustment amplifier**	
	Modification of the equation for calculation of analog output voltage in **4. 3. 1 Overview of D/A converter features**	
	Addition of the descriptions about the reference voltage in **4. 4. 1 Overview of low-pass filter features**	
	Modification of the registers listed in **4. 4. 3 Registers controlling the low-pass filter**	
	Addition of the descriptions about the reference voltage in **4. 5. 1 Overview of high-pass filter features**	
	Modification of the registers listed in **4. 5. 3 Registers controlling the high-pass filter**	
	Modification of the description in **4. 8. 3 Registers controlling the reference voltage generator**	
	Modification of **Caution** in **4. 9. 1 Overview of SPI features**	
	Addition of **Note** to **Table 4-11.**	

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Edition	Description	Chapter
Rev.1.00	Addition and Modification of the descriptions in **4. 10. 1 Overview of analog reset feature**	**CHAPTER 4 ANALOG BLOCK**
	Modification of the description and **Note** on **Table 4-13.**	
	Modification of the description and **Note**, and addition of **Caution** in **4. 10. 2 (1) Reset control register (RC)**	
	Erase the description of "(target)"	**CHAPTER 5 ELECTRICAL SPECIFICATIONS**
	Modification of the description and addition of **Remark 3** in **5. 1. 1 Absolute Maximum Ratings**	
	Addition of "**5. 1. 3 Absolute maximum ratings (common to microcontroller block and analog block)**"	
	Modification of the description and **Note** in **5. 2. 1. 1 X1 oscillator characteristics**	
	Modification of **Note 3** in **5. 2. 2. 1 Pin characteristics**	
	Addition of the specifications for P70 to P73 in terms of output current/voltage high and output current/voltage low in **5. 2. 2. 1 Pin characteristics**	
	Modification of the description and **Notes** in **5. 2. 2. 2 Supply current characteristics**	
	Change of the specification of the typical value for I_{DD3} (T_A=+50°C) in **5. 2. 2. 2 Supply current characteristics**	
	Addition of operation current flowing to low-speed on-chip oscillator (f_{IL}) in **5. 2. 2. 2 Supply current characteristics**	
	Addition of the descriptions and modification of **Remark** in **5. 2. 3 AC characteristics**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (1)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (2)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (3)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (4)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (5)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (6)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (7)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (8)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (9)**	
	Modification of the description in **5. 2. 4. 1 Serial array unit (10)**	
	Addition of "Internal reference voltage" and "Temperature sensor output voltage" to the input channel in **5. 2. 5. 1 A/D converter characteristics**	
	Change of the symbol for the internal reference voltage in **5. 2. 5. 2 Temperature sensor, internal reference voltage output characteristics**	
	Addition of **Note** in **5. 2. 5. 3 POR circuit characteristics**	
	Error correction of the description in **5. 2. 5. 4 LVD circuit characteristics**	
	Change of the specification for the slope in **5. 2. 5. 5 Supply voltage rise slope characteristics**	
	Change of the specification for the data retention supply voltage in **5. 2. 6 Data memory STOP mode low supply voltage data retention characteristics**	
	Addition of **Notes** in **5. 2. 7 Flash memory programming characteristics**	

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Edition	Description	Chapter
Rev.1.00	Modification of the description in **5. 2. 8 Timing specs for switching flash memory programming modes**	**CHAPTER 5 ELECTRICAL SPECIFICATIONS**
	Addition of the specification depending on the products in **5. 3. 3. 2 Gain adjustment amplifier characteristics**	
	Addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 2 Gain adjustment amplifier characteristics (2) 80-pin products**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 4 Low-pass filter characteristics**	
	Error correction of the description and addition of the specification for “CLK_SYNCH input voltage” in **5. 3. 3. 5 High-pass filter characteristics**	
Rev.0.04	Change of the name for CS from “Slave Select” to “Chip Select”	Whole pages
	Deletion of the word “interface” from the name of SPI	
	Error correction of the figures in **1. 4 Pin Configuration (Top View)**	**CHAPTER 1 OUTLINE**
	Error correction of the description (deletion of “SCLA0”, “SCLA1”) in **1. 4. 3 Pin identification (Microcontroller Block)**	
	Error correction of the figures in **1. 5 Block Diagram**	
	Error correction of the function names and modification of the description for the function in **2. 2 Pin Functions in Analog Block**	**CHAPTER 2 PIN FUNCTIONS**
	Error correction of the description for the pin of ANI30 (D/A converter -> A/D converter) in **2. 3. 4 P40 to P42 (port 4)**	
	Modification of the description in **2. 3. 43 I.C**	
	Addition of “Remarks” on the tables in **3. 1 Differences in Functions between RL78/G1E and RL78/G1A**	**CHAPTER 3 MICROCONTROLLER FUNCTION**
	Modification of the description on the tables (deletion of the same registers as RL78/G1A) in **3. 2 Differences in (Expanded) Special-Function Registers between RL78/G1E and RL78/G1A**	
	Modification of the description and change of the sequence flow of the setting procedure (2) in **3. 3. 3 Connecting to an external device with different potential (1.8 V, 2.5 V, 3 V)**	
	Addition of **3. 4. 4 Resonator and Oscillator Constants**	
	Error correction of the description on **Table 3-14.**	
	Addition of **3. 13 Safety Functions**	
	Modification of the gain setting of non-inverting amplifier in **5. 1 Overview of Configurable Amplifier Features** and in **5. 3 Registers Controlling the Configurable Amplifiers**	**CHAPTER 5 CONFIGURABLE AMPLIFIERS**
	Modification of the description in **8. 1 Overview of Low-Pass Filter Features**	**CHAPTER 8 LOW-PASS FILTER**
	Modification of the description in **9. 1 Overview of High-Pass Filter Features**	**CHAPTER 8 HIGH-PASS FILTER**
	Addition of **Note** in **11. 3 Registers Controlling the Variable Output Voltage Regulator**	**CHAPTER 11 VARIABLE OUTPUT VOLTAGE REGULATOR**

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Edition	Description	Chapter
Rev.0.04	Change of the specification for the typical value of I_{m124} in **15. 3. 2 Supply current characteristics**	**CHAPTER 15 ELECTRICAL SPECIFICATIONS (TARGET)**
	Addition of the table which describes the operation state of the circuit in **15. 3. 2 Supply current characteristics**	
	Error correction of the description and change of the specification in **15. 3. 3 Electrical specifications of each block**	
	Modification of the description for the current consumption and addition of the **Notes** in **15. 3. 3 Electrical specifications of each block (3) D/A converter**	
	Addition of the definition for “CLK_LPF” in **15. 3. 3 Electrical specifications of each block (4) Low-pass filter**	
	Addition of the definition for “CLK_HPF” in **15. 3. 3 Electrical specifications of each block (5) High-pass filter**	
	Error correction of the description and addition of **Note** for the dropout voltage in **15. 3. 3 Electrical specifications of each block (7) Variable output voltage regulator**	
	Error correction of the description in **15. 3. 3 Electrical specifications of each block (9) SPI**	
Rev.0.03	Change of Block Diagram in **1. 5. 2 RL78/G1E (80-pin)**	**CHAPTER 1 OUTLINE**
	Change of Table 3-12. Analog Input Channels of A/D Converter	**CHAPTER 15 ELECTRICAL SPECIFICATIONS (TARGET)**
	Change of ratings in **15. 1 Absolute Maximum Ratings**	
	Change of **15. 2. 1 (1) X1 oscillator characteristics**	
	Change of conditions and ratings in **15. 2. 2 (2) Supply current characteristics**	
	Addition of SNOOZE operating current to **15. 2. 2 (3) Supply current characteristics of peripheral functions**	
	Addition of diagrams (AC Timing Test Points to RESET Input Timing) to **15. 2. 3 AC characteristics**	
	Detection of Remarks 4 in Simplified I2C connection diagram (during communication between devices with the different voltages)	
	Addition of Division of A/D Converter Characteristics in **15. 2. 5. 1 A/D converter characteristics**	
	Change of ratings in **15. 2. 5. 2 Temperature sensor characteristics**	
	Change of ratings in **15. 2. 5. 3 POR circuit characteristics**	
	Change of conditions and ratings in **15. 3. 2 Supply current characteristics**	
	Change of conditions in **15. 3. 3 (4) Variable output voltage regulator**	
	Change of conditions in **15. 3. 3 (9) SPI interface**	
Rev.0.02	Change of conditions and ratings in **15. 2. 2 (2) Supply current characteristics**	**CHAPTER 15 ELECTRICAL SPECIFICATIONS (TARGET)**
	Change of ratings in **15. 2. 4. 1 (7) Communication between devices with different voltages**	
	Change of ratings in **15. 2. 5. (1) A/D converter characteristics**	

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Edition	Description	Chapter
Rev.0.02	Addition of new conditions (Retained for 20 years) to **15. 2. 10 Flash memory programming characteristics**	**CHAPTER 15 ELECTRICAL SPECIFICATIONS (TARGET)**
	Change of condition and ratings in **15. 3. 2 Supply Current characteristics**	
	Change of conditions and ratings and addition of settling time in **15. 3. 3 (1) Configurable amplifier block characteristics**	
	Change of conditions and ratings in **15. 3. 3 (2) Gain Adjustment amplifier**	
	Change of conditions and ratings in **15. 3. 3 (3) D/A converter**	
	Change of conditions and ratings in **15. 3. 3 (4) Low-pass filter**	
	Change of conditions and ratings in **15. 3. 3 (5) Temperature sensor**	
	Change of conditions and ratings in **15. 3. 3 (7) Variable output voltage regulator**	
	Change of conditions and ratings in **15. 3. 3 (9) SPI interface**	

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