# X28C512, X28C513

5V, Byte Alterable EEPROM

FN8106
Rev 2.00
June 7, 2006

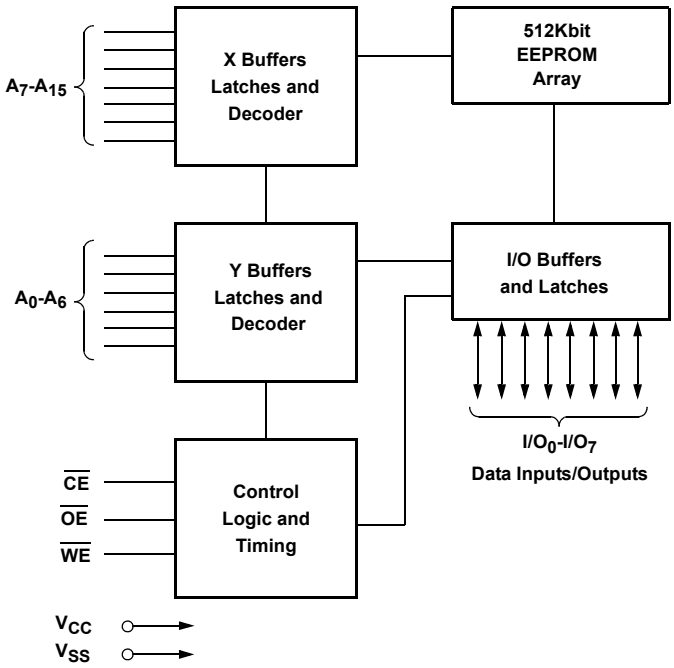
The X28C512, X28C513 are 64K x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable nonvolatile memories, the X28C512, X28C513 are 5V only devices. The X28C512, X28C513 feature the JEDEC approved pin out for byte wide memories, compatible with industry standard EPROMS.

The X28C512, X28C513 support a 128-byte page write operation, effectively providing a 39µs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C512, X28C513 also feature $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C512, X28C513 support the software data protection option.

## Features

- Access Time: 90ns
- Simple Byte and Page Write
  - Single 5V supply
    - No external high voltages or $V_{PP}$ control circuits
  - Self-timed
    - No erase before write
    - No complex programming algorithms
    - No overerase problem
- Low Power CMOS
  - Active: 50mA
  - Standby: 500µA
- Software Data Protection
  - Protects data against system level inadvertent writes
- High Speed Page Write Capability
- Highly Reliable Direct Write™ Cell
  - Endurance: 100,000 write cycles
  - Data retention: 100 years
  - Early end of write detection
  - $\overline{\text{DATA}}$ polling
  - Toggle bit polling
- Two PLCC and LCC Pinouts
  - X28C512
    - X28C010 EPROM pin compatible
  - X28C513
    - Compatible with lower density EEPROMs
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Block Diagram




## Ordering Information

| PART NUMBER | PART MARKING | ACCESS TIME (ns) | TEMP RANGE (°C) | PACKAGE |
|---|---|---|---|---|
| X28C512D | X28C512D | - | 0 to +70 | 32 Ld CERDIP |
| X28C512DM | X28C512DM | | -55 to +125 | 32 Ld CERDIP |
| X28C512J | X28C512J | | 0 to +70 | 32 Ld PLCC |
| X28C513EM | X28C513EM | | -55 to +125 | 32 Ld LCC |
| X28C512D-12 | X28C512D-12 | 120 | 0 to +70 | 32 Ld CERDIP |
| X28C512DI-12 | X28C512DI-12 | | -40 to +85 | 32 Ld CERDIP |
| X28C512DMB-12 | X28C512DMB-12 | | Mil-STD-883 | 32 Ld CERDIP |
| X28C512FMB-12 | X28C512FMB-12 | | Mil-STD-883 | 32 Ld Flat Pack |
| X28C512J-12* | X28C512J-12 | | 0 to +70 | 32 Ld PLCC |
| X28C512JZ-12* (See Note) | X28C512J-12 Z | | 0 to +70 | 32 Ld PLCC (Pb-free) |
| X28C512JI-12 | X28C512JI-12 | | -40 to +85 | 32 Ld PLCC |
| X28C512JIZ-12* (See Note) | X28C512JI-12 Z | | -40 to +85 | 32 Ld PLCC (Pb-free) |
| X28C512JM-12 | X28C512JM-12 | | -55 to +125 | 32 Ld PLCC |
| X28C512KM-12 | X28C512KM-12 | | -55 to +125 | 36 Ld CPGA |
| X28C512PI-12 | X28C512PI-12 | | -40 to +85 | 32 Ld PDIP |
| X28C512RMB-12 | X28C512RMB-12 | | Mil-STD-883 | 32 Ld Flat Pack |
| X28C513EM-12 | X28C513EM-12 | | -55 to +125 | 32 Ld LCC |
| X28C513EMB-12 | X28C513EMB-12 | | Mil-STD-883 | 32 Ld LCC |
| X28C513J-12* | X28C513J-12 | | 0 to +70 | 32 Ld PLCC |
| X28C513JZ-12* (Note) | X28C513J-12 Z | | 0 to +70 | 32 Ld PLCC (Pb-free) |
| X28C513JI-12* | X28C513JI-12 | | -40 to +85 | 32 Ld PLCC |
| X28C513JIZ-12* (Note) | X28C513JI-12 Z | | -40 to +85 | 32 Ld PLCC (Pb-free) |
| X28C513JM-12 | X28C513JM-12 | | -55 to +125 | 32 Ld PLCC |

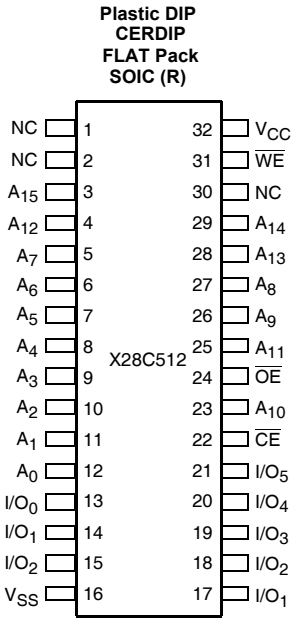
## *Ordering Information* (Continued)

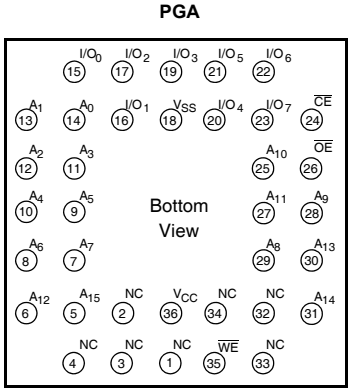
| PART NUMBER | PART MARKING | ACCESS TIME (ns) | TEMP RANGE (°C) | PACKAGE |
|---|---|---|---|---|
| X28C512D-15 | X28C512D-15 | 150 | 0 to +70 | 32 Ld CERDIP |
| X28C512DI-15 | X28C512DI-15 | | -40 to +85 | 32 Ld CERDIP |
| X28C512DMB-15 | X28C512DMB-15 | | Mil-STD-883 | 32 Ld CERDIP |
| X28C512J-15* | X28C512J-15 | | 0 to +70 | 32 Ld PLCC |
| X28C512JZ-15* (See Note) | X28C512J-15 Z | | 0 to +70 | 32 Ld PLCC (Pb-free) |
| X28C512JI-15* | X28C512JI-15 | | -40 to +85 | 32 Ld PLCC |
| X28C512JIZ-15* (See Note) | X28C512JI-15 Z | | -40 to +85 | 32 Ld PLCC (Pb-free) |
| X28C512JM-15 | X28C512JM-15 | | -55 to +125 | 32 Ld PLCC |
| X28C513EM-15 | X28C513EM-15 | | -55 to +125 | 32 Ld LCC |
| X28C513EMB-15 | X28C513EMB-15 | | Mil-STD-883 | 32 Ld LCC |
| X28C513J-15* | X28C513J-15 | | 0 to +70 | 32 Ld PLCC |
| X28C513JZ-15* (Note) | X28C513J-15 Z | | 0 to +70 | 32 Ld PLCC (Pb-free) |
| X28C513JI-15 | X28C513JI-15 | | -40 to +85 | 32 Ld PLCC |
| X28C513JIZ-15* (Note) | X28C513JI-15 Z | | -40 to +85 | 32 Ld PLCC (Pb-free) |
| X28C513JM-15 | X28C513JM-15 | | -55 to +125 | 32 Ld PLCC |
| X28C512DMB-20 | X28C512DMB-20 | 200 | Mil-STD-883 | 32 Ld CERDIP |
| X28C512JM-20 | X28C512JM-20 | | -55 to +125 | 32 Ld PLCC |
| X28C512KI-20 | X28C512KI-20 | | -40 to +85 | 36 Ld CPGA |
| X28C512KM-20 | X28C512KM-20 | | -55 to +125 | 36 Ld CPGA |
| X28C513EI-20 | X28C513EI-20 | | -40 to +85 | 32 Ld LCC |
| X28C513EM-20 | X28C513EM-20 | | -55 to +125 | 32 Ld LCC |
| X28C513EMB-20 | X28C513EMB-20 | | Mil-STD-883 | 32 Ld LCC |
| X28C513J-20T1 | X28C513J-20 | | 0 to +70 | 32 Ld PLCC Tape and Reel |
| X28C512EM-25 | X28C512EM-25 | 250 | -55 to +125 | 32 Ld LCC |
| X28C512JM-25 | X28C512JM-25 | | -55 to +125 | 32 Ld PLCC |
| X28C512KM-25 | X28C512KM-25 | | -55 to +125 | 36 Ld CPGA |
| X28C512KMB-25 | X28C512KMB-25 | | Mil-STD-883 | 36 Ld CPGA |
| X28C513EM-25 | X28C513EM-25 | | -55 to +125 | 32 Ld LCC |
| X28C513EMB-25 | X28C513EMB-25 | | Mil-STD-883 | 32 Ld LCC |

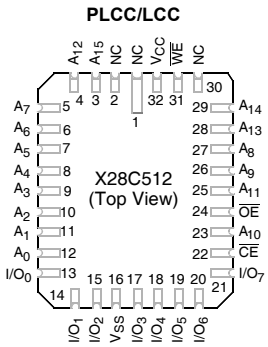
*Add "T1" suffix for tape and reel.

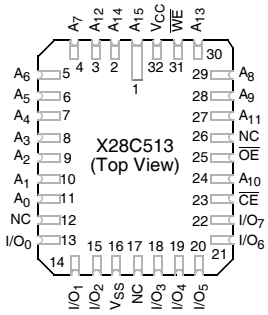
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Pinouts




## Pin Descriptions

### Addresses ($A_0$-$A_{15}$)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

### Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

### Data In/Data Out ($I/O_0$-$I/O_7$)

Data is written to or read from the X28C512, X28C513 through the I/O pins.

### Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C512, X28C513.

## Pin Names

| SYMBOL | DESCRIPTION |
|---|---|
| $A_0$-$A_{15}$ | Address Inputs |
| $I/O_0$-$I/O_7$ | Data Input/Output |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | +5V |
| $V_{SS}$ | Ground |
| NC | No Connect |

## Device Operation

### Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

### Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28C512, X28C513 support both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

### Page Write Operation

The page write feature of the X28C512, X28C513 allows the entire memory to be written in 2.5 seconds. Page write allows two to one hundred twenty-eight bytes of data to be consecutively written to the X28C512, X28C513, prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address ($A_7$ through $A_{15}$) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to one hundred twenty-seven bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively, the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

### Write Operation Status Bits

The X28C512, X28C513 provide the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

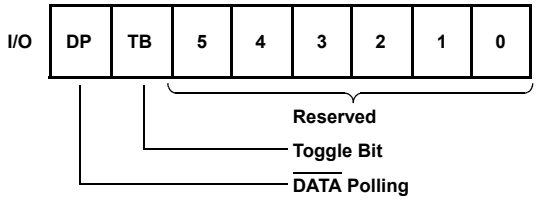



**FIGURE 1. STATUS BIT ASSIGNMENT**

### $\overline{DATA}$ Polling ($I/O_7$)

The X28C512, X28C513 feature $\overline{DATA}$ polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C512, X28C513, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on $I/O_7$ (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, $I/O_7$ will reflect true data.

### Toggle Bit ($I/O_6$)

The X28C512, X28C513 also provide another method for determining when the internal write cycle is complete. During the internal programming cycle, $I/O_6$ will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease, and the device will be accessible for additional read or write operations.

## $\overline{DATA}$ Polling $I/O_7$

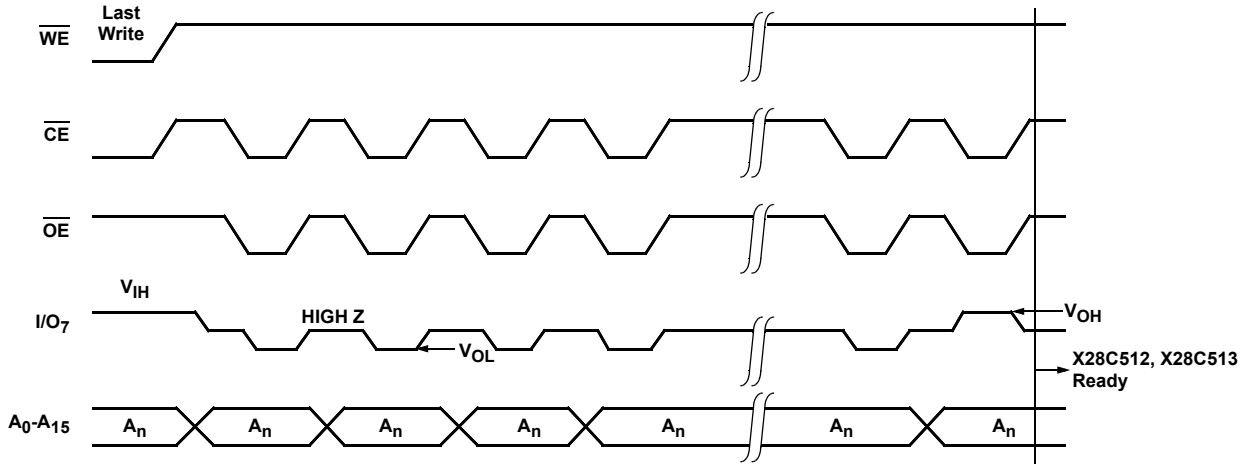



FIGURE 2A. $\overline{DATA}$ POLLING BUS SEQUENCE

$\overline{DATA}$ Polling can effectively halve the time for writing to the X28C512, X28C513. The timing diagram in Figure 2A illustrates the sequence of events on the bus. The software flow diagram in Figure 2B illustrates one method of implementing the routine.

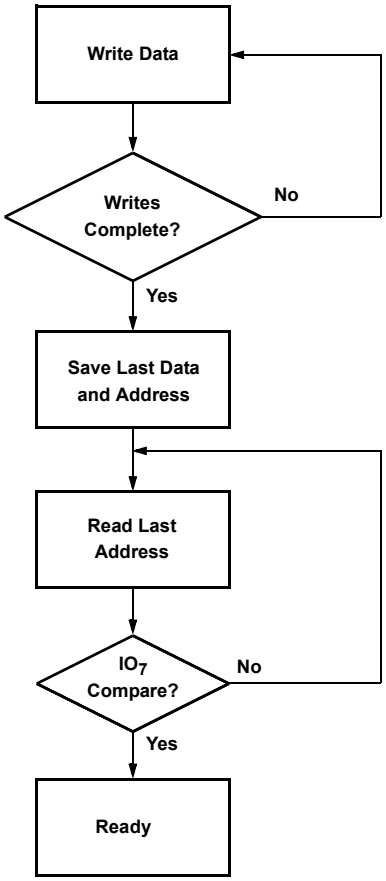
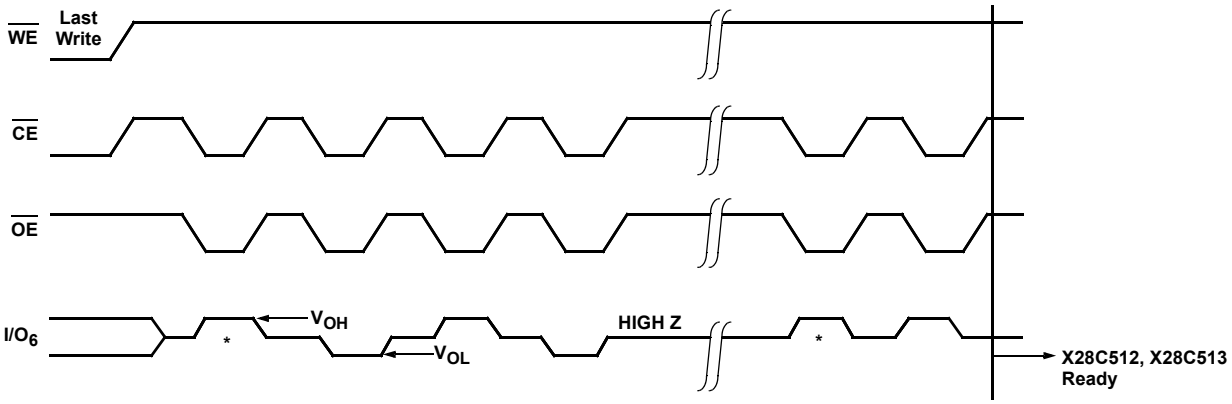



FIGURE 2B. $\overline{DATA}$ POLLING SOFTWARE FLOW

## The Toggle Bit I/$O_6$




* Beginning and ending state of I/$O_6$ will vary.

FIGURE 3A. TOGGLE BIT BUS SEQUENCE

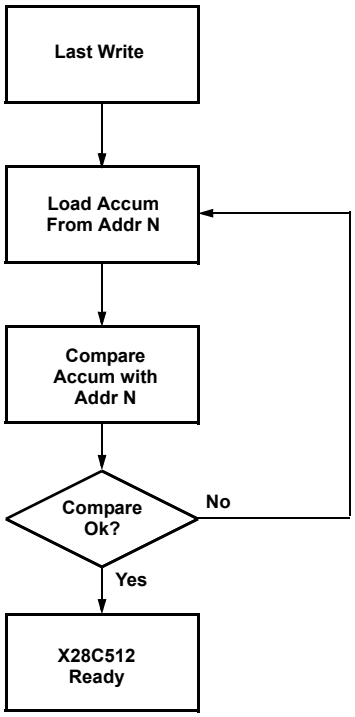



FIGURE 3B. TOGGLE BIT SOFTWARE FLOW

The Toggle Bit can eliminate the chore of saving and fetching the last address and data in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28C512, X28C513 memories that are frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3A illustrates the sequence of events on the bus. The software flow diagram in Figure 3B illustrates a method for polling the Toggle Bit.

## Hardware Data Protection

The X28C512, X28C513 provide three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse typically less than 10ns will not initiate a write cycle.
- Default $V_{CC}$ Sense—All write functions are inhibited when $V_{CC}$ is 3.6V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity. Write cycle timing specifications must be observed concurrently.

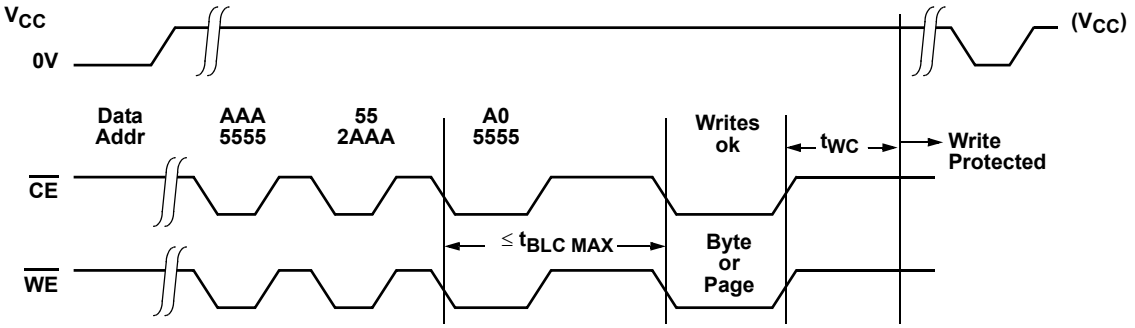
## Software Data Protection

The X28C512, X28C513 offer a software controlled data protection feature. The X28C512, X28C513 are shipped from Intersil with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once $V_{CC}$ was stable.

The X28C512, X28C513 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C512, X28C513 are also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device. Note: The data in the three-byte enable sequence is not written to the memory array.

### *Software Data Protection*




**Note: All other timings and control pins are per page write timing requirements**

**FIGURE 4A. TIMING SEQUENCE—SOFTWARE DATA PROTECT ENABLE SEQUENCE FOLLOWED BY BYTE OR PAGE WRITE**

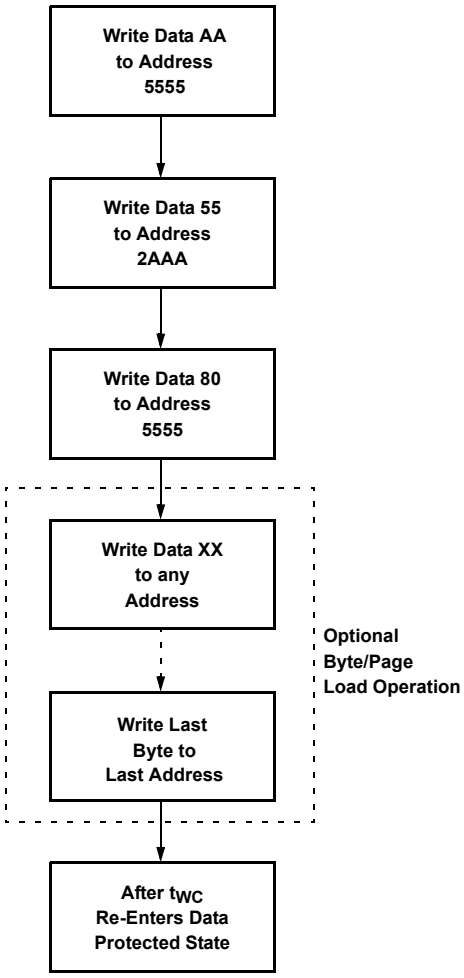



**FIGURE 4B. WRITE SEQUENCE FOR SOFTWARE DATA PROTECTION**

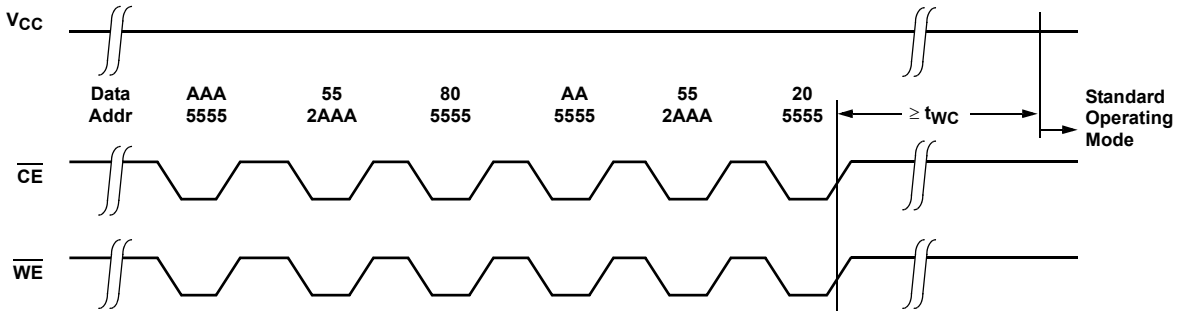
## *Software Algorithm*

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figures 4A and 4B for the sequence. The three byte sequence opens the page write window, enabling the host to write from one to one hundred twenty-eight bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C512, X28C513 will automatically disable further writes, unless another command is issued to cancel it. If no further commands are issued the X28C512, X28C513 will be write-protected during power-down and after any subsequent power-up. The state of $A_{15}$ while executing the algorithm is “don’t care”.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

### *Resetting Software Data Protection*




**Note: All other timings and control pins are per page write timing requirements**

**FIGURE 5A. Reset Software Data Protection Timing Sequence**

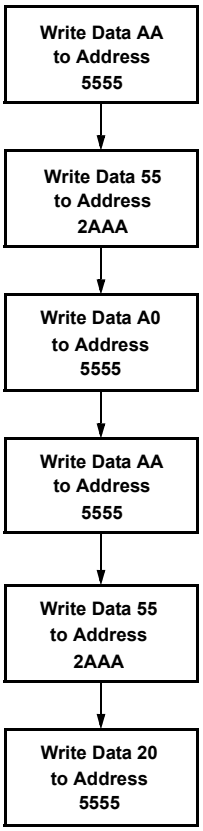



**FIGURE 5B. SOFTWARE SEQUENCE TO DEACTIVATE SOFTWARE DATA PROTECTION**

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After $t_{WC}$, the X28C512, X28C513 will be in standard operating mode.

**Note:** Once initiated, the sequence of write operations should not be interrupted.

## *System Considerations*

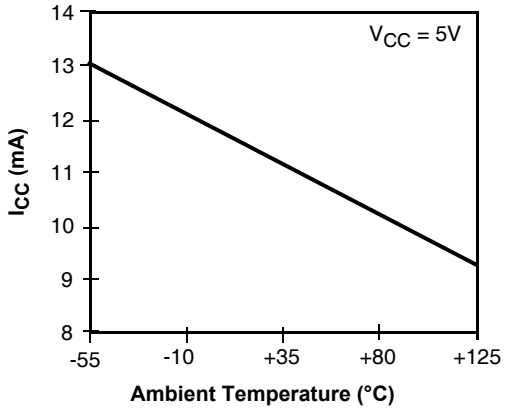
Because the X28C512, X28C513 are frequently used in large memory arrays, it is provided with a two-line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is/are outputting data on the bus.

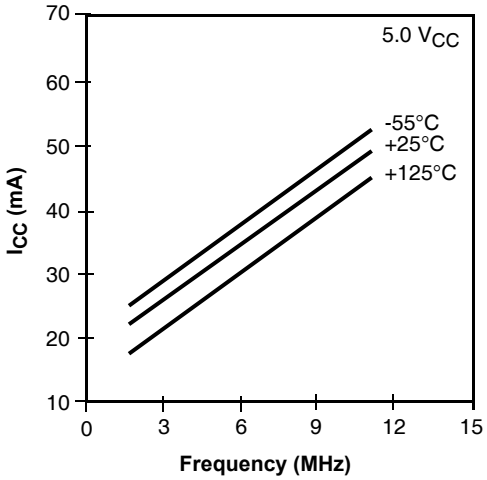
Because the X28C512, X28C513 have two power modes, (standby and active), proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between $V_{CC}$ and $V_{SS}$ at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between $V_{CC}$ and $V_{SS}$ for each 8 devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

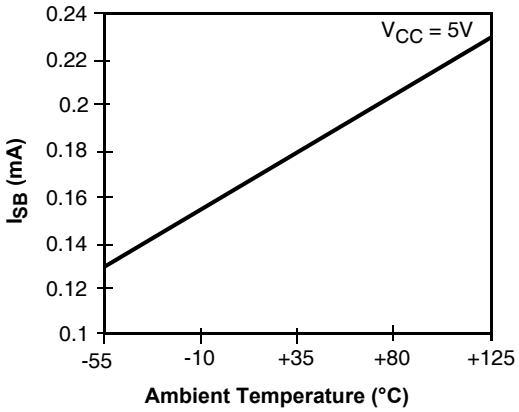
***Active Supply Current vs Ambient Temperature***




***$I_{CC}$ (RD) by Temperature Over Frequency***




***Standby Supply Current vs Ambient Temperature***



## Absolute Maximum Ratings

Temperature under bias
- X28C512, X28C513 . . . . . -10°C to +85°C
- X28C512I/513I . . . . . -65°C to +135°C
- X28C512M/513M . . . . . -65°C to +135°C

Storage temperature . . . . . -65°C to +150°C
Voltage on any pin with respect to $V_{SS}$ . . . . . -1V to +7V
D.C. output current. . . . . 5mA
Lead temperature (soldering, 10s). . . . . 300°C

## Recommended Operating Conditions

Temperature Range
- Commercial . . . . . 0°C to +70°C
- Industrial. . . . . -40°C to +85°C
- Military . . . . . -55°C to +125°C

Supply Voltage Limits . . . . . 5V ±10%

*CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC Electrical Specifications

Over recommended operating conditions, unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ current (active) (TTL inputs) | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{WE}$ = $V_{IH}$, All I/O's = open, address inputs = 0.4V/2.4V Levels @ f = 5MHz | | 50 | mA |
| $I_{SB1}$ | $V_{CC}$ current (standby) (TTL inputs) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = VIL, All I/O's = open, other inputs = $V_{IH}$ | | 3 | mA |
| $I_{SB2}$ | $V_{CC}$ current (standby) (CMOS inputs) | $\overline{CE}$ = $V_{CC}$ - 0.3V, $\overline{OE}$ = VIL, All I/O's = Open, Other Inputs = $V_{IH}$ | | 500 | µA |
| $I_{LI}$ | Input leakage current | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ | | 10 | µA |
| $I_{LO}$ | Output leakage current | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$, $\overline{CE}$ = $V_{IH}$ | | 10 | µA |
| $V_{IL}$ (Note 1) | Input LOW voltage | | -1 | 0.8 | V |
| $V_{IH}$ (Note 1) | Input HIGH voltage | | 2 | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output LOW voltage | $I_{OL}$ = 2.1mA | | 0.4 | V |
| $V_{OH}$ | Output HIGH voltage | $I_{OH}$ = -400µA | 2.4 | | V |

NOTE:

1. $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not tested.

## Power-Up Timing

| SYMBOL | PARAMETER | MAX | UNIT |
|---|---|---|---|
| $t_{PUR}$ (Note 2) | Power-up to read operation | 100 | µs |
| $t_{PUW}$ (Note 2) | Power-up to write operation | 5 | ms |

## Capacitance

$T_A$ = +25°C, f = 1MHz, $V_{CC}$ = 5V

| SYMBOL | PARAMETER | TEST CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_{I/O}$ (Note 2) | Input/output capacitance | $V_{I/O}$ = 0V | 10 | pF |
| $C_{IN}$ (Note 2) | Input capacitance | $V_{IN}$ = 0V | 10 | pF |

## Endurance and Data Retention

| PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|
| Endurance | 10,000 | | Cycles per byte |
| Endurance | 100,000 | | Cycles per page |
| Data retention | 100 | | Years |

NOTE:

2. This parameter is periodically sampled and not 100% tested.

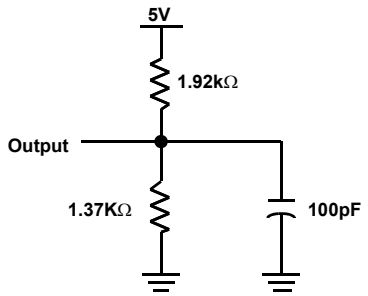
### A.C. Conditions of Test

| | |
|---|---|
| Input pulse levels | 0V to 3V |
| Input rise and fall times | 10ns |
| Input and output timing levels | 1.5V |

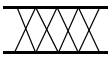
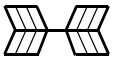
### Mode Selection

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | MODE | I/O | POWER |
|---|---|---|---|---|---|
| L | L | H | Read | $D_{OUT}$ | Active |
| L | H | L | Write | $D_{IN}$ | Active |
| H | X | X | Standby and write inhibit | High Z | Standby |
| X | L | X | Write inhibit | — | — |
| X | X | H | Write inhibit | — | — |

## *Equivalent A.C. Load Circuit*




## *Symbol Table*

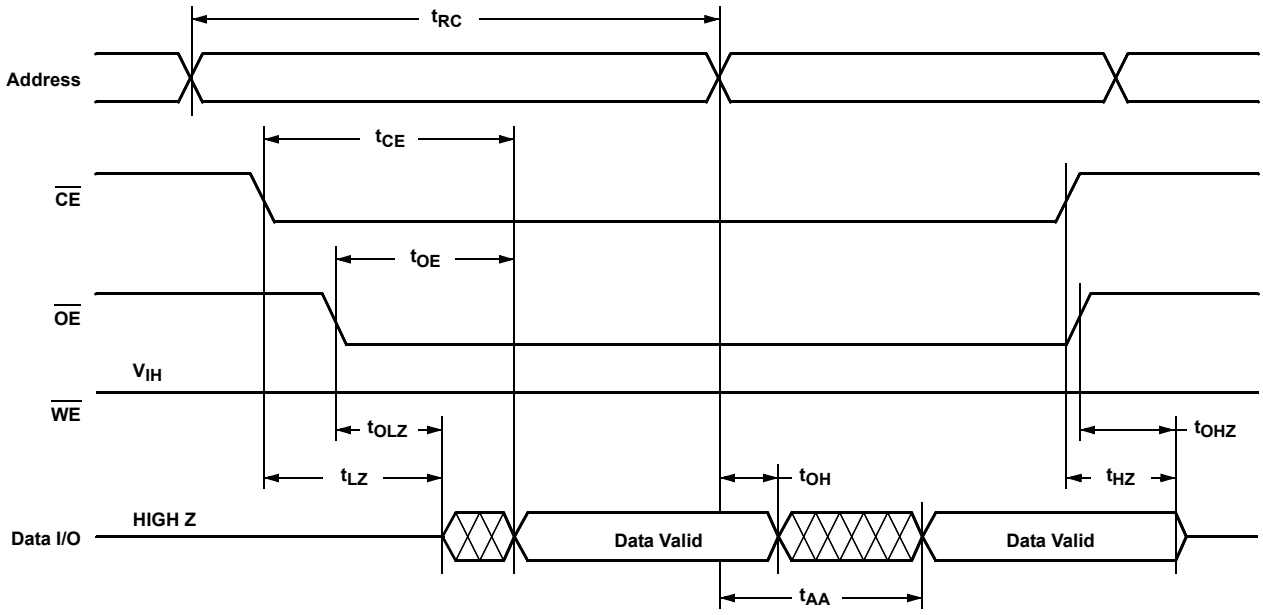
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
|  | Must be steady | Will be steady |
|  | May change from LOW to HIGH | Will change from LOW to HIGH |
|  | May change from HIGH to LOW | Will change from HIGH to LOW |
|  | Don't Care: Changes Allowed | Changing: State Not Known |
|  | N/A | Center Line is High Impedance |

## AC Electrical Specifications

Over the recommended operating conditions, unless otherwise specified.

| SYMBOL | PARAMETER | X28C512-90 / X28C513-90 | | X28C512-12 / X28C513-12 | | X28C512-15 / X28C513-15 | | X28C512-20 / X28C513-20 | | X28C512-25 / X28C513-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| **READ CYCLE LIMITS** | | | | | | | | | | | | |
| $t_{RC}$ | Read cycle time | 90 | | 120 | | 150 | | 200 | | 250 | | ns |
| $t_{CE}$ | Chip enable access time | | 90 | | 120 | | 150 | | 200 | | 250 | ns |
| $t_{AA}$ | Address access time | | 90 | | 120 | | 150 | | 200 | | 250 | ns |
| $t_{OE}$ | Output enable access time | | 40 | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{LZ}$ (Note 3) | $\overline{CE}$ LOW to active output | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OLZ}$ (Note 3) | $\overline{OE}$ LOW to active output | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZ}$ (Note 3) | $\overline{CE}$ HIGH to high Z output | | 40 | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{OHZ}$ (Note 3) | $\overline{OE}$ HIGH to high Z output | | 40 | | 50 | | 50 | | 50 | | 50 | ns |
| $t_{OH}$ | Output hold from address change | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

### *Read Cycle*



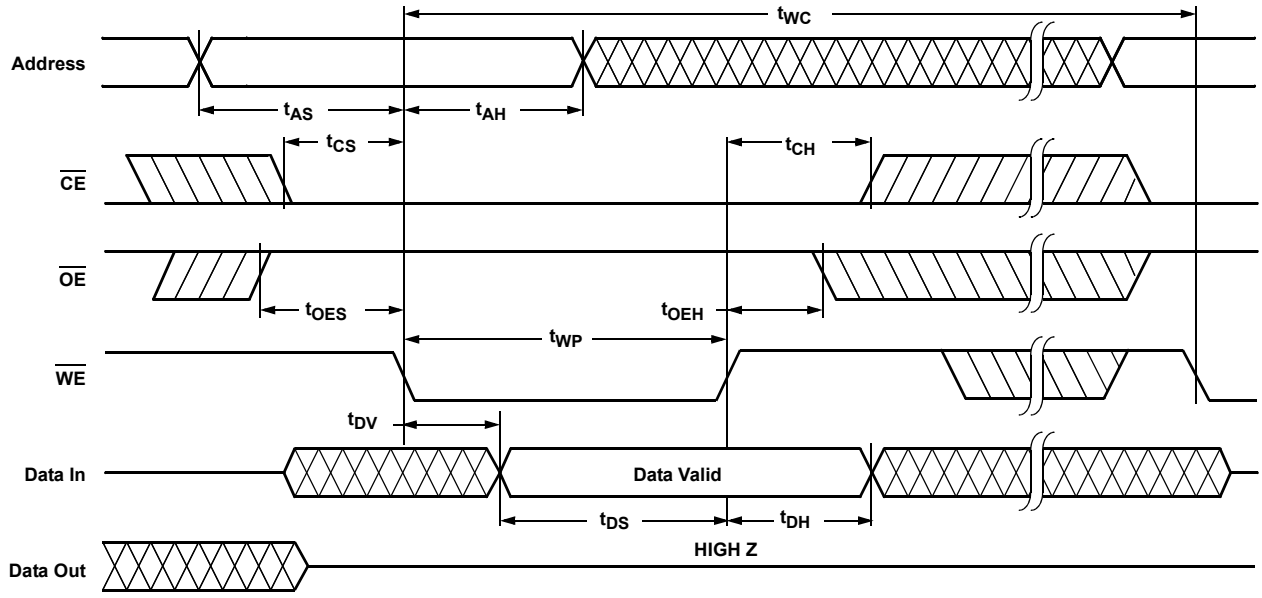

NOTE:

3. $t_{LZ}$ min., $t_{HZ}$, $t_{OLZ}$ min., and $t_{OHZ}$ are periodically sampled and not 100% tested. $t_{HZ}$ max. and $t_{OHZ}$ max. are measured, with $C_L$ = 5pF from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

## Write Cycle Limits

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{WC}$ (Note 4) | Write cycle time | | 10 | ms |
| $t_{AS}$ | Address setup time | 0 | | ns |
| $t_{AH}$ | Address hold time | 50 | | ns |
| $t_{CS}$ | Write setup time | 0 | | ns |
| $t_{CH}$ | Write hold time | 0 | | ns |
| $t_{CW}$ | $\overline{CE}$ pulse width | 100 | | ns |
| $t_{OES}$ | $\overline{OE}$ HIGH setup time | 10 | | ns |
| $t_{OEH}$ | $\overline{OE}$ HIGH hold time | 10 | | ns |
| $t_{WP}$ | $\overline{WE}$ pulse width | 100 | | ns |
| $t_{WPH}$ | $\overline{WE}$ High recovery | 100 | | ns |
| $t_{DV}$ | Data valid | | 1 | µs |
| $t_{DS}$ | Data setup | 50 | | ns |
| $t_{DH}$ | Data hold | 0 | | ns |
| $t_{DW}$ | Delay to next write | 10 | | µs |
| $t_{BLC}$ | Byte load cycle | 0.2 | 100 | µs |

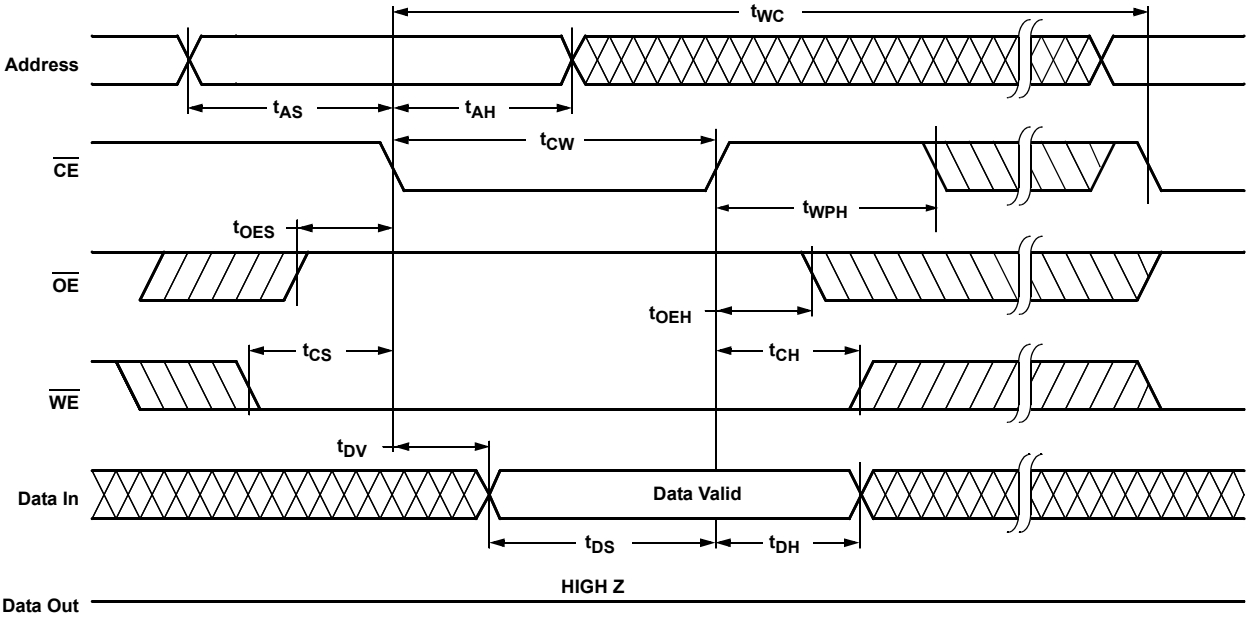
### *$\overline{WE}$ Controlled Write Cycle*



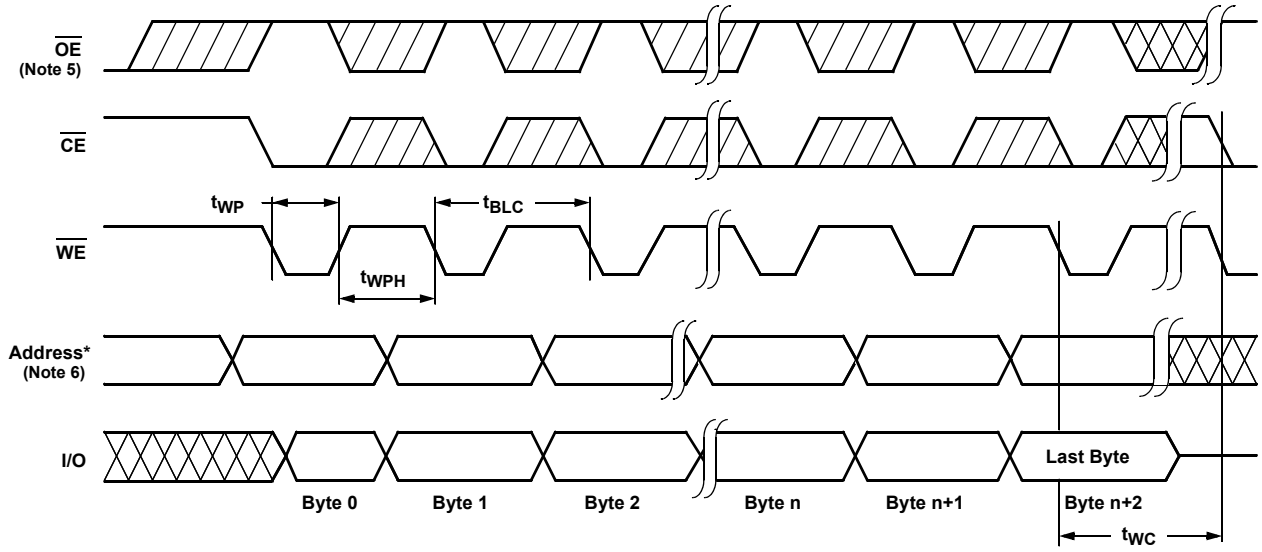

NOTE:

4. $t_{WC}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the internal write operation.

### $\overline{CE}$ Controlled Write Cycle




### Page Write Cycle

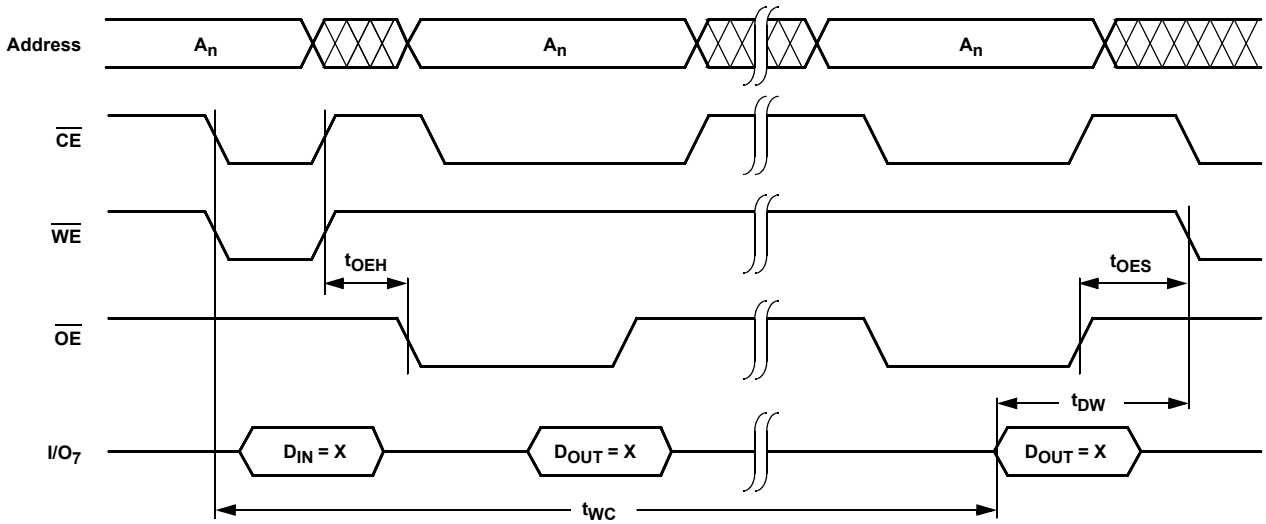



***For each successive write within the page write operation, $A_7$-$A_{15}$ should be the same or writes to an unknown address could occur.**

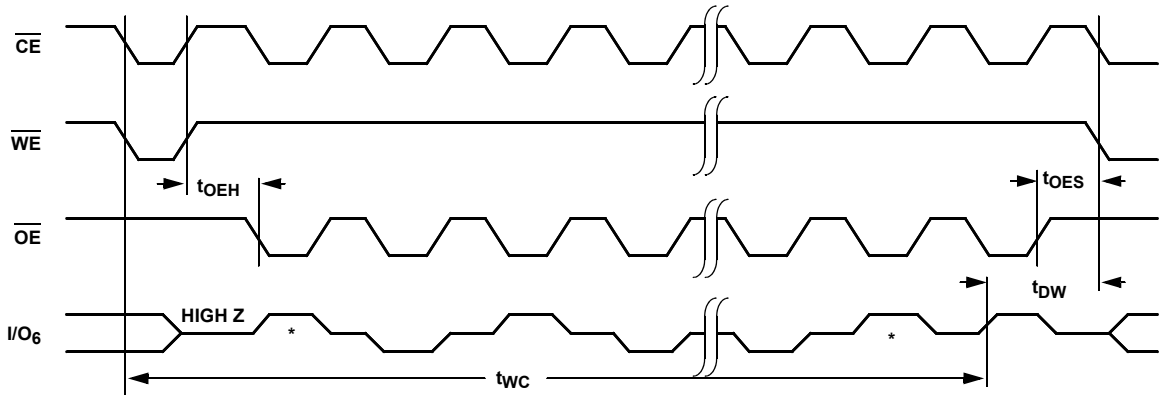
NOTES:

5. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.
6. The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

### $\overline{DATA}$ Polling Timing Diagram (Note 7)




### Toggle Bit Timing Diagram



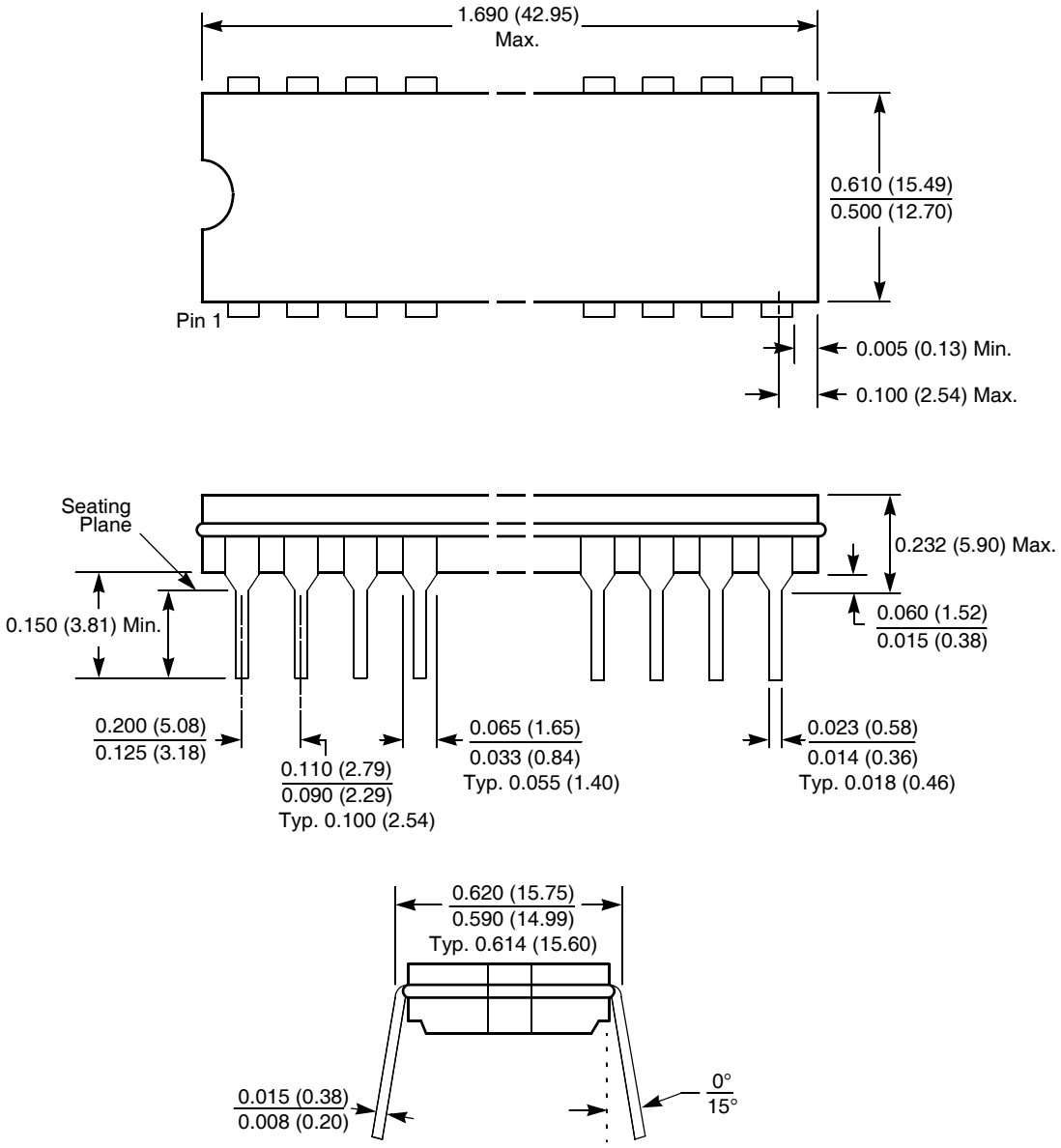

***Starting and ending state will vary, depending upon actual $t_{WC}$.**

NOTE:

7. Polling operations are by definition read cycles and are therefore subject to read cycle timings.

## *Packaging Information*

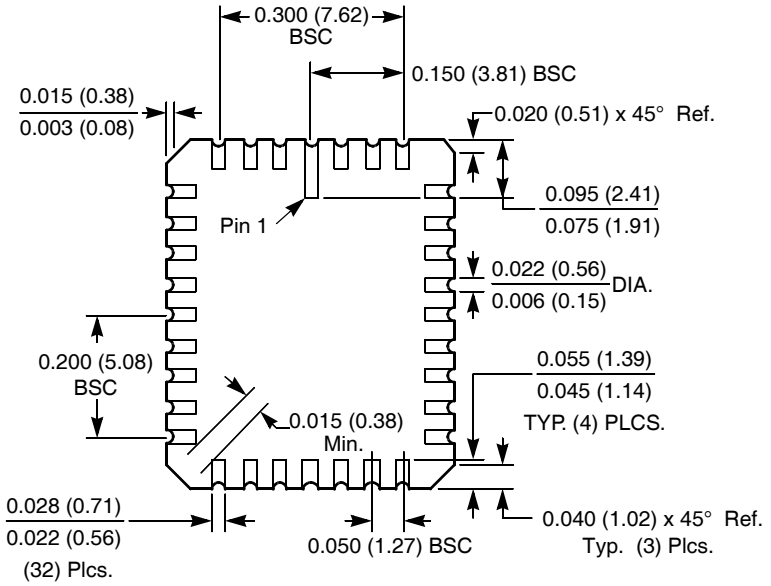
**32-Lead Hermetic Dual In-Line Package Type D**

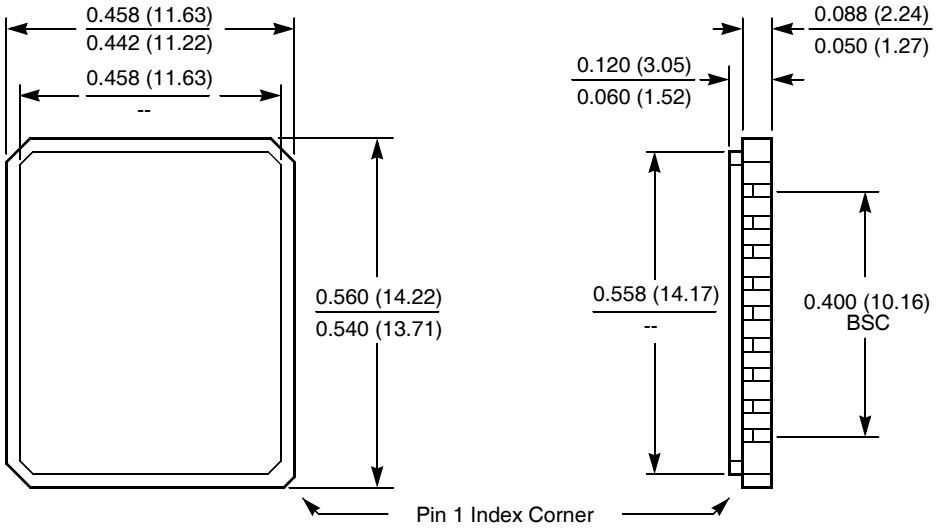



**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## *Packaging Information*

**32-Pad Ceramic Leadless Chip Carrier Package Type E**

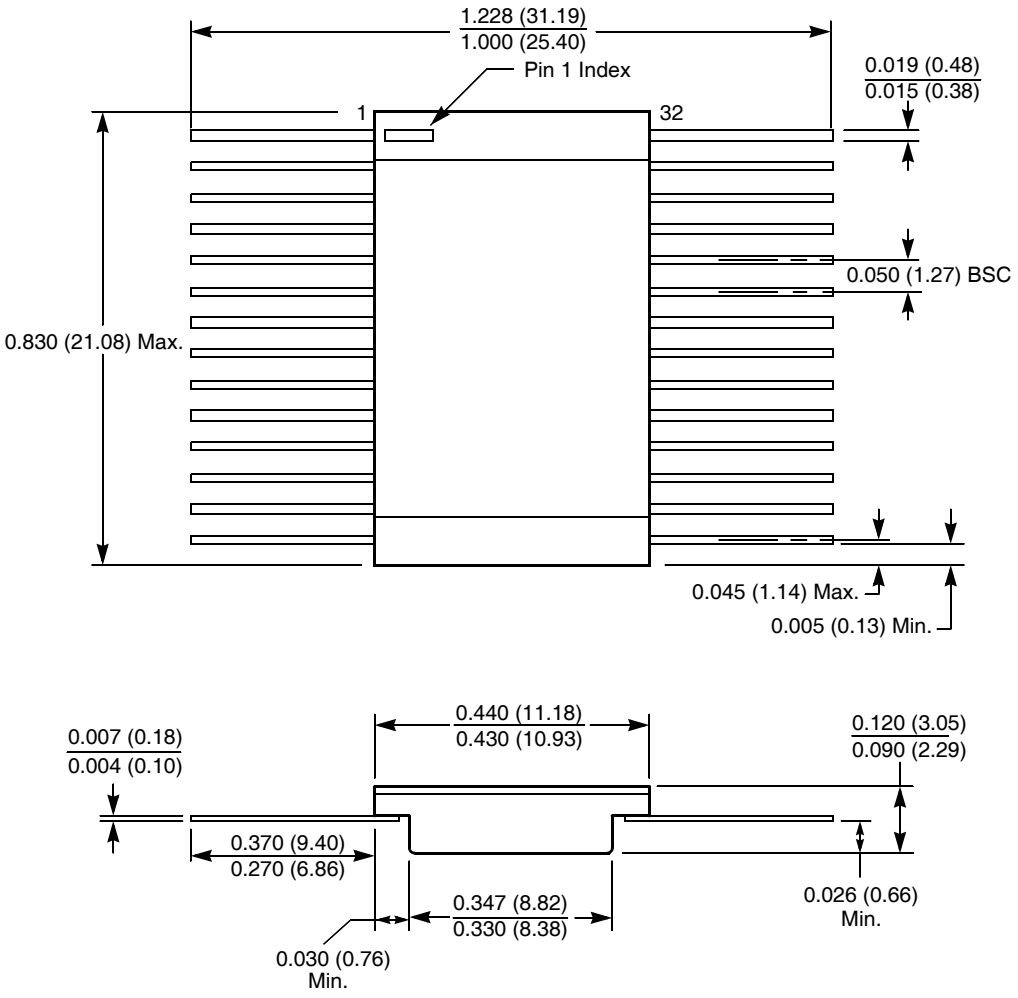



**NOTE:**
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

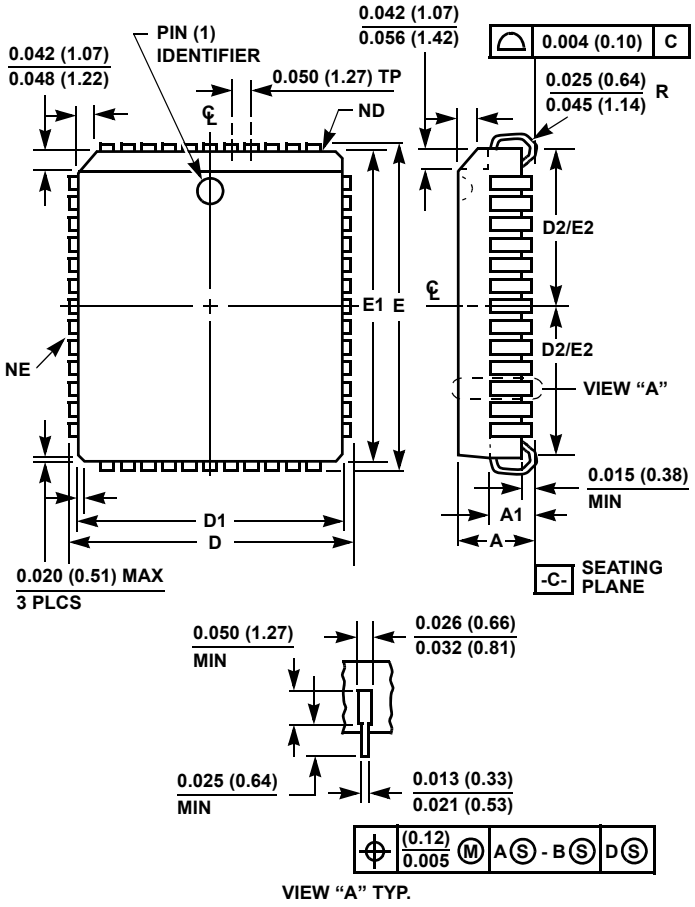
## *Packaging Information*

**32-Lead Ceramic Flat Pack Type F**




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## Plastic Leaded Chip Carrier Packages (PLCC)




**N32.45x55** (JEDEC MS-016AE ISSUE A)
**32 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.125 | 0.140 | 3.18 | 3.55 | - |
| A1 | 0.060 | 0.095 | 1.53 | 2.41 | - |
| D | 0.485 | 0.495 | 12.32 | 12.57 | - |
| D1 | 0.447 | 0.453 | 11.36 | 11.50 | 3 |
| D2 | 0.188 | 0.223 | 4.78 | 5.66 | 4, 5 |
| E | 0.585 | 0.595 | 14.86 | 15.11 | - |
| E1 | 0.547 | 0.553 | 13.90 | 14.04 | 3 |
| E2 | 0.238 | 0.273 | 6.05 | 6.93 | 4, 5 |
| N | 28 | | 28 | | 6 |
| ND | 7 | | 7 | | 7 |
| NE | 9 | | 9 | | 7 |

Rev. 0 7/98

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.
7. ND denotes the number of leads on the two shorts sides of the package, one of which contains pin #1. NE denotes the number of leads on the two long sides of the package.

© Copyright Intersil Americas LLC 2005-2006. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

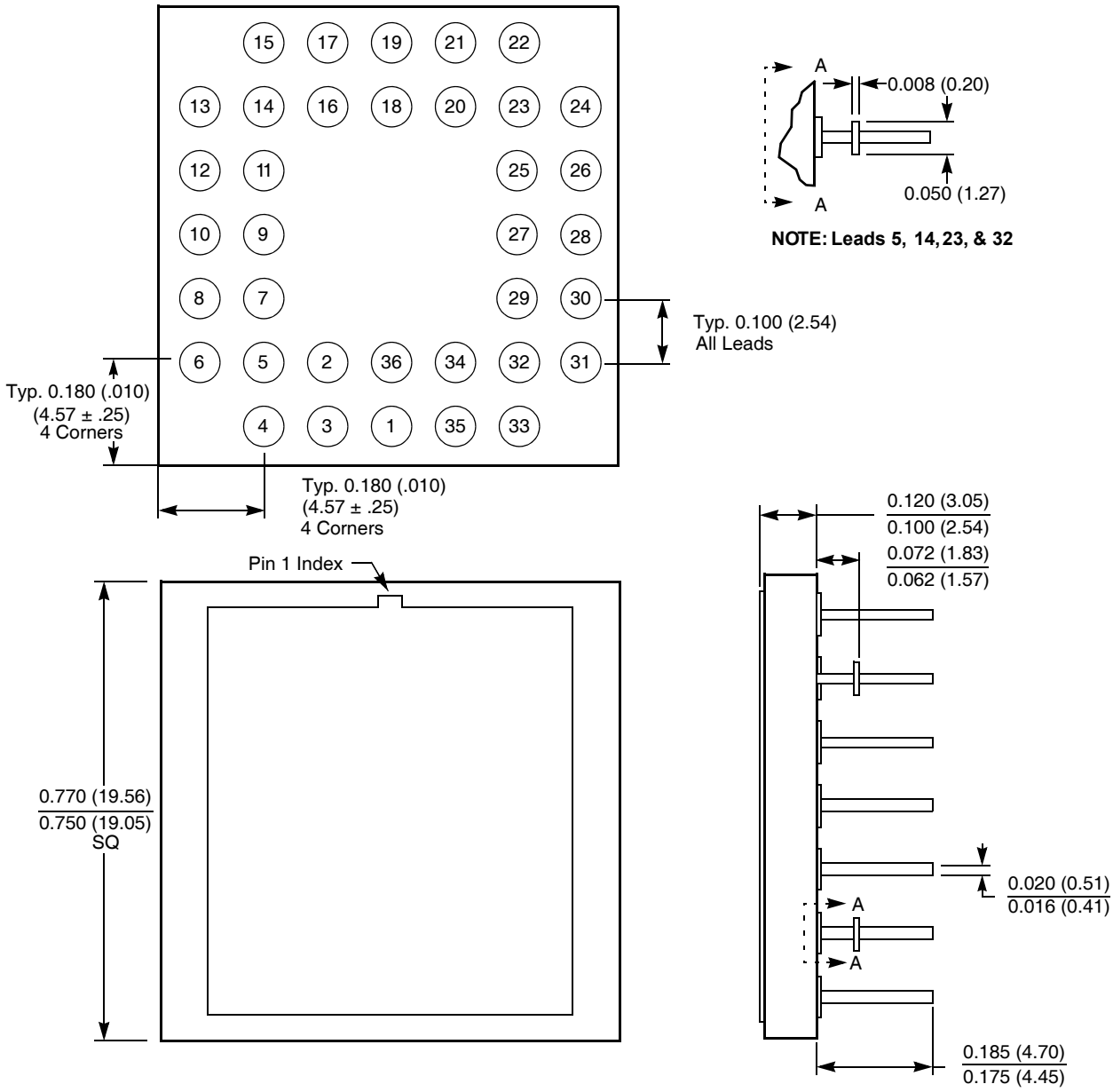
*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see www.intersil.com

## *Ceramic Pin Grid Array Package (CPGA)*

## G36.760x760A

**36 LEAD CERAMIC PIN GRID ARRAY PACKAGE**




NOTE: All dimensions in inches (in parentheses in millimeters).

Rev. 0 12/05