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The S-1004 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±1.0% ($-V_{DET(S)} \geq 2.2$ V). It operates with current consumption of 500 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin falls to 0 V.
The release signal can be delayed by setting a capacitor externally, and the release delay time accuracy at Ta = +25°C is ±15%.
Two output forms Nch open-drain output and CMOS output are available.

■ Features

- Detection voltage: 1.0 V to 5.0 V (0.1 V step)
- Detection voltage accuracy: ±1.0% ($2.2\ V \leq -V_{DET(S)} \leq 5.0\ V$)
  ±22 mV ($1.0\ V \leq -V_{DET(S)} < 2.2\ V$)
- Current consumption: 500 nA typ.
- Operation voltage range: 0.95 V to 10.0 V
- Hysteresis width: 5% ± 2%
- Release delay time accuracy: ±15% (C_D = 4.7 nF, Ta = +25°C)
- Output form: Nch open-drain output (Active "L")
  CMOS output (Active "L")
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- Power supply monitor for microcomputer and reset for CPU
- Constant voltage power supply monitor for TV, Blu-ray recorder and home appliance
- Power supply monitor for portable devices such as notebook PC, digital still camera and mobile phone

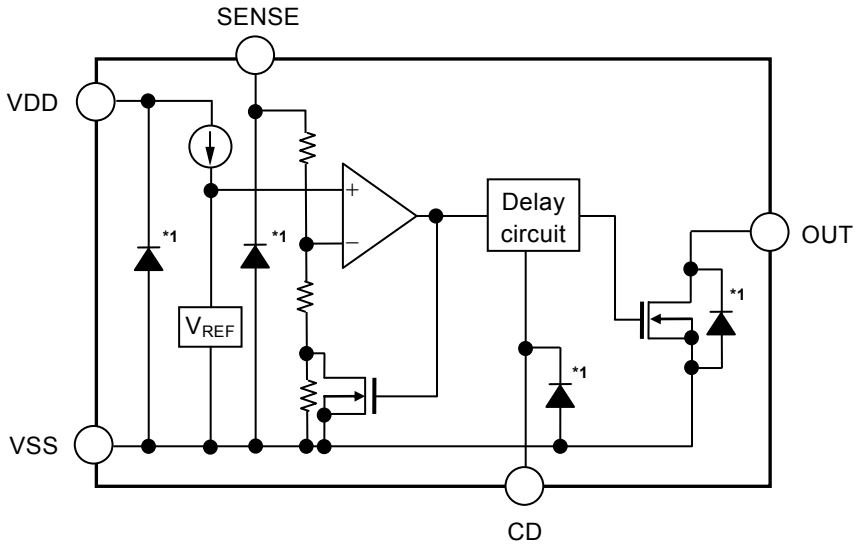
■ Packages

- SOT-23-5
- SNT-6A

■ Block Diagrams

1. S-1004 Series NA / NB type (Nch open-drain output)

Function	Status
Output logic	Active "L"

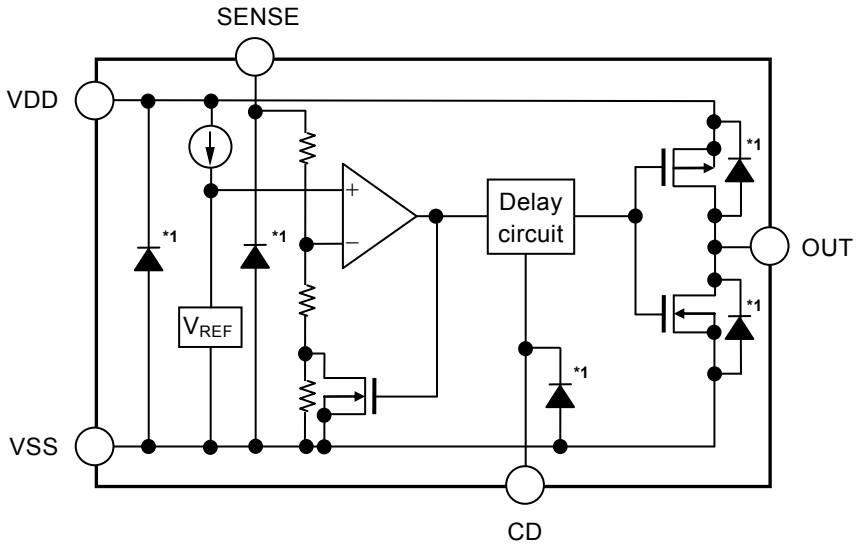


***1.** Parasitic diode

Figure 1

2. S-1004 Series CA / CB type (CMOS output)

Function	Status
Output logic	Active "L"



***1.** Parasitic diode

Figure 2

■ Product Name Structure

Users can select the output form and detection voltage value for the S-1004 Series.
Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product types**" regarding the product types, "**3. Packages**" regarding the package drawings and "**4. Product name list**" regarding details of product name.

1. Product name

S-1004 x x xx I - xxxx U

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - M5T1: SOT-23-5, Tape
  - I6T1: SNT-6A, Tape
- Operation temperature
  - I: Ta = −40°C to +85°C
- Detection voltage value
  - 10 to 50
  - (e.g., when the detection voltage is 1.0 V, it is expressed as 10.)
- Pin configuration*2
  - A, B
- Output form*3
  - N: Nch open-drain output (Active "L")*4
  - C: CMOS output (Active "L")*4

***1.** Refer to the tape drawing.
***2.** Refer to "■ **Pin Configurations**".
***3.** Refer to "**2. Function list of product types**".
***4.** If you request the product with output logic active "H", contact our sales office.

2. Function list of product types

Table 1

Product Type	Output Form	Output Logic	Pin Configuration	Package
NA	Nch open-drain output	Active "L"	A	SOT-23-5, SNT-6A
NB		Active "L"	B	SOT-23-5
CA	CMOS output	Active "L"	A	SOT-23-5, SNT-6A
CB		Active "L"	B	SOT-23-5

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

4. Product name list

4. 1 S-1004 Series NA type

Output form: Nch open-drain output (Active "L")

Table 3

Detection Voltage	SOT-23-5	SNT-6A
1.0 V ± 22 mV	S-1004NA10I-M5T1U	S-1004NA10I-I6T1U
1.1 V ± 22 mV	S-1004NA11I-M5T1U	S-1004NA11I-I6T1U
1.2 V ± 22 mV	S-1004NA12I-M5T1U	S-1004NA12I-I6T1U
1.3 V ± 22 mV	S-1004NA13I-M5T1U	S-1004NA13I-I6T1U
1.4 V ± 22 mV	S-1004NA14I-M5T1U	S-1004NA14I-I6T1U
1.5 V ± 22 mV	S-1004NA15I-M5T1U	S-1004NA15I-I6T1U
1.6 V ± 22 mV	S-1004NA16I-M5T1U	S-1004NA16I-I6T1U
1.7 V ± 22 mV	S-1004NA17I-M5T1U	S-1004NA17I-I6T1U
1.8 V ± 22 mV	S-1004NA18I-M5T1U	S-1004NA18I-I6T1U
1.9 V ± 22 mV	S-1004NA19I-M5T1U	S-1004NA19I-I6T1U
2.0 V ± 22 mV	S-1004NA20I-M5T1U	S-1004NA20I-I6T1U
2.1 V ± 22 mV	S-1004NA21I-M5T1U	S-1004NA21I-I6T1U
2.2 V ± 1.0%	S-1004NA22I-M5T1U	S-1004NA22I-I6T1U
2.3 V ± 1.0%	S-1004NA23I-M5T1U	S-1004NA23I-I6T1U
2.4 V ± 1.0%	S-1004NA24I-M5T1U	S-1004NA24I-I6T1U
2.5 V ± 1.0%	S-1004NA25I-M5T1U	S-1004NA25I-I6T1U
2.6 V ± 1.0%	S-1004NA26I-M5T1U	S-1004NA26I-I6T1U
2.7 V ± 1.0%	S-1004NA27I-M5T1U	S-1004NA27I-I6T1U
2.8 V ± 1.0%	S-1004NA28I-M5T1U	S-1004NA28I-I6T1U
2.9 V ± 1.0%	S-1004NA29I-M5T1U	S-1004NA29I-I6T1U
3.0 V ± 1.0%	S-1004NA30I-M5T1U	S-1004NA30I-I6T1U
3.1 V ± 1.0%	S-1004NA31I-M5T1U	S-1004NA31I-I6T1U
3.2 V ± 1.0%	S-1004NA32I-M5T1U	S-1004NA32I-I6T1U
3.3 V ± 1.0%	S-1004NA33I-M5T1U	S-1004NA33I-I6T1U
3.4 V ± 1.0%	S-1004NA34I-M5T1U	S-1004NA34I-I6T1U
3.5 V ± 1.0%	S-1004NA35I-M5T1U	S-1004NA35I-I6T1U
3.6 V ± 1.0%	S-1004NA36I-M5T1U	S-1004NA36I-I6T1U
3.7 V ± 1.0%	S-1004NA37I-M5T1U	S-1004NA37I-I6T1U
3.8 V ± 1.0%	S-1004NA38I-M5T1U	S-1004NA38I-I6T1U
3.9 V ± 1.0%	S-1004NA39I-M5T1U	S-1004NA39I-I6T1U
4.0 V ± 1.0%	S-1004NA40I-M5T1U	S-1004NA40I-I6T1U
4.1 V ± 1.0%	S-1004NA41I-M5T1U	S-1004NA41I-I6T1U
4.2 V ± 1.0%	S-1004NA42I-M5T1U	S-1004NA42I-I6T1U
4.3 V ± 1.0%	S-1004NA43I-M5T1U	S-1004NA43I-I6T1U
4.4 V ± 1.0%	S-1004NA44I-M5T1U	S-1004NA44I-I6T1U
4.5 V ± 1.0%	S-1004NA45I-M5T1U	S-1004NA45I-I6T1U
4.6 V ± 1.0%	S-1004NA46I-M5T1U	S-1004NA46I-I6T1U
4.7 V ± 1.0%	S-1004NA47I-M5T1U	S-1004NA47I-I6T1U
4.8 V ± 1.0%	S-1004NA48I-M5T1U	S-1004NA48I-I6T1U
4.9 V ± 1.0%	S-1004NA49I-M5T1U	S-1004NA49I-I6T1U
5.0 V ± 1.0%	S-1004NA50I-M5T1U	S-1004NA50I-I6T1U

4. 2 S-1004 Series NB type

Output form: Nch open-drain output (Active "L")

Table 4

Detection Voltage	SOT-23-5
1.0 V ± 22 mV	S-1004NB10I-M5T1U
1.1 V ± 22 mV	S-1004NB11I-M5T1U
1.2 V ± 22 mV	S-1004NB12I-M5T1U
1.3 V ± 22 mV	S-1004NB13I-M5T1U
1.4 V ± 22 mV	S-1004NB14I-M5T1U
1.5 V ± 22 mV	S-1004NB15I-M5T1U
1.6 V ± 22 mV	S-1004NB16I-M5T1U
1.7 V ± 22 mV	S-1004NB17I-M5T1U
1.8 V ± 22 mV	S-1004NB18I-M5T1U
1.9 V ± 22 mV	S-1004NB19I-M5T1U
2.0 V ± 22 mV	S-1004NB20I-M5T1U
2.1 V ± 22 mV	S-1004NB21I-M5T1U
2.2 V ± 1.0%	S-1004NB22I-M5T1U
2.3 V ± 1.0%	S-1004NB23I-M5T1U
2.4 V ± 1.0%	S-1004NB24I-M5T1U
2.5 V ± 1.0%	S-1004NB25I-M5T1U
2.6 V ± 1.0%	S-1004NB26I-M5T1U
2.7 V ± 1.0%	S-1004NB27I-M5T1U
2.8 V ± 1.0%	S-1004NB28I-M5T1U
2.9 V ± 1.0%	S-1004NB29I-M5T1U
3.0 V ± 1.0%	S-1004NB30I-M5T1U
3.1 V ± 1.0%	S-1004NB31I-M5T1U
3.2 V ± 1.0%	S-1004NB32I-M5T1U
3.3 V ± 1.0%	S-1004NB33I-M5T1U
3.4 V ± 1.0%	S-1004NB34I-M5T1U
3.5 V ± 1.0%	S-1004NB35I-M5T1U
3.6 V ± 1.0%	S-1004NB36I-M5T1U
3.7 V ± 1.0%	S-1004NB37I-M5T1U
3.8 V ± 1.0%	S-1004NB38I-M5T1U
3.9 V ± 1.0%	S-1004NB39I-M5T1U
4.0 V ± 1.0%	S-1004NB40I-M5T1U
4.1 V ± 1.0%	S-1004NB41I-M5T1U
4.2 V ± 1.0%	S-1004NB42I-M5T1U
4.3 V ± 1.0%	S-1004NB43I-M5T1U
4.4 V ± 1.0%	S-1004NB44I-M5T1U
4.5 V ± 1.0%	S-1004NB45I-M5T1U
4.6 V ± 1.0%	S-1004NB46I-M5T1U
4.7 V ± 1.0%	S-1004NB47I-M5T1U
4.8 V ± 1.0%	S-1004NB48I-M5T1U
4.9 V ± 1.0%	S-1004NB49I-M5T1U
5.0 V ± 1.0%	S-1004NB50I-M5T1U

4. 3 S-1004 Series CA type

Output form: CMOS output (Active "L")

Table 5

Detection Voltage	SOT-23-5	SNT-6A
1.0 V ± 22 mV	S-1004CA10I-M5T1U	S-1004CA10I-I6T1U
1.1 V ± 22 mV	S-1004CA11I-M5T1U	S-1004CA11I-I6T1U
1.2 V ± 22 mV	S-1004CA12I-M5T1U	S-1004CA12I-I6T1U
1.3 V ± 22 mV	S-1004CA13I-M5T1U	S-1004CA13I-I6T1U
1.4 V ± 22 mV	S-1004CA14I-M5T1U	S-1004CA14I-I6T1U
1.5 V ± 22 mV	S-1004CA15I-M5T1U	S-1004CA15I-I6T1U
1.6 V ± 22 mV	S-1004CA16I-M5T1U	S-1004CA16I-I6T1U
1.7 V ± 22 mV	S-1004CA17I-M5T1U	S-1004CA17I-I6T1U
1.8 V ± 22 mV	S-1004CA18I-M5T1U	S-1004CA18I-I6T1U
1.9 V ± 22 mV	S-1004CA19I-M5T1U	S-1004CA19I-I6T1U
2.0 V ± 22 mV	S-1004CA20I-M5T1U	S-1004CA20I-I6T1U
2.1 V ± 22 mV	S-1004CA21I-M5T1U	S-1004CA21I-I6T1U
2.2 V ± 1.0%	S-1004CA22I-M5T1U	S-1004CA22I-I6T1U
2.3 V ± 1.0%	S-1004CA23I-M5T1U	S-1004CA23I-I6T1U
2.4 V ± 1.0%	S-1004CA24I-M5T1U	S-1004CA24I-I6T1U
2.5 V ± 1.0%	S-1004CA25I-M5T1U	S-1004CA25I-I6T1U
2.6 V ± 1.0%	S-1004CA26I-M5T1U	S-1004CA26I-I6T1U
2.7 V ± 1.0%	S-1004CA27I-M5T1U	S-1004CA27I-I6T1U
2.8 V ± 1.0%	S-1004CA28I-M5T1U	S-1004CA28I-I6T1U
2.9 V ± 1.0%	S-1004CA29I-M5T1U	S-1004CA29I-I6T1U
3.0 V ± 1.0%	S-1004CA30I-M5T1U	S-1004CA30I-I6T1U
3.1 V ± 1.0%	S-1004CA31I-M5T1U	S-1004CA31I-I6T1U
3.2 V ± 1.0%	S-1004CA32I-M5T1U	S-1004CA32I-I6T1U
3.3 V ± 1.0%	S-1004CA33I-M5T1U	S-1004CA33I-I6T1U
3.4 V ± 1.0%	S-1004CA34I-M5T1U	S-1004CA34I-I6T1U
3.5 V ± 1.0%	S-1004CA35I-M5T1U	S-1004CA35I-I6T1U
3.6 V ± 1.0%	S-1004CA36I-M5T1U	S-1004CA36I-I6T1U
3.7 V ± 1.0%	S-1004CA37I-M5T1U	S-1004CA37I-I6T1U
3.8 V ± 1.0%	S-1004CA38I-M5T1U	S-1004CA38I-I6T1U
3.9 V ± 1.0%	S-1004CA39I-M5T1U	S-1004CA39I-I6T1U
4.0 V ± 1.0%	S-1004CA40I-M5T1U	S-1004CA40I-I6T1U
4.1 V ± 1.0%	S-1004CA41I-M5T1U	S-1004CA41I-I6T1U
4.2 V ± 1.0%	S-1004CA42I-M5T1U	S-1004CA42I-I6T1U
4.3 V ± 1.0%	S-1004CA43I-M5T1U	S-1004CA43I-I6T1U
4.4 V ± 1.0%	S-1004CA44I-M5T1U	S-1004CA44I-I6T1U
4.5 V ± 1.0%	S-1004CA45I-M5T1U	S-1004CA45I-I6T1U
4.6 V ± 1.0%	S-1004CA46I-M5T1U	S-1004CA46I-I6T1U
4.7 V ± 1.0%	S-1004CA47I-M5T1U	S-1004CA47I-I6T1U
4.8 V ± 1.0%	S-1004CA48I-M5T1U	S-1004CA48I-I6T1U
4.9 V ± 1.0%	S-1004CA49I-M5T1U	S-1004CA49I-I6T1U
5.0 V ± 1.0%	S-1004CA50I-M5T1U	S-1004CA50I-I6T1U

4. 4 S-1004 Series CB type

Output form: CMOS output (Active "L")

Table 6

Detection Voltage	SOT-23-5
1.0 V ± 22 mV	S-1004CB10I-M5T1U
1.1 V ± 22 mV	S-1004CB11I-M5T1U
1.2 V ± 22 mV	S-1004CB12I-M5T1U
1.3 V ± 22 mV	S-1004CB13I-M5T1U
1.4 V ± 22 mV	S-1004CB14I-M5T1U
1.5 V ± 22 mV	S-1004CB15I-M5T1U
1.6 V ± 22 mV	S-1004CB16I-M5T1U
1.7 V ± 22 mV	S-1004CB17I-M5T1U
1.8 V ± 22 mV	S-1004CB18I-M5T1U
1.9 V ± 22 mV	S-1004CB19I-M5T1U
2.0 V ± 22 mV	S-1004CB20I-M5T1U
2.1 V ± 22 mV	S-1004CB21I-M5T1U
2.2 V ± 1.0%	S-1004CB22I-M5T1U
2.3 V ± 1.0%	S-1004CB23I-M5T1U
2.4 V ± 1.0%	S-1004CB24I-M5T1U
2.5 V ± 1.0%	S-1004CB25I-M5T1U
2.6 V ± 1.0%	S-1004CB26I-M5T1U
2.7 V ± 1.0%	S-1004CB27I-M5T1U
2.8 V ± 1.0%	S-1004CB28I-M5T1U
2.9 V ± 1.0%	S-1004CB29I-M5T1U
3.0 V ± 1.0%	S-1004CB30I-M5T1U
3.1 V ± 1.0%	S-1004CB31I-M5T1U
3.2 V ± 1.0%	S-1004CB32I-M5T1U
3.3 V ± 1.0%	S-1004CB33I-M5T1U
3.4 V ± 1.0%	S-1004CB34I-M5T1U
3.5 V ± 1.0%	S-1004CB35I-M5T1U
3.6 V ± 1.0%	S-1004CB36I-M5T1U
3.7 V ± 1.0%	S-1004CB37I-M5T1U
3.8 V ± 1.0%	S-1004CB38I-M5T1U
3.9 V ± 1.0%	S-1004CB39I-M5T1U
4.0 V ± 1.0%	S-1004CB40I-M5T1U
4.1 V ± 1.0%	S-1004CB41I-M5T1U
4.2 V ± 1.0%	S-1004CB42I-M5T1U
4.3 V ± 1.0%	S-1004CB43I-M5T1U
4.4 V ± 1.0%	S-1004CB44I-M5T1U
4.5 V ± 1.0%	S-1004CB45I-M5T1U
4.6 V ± 1.0%	S-1004CB46I-M5T1U
4.7 V ± 1.0%	S-1004CB47I-M5T1U
4.8 V ± 1.0%	S-1004CB48I-M5T1U
4.9 V ± 1.0%	S-1004CB49I-M5T1U
5.0 V ± 1.0%	S-1004CB50I-M5T1U

■ Pin Configurations

1. S-1004 Series NA / CA type

1. 1 SOT-23-5

Top view

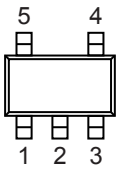


Figure 3

Table 7 Pin Configuration A

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Power supply pin
3	VSS	GND pin
4	CD	Connection pin for delay capacitor
5	SENSE	Detection voltage input pin

1. 2 SNT-6A

Top view



Figure 4

Table 8 Pin Configuration A

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Power supply pin
3	SENSE	Detection voltage input pin
4	CD	Connection pin for delay capacitor
5	NC*1	No connection
6	VSS	GND pin

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

2. S-1004 Series NB / CB type

2. 1 SOT-23-5

Top view

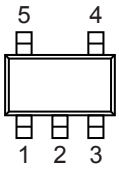


Figure 5

Table 9 Pin Configuration B

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VSS	GND pin
3	VDD	Power supply pin
4	SENSE	Detection voltage input pin
5	CD	Connection pin for delay capacitor

■ Absolute Maximum Ratings

Table 10

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		$V_{DD} - V_{SS}$	12.0	V
CD pin input voltage		V_{CD}	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
SENSE pin input voltage		V_{SENSE}	$V_{SS} - 0.3$ to 12.0	V
Output voltage	Nch open-drain output product	V_{OUT}	$V_{SS} - 0.3$ to 12.0	V
	CMOS output product		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Output current		I_{OUT}	50	mA
Power dissipation	SOT-23-5	P_D	600[*1]	mW
	SNT-6A		400[*1]	mW
Operation ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

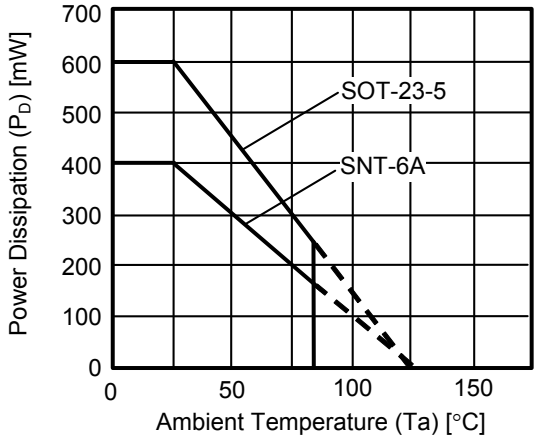


Figure 6 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Nch open-drain output product

Table 11

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	0.95 V ≤ V_{DD} ≤ 10.0 V	1.0 V ≤ $-V_{DET(S)}$ < 2.2 V	$-V_{DET(S)}$ − 0.022	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.022	V	1
			2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V	$-V_{DET(S)}$ × 0.99	$-V_{DET(S)}$	$-V_{DET(S)}$ × 1.01	V	1
Hysteresis width	V_{HYS}	−		$-V_{DET}$ × 0.03	$-V_{DET}$ × 0.05	$-V_{DET}$ × 0.07	V	1
Current consumption*2	I_{SS}	V_{DD} = 10.0 V, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V		−	0.50	0.90	μA	2
Operation voltage	V_{DD}	−		0.95	−	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*3 = 0.5 V V_{SENSE} = 0.0 V	V_{DD} = 0.95 V	0.59	1.00	−	mA	3
			V_{DD} = 1.2 V	0.73	1.33	−	mA	3
			V_{DD} = 2.4 V	1.47	2.39	−	mA	3
			V_{DD} = 4.8 V	1.86	2.50	−	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{DS}*3 = 10.0 V, V_{SENSE} = 10.0 V		−	−	0.08	μA	3
Detection voltage temperature coefficient*4	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40°C to +85°C		−	±100	±350	ppm/°C	1
Detection delay time*5	t_{DET}	V_{DD} = 5.0 V		−	40	−	μs	4
Release delay time*6	t_{RESET}	V_{DD} = $-V_{DET(S)}$ + 1.0 V, C_D = 4.7 nF		10.79	12.69	14.59	ms	4
SENSE pin resistance	R_{SENSE}	1.0 V ≤ $-V_{DET(S)}$ < 1.2 V		5.0	19.0	42.0	MΩ	2
		1.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V		6.0	30.0	98.0	MΩ	2

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3** or **Table 4**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\ [\text{mV/°C}]^{*1} = -V_{DET(S)}\ (\text{typ.})[\text{V}]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [\text{ppm/°C}]^{*3} \div 1000$$

- ***1.** Temperature change of the detection voltage
- ***2.** Set detection voltage
- ***3.** Detection voltage temperature coefficient

***5.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2, after the output pin is pulled up to 5.0 V by the resistance of 470 kΩ.

***6.** The time period from when the pulse voltage of 0.95 V → 10.0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} × 90%, after the output pin is pulled up to V_{DD} by the resistance of 100 kΩ.

2. CMOS output product

Table 12

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage[*1]	$-V_{DET}$	0.95 V ≤ V_{DD} ≤ 10.0 V	1.0 V ≤ $-V_{DET(S)}$ < 2.2 V	$-V_{DET(S)}$ − 0.022	$-V_{DET(S)}$	$-V_{DET(S)}$ + 0.022	V	1
			2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V	$-V_{DET(S)}$ × 0.99	$-V_{DET(S)}$	$-V_{DET(S)}$ × 1.01	V	1
Hysteresis width	V_{HYS}	−		$-V_{DET}$ × 0.03	$-V_{DET}$ × 0.05	$-V_{DET}$ × 0.07	V	1
Current consumption[*2]	I_{SS}	V_{DD} = 10.0 V, V_{SENSE} = $-V_{DET(S)}$ + 1.0 V		−	0.50	0.90	μA	2
Operation voltage	V_{DD}	−		0.95	−	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}[*3] = 0.5 V V_{SENSE} = 0.0 V	V_{DD} = 0.95 V	0.59	1.00	−	mA	3
			V_{DD} = 1.2 V	0.73	1.33	−	mA	3
			V_{DD} = 2.4 V	1.47	2.39	−	mA	3
			V_{DD} = 4.8 V	1.86	2.50	−	mA	3
		Output transistor Pch V_{DS}[*3] = 0.5 V V_{SENSE} = 10.0 V	V_{DD} = 4.8 V	1.62	2.60	−	mA	5
			V_{DD} = 6.0 V	1.78	2.86	−	mA	5
Detection voltage temperature coefficient[*4]	$\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$	Ta = −40°C to +85°C		−	±100	±350	ppm/°C	1
Detection delay time[*5]	t_{DET}	V_{DD} = 5.0 V		−	40	−	μs	4
Release delay time[*6]	t_{RESET}	V_{DD} = $-V_{DET(S)}$ + 1.0 V, C_D = 4.7 nF		10.79	12.69	14.59	ms	4
SENSE pin resistance	R_{SENSE}	1.0 V ≤ $-V_{DET(S)}$ < 1.2 V		5.0	19.0	42.0	MΩ	2
		1.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V		6.0	30.0	98.0	MΩ	2

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 5** or **Table 6**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** V_{DS}: Drain-to-source voltage of the output transistor

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\ [\text{mV/°C}]^{*1} = -V_{DET(S)}\ (\text{typ.})[\text{V}]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [\text{ppm/°C}]^{*3} \div 1000$$

- ***1.** Temperature change of the detection voltage
- ***2.** Set detection voltage
- ***3.** Detection voltage temperature coefficient

***5.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} / 2.

***6.** The time period from when the pulse voltage of 0.95 V → 10.0 V is applied to the SENSE pin to when V_{OUT} reaches V_{DD} × 90%.

■ Test Circuits

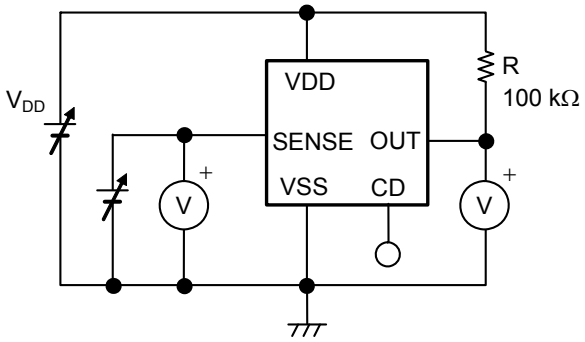


Figure 7 Test Circuit 1
(Nch open-drain output product)

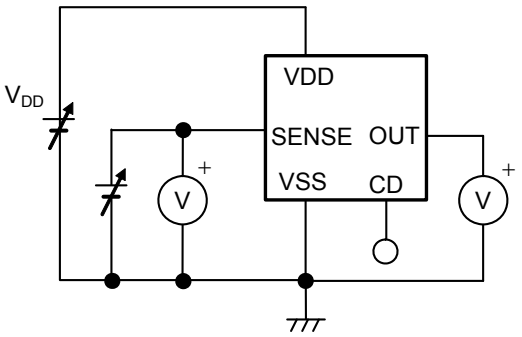


Figure 8 Test Circuit 1
(CMOS output product)

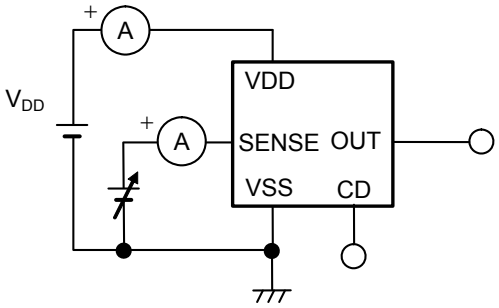


Figure 9 Test Circuit 2

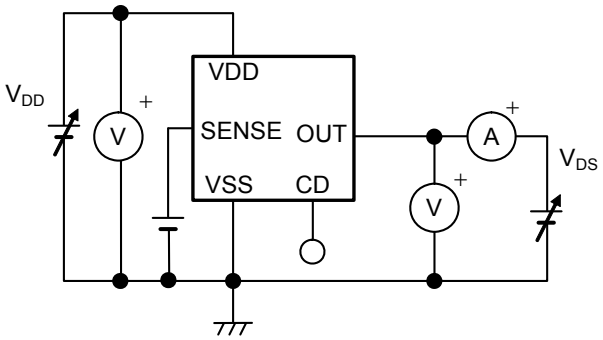


Figure 10 Test Circuit 3

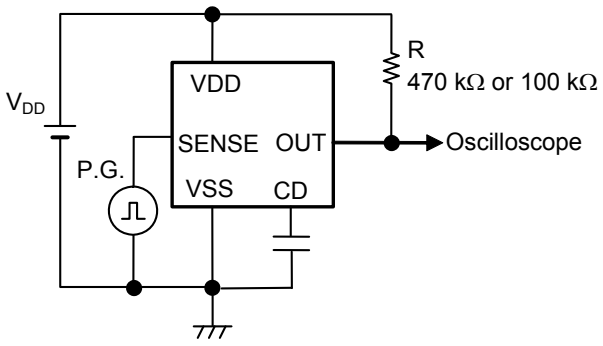


Figure 11 Test Circuit 4
(Nch open-drain output product)

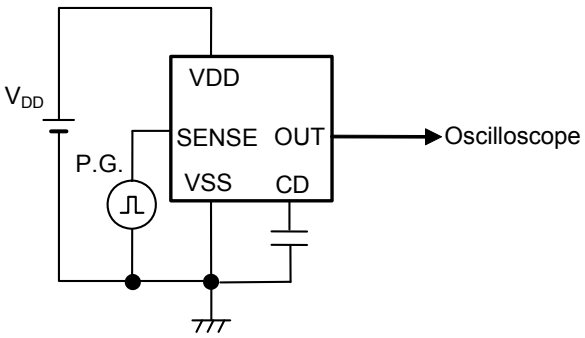


Figure 12 Test Circuit 4
(CMOS output product)

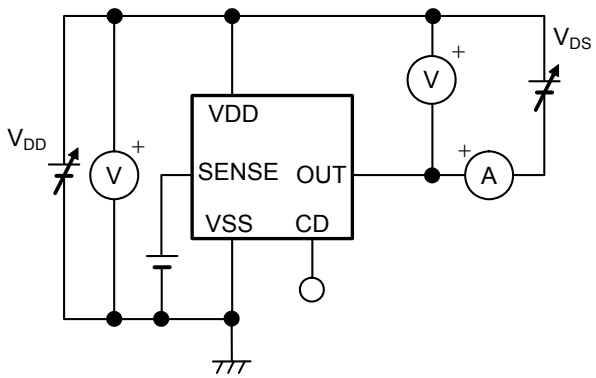
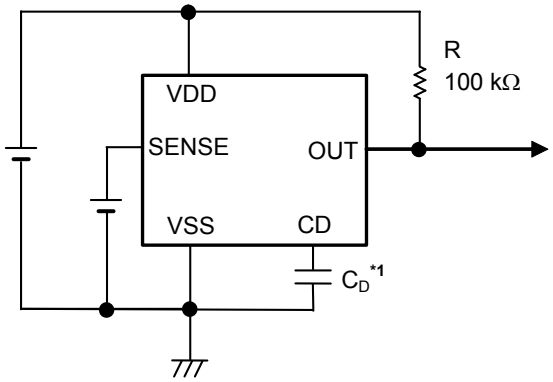


Figure 13 Test Circuit 5

■ Standard Circuits

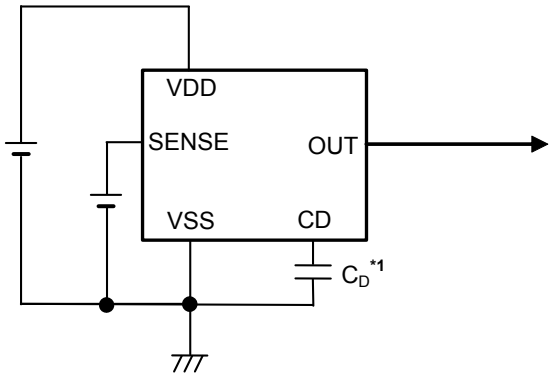
1. Nch open-drain output product



***1.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 14

2. CMOS output product



***1.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 15

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 18** or **Figure 19** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 16**).

Example: In the S-1004Cx18, the detection voltage is either one in the range of $1.778\ V \le -V_{DET} \le 1.822\ V$.
This means that some S-1004Cx18 have $-V_{DET} = 1.778$ V and some have $-V_{DET} = 1.822$ V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 18** or **Figure 19** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 17**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \le +V_{DET} \le -V_{DET} \times 1.07$.

Example: For the S-1004Cx18, the release voltage is either one in the range of $1.832\ V \le +V_{DET} \le 1.949\ V$.
This means that some S-1004Cx18 have $+V_{DET} = 1.832$ V and some have $+V_{DET} = 1.949$ V.

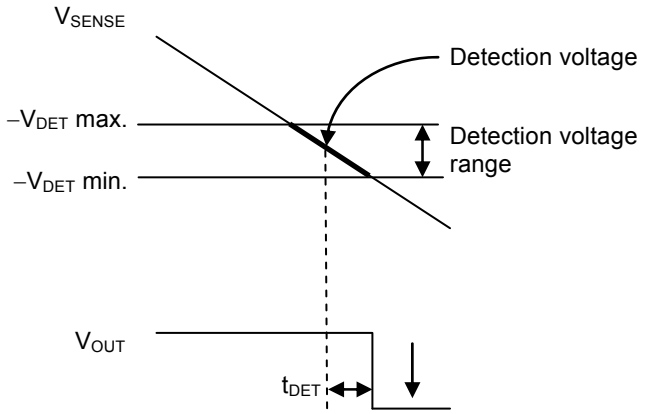


Figure 16 Detection Voltage

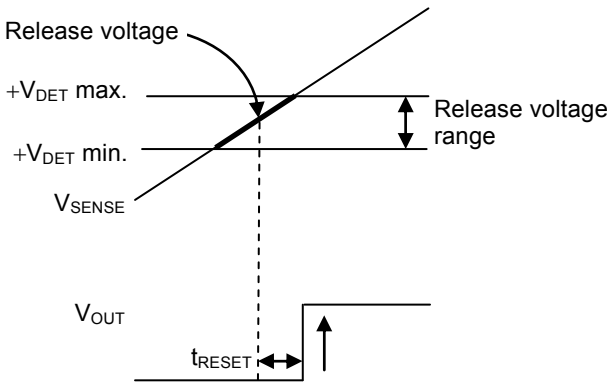


Figure 17 Release Voltage

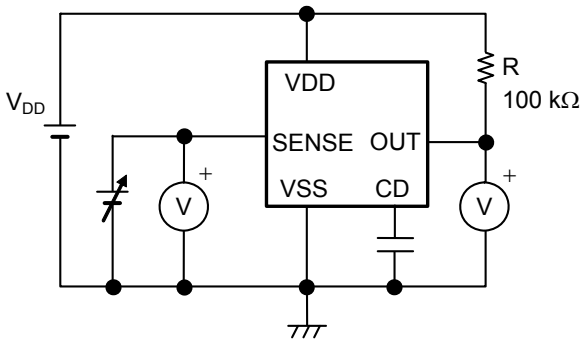


Figure 18 Test Circuit of Detection Voltage and Release Voltage (Nch open-drain output product)

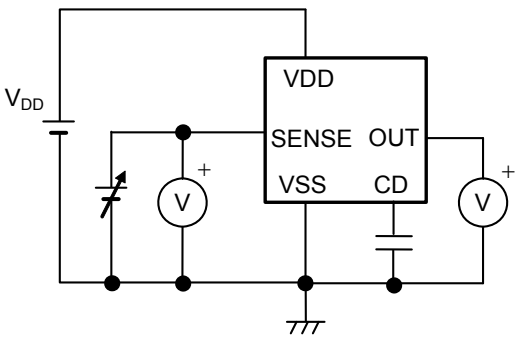


Figure 19 Test Circuit of Detection Voltage and Release Voltage (CMOS output product)

3. Hysteresis width (V_{HYS})

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = V_{HYS} in "**Figure 23 Timing Chart of S-1004 Series NA / NB Type**" and "**Figure 25 Timing Chart of S-1004 Series CA / CB Type**"). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

4. Release delay time (t_{RESET})

The release delay time is the time period from when the input voltage to the SENSE pin exceeds the release voltage ($+V_{DET}$) to when the output from the OUT pin inverts. The release delay time changes according to the delay capacitor (C_D).

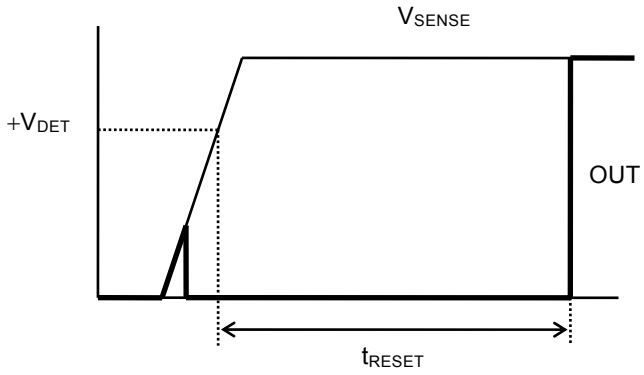


Figure 20 Release Delay Time

5. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

6. Oscillation

In applications where an input resistor is connected (**Figure 21**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (at the time of release) causes a voltage drop equal to [feed-through current] × [input resistance]. Since the VDD pin and the SENSE pin are shorted as in **Figure 21**, the SENSE pin voltage drops at the time of release. Then the SENSE pin voltage drops below the detection voltage and the output goes from "H" to "L". In this status, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

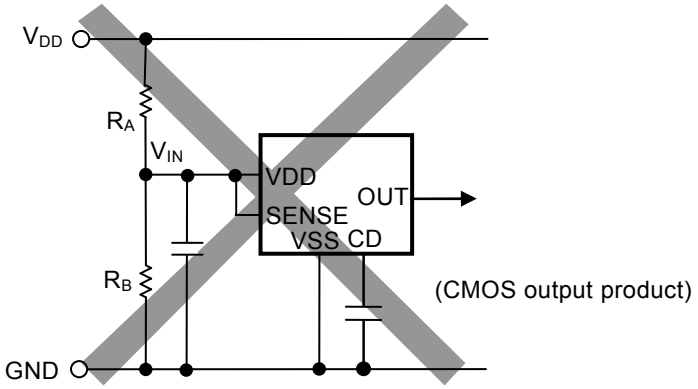


Figure 21 Example for Bad Implementation Due to Detection Voltage Change

■ Operation

1. Basic operation

1. 1 S-1004 Series NA / NB type

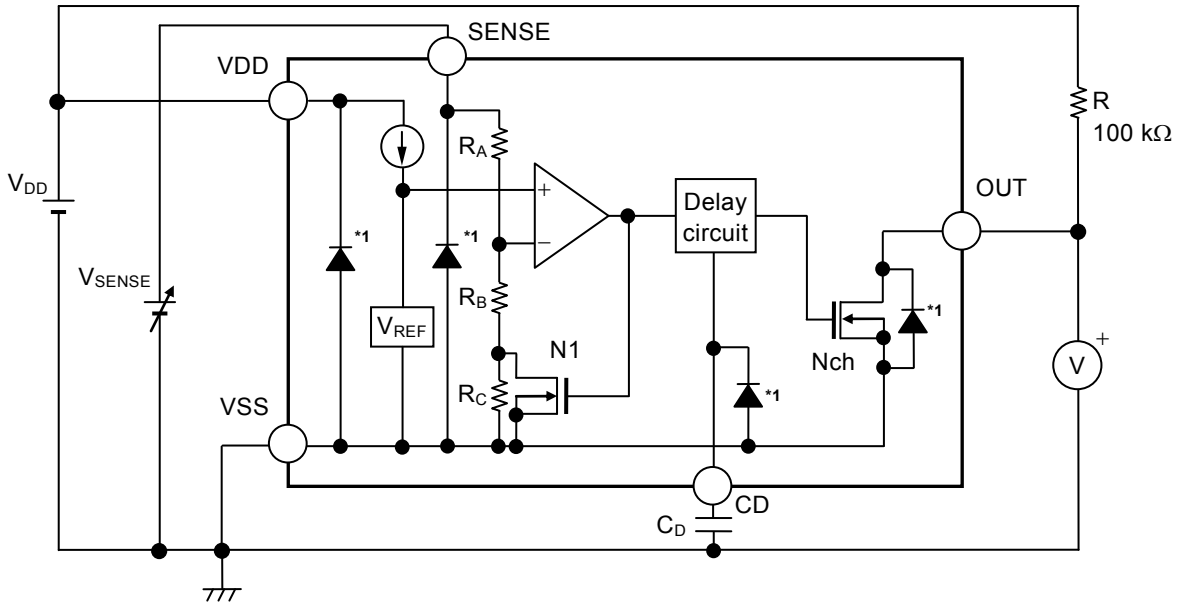
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output V_{DD} ("H") when the output is pulled up. Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).
When V_{SENSE} decreases to $-V_{DET}$ or lower (point A in **Figure 23**), the Nch transistor is turned on. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{DET}).
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{SS} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 23**), the Nch transistor is turned off. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{RESET}) when the output is pulled up.



***1.** Parasitic diode

Figure 22 Operation of S-1004 Series NA / NB Type

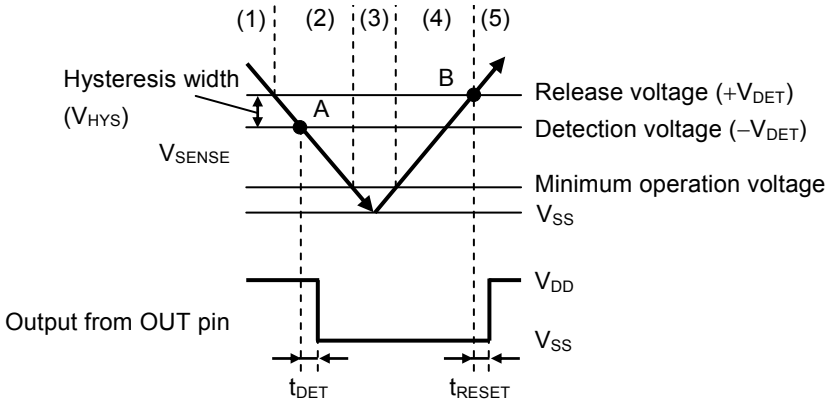


Figure 23 Timing Chart of S-1004 Series NA / NB Type

1. 2 S-1004 Series CA / CB type

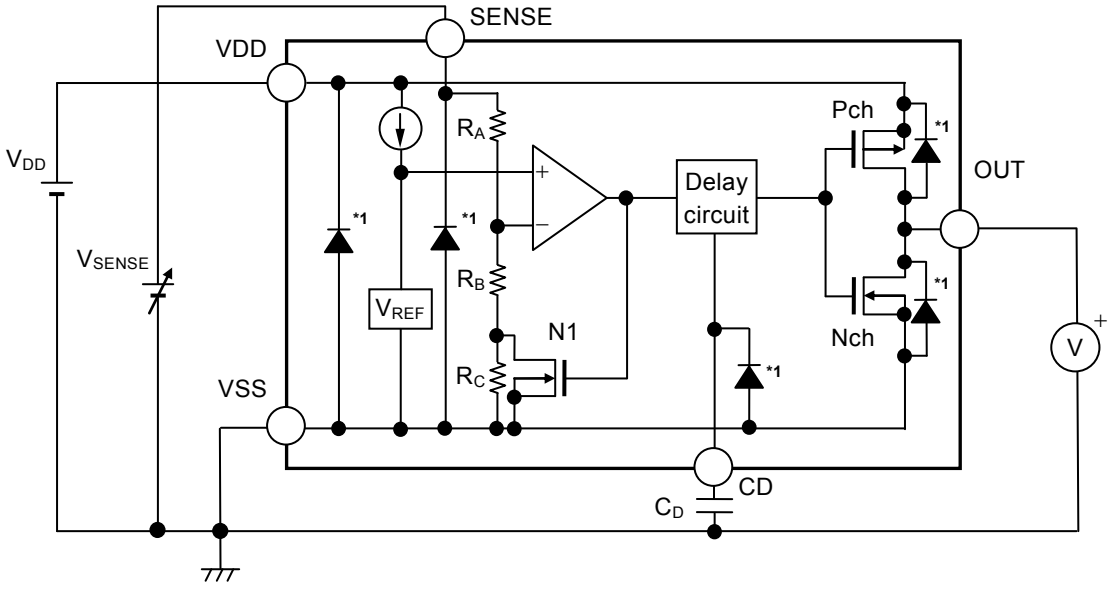
(1) When the power supply voltage (V_{DD}) is the minimum operation voltage or higher, and the SENSE pin voltage (V_{SENSE}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output V_{DD} ("H"). Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if V_{SENSE} decreases to $+V_{DET}$ or lower, V_{DD} is output when V_{SENSE} is higher than the detection voltage ($-V_{DET}$).
When V_{SENSE} decreases to $-V_{DET}$ or lower (point A in **Figure 25**), the Nch transistor is turned on and the Pch transistor is turned off. And then V_{SS} ("L") is output from the OUT pin after the elapse of the detection delay time (t_{DET}).
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if V_{SENSE} further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when V_{DD} is minimum operation voltage or higher.

(4) Even if V_{SENSE} exceeds $-V_{DET}$, V_{SS} is output when V_{SENSE} is lower than $+V_{DET}$.

(5) When V_{SENSE} increases to $+V_{DET}$ or higher (point B in **Figure 25**), the Nch transistor is turned off and the Pch transistor is turned on. And then V_{DD} is output from the OUT pin after the elapse of the release delay time (t_{RESET}).



***1.** Parasitic diode

Figure 24 Operation of S-1004 Series CA / CB Type

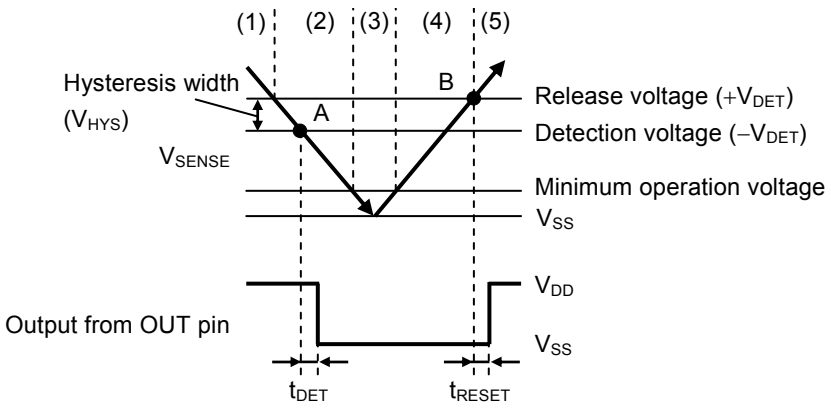


Figure 25 Timing Chart of S-1004 Series CA / CB Type

2. SENSE pin

2. 1 Error when detection voltage is set externally

By connecting a node that was resistance-divided by the resistor (R_A) and the resistor (R_B) to the SENSE pin as seen in **Figure 26**, the detection voltage can be set externally.
For conventional products without the SENSE pin, R_A cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if R_A is large, problems such as oscillation or larger error in the hysteresis width may occur.
In the S-1004 Series, R_A and R_B are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance (R_{SENSE}) that will occur.
Although R_{SENSE} in the S-1004 Series is large (5 MΩ min.) to make the error small, R_A and R_B should be selected such that the error is within the allowable limits.

2. 2 Selection of R_A and R_B

In **Figure 26**, the relation between the external setting detection voltage (V_{DX}) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (1)$$

However, in reality there is an error in the current flowing through R_{SENSE}.
When considering this error, the relation between V_{DX} and $-V_{DET}$ is calculated as follows.

$$\begin{aligned} V_{DX} &= -V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{\dfrac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times -V_{DET} \quad \cdots (2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \dfrac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100\ [\%] \quad \cdots (3)$$

As seen in equation (3), the smaller the resistance values of R_A and R_B compared to R_{SENSE}, the smaller the error rate becomes.
Also, the relation between the external setting hysteresis width (V_{HX}) and the hysteresis width (V_{HYS}) is calculated by equation below. Error due to R_{SENSE} also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (4)$$

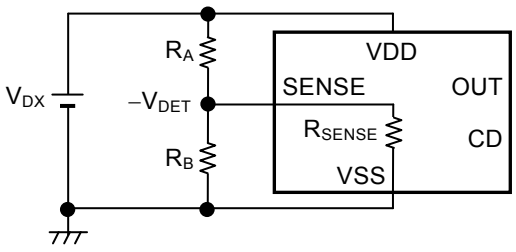


Figure 26 Detection Voltage External Setting Circuit

Caution If R_A and R_B are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.

2. 3 Power on sequence

Apply power in the order, the VDD pin then the SENSE pin.
As seen in **Figure 27**, when $V_{SENSE} \geq +V_{DET}$, the OUT pin output (V_{OUT}) rises and the S-1004 Series becomes the release status (normal operation).

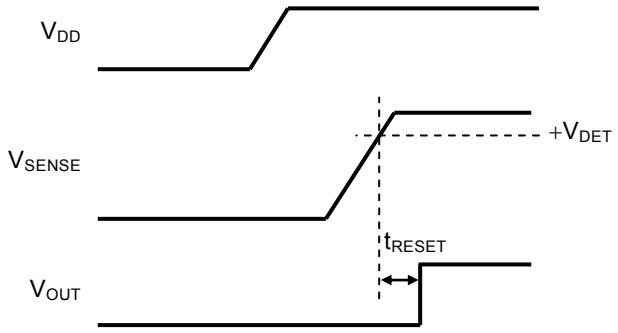


Figure 27

Caution If power is applied in the order the SENSE pin then the VDD pin, an erroneous release may occur even if $V_{SENSE} < +V_{DET}$.

2. 4 Precautions when shorting between the VDD pin and the SENSE pin

2. 4. 1 Input resistor

Do not connect the input resistor (R_A) when shorting between the VDD pin and the SENSE pin.
A feed-through current flows through the VDD pin at the time of release. When connecting the circuit shown as **Figure 28**, the feed-through current of the VDD pin flowing through R_A will cause a drop in V_{SENSE} at the time of release.
At that time, oscillation may occur if $V_{SENSE} \leq -V_{DET}$.

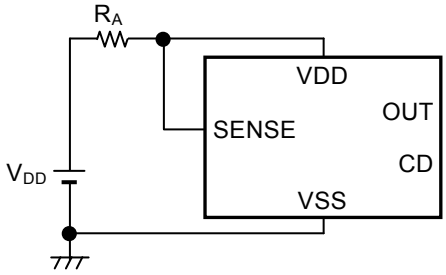


Figure 28

2. 4. 2 Parasitic resistance and parasitic capacitance

Due to the difference in parasitic resistance and parasitic capacitance of the VDD pin and the SENSE pin, power may be applied to the SENSE pin first.
Note that an erroneous release may occur if this happens (refer to "**2. 3 Power on sequence**").

Caution In CMOS output product, make sure that the VDD pin input impedance does not become too high, regardless of the above. Since a feed-through current is large, a malfunction may occur if the VDD pin voltage changes greatly at the time of release.

2. 5 Malfunction when V_{DD} falls

As seen in **Figure 29**, note that if the VDD pin voltage (V_{DD}) drops steeply below 1.2 V when $-V_{DET} < V_{SENSE} < +V_{DET}$, erroneous detection may occur.
When $V_{DD_Low} \geq 1.2$ V, erroneous detection does not occur.
When $V_{DD_Low} < 1.2$ V, the more the V_{DD} falling amplitude increases or the shorter the falling time becomes, the easier the erroneous detection.
Perform thorough evaluation in actual application.

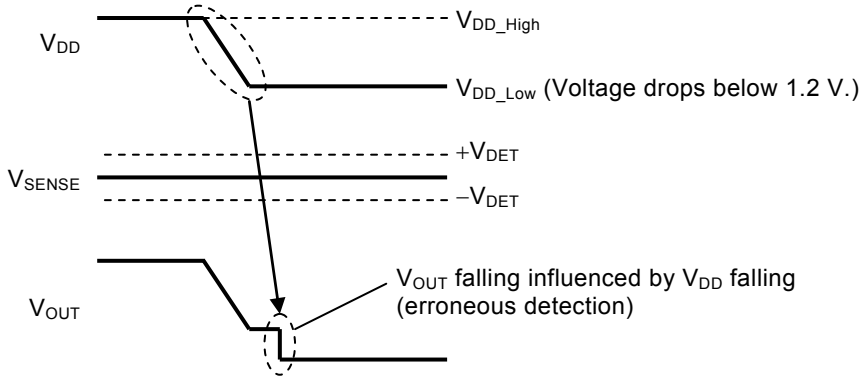


Figure 29

The S-1004Cx50 example in **Figure 30** shows an example of erroneous detection boundary conditions.

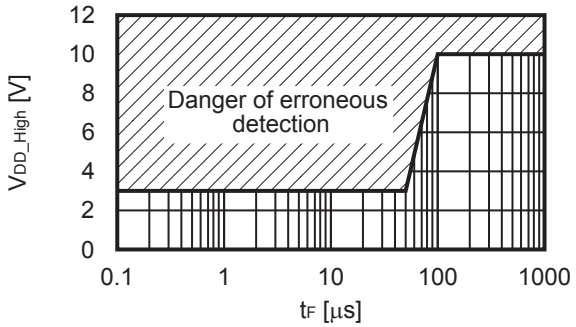


Figure 30

Remark Test conditions

Product name:	S-1004Cx50
V_{SENSE}:	$-V_{DET(S)} + 0.1$ V
V_{DD_High}:	VDD pin voltage before falling
V_{DD_Low}:	VDD pin voltage after falling (0.95 V)
ΔV_{DD}:	$V_{DD_High} - V_{DD_Low}$
t_F:	Falling time of V_{DD} from $V_{DD_High} - \Delta V_{DD} \times 10\%$ to $V_{DD_Low} + \Delta V_{DD} \times 10\%$

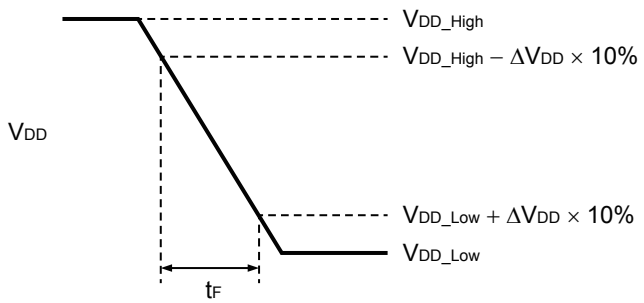


Figure 31

3. Delay circuit

The delay circuit has the function that adjusts the release delay time (t_{RESET}) from when the SENSE pin voltage (V_{SENSE}) reaches release voltage ($+V_{DET}$) to when the output from OUT pin inverts.
t_{RESET} is determined by the delay coefficient, the delay capacitor (C_D), and the release delay time when the CD pin is open (t_{RESET0}), and calculated by the equation below.

$$t_{RESET}\ [ms] = \text{Delay coefficient} \times C_D\ [nF] + t_{RESET0}\ [ms]$$

Table 13

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +85°C	1.78	2.29	3.13
Ta = +25°C	2.30	2.66	3.07
Ta = −40°C	2.68	3.09	3.57

Table 14

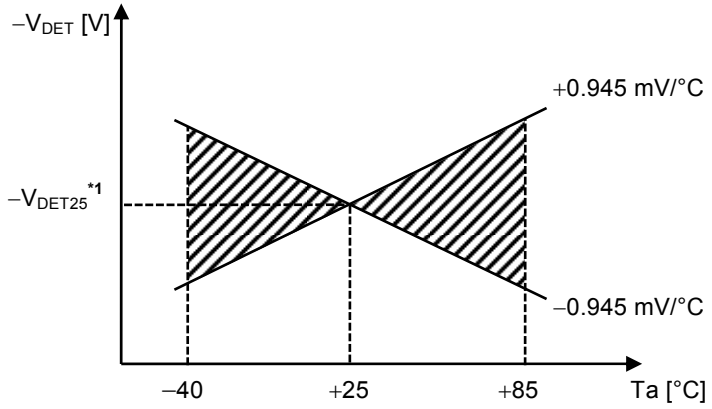
Operation Temperature	Release Delay Time when CD Pin is Open (t_{RESET0})		
	Min.	Typ.	Max.
Ta = +85°C	0.020 ms	0.049 ms	0.130 ms
Ta = +25°C	0.021 ms	0.059 ms	0.164 ms
Ta = −40°C	0.024 ms	0.074 ms	0.202 ms

Caution 1. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.
2. There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value (30 nA to 200 nA).
3. The detection delay time (t_{DET}) cannot be adjusted by C_D.

4. Other characteristics

4. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 32** shows the temperature characteristics of detection voltage in the operation temperature range.



***1.** $-V_{DET25}$ is a detection voltage value at Ta = +25°C.

Figure 32 Temperature Characteristics of Detection Voltage (Example for $-V_{DET}$ = 2.7 V)

4. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta+V_{DET}}{\Delta Ta}$ of the release voltage is calculated by using the temperature change $\frac{\Delta-V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta+V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

The temperature change of the release voltage and the detection voltage has the same sign consequently.

4. 3 Temperature characteristics of hysteresis voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta+V_{DET}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta+V_{DET}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

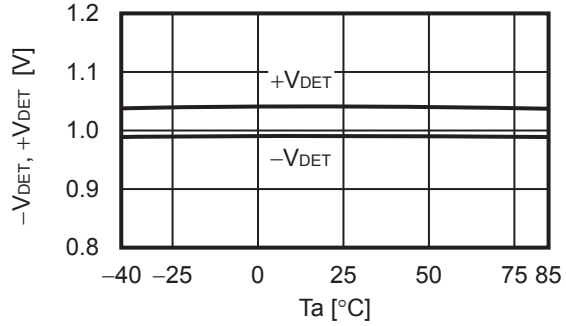
■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product of the S-1004 Series, the feed-through current flows at the time of detection and release. If the VDD pin input impedance is high, malfunction may occur due to the voltage drop by the feed-through current when releasing.
- In CMOS output product, oscillation may occur if a pull-down resistor is connected and falling speed of the SENSE pin voltage (V_{SENSE}) is slow near the detection voltage when the VDD pin and the SENSE pin are shorted.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

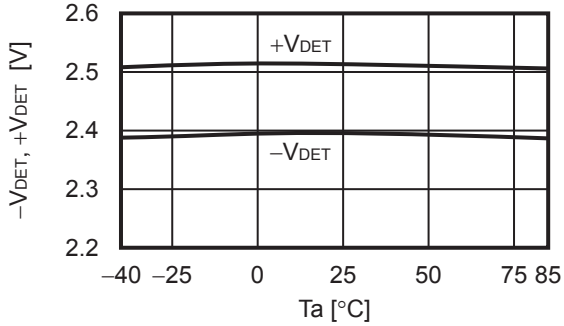
■ Characteristics (Typical Data)

1. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

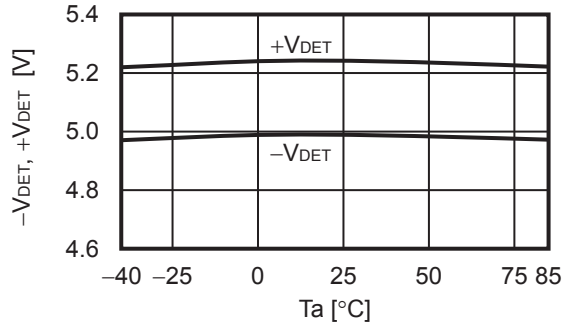
S-1004Cx10 V_{DD} = 5.0 V



S-1004Cx24 V_{DD} = 5.0 V

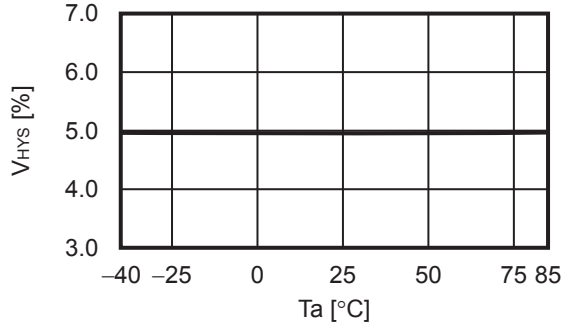


S-1004Cx50 V_{DD} = 5.0 V

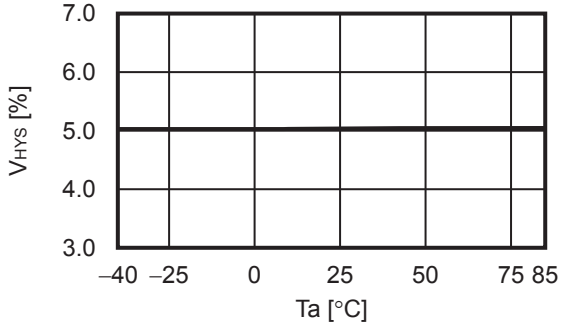


2. Hysteresis width (V_{HYS}) vs. Temperature (Ta)

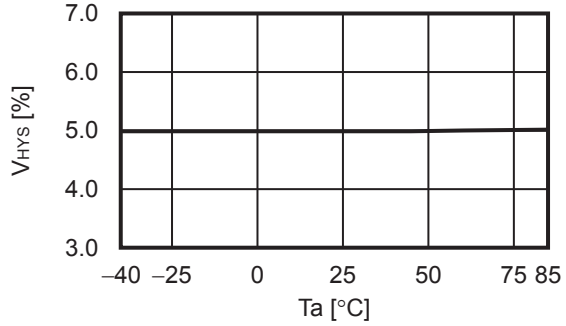
S-1004Cx10 V_{DD} = 5.0 V



S-1004Cx24 V_{DD} = 5.0 V

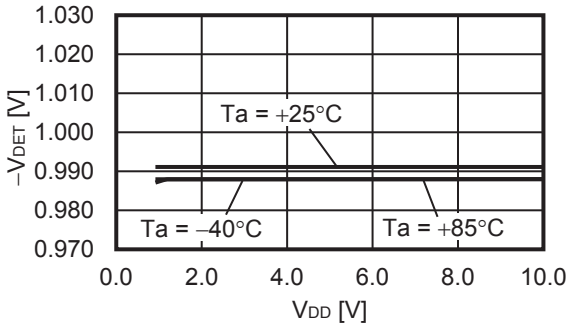


S-1004Cx50 V_{DD} = 5.0 V

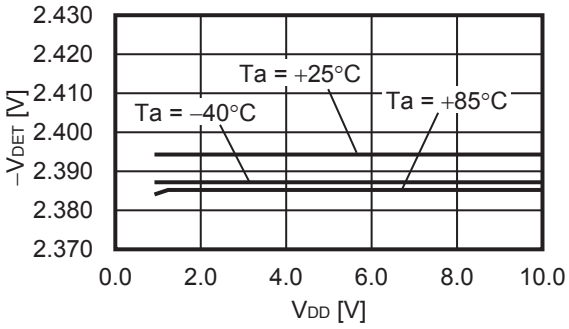


3. Detection voltage ($-V_{DET}$) vs. Power supply voltage (V_{DD})

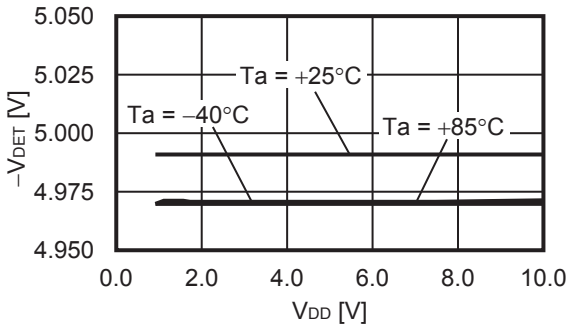
S-1004Cx10



S-1004Cx24

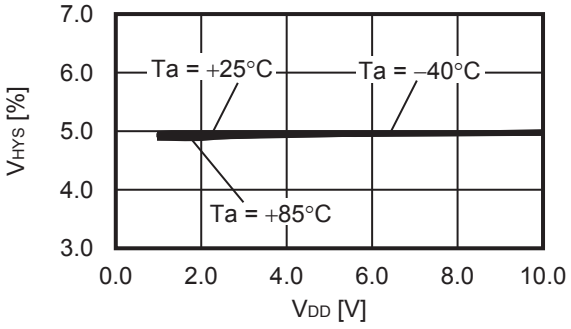


S-1004Cx50

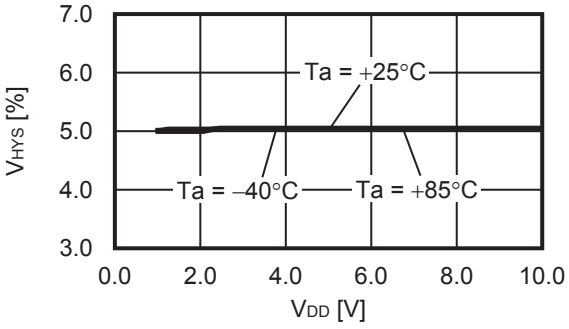


4. Hysteresis width (V_{HYS}) vs. Power supply voltage (V_{DD})

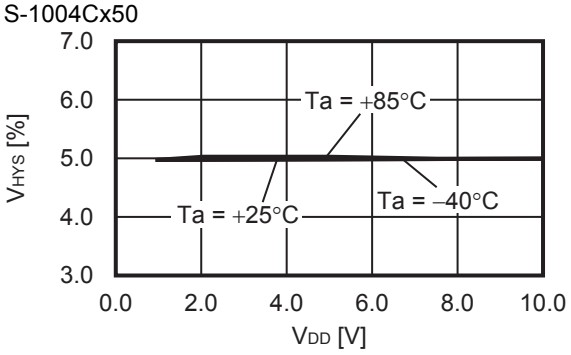
S-1004Cx10



S-1004Cx24

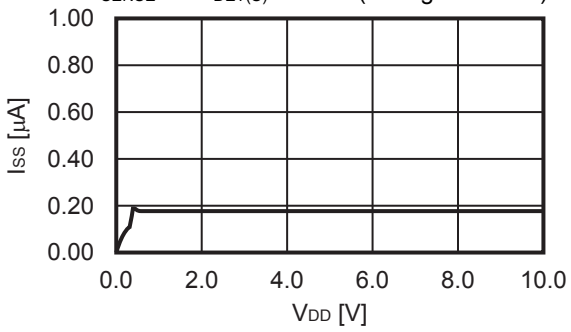


S-1004Cx50

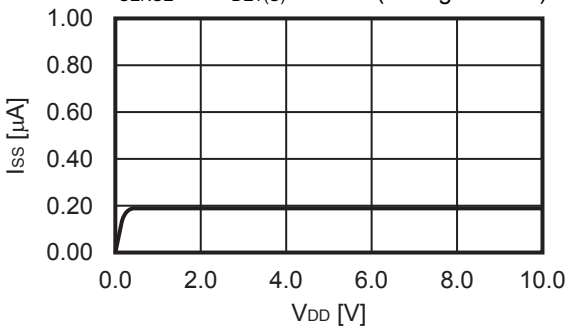


5. Current consumption (I_{SS}) vs. Power supply voltage (V_{DD})

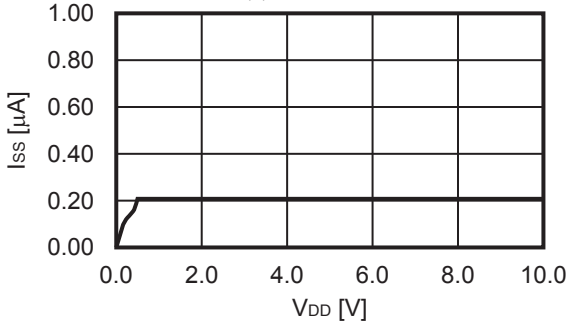
S-1004Cx10 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)



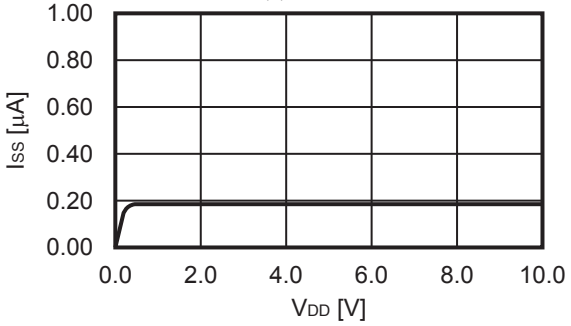
S-1004Cx10 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



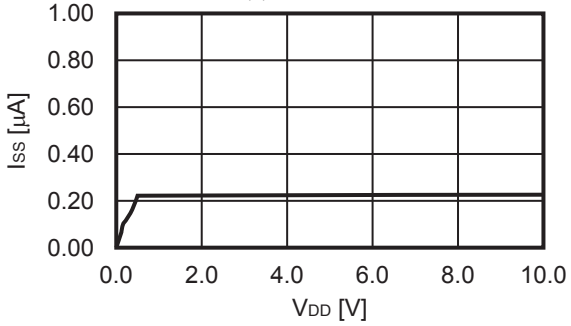
S-1004Cx24 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)



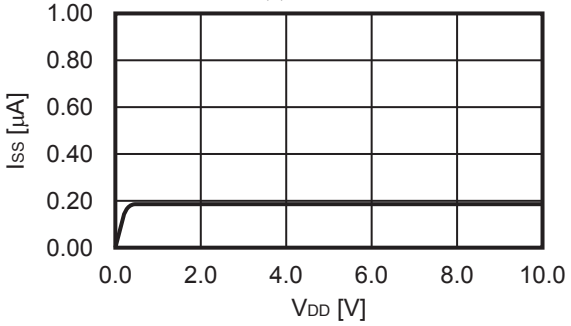
S-1004Cx24 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



S-1004Cx50 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)

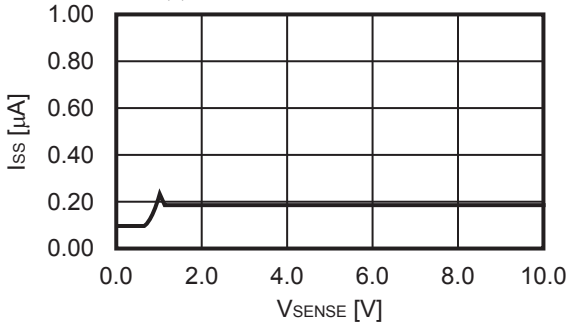


S-1004Cx50 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)

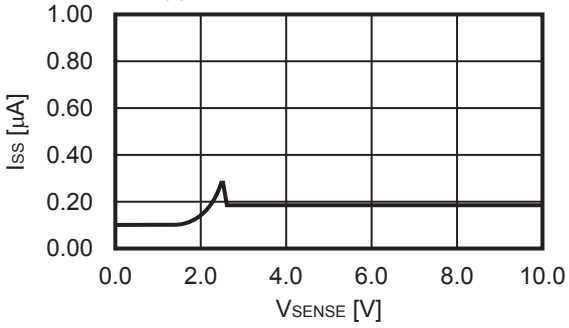


6. Current consumption (I_{SS}) vs. SENSE pin input voltage (V_{SENSE})

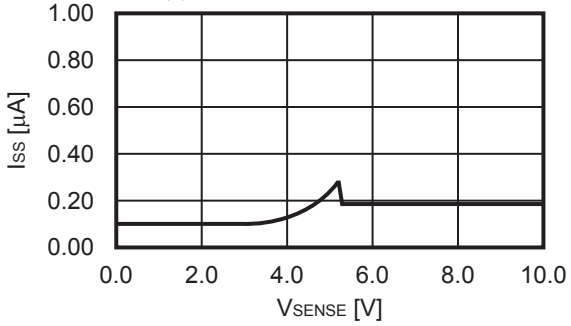
S-1004Cx10 Ta = +25°C,
$V_{DD} = -V_{DET(S)} + 1.0$ V, V_{SENSE} = 0.0 V → 10.0 V



S-1004Cx24 Ta = +25°C,
$V_{DD} = -V_{DET(S)} + 1.0$ V, V_{SENSE} = 0.0 V → 10.0 V

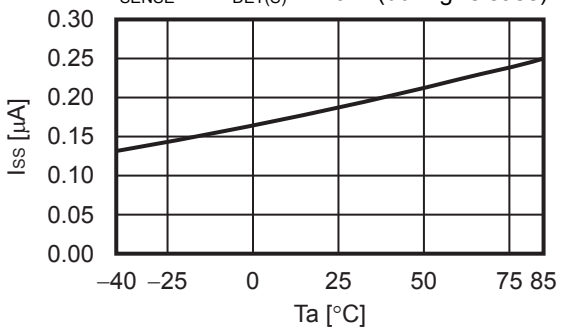


S-1004Cx50 Ta = +25°C,
$V_{DD} = -V_{DET(S)} + 1.0$ V, V_{SENSE} = 0.0 V → 10.0 V

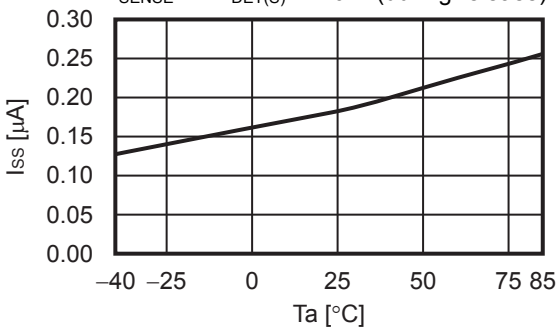


7. Current consumption (I_{SS}) vs. Temperature (Ta)

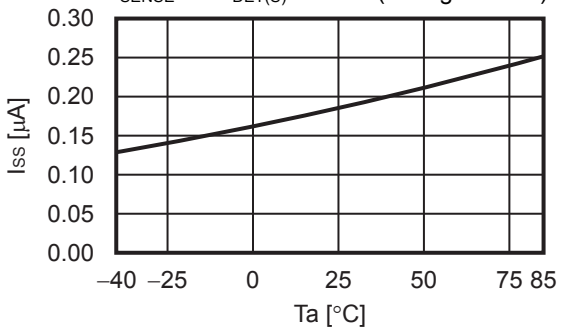
S-1004Cx10 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



S-1004Cx24 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)

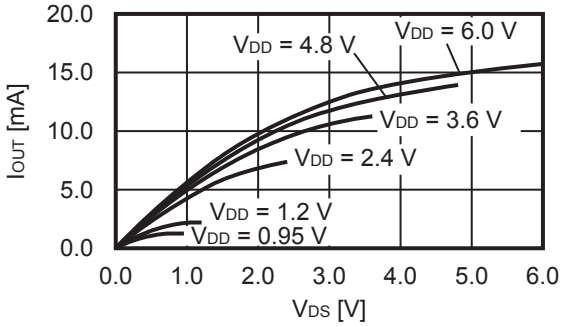


S-1004Cx50 $V_{DD} = -V_{DET(S)} + 1.0$ V,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



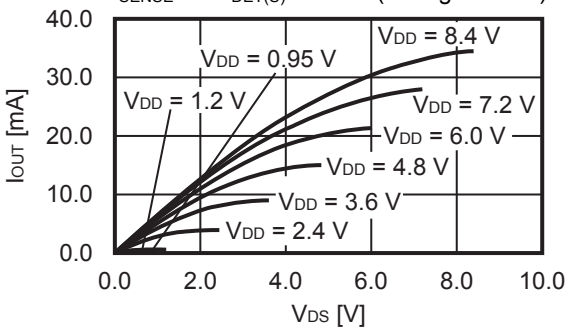
8. Nch transistor output current (I_{OUT}) vs. V_{DS}

S-1004Nx12 Ta = +25°C,
V_{SENSE} = 0.0 V (during detection)



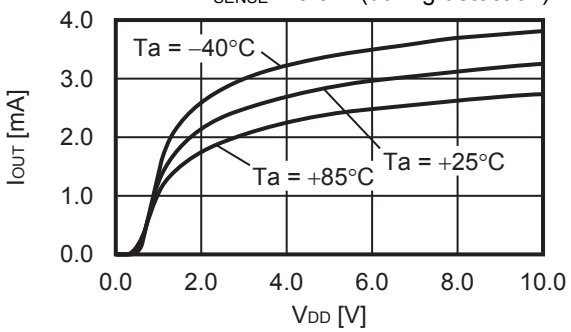
9. Pch transistor output current (I_{OUT}) vs. V_{DS}

S-1004Cx12 Ta = +25°C,
V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)



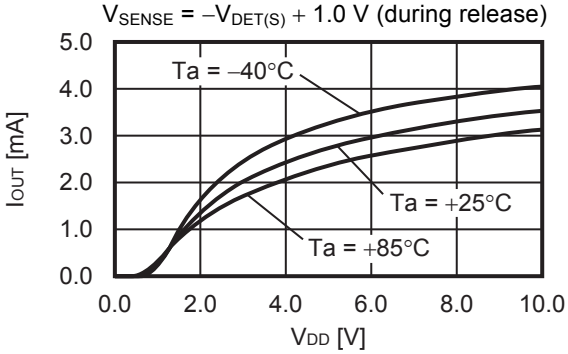
10. Nch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})

S-1004Nx12 V_{DS} = 0.5 V,
V_{SENSE} = 0.0 V (during detection)



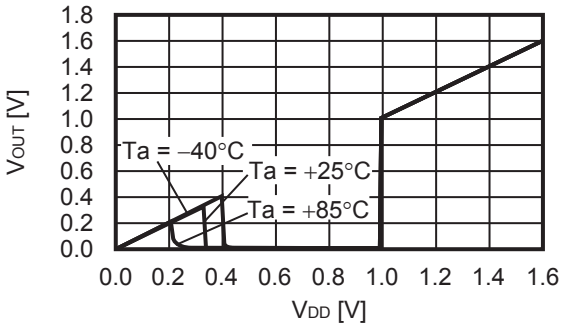
11. Pch transistor output current (I_{OUT}) vs. Power supply voltage (V_{DD})

S-1004Cx12 V_{DS} = 0.5 V,
V_{SENSE} = $-V_{DET(S)}$ + 1.0 V (during release)

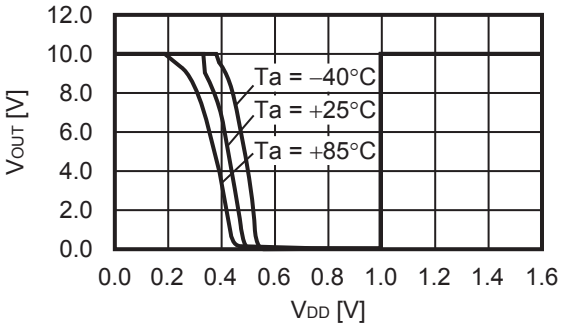


12. Minimum operation voltage (V_{OUT}) vs. Power supply voltage (V_{DD})

S-1004Nx10 V_{SENSE} = V_{DD},
Pull-up to V_{DD}, Pull-up resistance: 100 kΩ

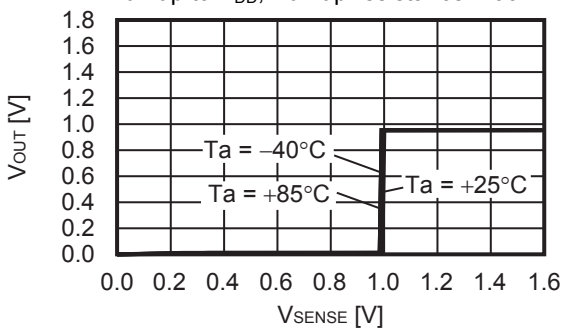


S-1004Nx10 V_{SENSE} = V_{DD},
Pull-up to 10 V, Pull-up resistance: 100 kΩ

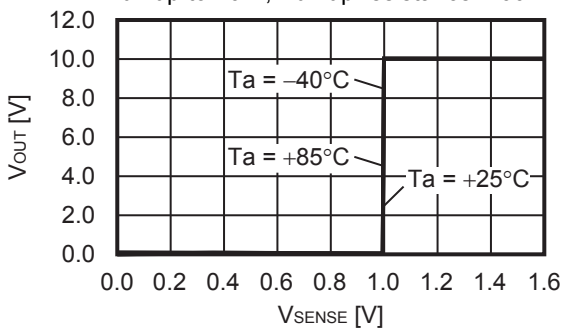


13. Minimum operation voltage (V_{OUT}) vs. SENSE pin input voltage (V_{SENSE})

S-1004Nx10 V_{DD} = 0.95 V,
Pull-up to V_{DD}, Pull-up resistance: 100 kΩ



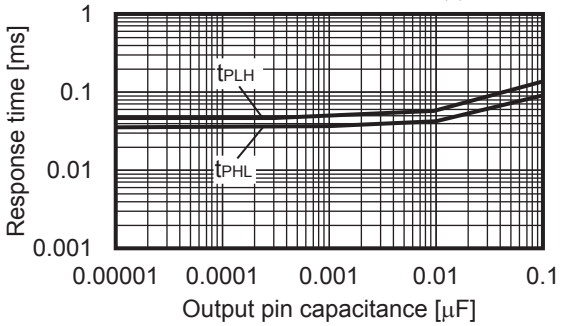
S-1004Nx10 V_{DD} = 0.95 V,
Pull-up to 10 V, Pull-up resistance: 100 kΩ



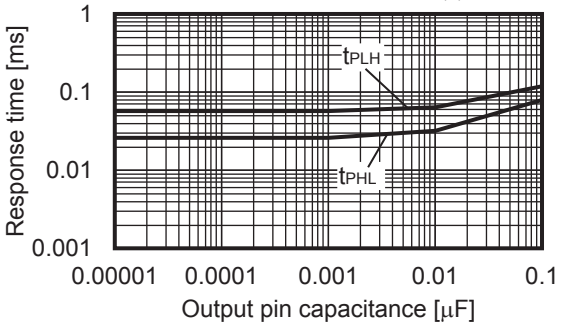
Remark V_{DS}: Drain-to-source voltage of the output transistor

14. Dynamic response vs. Output pin capacitance (C_{OUT}) (CD pin; open)

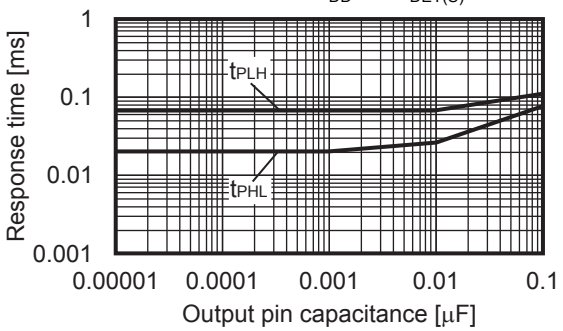
S-1004Cx10 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V



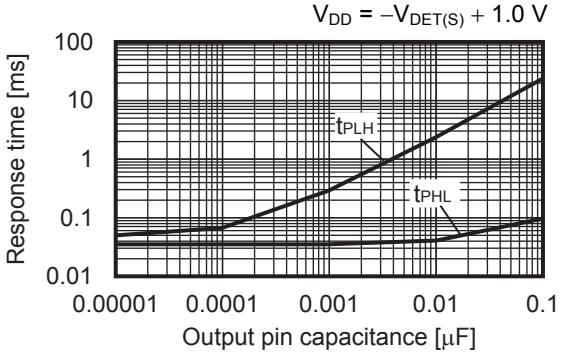
S-1004Cx24 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V



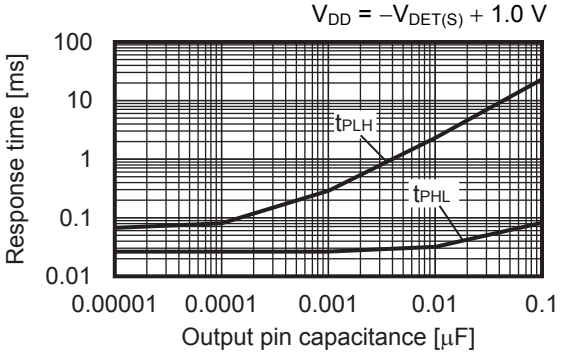
S-1004Cx50 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V



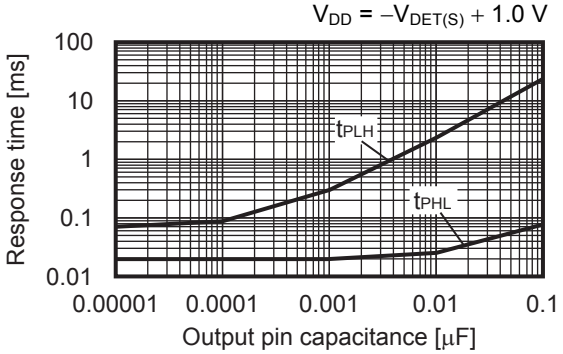
S-1004Nx10 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V

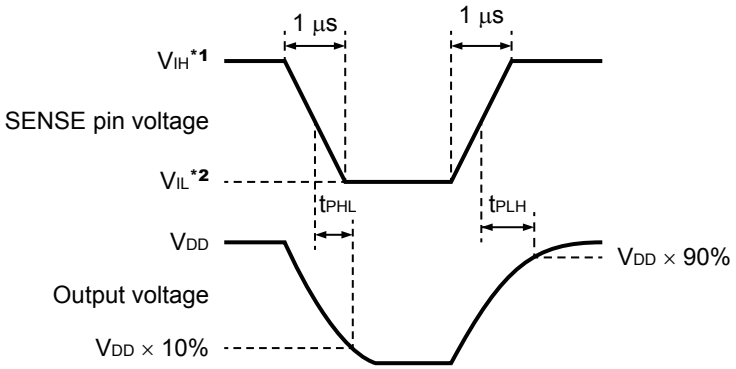


S-1004Nx24 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V



S-1004Nx50 Ta = +25°C, $V_{DD} = -V_{DET(S)} + 1.0$ V





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.95 V

Figure 33 Test Condition of Response Time

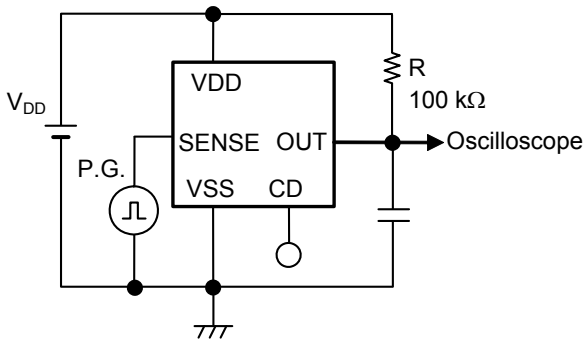


Figure 34 Test Circuit of Response Time (Nch open-drain output product)

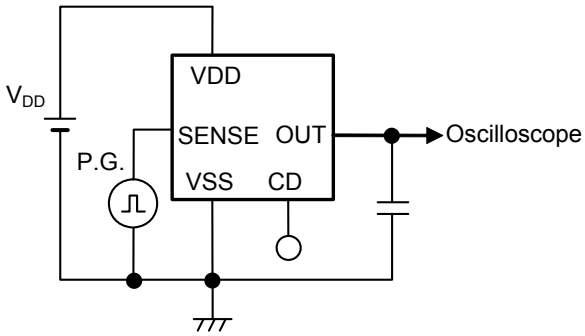
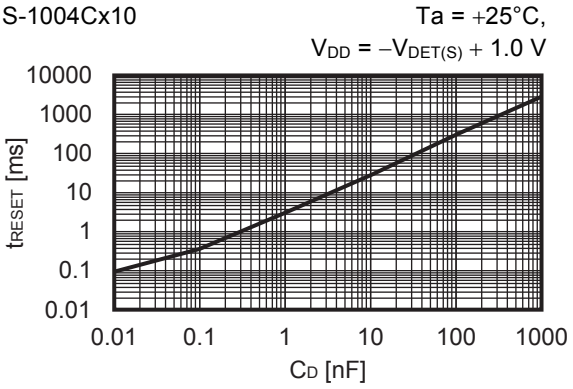


Figure 35 Test Circuit of Response Time (CMOS output product)

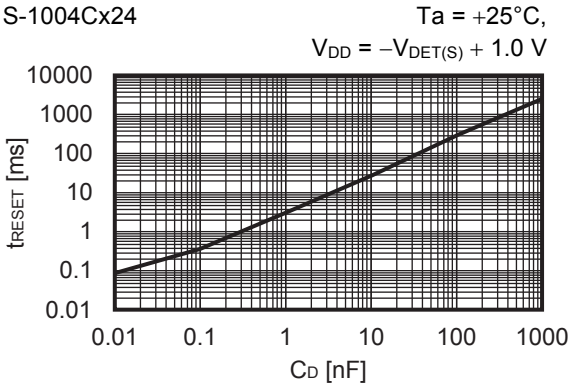
Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

15. Release delay time (t_{RESET}) vs. CD pin capacitance (C_D) (Without output pin capacitance)

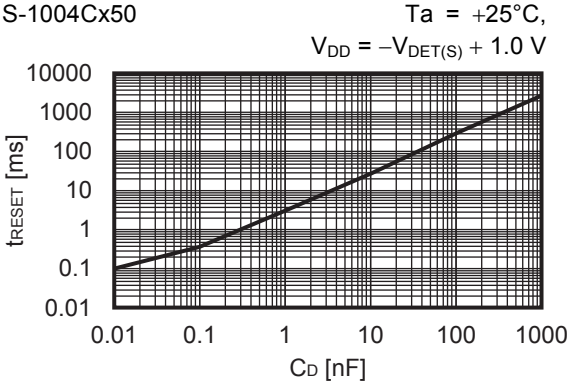
S-1004Cx10



S-1004Cx24

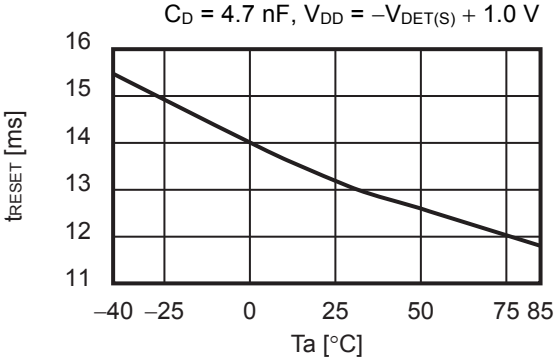


S-1004Cx50

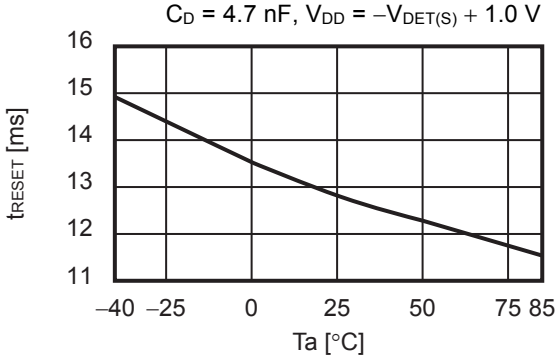


16. Release delay time (t_{RESET}) vs. Temperature (Ta)

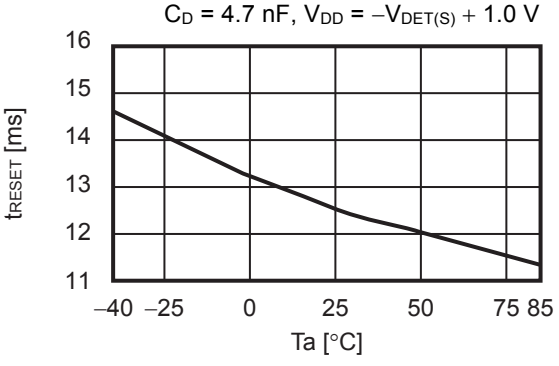
S-1004Cx10



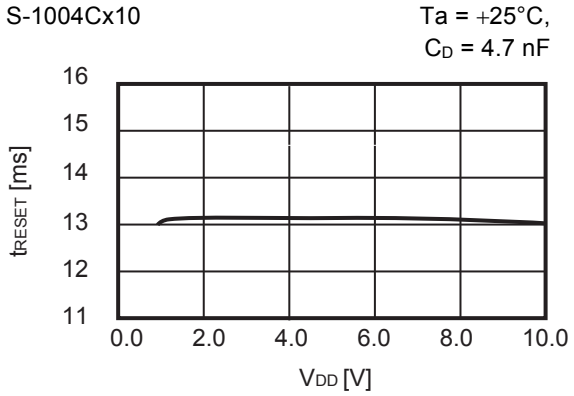
S-1004Cx24

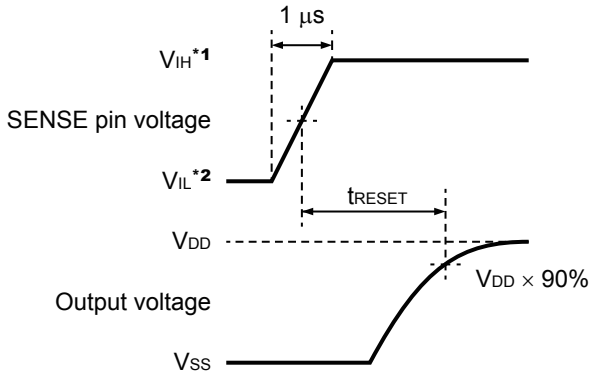


S-1004Cx50



17. Release delay time (t_{RESET}) vs. Power supply voltage (V_{DD})





***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.95 V

Figure 36 Test Condition of Release Delay Time

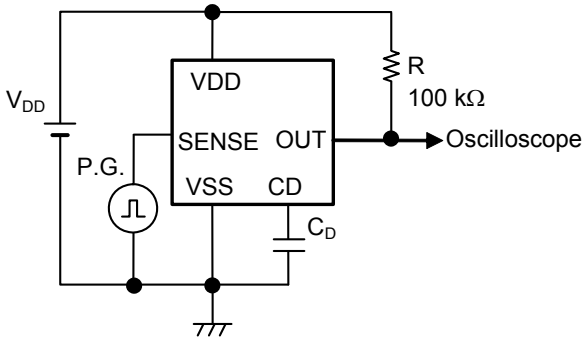


Figure 37 Test Circuit of Release Delay Time (Nch open-drain output product)

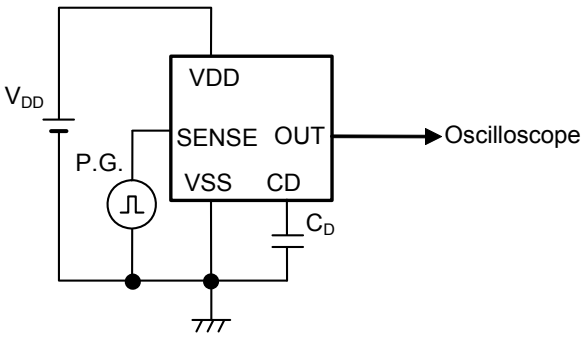


Figure 38 Test Circuit of Release Delay Time (CMOS output product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Application Circuit Examples

1. Microcomputer reset circuits

In microcomputers, when the power supply voltage is lower than the minimum operation voltage, an unspecified operation may be performed or the contents of the memory register may be lost. When power supply voltage returns to the normal level, the microcomputer needs to be initialized. Otherwise, the microcomputer may malfunction after that. Reset circuits to protect microcomputer in the event of current being momentarily switched off or lowered.
Using the S-1004 Series which has the low minimum operation voltage, the high-accuracy detection voltage and the hysteresis width, reset circuits can be easily constructed as seen in **Figure 39** and **Figure 40**.

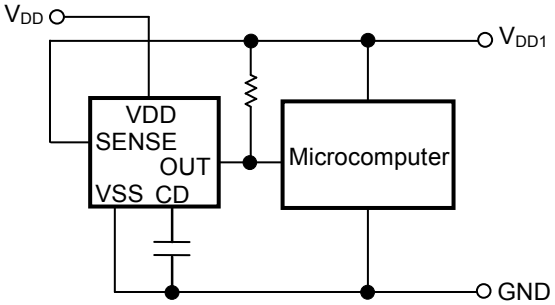


Figure 39 Example of Reset Circuit (Nch open-drain output product)

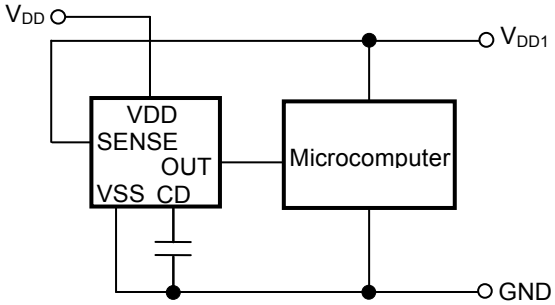


Figure 40 Example of Reset Circuit (CMOS output product)

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

2. Change of detection voltage

If there is not a product with a specified detection voltage value in the S-1004 Series, the detection voltage can be changed by using a resistance divider or a diode, as seen in **Figure 41** to **Figure 44**.
In **Figure 41** and **Figure 42**, hysteresis width also changes.

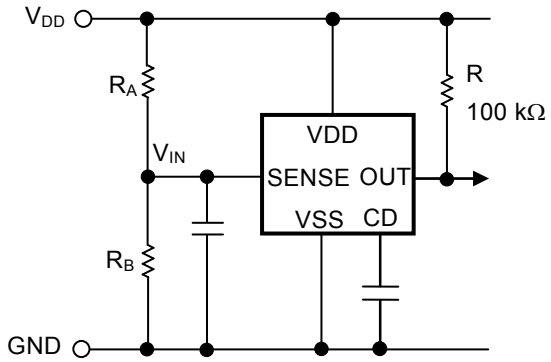


Figure 41 Detection voltage change when using a resistance divider (Nch open-drain output product)

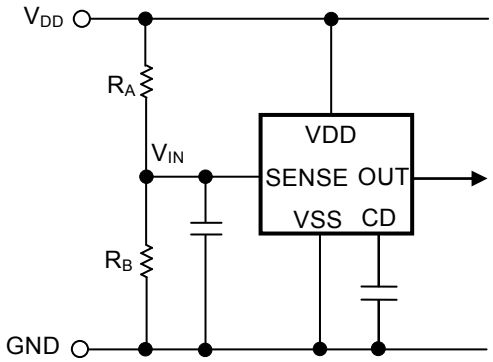


Figure 42 Detection voltage change when using a resistance divider (CMOS output product)

Remark Detection voltage = $\frac{R_A + R_B}{R_B} \bullet -V_{DET}$

Hysteresis width = $\frac{R_A + R_B}{R_B} \bullet V_{HYS}$

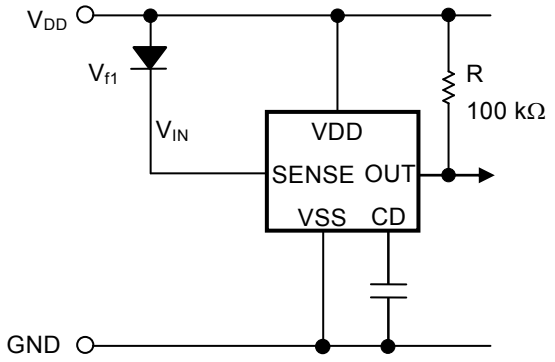


Figure 43 Detection voltage change when using a diode (Nch open-drain output product)

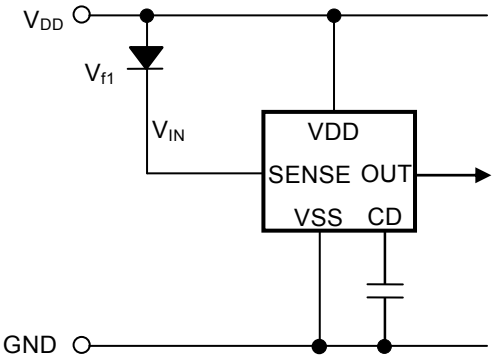
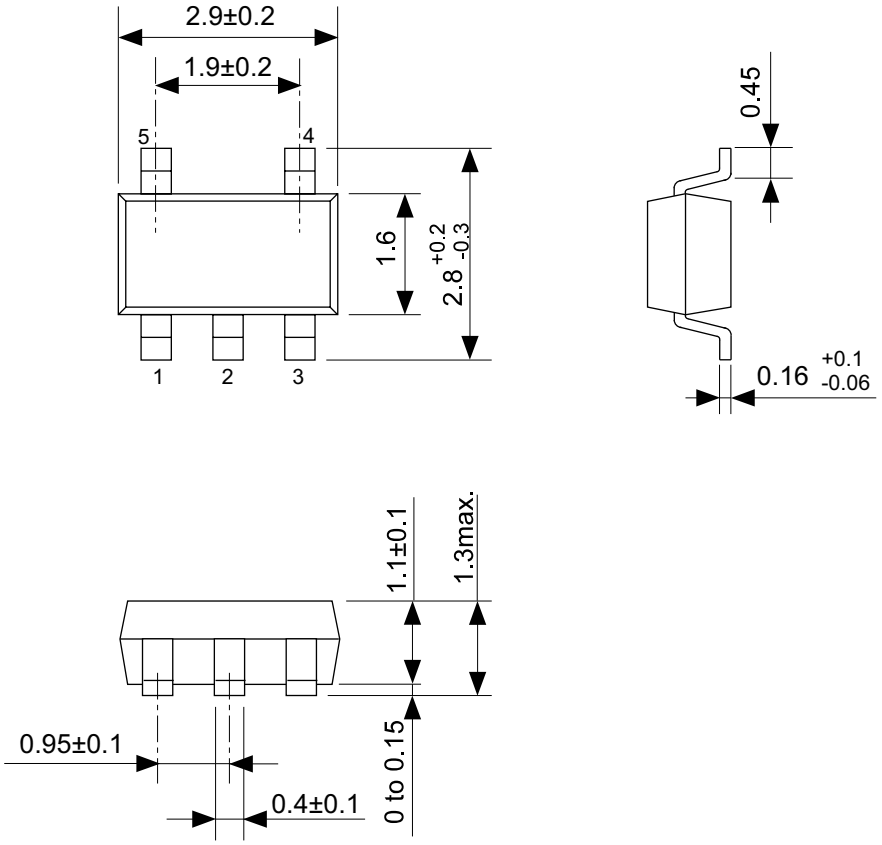


Figure 44 Detection voltage change when using a diode (CMOS output product)

Remark Detection voltage = $V_{f1} + (-V_{DET})$

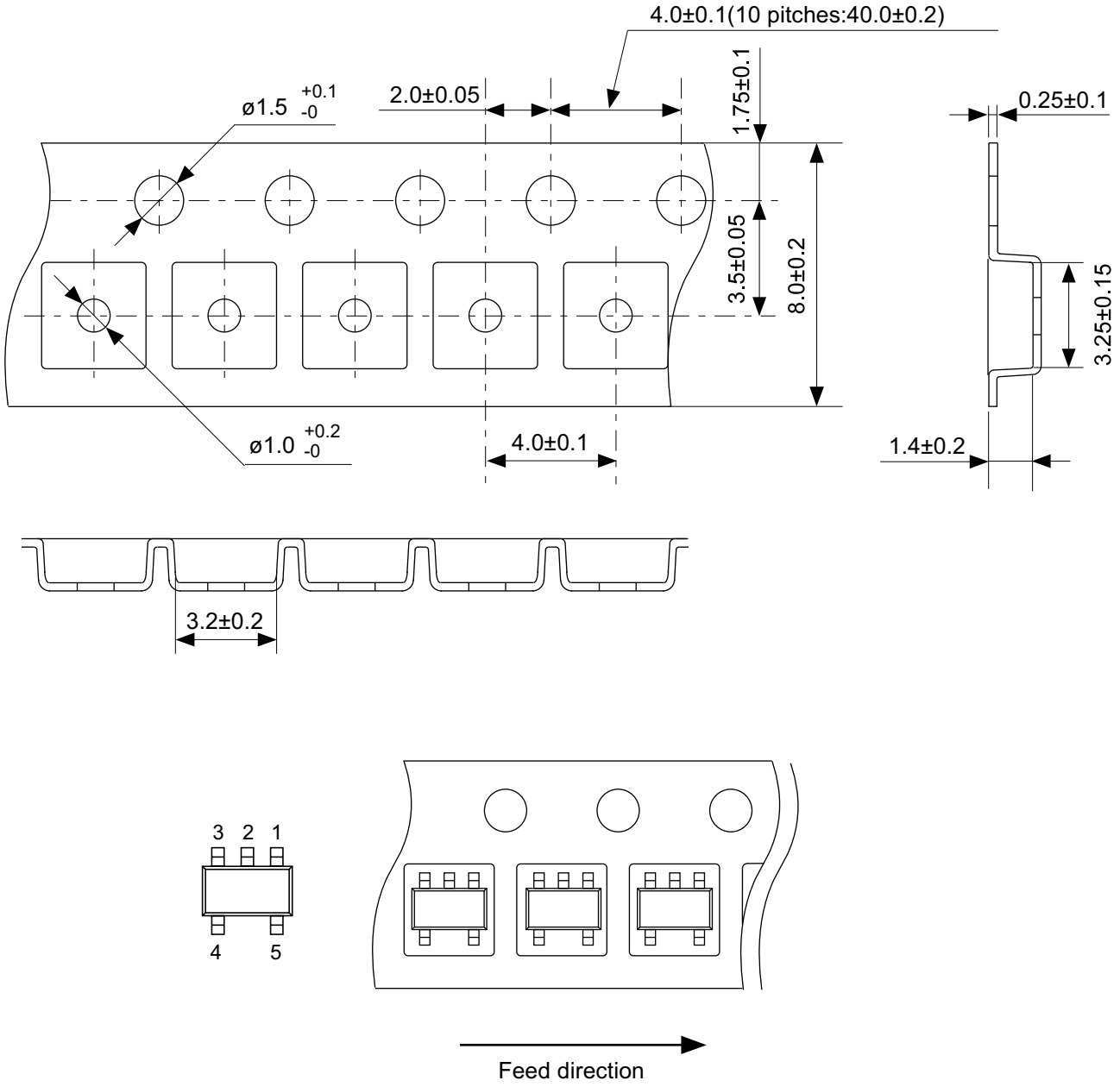
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. Set the constants referring to "2. 1 Error when detection voltage is set externally" in "■ Operation".



No. MP005-A-P-SD-1.3

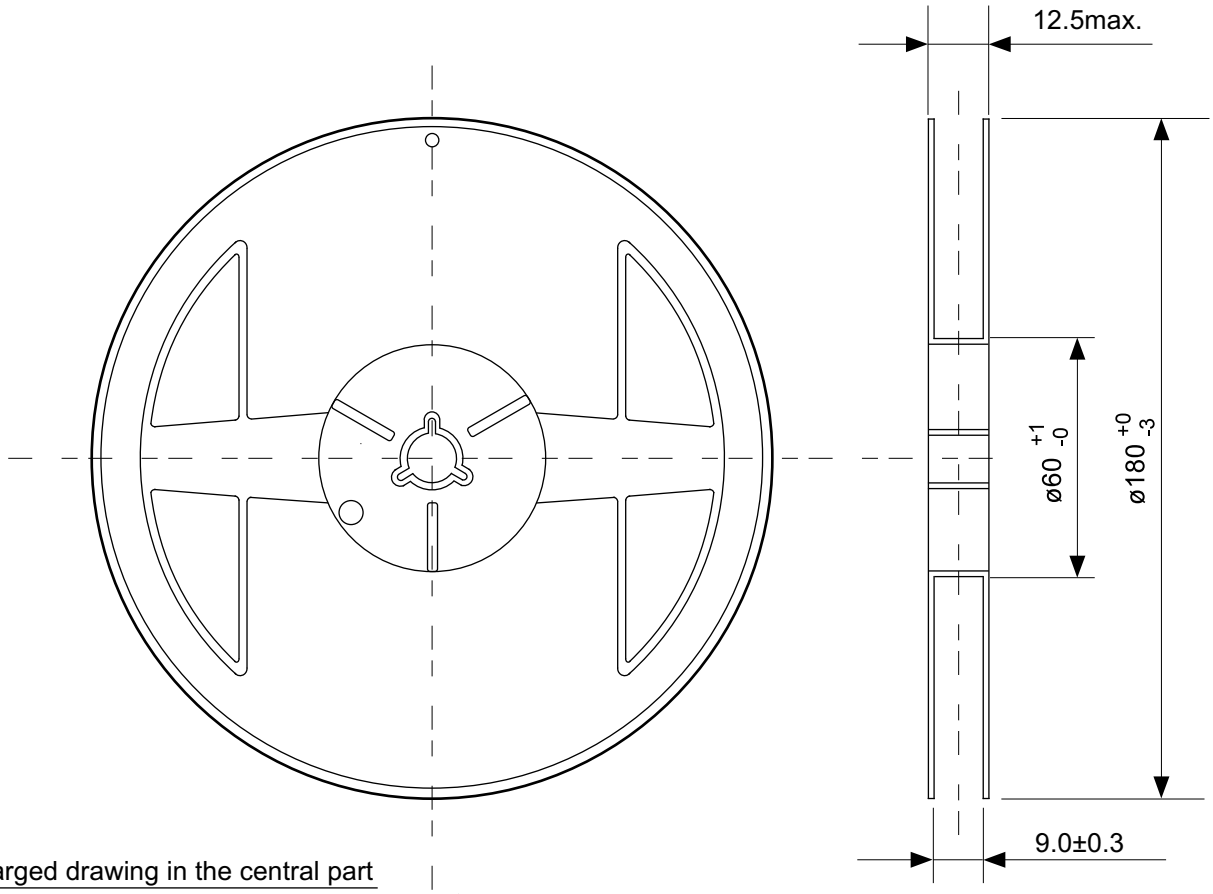
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

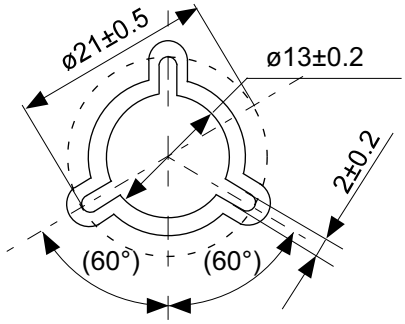


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

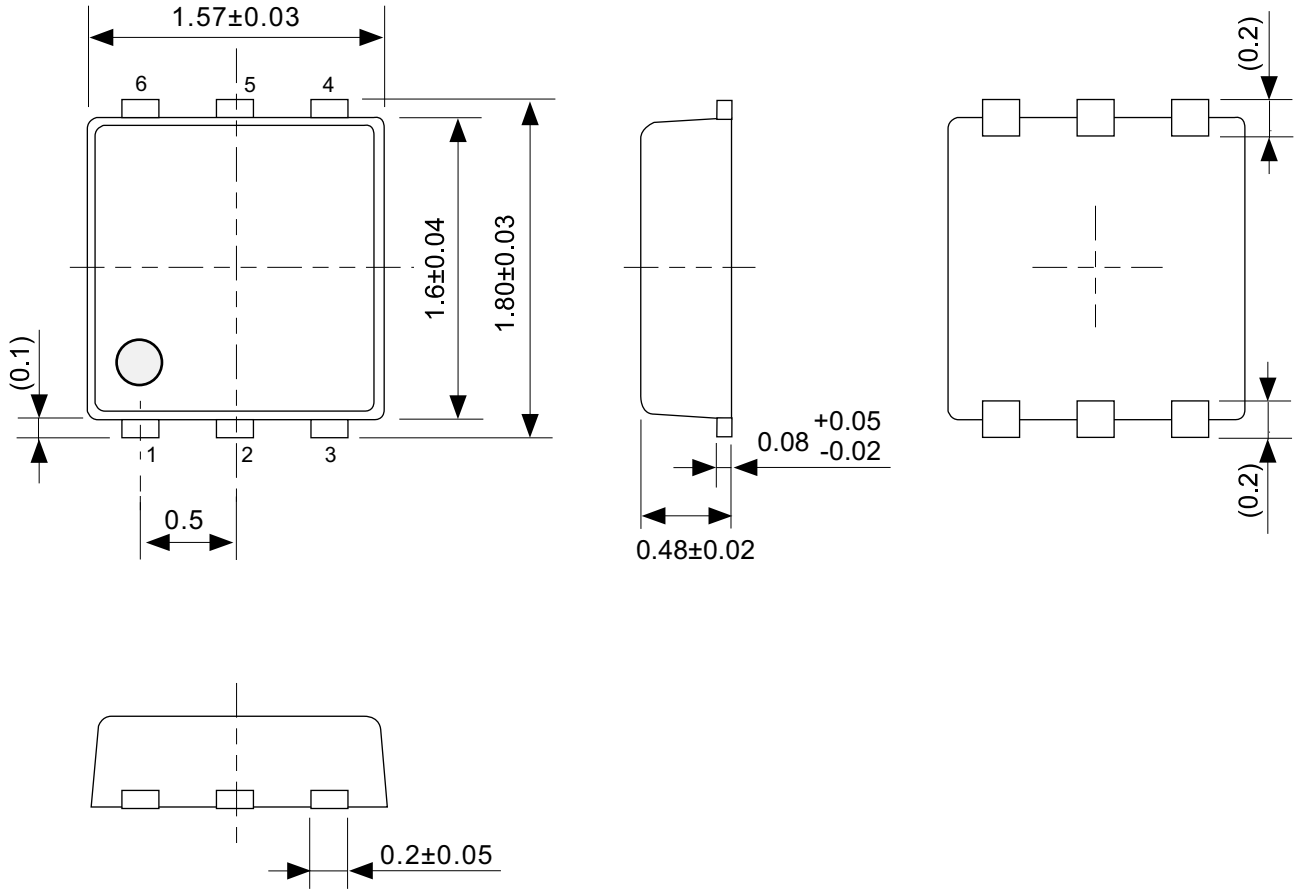


Enlarged drawing in the central part



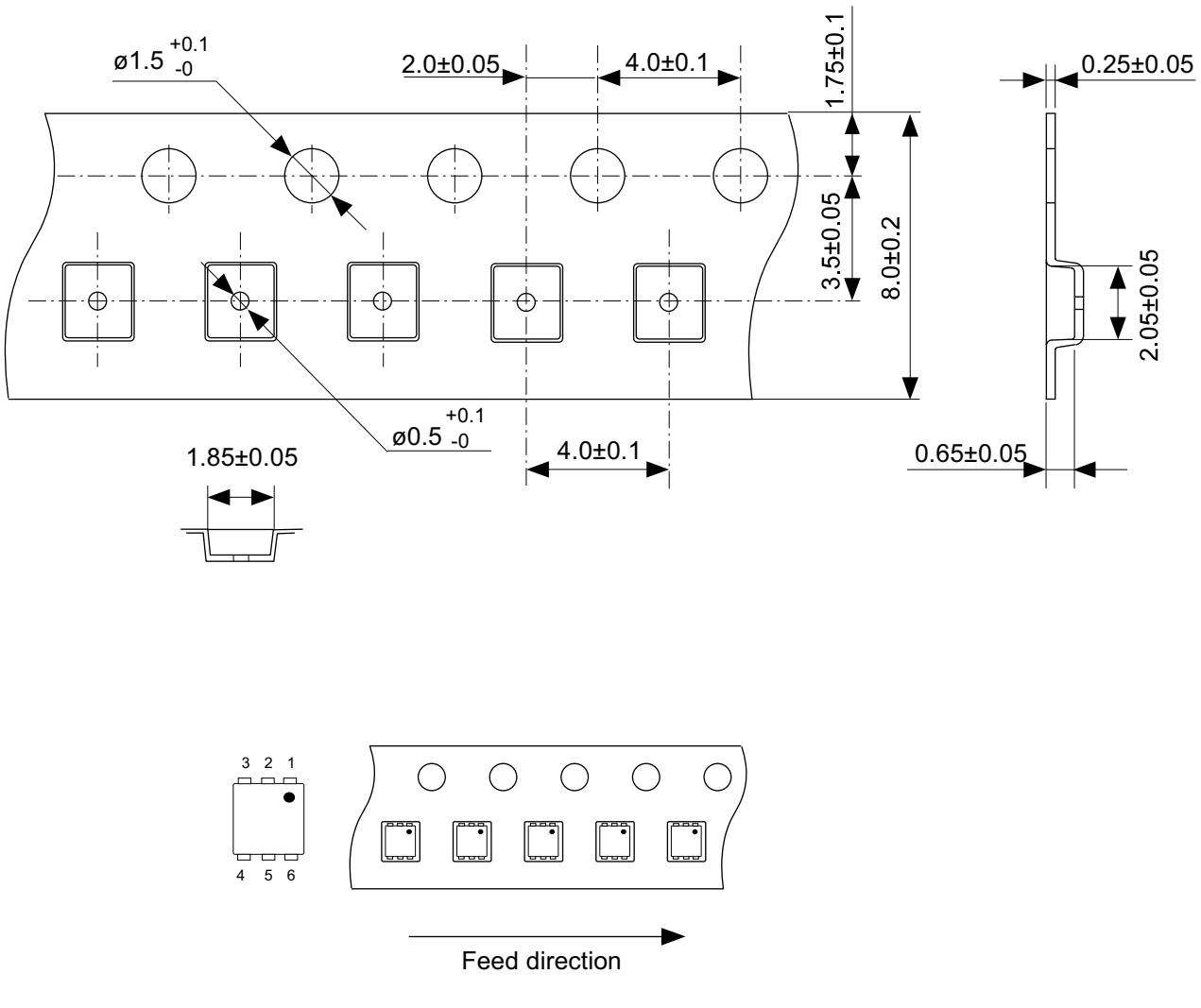
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



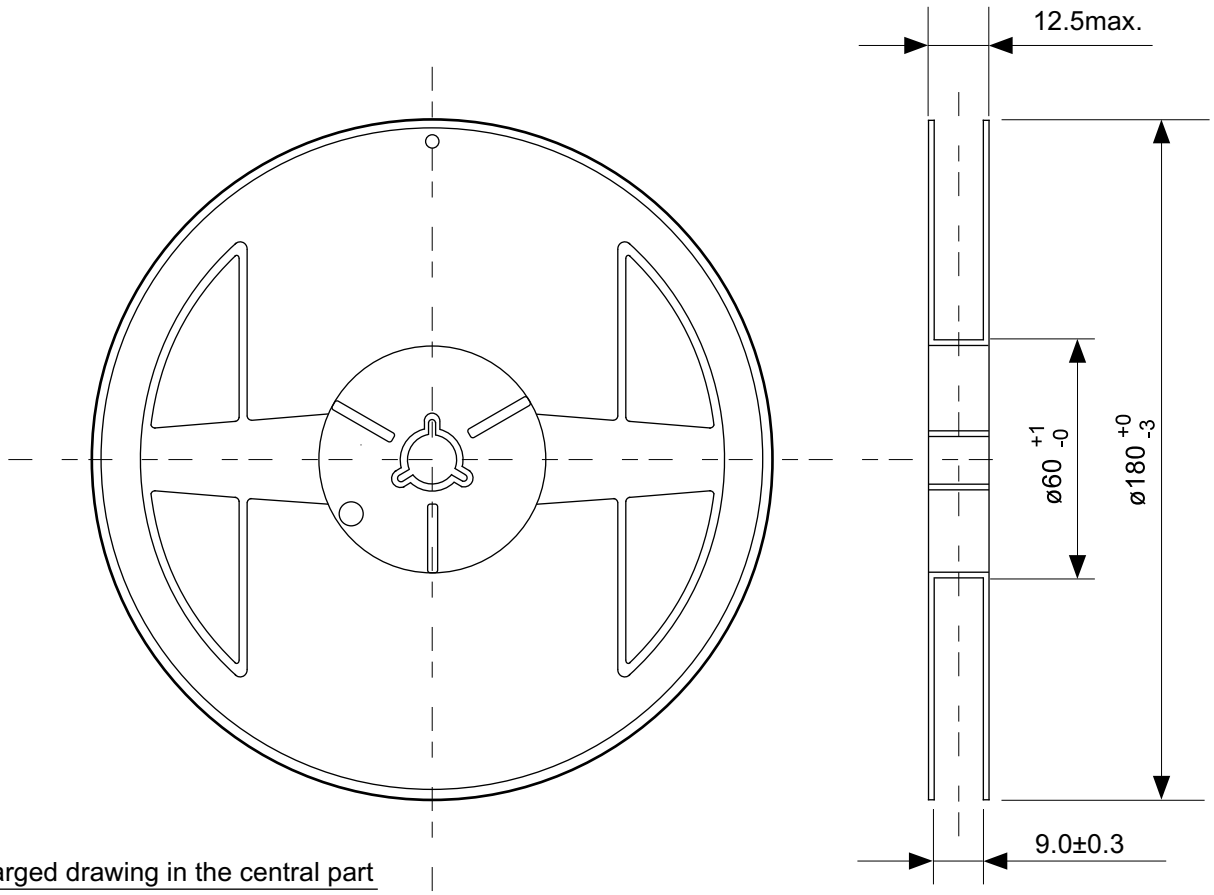
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

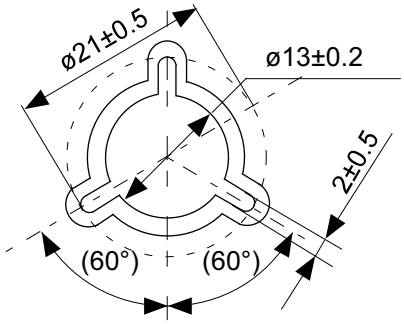


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

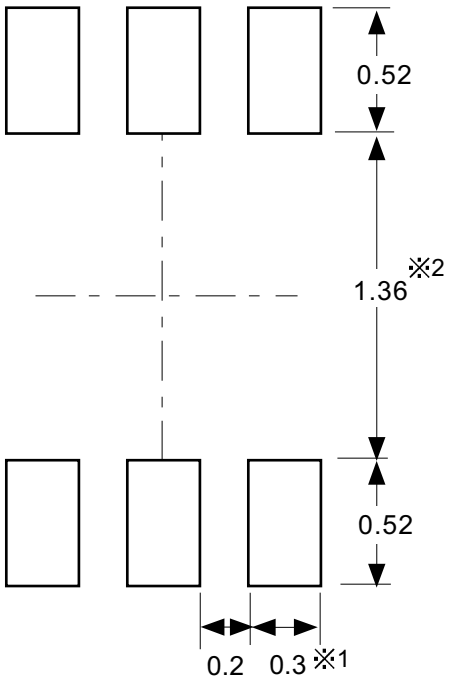


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的[illegible] (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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