NXP Semiconductors
Data Sheet: Technical Data

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S32R274

S32R274/S32R264 Series Data Sheet

Supports S32R274K, S32R274J, S32R264K and S32R264J

Features

- On-chip modules available within the device include the following features:
- Safety core: Power Architecture® e200Z4 32-bit CPU with checker core
- Dual issue computation cores: Power Architecture® e200Z7 32-bit CPU
- 2 MB on-chip code flash (FMC flash) with ECC
- 1.5 MB on-chip SRAM with ECC
- RADAR processing
  - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
  - Cross Timing Engine (CTE) for precise timing generation and triggering
  - Waveform generation module (WGM) for chirp ramp generation
  - 4x 12-bit ΣΔ-ADC with 10 MSps
  - One DAC with 10 MSps
  - MIPICSI2 interface to connect external ADCs
- Memory Protection
  - Each core memory protection unit provides 24 entries
  - Data and instruction bus system memory protection unit (SMPU) with 16 region descriptors each
  - Register protection
- Clock Generation
  - 40 MHz external crystal (XOSC)
  - 16 MHz Internal oscillator (IRCOSC)
  - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
  - Low-jitter PLL to ΣΔ-ADC and DAC clock generation (not supported on SC66760x devices)
- Functional Safety
  - Enables up to ASIL-D applications
  - FCCU for fault collection and fault handling
  - MEMU for memory error management
  - Safe eDMA controller
  - Self-Test Control Unit (STCU2)
  - Error Injection Module (EIM)
  - On-chip voltage monitoring
  - Clock Monitor Unit (CMU)
- Security
  - Cryptographic Security Engine (CSE2)
  - Supports censorship and life-cycle management
- Timers
  - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
  - Three System Timer Module (STM)
  - Three Software Watchdog Timers (SWT)
  - Two eTimer modules with 6 channels each
  - One FlexPWM module for 12 PWM signals
- Communication Interfaces
  - Two Serial Peripheral interface (SPI) modules
  - One LINFlexD module
  - Two inter-IC communication interface (I2C) modules
  - One dual-channel FlexRay module with 128 message buffers
  - Three FlexCAN modules with configurable buffers - CAN FD optionally supported on 2 FlexCAN modules
  - One ENET MAC supporting MII/RMII/RGMII interface
  - ZipWire high-speed serial communication
- Debug Functionality
  - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
  - e200Z7 core and e200Z4 core: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Two analog-to-digital converters (SAR ADC)
  - Each ADC supports up to 16 input channels
  - Cross Trigger Unit (CTU)
- On-chip voltage DC/DC regulator for core clock (VREG)
- Two Temperature Sensors (TSENS)

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1 Introduction

1.1 Family comparison

The following table provides a comparison of the devices: S32R274, S32R264, and MPC5775K . This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

Table 1. S32R274 and S32R264 Family Comparison

Feature	S32R274K	S32R274J	S32R264K	S32R264J	MPC5775K
CPUs	e200z420 lock-step 2x e200z7260				
SIMD	SPE2 + EFP2 (z7)				
Maximum Operating Frequency	240 MHz (z7 cores) / 180 MHz (z4)	266 MHz (z7 cores) / 133 MHz (z4)	240 MHz (z7 cores) / 180 MHz (z4)	266 MHz (z7 cores) / 133 MHz (z4)	266 MHz (z7 cores) / 133 MHz (z4)
Flash	2 MB with ECC				4 MB with ECC
EEPROM support	64 KB (emulation)				96 KB (emulation)
RAM	1.5 MB with ECC				
ECC	end-to-end				
MPU	Core MPU: 24 entries per core, System MPU: 2x16 entries				
eDMA	safe eDMA with 32 channels, 64 triggers				
Control ADC	2x 12-bit SAR ADC, 1 MSps input mux for 16 external channels				4x 12-bit SAR ADC, 1 MSps, input mux for 37 external channels
SD-ADC	4 channels, 10 MSps		–	–	8 channels, 10 MSps
SPT	1x				
CTE	1x				
WGM	1x				
CTU	1x				2x
SWT	3x				
STM	3x				
PIT	2x				
CRC	2x				
SEMA42	1x				
LINFlexD	1x				4x
CAN	3x FlexCAN including 2x FlexCAN-FD				4x FlexCAN + 1x MCAN-FD

Table continues on the next page...

Table 1. S32R274 and S32R264 Family Comparison (continued)

Feature	S32R274K	S32R274J	S32R264K	S32R264J	MPC5775K
SPI	2x				4x
I^2C	2x				3x
Zipwire	1x LFAST+SIPI, 320 MHz				
FlexRay	1x dual channel				
Ethernet	10/100 and >100 Mbps, RMII/MII/RGMII I/F, AVB support				10/100 Mbps, RMII/MII I/F, AVB support
FlexPWM	1x, 12 PWM channels				2x, 12 PWM channels each
eTimer	2x, 6 channels each				3x, 6 channels each
External ADC interface	1x 4 lanes MIPICSI2 Rx, 1 Gbps/lane				1x PDI (16-bit data, clock, sync)
IRCOSC	16 MHz				
XOSC	40 MHz				
FMPLL	dual system PLL, 1x FM modulated				
DAC	1x 12-bit 10 MSps		–[1]	–[1]	1x 12-bit 2 MSps
SIUL2	1x				
BAM	1x				
INTC	1x				
SSCM	1x				
FCCU/FOSU	1x				
MEMU	1x				
STCU2	1x				
CSE	1x				-
PASS/TDM	1x				-
MC_ME	1x				
MC_CGM	1x				
MC_RGM	1x				
TSENS	2x				
Debug	JTAGC, JTAGM, CJTAG, with class3+ Nexus, Aurora only				
Safety level	ISO26262 SEooC ASIL-B to ASIL-D				
Temp. range (Tj)	-40 to 150˚C				

1. DAC is not supported in S32R264x devices. Hence, ignore its occurrences in this document for S32R264K and S32R264J.

1.2 Feature list

On-chip modules available within the device include the following features:

- Safety core: Power Architecture® e200Z4 32-bit CPU with checker core

    - 2 cycle delayed lockstep
    - Harvard architecture with 64-bit bus for data and instructions
    - Dual issue: up to two instructions per clock cycle
    - 8 KB instruction cache and 4 KB data cache
    - 64 KB data local memory
        - with background load/store: backdoor access
        - 0-wait state for all read and 32/64-bit write accesses
        - Low number of wait states for backdoor accesses
    - Support for decorated storage
    - Variable Length Encoding (VLE) compliant for higher code density
    - Single precision floating point operations
- Computation cores: Power Architecture® e200Z7 32-bit CPU
    - Dual issue: up to two instructions per clock cycle
    - Harvard architecture with 64-bit bus for data instructions
    - 16 KB instruction cache and 16 KB data cache
    - 64 KB data local memory
        - with background load/store: backdoor access
        - 0-wait state for all read and 32/64-bit write accesses
        - Low number of wait states for backdoor accesses
    - Support for decorated storage
    - Using variable length encoding (VLE) for higher code density
    - 4-way integer processing unit (SPE2)
    - 2-way single-precision Floating Point Unit (EFPU2)
- 2 MB on-chip code flash (FMC flash) with ECC
    - Three ports (one per CPU) shared between code and data flash with 4 × 256 bit buffer for code and data flash including prefetch functions
    - Data flash is part of the code flash module
    - Including 64 KB EEPROM emulation
- 1.5 MB on-chip SRAM with ECC
    - Decorated memory controller to support atomic read-modify-write operations
    - Single- and double-bit error visibility is supported
    - Up to four ports (one per CPU and SPT) and up to 8 banks allow simultaneous accesses from different masters to different banks
- RADAR processing
    - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
    - Cross Timing Engine (CTE) for precise timing generation and triggering
    - Waveform generation module (WGM) for chirp ramp generation
    - 4x 12-bit ΣΔ-ADC with 10 MSps (not supported on S32R264 devices)
    - One DAC with 10 MSps (not supported on S32R264 devices)
    - MIPICSI2 interface to connect external ADCs

    - Four data lanes, with up to 1 Gbps per lane and in total
    - One clock lane
- Memory Protection
    - Each core memory protection unit provides 24 entries
    - Data and instruction bus system memory protection Unit (SMPU) with 16 region descriptors each
    - Register protection
- Clock Generation
    - 40 MHz external crystal (XOSC)
    - 16 MHz Internal oscillator (IRCOSC)
    - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
    - Low-jitter PLL to ΣΔ-ADC and DAC clock generation
- Functional Safety
    - Enables up to ASIL-D applications
    - End to end ECC ensuring full protection of all data accesses throughout the system, from each of the systems masters through the crossbar and into the memories and peripherals
    - FCCU for fault collection and fault handling
    - MEMU for memory error management
    - Safe eDMA controller
    - User selectable Memory BIST (MBIST) can be enabled to run out of various reset conditions or during runtime
    - Self-Test Control Unit (STCU2)
    - Error Injection Module (EIM)
    - On-chip voltage monitoring
    - Clock Monitor Unit (CMU) to support monitoring of critical clocks
- Security
    - Cryptographic Security Engine (CSE2) enabling advanced security management
    - Supports censorship and life-cycle management via Password and Device Security (PASS) module
    - Diary control for tamper detection (TDM)
- Support Modules
    - Global Interrupt controller (INTC) capable of routing interrupts to any CPU
    - Semaphore unit to manage access to shared resources
    - Two CRC computation units with four polynomials
    - 32-channel eDMA controller with multiple transfer request sources using DMAMUX
    - Boot Assist Module (BAM) supports internal flash programming via a serial link (LIN / CAN)
- Timers
    - Two Periodic Interval Timers (PIT) with 32-bit counter resolution

    - Three System Timer Module (STM)
    - Three Software Watchdog Timers (SWT)
    - Two eTimer modules with 6 channels each
    - One FlexPWM module for 12 PWM signals
- Communication Interfaces
    - Two Serial Peripheral interface (SPI) module
    - Two inter-IC communication interface (I2C) modules
    - One LINFlexD module
    - One dual-channel FlexRay module with 128 message buffers
    - Three FlexCAN modules with configurable buffers
        - CAN FD optionally supported on 2 FlexCAN modules
    - One ENET MAC supporting MII/RMII/RGMII interface
        - Supports 10/100 Mbps (MII/RMII/RGMII) and >100 Mbps (RGMII)
        - Supports IEEE1588 timestamps and PTP
    - Zipwire high-speed serial communication
        - Supports LFAST and SIPI protocol
        - Fast interprocessor communication with 320 Mbps gross data rate
        - DMA based access to memory resources
- Debug Functionality
    - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
    - e200Z7 core and e200Z4 core: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+
    - All platform bus masters except CSE can be monitored via Nexus/Aurora
    - Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) (IEEE 1149.1) and 1149.7 (cJTAG)
    - On-chip control for Nexus development interface by JTAGM module
- Two analog-to-digital converters (SAR ADC)
    - Each ADC supports up to 16 input channels
    - Cross Trigger Unit to enable synchronization of ADC conversions with eTimer
- On-chip voltage DC/DC regulator for core clock (VREG)
- Two Temperature Sensors (TSENS)

S32R264 feature changes with respect to S32R274 are as follows:

- SD-ADC’s removed
- DAC removed
- SDPLL replaced with AFEPLL
- Improved radiated emissions in the GLONASS band. Full EMC reports are available from NXP on request for both S32R264, and S32R274 to allow the customer to select the most suitable part for their usecase.

1.3 Block diagram

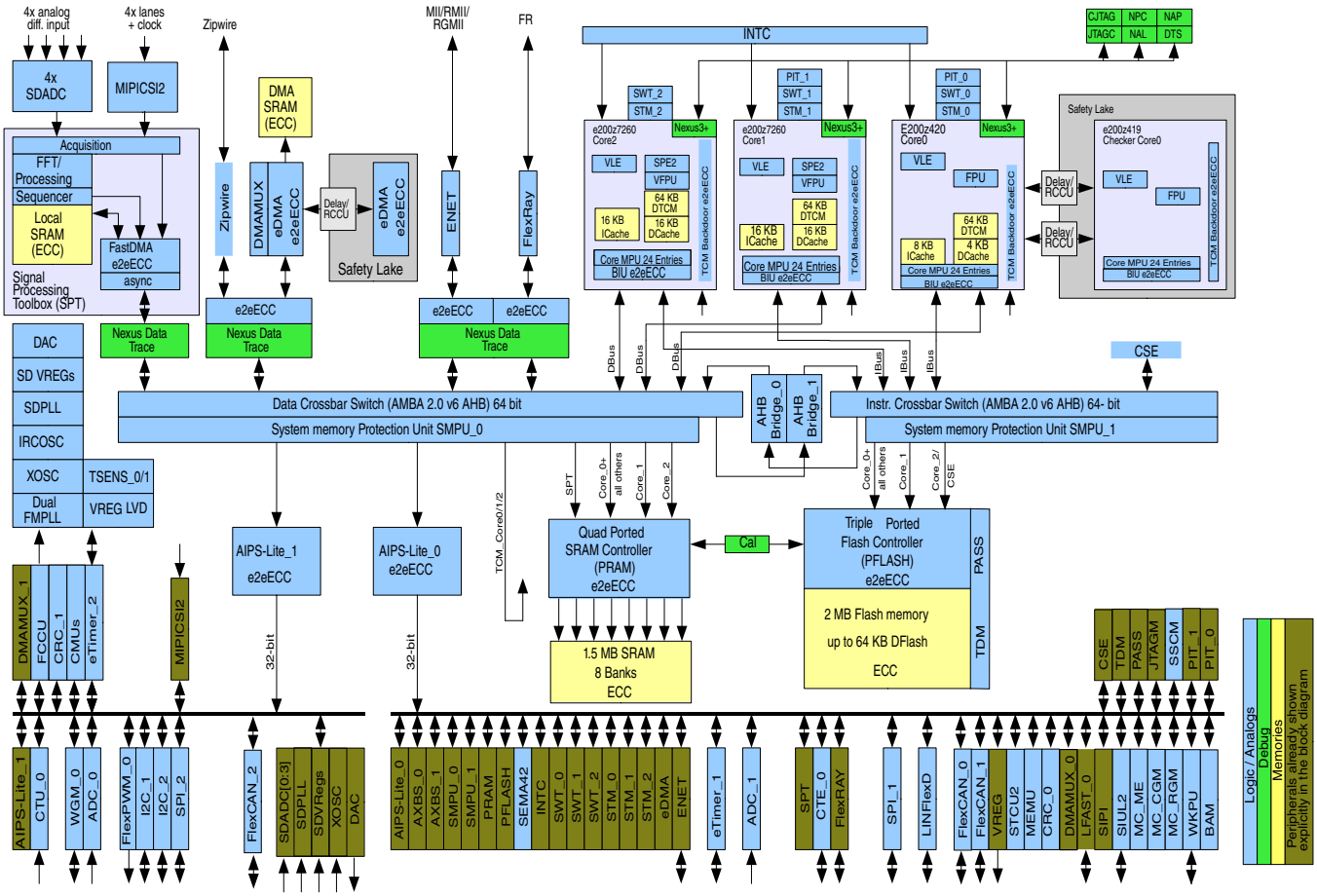


Figure 1. S32R274 block diagram

NOTE

S32R264 devices support AFE PLL while S32R274 devices support SDPLL.

2 Ordering parts

2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the device number.

3 Part identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Fields

This section lists the possible values for each field in the part number (not all combinations are valid):

Table 2. Configuration

257MAPBGA	Configuration	Performance	Temperature
FS32R274KSK2MMM	S	K	M
FS32R274KCK2MMM	C	K	M
FS32R274VBK2MMM	B	V	M
FS32R274VCK2MMM	C	V	M
FS32R274KSK2VMM	S	K	V
FS32R274KCK2VMM	C	K	V
FS32R274VBK2VMM	B	V	V
FS32R274VCK2VMM	C	V	V
FS32R274JSK2MMM	S	J	M
FS32R264KBK0MMM	B	K	M
FS32R264KCK0MMM	C	K	M
FS32R264JBK0MMM	B	J	M
FS32R264JCK0MMM	C	J	M

Table 3. Configuration

Configuration	2 MB Flash	1.5 MB RAM	CSE
B or S	Yes	Yes	Yes
C	Yes	Yes	No

Table 4. Performance

Perf (MHz)	Z7	Z7	Z4	Z4
K	240	240	120	120

Table continues on the next page...

Table 4. Performance (continued)

Perf (MHz)	Z7	Z7	Z4	Z4
V	200	200	100	100
J	266	266	133	133

Table 5. Temperature values

Temperature	T_A
M	-40 ºC to 125 ºC
V	-40 ºC to 105 ºC

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 6. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD_HV_PMU}$	3.3 V PMU supply voltage	—	–0.3	4.0[1, 2]	V
$V_{DD_HV_REG3V8}$	REG3V8 Supply Voltage	—	–0.3	5.5	V
$V_{DD_HV_IO*}$	3.3 V Input/Output Supply Voltage, LFAST IO Supply, RGMII IO Supply and PWM IO Supply	—	–0.3	3.63[1, 2]	V
$V_{SS_HV_IOx}$	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD_HV_FLA}$	3.3 V flash supply voltage	—	–0.3	3.63[1, 2]	V
$V_{DD_HV_RAW}$	AFE RAW supply voltage	—	–0.1	4	V
$V_{DD_HV_DAC}$	AFE DAC supply voltage	—	–0.1	4	V
$V_{DD_LV_IO*}$	Aurora supply voltage	—	–0.3	1.5	V
V_{DD}	1.25 V core supply voltage[3, 4, 5]	—	–0.3	1.5	V
V_{SS}	1.25 V core supply ground[3, 4, 5]	—	–0.3	0.3	V
$V_{SS_LV_OSC}$	Oscillator amplifier ground	—	–0.1	0.1	V

Table continues on the next page...

Table 6. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD_LV_PLL0}$	System PLL supply voltage	—	–0.3	1.5	V
$V_{DD_LV_LFASTPLL}$	LFAST PLL supply voltage	—	–0.3	1.5	V
$V_{DD_HV_ADCREF0/1}$	ADC_0 and ADC_1 high reference voltage	—	–0.3	5.5	V
$V_{SS_HV_ADCREF0/1}$	ADC_0 and ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADC}$	3.3 V ADC supply voltage	—	–0.3	4.0 [1, 2]	V
$V_{SS_HV_ADC}$	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	Supply ramp rate[6]	—	0.00005	0.1	V/µs
V_{IN_XOSC}	Voltage on XOSC pins with respect to ground	—	-0.3	1.47	V
V_{INA}	Voltage on SAR ADC analog pin with respect to ground ($V_{SS_HV_ADCREFx}$)	—	–0.3	6.0	V
V_{INA_SD}	Voltage on Sigma-Delta ADC analog pin with respect to ground[7]	Powered up [8]	-0.3	$V_{DD_HV_RAW}$ + 0.3	V
		Powered down [9]	-0.3	1.47	
V_{IN}	Voltage on any digital pin with respect to ground ($V_{SS_HV_IOx}$)	Relative to $V_{DD_HV_IOx}$	–0.3	$V_{DD_HV_IOx}$ + 0.3 [10]	V
$V_{DD_LV_DPHY}$	MIPICSI2 DPHY voltage supply[3, 4, 5]	—	–0.3	1.5	V
$V_{SS_LV_DPHY}$	MIPICSI2 DPHY supply ground[3, 4, 5]	—	–0.3	0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition[11]	—	–10	10[12]	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	Storage temperature	—	–55	150	°C

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum T_J = 150°C; remaining time as defined in note 5 and note 6.
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum T_J = 150°C; remaining time as defined in note 6.
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum T_J=150°C.
6. TV_{DD} is relevant for all external supplies.
7. ADC inputs include an overvoltage detect function that detects any voltage higher than 1.2 V with respect to ground on either ADC input and open circuit (disconnect) the input in order to prevent damage to the ADC internal circuitry. The ADC input remains disconnected until the inputs return to the normal operating range.
8. SDADC is powered up and overvoltage protection is ON.
9. SDADC is powered up and overvoltage protection is OFF.
10. Only when $V_{DD_HV_IOx}$ < 3.63 V.
11. No input current injection circuitry on AFE pins.
12. The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.

4.2 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

Table 7. Device operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
$V_{DD_HV_PMU}$	3.3V PMU Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD_HV_REG3V8}$	REG3V8 Supply Voltage	—	3.13	3.8	5.5	V
V_{DD}	Core Supply Voltage	—	1.19[2]	1.25	1.31[3]	V
$V_{DD_HV_IO*}$	Main GPIO 3V Supply Voltage, LFAST IO Supply, RGMII IO Supply, PWM IO Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD_LV_IO_*}$[4]	Aurora Supply Voltage	—	1.19	1.25	1.31	V
$V_{DD_LV_PLL0}$	System PLL Supply Voltage	—	1.19[2]	—	1.31	V
$V_{DD_LV_LFASTPLL}$	LFAST PLL Supply Voltage	—	1.19	—	1.31	V
$V_{DD_HV_FLA}$[5]	Flash Supply Voltage	—	3.13[2]	3.3	3.6	V
$V_{DD_HV_ADC}$	SAR ADC Supply Voltage (HVD supervised)	—	3.13[2]	3.3	3.6[6]	V
$V_{DD_HV_RAW}$	3.3V AFE RAW Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD_HV_DAC}$	3.3V AFE DAC Supply Voltage	—	3.13	3.3	3.6	V
$V_{DD_HV_ADCREF0/1}$	ADC_0 and ADC_1 high reference voltage	—	3.13	3.3	3.6	V
V_{IN}	Voltage on digital pin with respect to ground ($V_{SS_HV_IOx}$)	—	—	—	$V_{DD_HV_IOx}$ +0.3	V
V_{INSDPP}	Sigma-Delta ADC Input Voltage (peak-peak)[7, 8]	Differential	—	—	1.2	V
V_{INSR}	Sigma-Delta ADC Input Slew Rate[7]	—	—	—	165	V/µs
R_{TRIM_TOL}	External Trim Resistor tolerance	±0.1%	40.16	40.2	40.25	kΩ
R_{TRIM_TEMPCO}	External Trim Resistor Temperature Coefficient	—	—	—	25	ppm/°C
V_{INA}[9]	Voltage on SAR ADC analog pin with respect to ground ($V_{SS_HV_ADCREFx}$)	—	—	—	$V_{DD_HV_ADCREFx}$	V
$V_{DD_LV_DPHY}$	MIPICSI2 DPHY voltage supply[10]		1.19	1.25	1.31	V
T_A,[11]	Ambient temperature at full performance [12]	—	–40	—	125	°C

Table continues on the next page...

Table 7. Device operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max[1]	Unit
T_J[11]	Junction temperature	—	–40	—	150	°C
F_{XTAL}	XOSC Crystal Frequency[13]	—	—	40	—	MHz
AFE Bypass Modes Only						
Single-Ended External Clock[14]						
$EXTAL_{clk}$	EXTAL external clock frequency			40		MHz
$V_{inxoscjit}$	EXTAL external clock Cycle to Cycle Jitter (RMS)	—	—	—	2.5[15]	ps
$V_{inxoscclkvil}$	EXTAL external clock input low voltage	—	0	—	0.4	V
$V_{inxoscclkvih}$	EXTAL external clock input high voltage	—	1	—	1.23	V
t_r/t_f	Rise/fall time of EXTAL external clock input				1	ns
t_{dc}	Duty Cycle of EXTAL external clock input		47	50	53	%
Differential LVDS External Clock						
$LVDS_{clk}$	LVDS external clock frequency			40		MHz
$LVDSV_{inxoscclk}$	LVDS external clock input voltage		0		1.36	V
$LVDSV_{inxoscclk(p-p)}$	LVDS external clock input voltage (peak-peak)	Voltage driven, AC coupled Differential	0.45	0.70	1.12	V
$LVDSI_{inxoscclk}$	LVDS external clock input current	Current driven, DC coupled.	3.0	3.5	4.0	mA
$LVDSV_{inxoscjit}$	LVDS external clock Jitter (RMS) [15]				2.5	ps
t_r/t_f	Rise/fall time of LVDS external clock input	20% - 80%			1.5	ns
t_{dcLVDS}	Duty Cycle of LVDS external clock input		47	50	53	%

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. Aurora supply must connect to core supply voltage at board level.
5. The ground connection for the $V_{DD_HV_FLA}$ is shared with V_{SS}.
6. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
7. Around common mode voltage of 0.7 V. Input voltage cannot exceed 1.4 V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared).
8. SDADC input voltage full scale is 1.2 Vpp
9. On channels shared between ADC0 and 1, $V_{DD_HV_ADCREFx}$ is the lower of $V_{DD_HV_ADCREF0/1}$.
10. $V_{DD_LV_DPHY}$ supply should be shorted to core supply voltage VDD on board. Refer to AN5251. Contact your NXP sales representative for details.

11. While determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is critical that the junction temperature specification is not exceeded under any condition.
12. Full performance means full frequency.
13. Recommended Crystal 40 MHz (ESR≤30 Ω), 8 pF load capacitance.
14. External mode can be used as differential input with EXTAL and XTAL
15. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.

4.3 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

Table 8. Current consumption characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD_CORE}	Core current in run mode	All cores at max frequency. 1.31 V. Tj = 150°C (240 MHz) All cores at max frequency. 1.31 V. Tj = 150°C (266 MHz)	-	-	1480[1] 1642[1]	mA
$I_{DD_HV_FLA}$	Flash operating current	Tj = 150°C. $V_{DD_HV_FLA}$ = 3.6 V	-	3[2]	40[3]	mA
$I_{DD_LV_AURORA}$	Aurora operating current	Tj = 150°C. $V_{DD_LV_AURORA}$ = 1.31 V. 4 TX lanes enabled.	-	-	60	mA
$I_{DD_HV_ADC}$	ADC operating current	Tj = 150°C. $V_{DD_HV_ADC}$ = 3.6 V. 2 ADCs operating at 80 MHz.	-	2	5	mA
$I_{DD_HV_ADCREF}$	Reference current per ADC[4] Reference current per temp sensor[5]	Tj = 150°C. $V_{DD_HV_ADCREFx}$ = 3.6 V. ADC operating at 80 MHz.	- -	- -	1.5 0.75	mA
$I_{DD_HV_RAW}$	AFE SD and regulator operating current	Tj = 150°C. $V_{DD_HV_RAW}$ = 3.6 V. SD-PLL, AFE regulators and 4 SD enabled.	-	70[6]	75	mA
$I_{DD_HV_DAC}$	AFE DAC operating current	Tj = 150°C. $V_{DD_HV_DAC}$ = 3.6 V. DAC enabled.	-	10	15	mA
$I_{DD_HV_PMU}$	PMU operating current	Tj = 150°C. VDD_HV_PMU = 3.6 V. Internal regulation enabled.	-	2	10	mA
$I_{DD_LV_DPHY}$	MIPICSI2 DPHY operating current in HS-RX mode	Tj = 150°C, $V_{DD_LV_DPHY}$ =1.31 V	-	14.9	23.2	mA

1. Strong dependence on use case, cache usage.
2. Measured during flash read.
3. Peak Flash current measured during read while write (RWW) operation.
4. ADC0 and 1 on ADCREF0/1.
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/1.
6. Typical number is approximately 10 mA per each SD-ADC enabled, 12 mA for SD-PLL and 15 mA for the AFE regulators.

4.4 Voltage regulator electrical characteristics

Table 9. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POR-R	1.25 V VDD core POR release	—	0.97	1.02	1.06	V
POR-E	1.25 V VDD core POR engage	—	0.93	0.98	1.02	V
LVD12R	Low-Voltage Detection 1.25 V release (Core VDD supply, and PLL0/1 supply LVDs)	Untrimmed	1.122	1.157	1.192	V
LVD12R-trim		Trimmed	1.142	1.157	1.172	V
LVD12E	Low-Voltage Detection 1.25 V engage (Core VDD supply and PLL0/1 supply LVDs)	Untrimmed	1.102	1.137	1.172	V
LVD12E-trim		Trimmed	1.122	1.137	1.152	V
HVD12R-trim	High-Voltage Detection 1.25 V release (Core VDD)	Trimmed	1.33	1.35	1.37	V
HVD12E-trim	High-Voltage Detection 1.25 V engage (Core VDD supply)	Trimmed	1.36	1.38	1.40	V
LVD_MIPI12R-trim	Low-Voltage Detection 1.25V release (MIPICSI2 DPHY supply)	—	1.130	1.157	1.184	V
LVD_MIPI12E-trim	Low-Voltage Detection 1.25V engage (MIPICSI2 DPHY supply)	—	1.111	1.137	1.163	V
POR-R-VDD_HV_PMU	3.3 V PMU supply voltage POR release threshold	—	2.54	2.645	2.735	V
POR-E-VDD_HV_PMU	3.3 V PMU supply voltage POR engage threshold	—	2.50	2.60	2.695	V
LVD33R	3.3V Low-Voltage Detection Release Threshold (PMC, FLASH, IO, ADC)	Untrimmed	2.90	3.02	3.13	V
LVD33R-trim		Trimmed	3.00	3.05	3.10	V
LVD33E	3.3V Low-Voltage Detection Engage Threshold (PMC, FLASH, IO, ADC)	Untrimmed	2.86	2.98	3.09	V
LVD33E-trim		Trimmed	2.96	3.01	3.06	V
HVD33R	3.3V High-Voltage Detection Release Threshold (ADC)	Untrimmed	3.45	3.61	3.75	V
HVD33R-trim		Trimmed	3.47	3.53	3.58	V
HVD33E	3.3V High-Voltage Detection Engage Threshold (ADC)	Untrimmed	3.51	3.65	3.79	V
HVD33E-trim		Trimmed	3.51	3.57	3.62	V
UVL30R	SMPS under-voltage lockout release threshold	Untrimmed	2.75	2.90	3.05	V
UVL25E	SMPS under-voltage lockout engage threshold		2.40	2.55	2.7	V
DGLITCHE	Voltage Detector Deglitcher Filter Time - Engage	—	2.0	3.5	5	µs
DGLITCHR	Voltage Detector Deglitcher Filter Time - Release	—	5	7	12	µs
RSTDGLTC	VREG_POR_B Input Deglitch Filter Time	—	200	320	500	ns
RSTPUP	VREG_POR_B Pin Pull-up Resistance	—	37	75	150	kΩ
REGENPUP	VREG_SEL Pin Pull-up Resistance	—	37	75	150	kΩ
VSMPS	Internal switched regulator output voltage [1]	Load Current from 10 mA to 1.8 A	1.19	1.255	1.35	V

Table continues on the next page...

Table 9. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FSMPS	Internal switched regulator operating frequency without modulation	Untrimmed	0.65	1.00	1.35	MHz
		Trimmed	0.93	1.00	1.07	MHz
FSMPS-M7.5	Internal switched regulator frequency modulation	—	—	7.5	—	%
FSMPS-M15		—	—	15	—	%
FSMPS-M30		—	—	30	—	%
VREGSWPUP	Internal switched regulator gate-driver pull-up resistance[2]	—	—	—	—	—
VREF_BG_T	PMC bandgap reference voltage for SARADC	Trimmed	1.20	1.22	1.237	V
Vih (VREG_POR_B)	VREG_POR_B pin High Voltage level	—	0.7 x VDD_HV_PMU	—	VDD_HV_PMU + 0.3	V
Vil (VREG_POR_B)	VREG_POR_B pin Low Voltage level	—	-0.3	—	0.3 x VDD_HV_PMU	V
LVDAFER	Low Voltage Detection 3.3V Release (AFE VDD_HV_DAC and VDD_HV_RAW supplies)		2.75	2.80	2.90	V
LVDAFEE	Low Voltage Detection 3.3V Engage (AFE VDD_HV_DAC and VDD_HV_RAW supplies)		2.68	2.77	2.86	V

1. Min/Max includes transient load conditions. Steady state voltage is within the core supply operating specifications.
2. There is a strong pull up from VREG_SWP to VDD_HV_REG3V8 which is connected when SMPS is disabled. The pullup has resistance less than 1 Kohm, therefore VREG_SWP should not be connected to ground if unused.

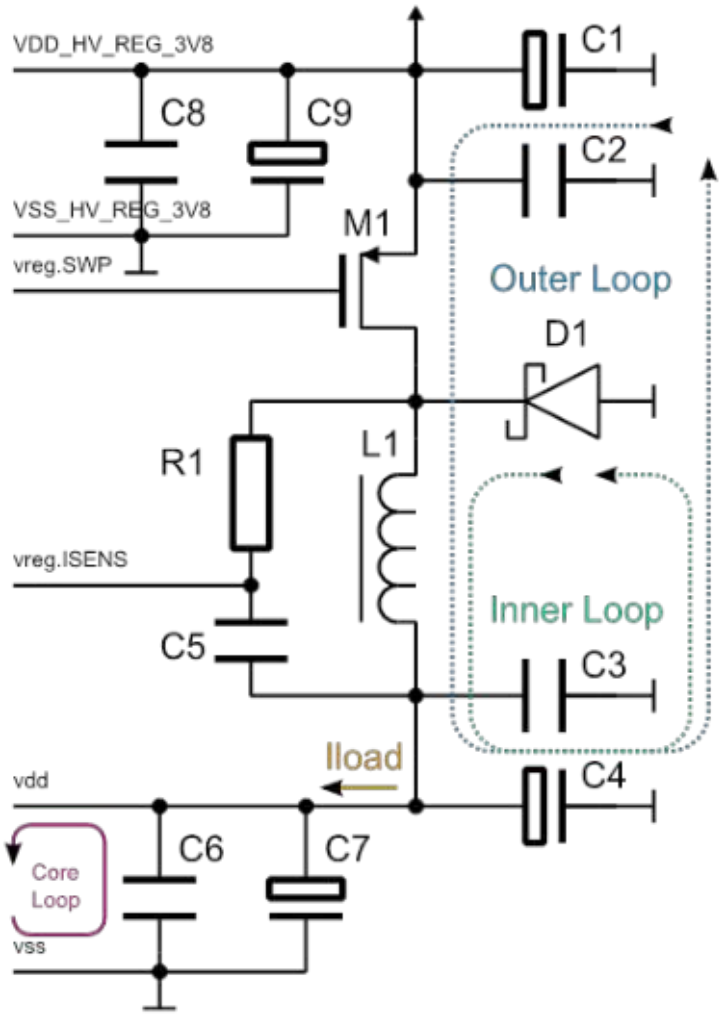


Figure 2. SMPS External Components Configuration

Table 10. SMPS External Components

Ref	Description
M1	SI3443, 2SQ2315
L1	2.2 uH 3A < 100 mΩ series resistance (Ex. Bourns SRU8043-2R2Y)
D1	SS8P3L 8A Schottcky Diode
R1	24 kΩ
C1	10 µF Ceramic
C2	100 nF Ceramic
C3	100 nF Ceramic (place close to inductor)
C4	10 uF Ceramic (place close to inductor)
C5	1 nF Ceramic
C6	4 x 100 nF + 4 x 10nF Ceramic (place close to MCU supply pins)
C7	4 x 10 µF Ceramic (place close to MCU supply pins)
C8	100 nF Ceramic
C9	1 µF Ceramic (Unless C1 is really close to the pin)

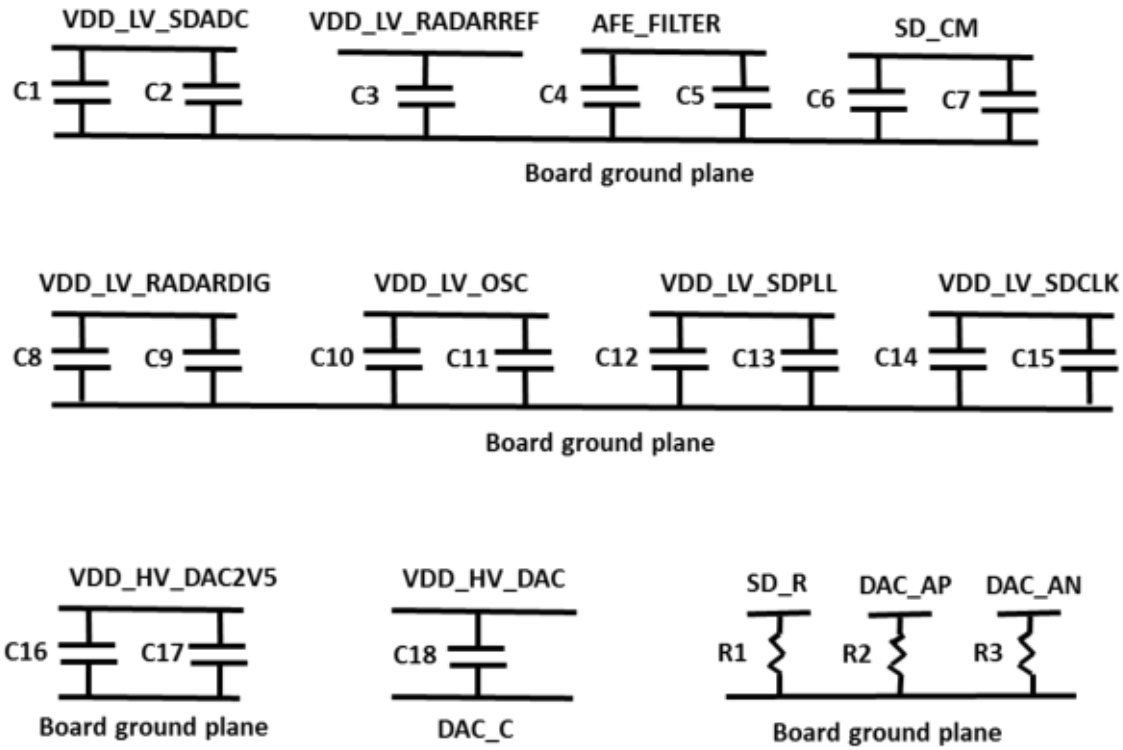


Figure 3. Radar AFE External Components Configuration

Table 11. Radar AFE External Components

Component	Component Value	Tolerance	Placement Priority of larger cap. [1]	Placement Priority of smaller cap[1]	Special notes
C1	0.47 µF	±35%	3	—	—
C2	0.1 µF	±35%	—	1	—
C3	1.0 µF	±35%	7	—	—
C4	1.0 µF	±35%	2	—	—
C5	0.1 µF	±35%	—	4	—
C6	1.0 µF	±35%	8	—	—
C7	0.1 µF	±35%	—	6	—
C8	1.0 µF	±35%	6	—	—
C9	0.1 µF	±35%	—	5	—
C10	1.0 µF	±35%	4	—	—
C11	0.1 µF	±35%	—	2	—
C12	1.0 µF	±35%	5	—	—
C13	0.1 µF	±35%	—	3	—
C14	1.0 µF	±35%	10	—	—
C15	0.1 µF	±35%	—	8	—
C16	1.0 µF	±35%	9	—	—
C17	0.1µF	±35%	—	7	—

Table continues on the next page...

Table 11. Radar AFE External Components (continued)

Component	Component Value	Tolerance	Placement Priority of larger cap. [1]	Placement Priority of smaller cap[1]	Special notes
C18	10 µF	—	1	—	X7R type
C19	220 nF	—	—	—	Sigma Delta ADC input capacitor. See Figure 9
C20	220 nF	—	—	—	Sigma Delta ADC input capacitor. See Figure 9
R1	40.2 kΩ	±0.1%	—	—	tempco = 25ppm/C
R2	300 Ω	—	—	—	DAC RI See Table 27
R3	300 Ω	—	—	—	DAC RI See Table 27
Crystal	40MHz	—	—	—	Connected between XOSC_EXTAL/ XOSC_XTAL, ESR ≤ 30Ω

1. All Radar AFE external bypass capacitors should be placed as close as possible to the associated package pin. As shown in Radar AFE External Components Configuration figure, most pins have two values of bypass capacitor. Greater than 0.1 µF is referred to as the larger cap. 0.1 µF is referred to as the smaller cap.

4.5 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 12. ESD ratings

No.	Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
1	$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C	H1C	2000	V

Table continues on the next page...

Table 12. ESD ratings (continued)

No.	Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
			conforming to AEC-Q100-002			
2	$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500[3] 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500 V for non-AFE pins, 250 V for AFE pins.

5 I/O Parameters

5.1 I/O pad DC electrical characteristics

NMI, TCK, TMS, JCOMP are treated as GPIO.

Table 13. I/O pad DC electrical specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65*$V_{DD_HV_IO}$	$V_{DD_HV_IO}$ + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	-0.3	0.35*$V_{DD_HV_IO}$	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * $V_{DD_HV_IO}$	$V_{DD_HV_IO}$ + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	-0.3	0.40 * $V_{DD_HV_IO}$	V
Vhys	CMOS Input Buffer Hysteresis	0.1 * $V_{DD_HV_IO}$	—	V
Vih_{TTL}	TTL Input high level voltage (All SAR_ADC input pins)	2	$V_{DD_HV_ADCREFx}$ + 0.3	V
Vil_{TTL}	TTL Input low level voltage (All SAR_ADC input pins)	-0.3	0.56	V
$Vhyst_{TTL}$	TTL Input hysteresis voltage (All SAR_ADC input pins)	0.3	—	V
Pull_Ioh	Weak Pullup Current[1]	10	55	µA
Pull_Iol	Weak Pulldown Current[2]	10	55	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[3]	0.8 * $V_{DD_HV_IO}$	—	V
Vol	Output Low Voltage[4]	—	0.2 * $V_{DD_HV_IO}$	V
Ioh_f	Full drive Ioh[5] (ipp_sre[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[5] (ipp_sre[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[5] (ipp_sre[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[5] (ipp_sre[1:0] = 10)	10.5	60	mA

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD_HV_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.1.1 RGMII pad DC electrical characteristics

Table 14. RGMII pad DC electrical specifications

Symbol	Parameter	Value		Unit
		Min	Max	
Vih	CMOS Input Buffer High Voltage	0.65 x $V_{DD_HV_IO}$	$V_{DD_HV_IO}$ + 0.3	V
Vil	CMOS Input Buffer Low Voltage	-0.3	0.35 x $V_{DD_HV_IO}$	V
Pull_Ioh	Weak Pullup Current[1]	10	55	µA
Pull_Iol	Weak Pulldown Current[2]	10	55	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[3]	0.8 x $V_{DD_HV_IO}$	—	V
Vol	Output Low Voltage[4]	—	0.2 * $V_{DD_HV_IO}$	V
Ioh_f	Full drive Ioh[5]	8	26	mA
Iol_f	Full drive Iol[6]	8	24	mA

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD_HV_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh_f value is measured with 0.8*VDDE applied to the pad.
6. Iol_f is measured when 0.2*VDDE is applied to the pad.

5.2 I/O pad AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD_HV_IO}$ supply defined in Table 7.

Table 15. Functional Pad electrical characteristics

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)[2]		Drive Load (pF)	SIUL2_MSCR[SRC]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)	2.5/2.5	8.25/7.5	0.7/0.6	3/3	50	11
	6.4/5	19.5/19.5	2.5/2.0	12/12	200	
	2.2/2.5	8/8	0.4/0.3	3.5/3.5	25	10
	2.9/3.5	12.5/11	1.0/0.8	6.5/6.5	50	
	11/8	35/31	6.5/3.0	25/21	200	

Table continues on the next page...

Table 15. Functional Pad electrical characteristics (continued)

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)[2]		Drive Load (pF)	SIUL2_MSCR[SRC]
	Min	Max	Min	Max		MSB,LSB
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Measured from 20% - 80% of output voltage swing
3. Slew rate control modes
4. Input slope = 2ns

NOTE

Data based on characterization results, not tested in production.

Table 16. Functional Pad AC Specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
pad_sr_hv(Cp)	Parasitic Input Pin Capacitance	4.5	4.7	5.0	pF

5.3 Aurora LVDS driver electrical characteristics

NOTE

The Aurora interface is AC coupled, so there is no common-mode voltage specification.

Table 17. Aurora LVDS driver electrical characteristics

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
F_{TXRX}	Data rate	—	—	1.15	Gbps
Transmitter Specifications					
$V_{diffout}$	Differential output voltage swing (terminated)	+/- 400	+/- 600	+/- 800	mV
T_{rise}/T_{fall}	Rise/Fall time (10% - 90% of swing)	60			ps
Receiver Specifications					
V_{diffin}	Differential voltage	+/- 100		+/- 800	mV
Termination					

Table continues on the next page...

Table 17. Aurora LVDS driver electrical characteristics (continued)

Symbol	Parameter[1]	Value			Unit
		Min	Typ	Max	
R_{V_L}	Terminating Resistance (external)	99	100	101	Ohms
C_P	Parasitic Capacitance (pad + bondwire + pin)			1	pF
L_P	Parasitic Inductance			7	nH
STARTUP					
T_{STRT_BIAS}	Bias startup time	—	—	5	µs
T_{STRT_TX}	Transmitter startup time[2]	—	—	5	µs
T_{STRT_RX}	Receiver startup time[2]	—	—	5	µs
LVDS_RXOUT[3]	Receiver o/p duty cycle	30		70	%

1. Conditions for these values are $V_{DD_LV_IO_AURORA}$ = 1.19V to 1.32V, T_J = –40 / 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
3. Receiver o/p duty cycle is measured with 1.25 Gbps, 50% duty cycle, max 1 ns rise/fall time, 100 mV voltage swing signal applied at the receiver input.

5.4 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET_B pin.

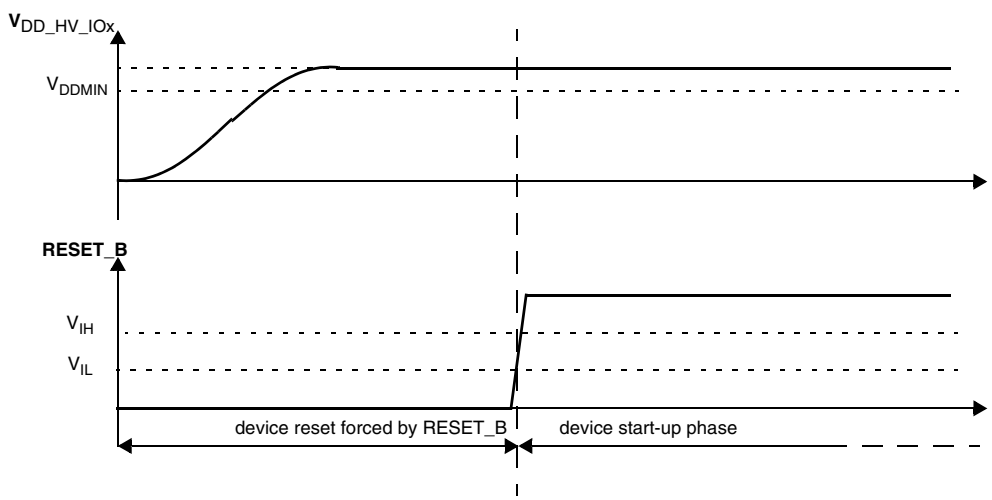


Figure 4. Start-up reset requirements

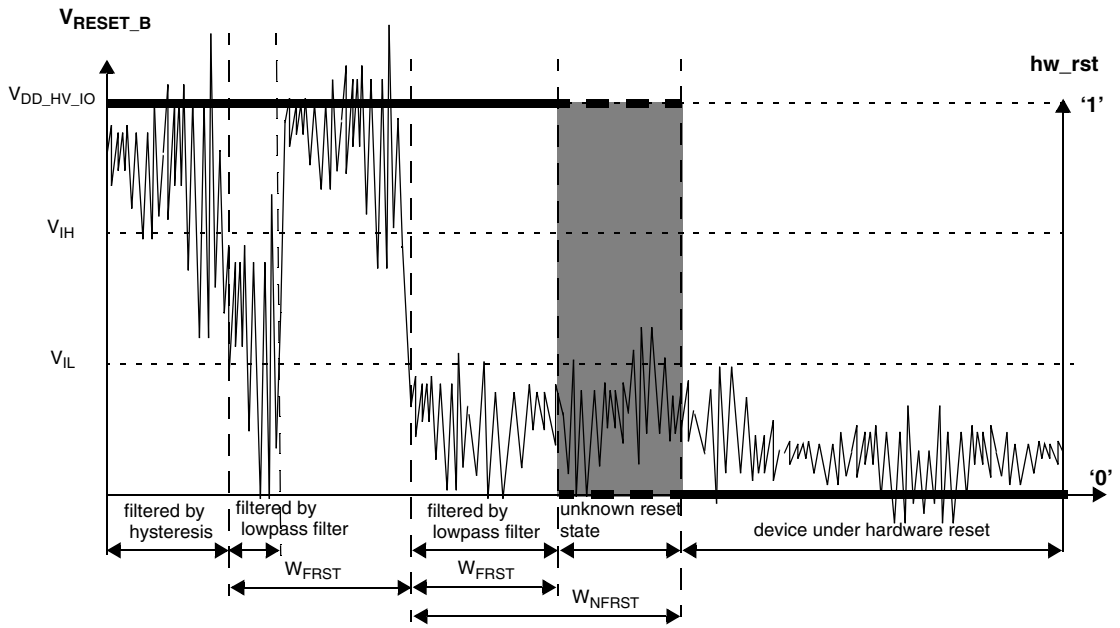


Figure 5. Noise filtering on reset signal

Table 18. RESET_B electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD_HV_IOx}$ + 0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.56	V
V_{HYS}[2]	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
I_{OL_R}	Strong pull-down current	Device under power-on reset $V_{DD_HV_IO}$ = 1.2 V V_{OL} = 0.35 x $V_{DD_HV_IO}$	0.2	—	—	mA
		Device under power-on reset $V_{DD_HV_IO}$=3.0 V V_{OL} = 0.35 x $V_{DD_HV_IO}$	15	—	—	mA
W_{FRST}	RESET_B input filtered pulse	—	—	—	500	ns
W_{NFRST}	RESET_B input not filtered pulse	—	2400	—	—	ns
$\lvert I_{WPD} \rvert$	Weak pull-down current absolute value	V_{IN} = $V_{DD_HV_IOx}$	30	—	100	µA

1. $V_{DD_HV_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.

6 Peripheral operating requirements and behaviours

6.1 Clocks and PLL Specifications

6.1.1 40 MHz Oscillator (XOSC) electrical characteristics

The device provides an oscillator/resonator driver.

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

Table 19. XOSC electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$XOSC_{fout}$	Oscillator frequency			40		MHz
t_{stab}	Oscillator start-up time				2	ms
t_{jitcc}	Cycle to cycle jitter (peak – peak)				2.5[1]	ps
	Output Duty Cycle		45	50	55	%
Cin	Input Capacitance [2]	Extal and Xtal each	3.0	4.0	5.0	pF
R_{inLVDS}	LVDS bypass mode input termination[3]	Between Extal and Xtal	75	100	125	ohm
V_{CMLVDS}	LVDS Common Mode Voltage	Vdda/2	0.60	0.70	0.80	V

1. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.
2. When using a 40 MHz crystal, the recommended load capacitance is 8 pF. Need quiet ground connection on the board and external crystal/load capacitor placement as close to the Extal and Xtal pins as possible to allow good jitter performance.
3. The termination resistance is only active when the AFE is powered (VDD_HV_RAW, VDD_HV_DAC and the AFE regulators are powered up) and the XOSC is powered down (default case once device is out of reset) or the XOSC is configured in differential bypass mode.

6.1.2 FMPLL electrical characteristics

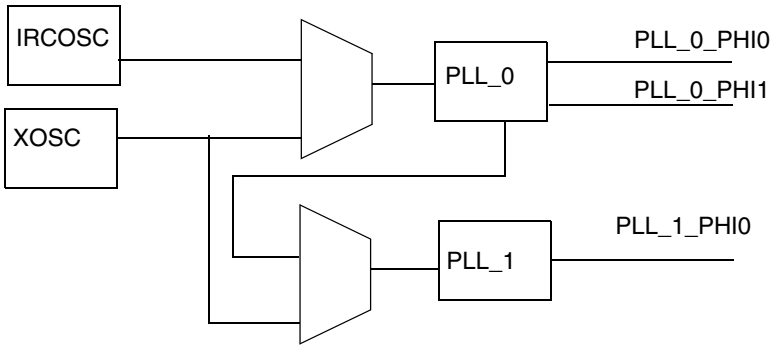


Figure 6. PLL integration

Table 20. PLL0 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL0IN}	PLL0 input clock[2, 3]	—	14	—	44	MHz
Δ_{PLL0IN}	PLL0 input clock duty cycle[2]	—	40	—	60	%
$f_{PLL0VCO}$	PLL0 VCO frequency	—	600	—	1250	MHz
$f_{PLL0PHI0}$	PLL0 output clock PHI0	—	4.76	—	625[4]	MHz
$f_{PLL0PHI1}$	PLL0 output clock PHI1	—	20	—	156	MHz
$t_{PLL0LOCK}$	PLL0 lock time	—	—	—	100	µs
$\Delta_{PLL0LTJ}$	PLL0 long term jitter f_{PLL0IN} = 8 MHz (resonator)[5]	$f_{PLL0PHI0}$ = 40 MHz, 1 µs			± 1	ns
		$f_{PLL0PHI0}$ = 40 MHz, 13 µs			± 1	ns
I_{PLL0}	PLL0 consumption		—	—	5	mA

1. $V_{DD_LV_PLL0}$ =1.25 V ± 5%, T_J = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. f_{PLL0IN} frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8 MHz-20 MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD_LV_PLL0}$ noise due to application in the range $V_{DD_LV_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 KHz) will be filtered.

Table 21. FMPLL1 electrical characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{PLL1IN}	PLL1 input clock[2]	—	38	—	78	MHz
Δ_{PLL1IN}	PLL1 input clock duty cycle[2]	—	35	—	65	%
$f_{PLL1VCO}$	PLL1 VCO frequency	—	600	—	1250	MHz
$f_{PLL1PHI0}$	PLL1 output clock PHI0	—	4.76	—	625	MHz
$t_{PLL1LOCK}$	PLL1 lock time	—	—	—	100	µs
$f_{PLL1MOD}$	PLL1 modulation frequency	—	—	—	250	kHz
$\lvert\delta_{PLL1MOD}\rvert$	PLL1 modulation depth (when enabled)	Center spread	0.25	—	2	%
		Down spread	0.5	—	4	%
I_{PLL1}	PLL1 consumption		—	—	6	mA

1. $V_{DD_LV_PLL0}$ = 1.25 V ± 5%, T_J = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

6.1.3 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

Table 22. Internal RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{Target}	IRC target frequency	—	—	16	—	MHz
$F_{untrimmed}$	IRC frequency (untrimmed)	—	9.6	—	24	MHz
δF_{var}	IRC trimmed frequency variation [1]	—	-8	—	8	%
$T_{startup}$	Startup time		—	—	5	µs

1. The typical user trim step size (δf_{TRIM}) is 0.3% of current frequency for application of positive trim and 0.26% of current frequency for application of negative trim, based on characterization results.

6.1.4 320 MHz AFE PLL electrical characteristics

Table 23. 320 MHz AFE PLL parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLL_{fout}	Output Frequency	—	—	320	—	MHz
PLL_{fin}	Input Frequency	—	—	—	40	MHz
t_{cal}	Calibration Time [1]	LW64 = 1 LW64 = 0	—	—	150 500	µs
t_{lock}	Lock Time	after calibration	—	—	75	µs
t_{jitcck}	Cycle to cycle jitter (peak – peak)	—	—	—	10	ps
—	Output duty cycle	—	48	50	52	%

1. The LW64 bit sets the wait time before the PLL frequency is measured after each calibration step to allow for stabilization. If LW64 is '0', wait time of 256 reference clock cycles is used. If LW64 is'1', wait time of 64 reference clock cycles is used.

6.1.5 LFAST PLL electrical characteristics

The specifications in the following table apply to the interprocessor bus LFAST interface.

Table 24. LFAST PLL electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{RF_REF}	PLL reference clock frequency	—	10	—	26	MHz
ERR_{REF}	PLL reference clock frequency error	—	–1	—	1	%
DC_{REF}	PLL reference clock duty cycle	—	45	—	55	%
f_{VCO}	PLL VCO frequency	—	—	640[1]	—	MHz
t_{LOCK}	PLL phase lock[2]	—	—	—	40	µs
ΔPER_{REF}	Input reference clock jitter (peak to peak)	Single period, f_{RF_REF} = 10 MHz	—	—	300	ps

Table continues on the next page...

Table 24. LFAST PLL electrical characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Long term, f_{RF_REF} = 10 MHz	–500	—	500	
ΔPER_{EYE}	Output Eye Jitter (peak to peak)[3]	Random Jitter (Rj)	—	84	101	ps
		Deterministic Jitter (Dj)	—	80	96	ps
		Total Jitter @BER 10^{-9}	—	1.09	1.31	bits per second
$I_{VDD_LV_LFASTPLL}$	$V_{DD_LV_LFASTPLL}$ Supply Current	Normal Mode	—	6	10	mA
		Peak	—	7	11	mA
		Power Down	—	0.5	27	µA

1. The 640 MHz frequency is achieved with a 10 MHz or 20 MHz reference clock. With a 26 MHz reference, the VCO frequency is 624 MHz.
2. The time from the PLL enable bit register write to the start of phase locks is maximum 2 clock cycles of the peripheral bridge clock that is connected to the PLL on the device.
3. Measured at the transmitter output across a 100 Ω termination resistor on a device evaluation board.

7 Analog modules

7.1 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

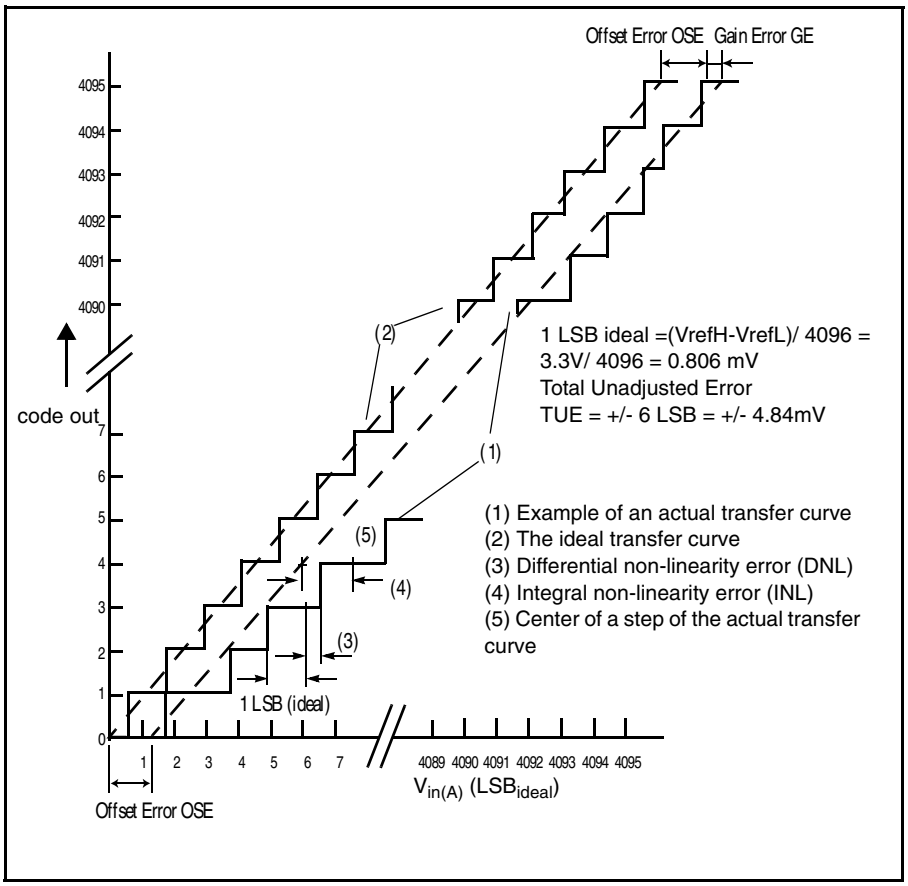


Figure 7. ADC characteristics and error definitions

7.1.1 Input equivalent circuit

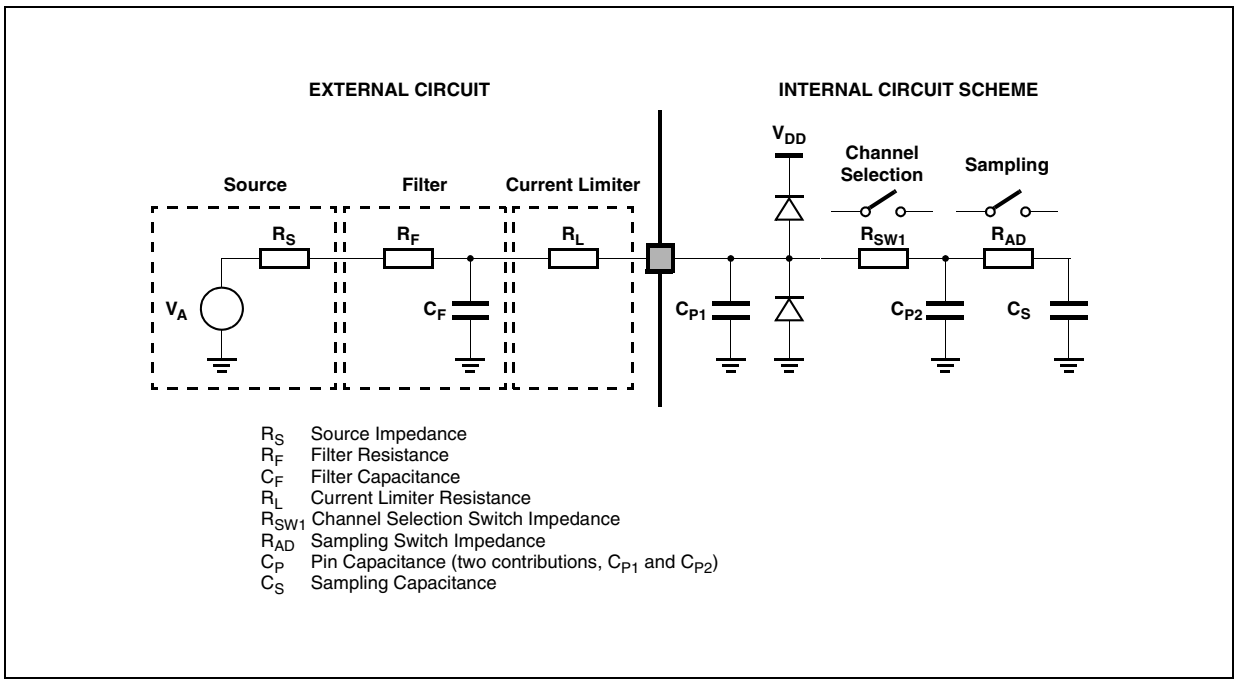


Figure 8. Input equivalent circuit

Table 25. ADC conversion characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	20	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 200 ohm source impedance	275	—	—	ns
$t_{sampleC}$	SAR selftest C-algorithm sample time	—	300	—	—	ns
$T_{sampleS}$	SAR selftest S-algorithm sample time	—	1	—	—	µs
$T_{sampleBG}$	Bandgap sample time	—	1.87	—	—	µs
$T_{sampleTS}$	Temperature sensor sample time	—	3.18	—	—	µs
t_{conv}	Conversion time[4]	80 MHz	650	—	—	ns
$C_{S'}$ [5]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity[6]	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB

Table continues on the next page...

Table 25. ADC conversion characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ		–6	—	6	LSB
$TUE_{IS1WWINJ}$	Total unadjusted error for IS1WWINJ		–6	—	6	LSB
IS1WINJ (pad going to one ADC)	(single ADC channel)					
	Max leakage	150 °C	—	—	250	nA
	Max positive/negative injection		–3	—	3[8]	mA
IS1WWINJ (pad going to two ADCs)	(double ADC channel)					
	Max leakage	150 °C	—	—	300	nA
	Max positive/negative injection [7]	|Vref_ad0 - Vref_ad1| < 150 mV	–3.6	—	3.6	mA
SNR	Signal-to-noise ratio	3.3 V reference voltage	67	—	—	dB
THD	Total harmonic distortion	@ 50 KHz	65	—	—	dB
SINAD	Signal-to-noise and distortion	Fin < 50 KHz	6.02 x ENOB + 1.76			dB
ENOB	Effective number of bits	Fin < 50 KHz	10.5	—	—	bits

1. $V_{DD_HV_ADC}$ = 3.3 V -5%,+10%, T_J = –40 to +150°C, unless otherwise specified and analog input voltage from V_{AGND} to $V_{DD_HV_ADCREFx}$.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. SeeInput equivalent circuit figure.
6. No missing codes.
7. ADC specifications are met only if injection is within these specified limits
8. Max injection current for all ADC IOs is ± 10 mA

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel. Aurora interface along with SAR-ADC would degrade SAR-ADC performance. General Purpose Input (GPI) functionality should not be used on any of the SAR-ADC channels when SARADC is functional.

7.2 Sigma Delta ADC electrical characteristics

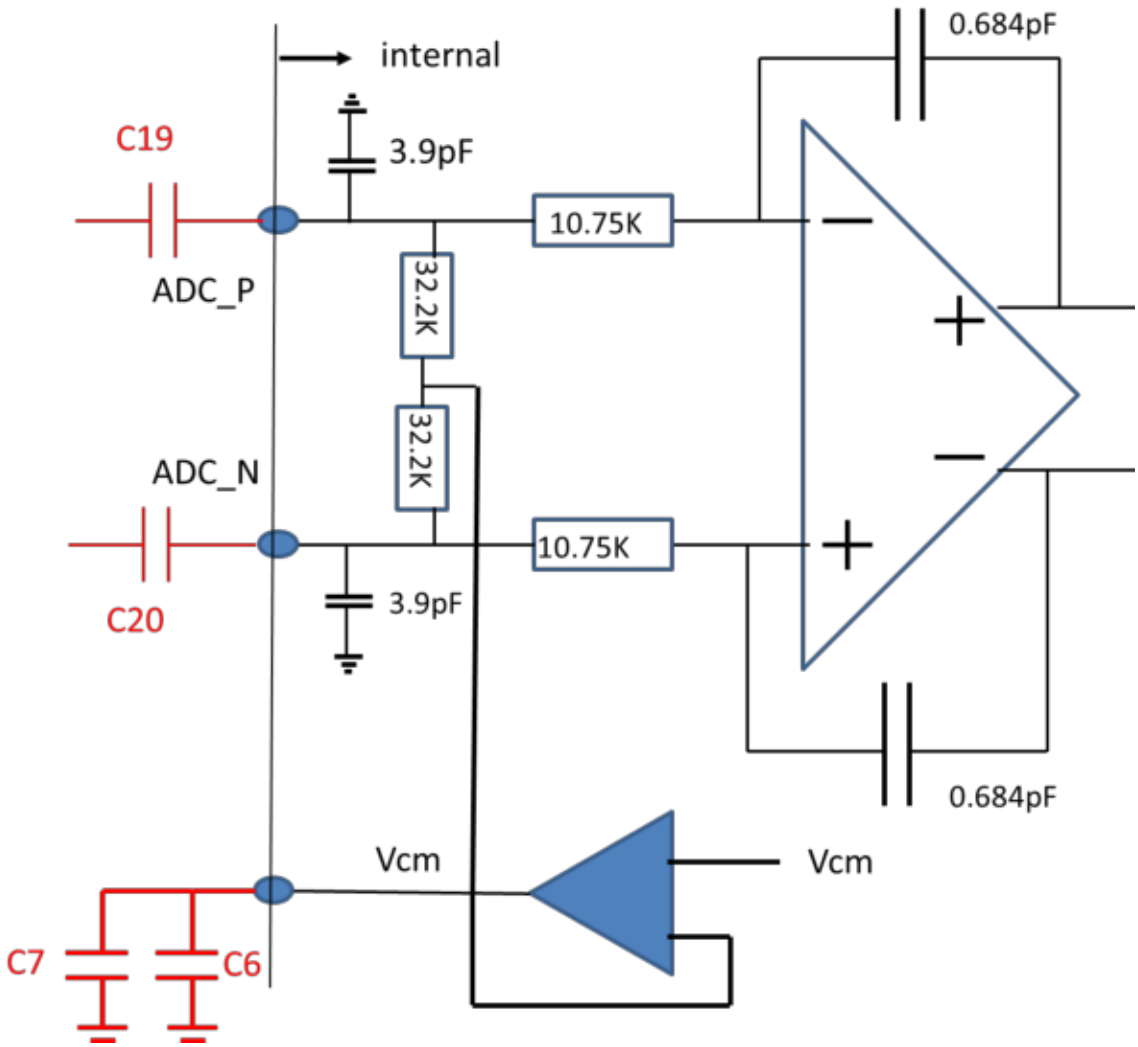


Figure 9. ADC input equivalent circuit

Table 26. Sigma Delta ADC Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SPS_{SDA}	Sample Rate	After Decimation Filtering	—	10	10	MS/S
L_{SDA}	Latency	@ 10 MS/s, full step input to 50% output. Decimation filter delay not included	—	—	0.1	µs
RT_{SDA}	Recovery Time	After overload condition	—	—	0.5	µs
$SNR_{SDA_MM_ON}$ [1]	Signal-to-Noise Ratio Mismatch Shaper on	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp.	63	67	—	dBFS

Table continues on the next page...

Table 26. Sigma Delta ADC Parameters (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 67 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.				
$SNDR_{SDA_MM_ON}$[1]	Signal-to-Noise-and-Distortion Ratio Mismatch Shaper on	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz. (using full-bandwidth decimation filter coefficients). Production test frequencies 449 KHz and 4 MHz. Production test amplitude is -6 dBFS = 0.6 Vpp. Characterized under the following conditions: • 0.6 Vpp (i.e. -6 dBFS) input signals applied at the following frequencies one at a time: 20.77 KHz, 317.7 KHz, 857.7 KHz, 1.411 MHz, 2.95 MHz, 3.897 MHz, and 4.997 MHz and the SNDR in dBFS is then calculated. • SNR at 5 MHz will be reduced by 5 dB due to decimation filter roll off. • The SNR is specified to be 64 dBFS typical for input frequencies between 20 KHz and 4 MHz. Mismatch shaper on.	62	64	—	dBFS
$IFDR_{SDA}$	Interference Free Dynamic Range	20 ms integration, ADC inputs tied together at the package pin. One side of the AC coupling capacitors associated with each input should remain connected to the ADC input and the other side of the capacitor should connected to ground.	90	—	—	dBFS
$IMD_{SDA_MM_ON}$	Intermodulation Distortion Mismatch Shaper on	Input Frequency Range and integration bandwidth are from 20 KHz to 5 MHz (using full-bandwidth decimation filter coefficients). Characterized under the following conditions: • Two distinct sets of signal pairs at the specified frequencies and at an amplitude of -8 dBFs (i.e. 0.23886 Vpeak = 0.47772 Vpp differential) are applied one signal pair at a time. • Signal pair #1 is f1 = 1 MHz and f2 = 1.1 MHz and signal pair #2 is f1 = 390.625 KHz and f2 = 546.875 KHz. • All inter modulation products are checked. Mismatch Shaper on.	62	—	—	dBc
GM	Gain Mismatching	(ADCx to ADCy)	-3.5	—	3.5	%
OE	Input Offset Error	—	-25	—	25	mV

Table continues on the next page...

Table 26. Sigma Delta ADC Parameters (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OEV	Offset Variation	t = 50 ms, T = constant, data averaged in 1 ms increments	-0.07	—	0.07	mV
V_{cm}	Common Mode Voltage[2]	SDADC switched on	—	vdda/2 – 30 mV	—	V
xtalk	Crosstalk (from any ADC to the other ADCs)	Processing a full scale signal.	—	—	-40	dB
Zin	Input Impedance	Maximum input impedance occurs for input signals at 20 KHz and minimum input impedance occurs at input frequencies greater than 1 MHz[3]	7.3	—	33.5	kΩ
R_{cm}	Resistance from each SDADC input to V_{cm} (see Figure 9)	-	27.3	32.2	37.0	kΩ
R_SDADC	Resistance from each SDADC input pin to differential amplifier input (see Figure 9)	-	9.0	10.75	12.5	kΩ
C_SDADC	SDADC integrator capacitors (see Figure 9)	-	0.636	0.684	0.732	pF
C_{in} parasitic	parasitic input capacitance from ADC input to ground	-	2.0	3.9	4.9	pF
DT	Analog Delay Variation	(ADCx to ADCy)		—	1	ns
AA	Alias Suppression	ADC input frequency between 315 and 325 MHz	50	—	—	dB
STFoob	ADC out of band Signal Transfer Function peaking	Out of band Signal Transfer function peaking from 20 MHz to 40 MHz	0	2	3	dB
PR	passband ripple	From 20 KHz to 4 MHz (default decimation filter coefficients must be used)	-0.5	0.0	0.5	dB
OOBA[4]	Out Of Band Attenuation	Default decimation filter coefficients must be used 5 MHz 6 MHz 7 MHz 10 MHz 15 MHz	 -4.5 -10 -20 -40 -60	—	—	dB

1. Derate specification by 2 dBFS for T_j less than 0°C.
2. vdda is an internally regulated and trimmed 1.45V ± 10mV voltage.
3. The input structure of the ADC is an active RC integrator which has a frequency dependent input impedance as indicated in ADC input equivalent circuit.
4. All attenuation values are relative to 0 dB in the ADC passband.

7.3 DAC electrical specifications

NOTE

- All data is measured in single ended mode. Differential mode is guaranteed by design.
- Specifications guaranteed only if factory trims are not overridden.

Table 27. DAC parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N_{BIT}	Bits	Base bits PWM bits	—	12 4 (extra lsb's)	—	Bits
SPS_{DAC}	Sample rate	—	—	10	—	MSamples/s
DNL	Linearity[1]	—	-24	—	4	LSB
V_{out}	Output Voltage[1, 2, 3]	Single-Ended, Rl = 300 Ω	1.2	—	1.35	V
I_{out}	Full-Scale Output Current	DAC full-scale adjust bits set to 01 or 10	4.0	—	4.5	mA
N_{DAC}	DAC output noise [1, 4]	@250 kHz @100 kHz @10 kHz @1 kHz		—	20 30 65 170	nV/sqrt(Hz)
SOE	Static Offset Error[1, 2]	Single-Ended Differential with the full-scale adjust bits set to either 01 or 10	60 -30	75 0	100 30	mV
TOE	Transient Offset Error[1, 2, 5]	After low-pass filter and averaging	—	—	0.05	LSB
t_{DV}	Transient Time Delay Variation [1, 2, 6]	LSB step MSB step	—	—	1 10	ns
Oc	Output compliance	single-ended, only the DNL specification is guaranteed. The TOE and Tdv may be degraded.	0	—	1.35	V
tempco	Temperature coefficient	—	–1	—	1.0	LSB/K[2]
PSRR	Power Supply Rejection Ratio[7]	Freq < 250 KHz	30	—	—	dB

1. DAC linearity, output swing, noise, TOE, and Tdv specifications are all based upon a 300 Ω DAC output load resistor and assume that the full-scale adjust bits are set to either 01 or 10. These specifications will NOT be met for other DAC output load resistor values.
2. Once all of the LVDs have cleared and the DAC is powered on, a one-time wait time of 300 ms is required before the DAC output signal is valid.
3. The full-scale DAC output is trimmed to 1.30 V ±10 mV with all DAC inputs set to 1 including both full-scale adjust bits.
4. Rl = 300 Ω, 10uF capacitor between Vdd_HV_DAC and DAC_C, ideal supply
5. Difference between ideal and real (Va+Vb/2), for all base and PWM LSBs
6. Falling edge to falling edge or rising edge to rising edge. Any transition DACn -> DACn + 1

7. DAC PSRR is 30 dB minimum for DAC output levels of 1/3 of full-scale or less. DAC PSRR is 24 dB minimum with the DAC output at full-scale.

8 Memory modules

8.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 28 shows the estimated Program/Erase times.

Table 28. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

8.2 Flash memory Array Integrity and Margin Read specifications

Table 29. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

8.3 Flash memory module life specifications

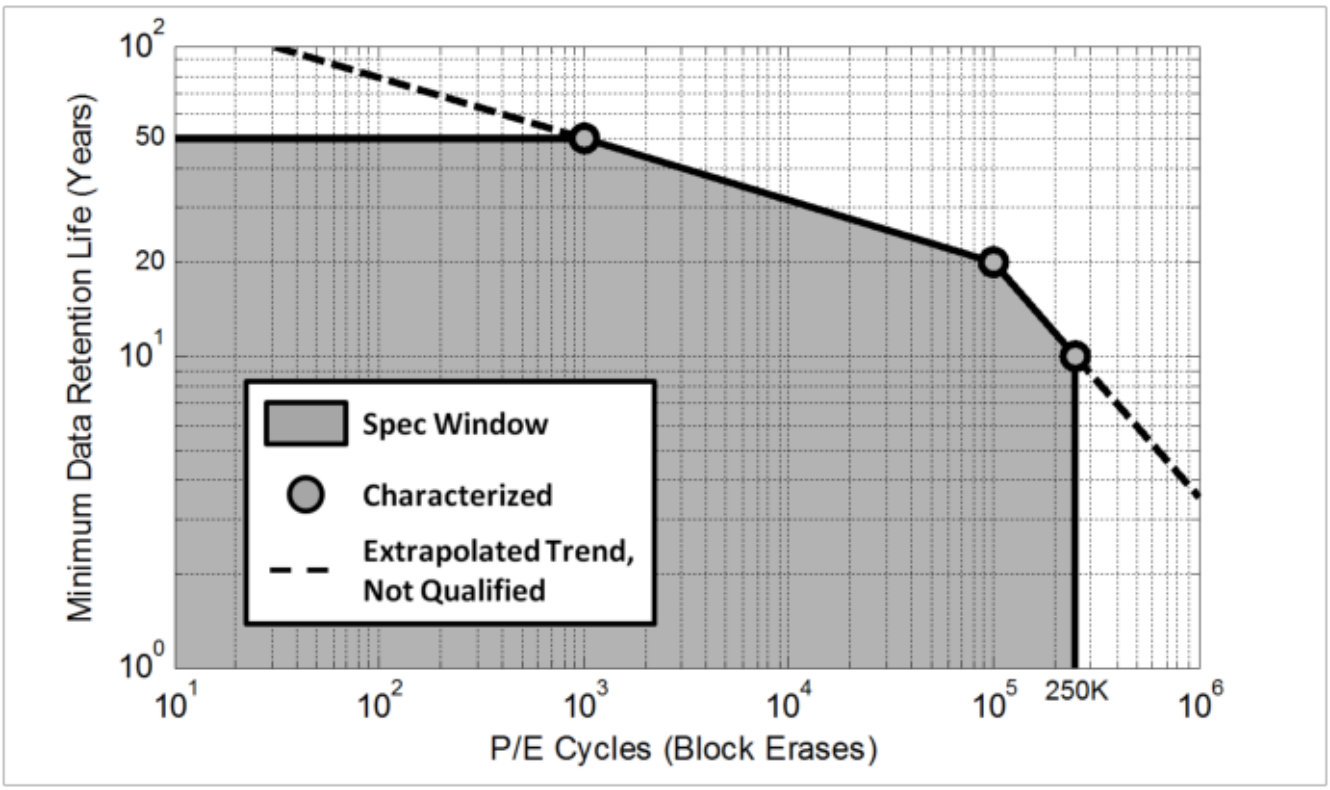
Table 30. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

8.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



8.5 Flash memory AC timing specifications

Table 31. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs

Table continues on the next page...

Table 31. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

8.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1,2,3[RWSC] and PCRC1,2,3[APC] fields at various operating frequencies, based on specified intrinsic flash memory access timed of the Flash memory.

Table 32. Flash read wait state and address pipeline control guidelines

Operating Frequency (fsys = SYS_CLK)	RWSC	APC	Flash read latency on min-cache miss (# of fcpu clock periods)	Flash read latency on mini-cache hit (# of fcpu clock periods)
0 MHz < fsys <= 33 MHz	0	0	3	1

Table continues on the next page...

Table 32. Flash read wait state and address pipeline control guidelines (continued)

Operating Frequency (fsys = SYS_CLK)	RWSC	APC	Flash read latency on min-cache miss (# of fcpu clock periods)	Flash read latency on mini-cache hit (# of fcpu clock periods)
33 MHz < fsys <= 100 MHz	2	1	5	1
100 MHz < fsys <= 120 MHz	3	1	6	1

9 Communication modules

9.1 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

9.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 1 ns and output load of 25 pF.

Table 33. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

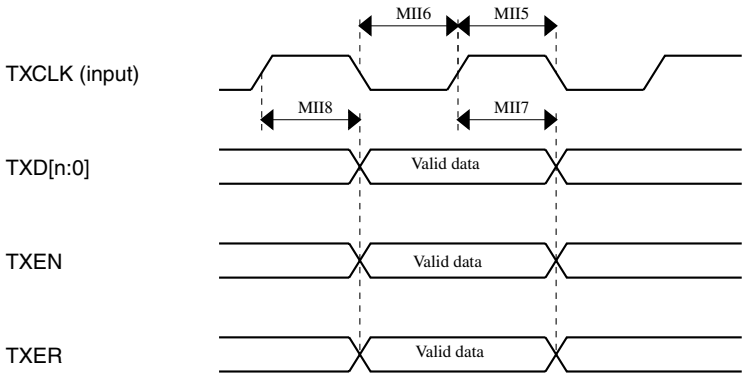


Figure 10. MII transmit signal timing diagram

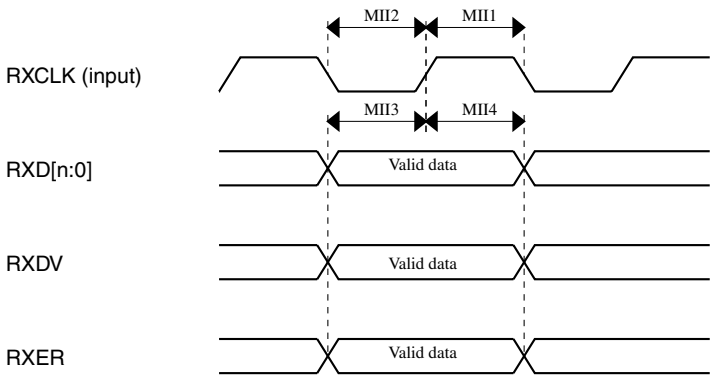


Figure 11. MII receive signal timing diagram

9.1.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 1 ns and output load of 25 pF.

Table 34. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

Table continues on the next page...

Table 34. RMII signal switching specifications (continued)

Num	Description	Min.	Max.	Unit
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

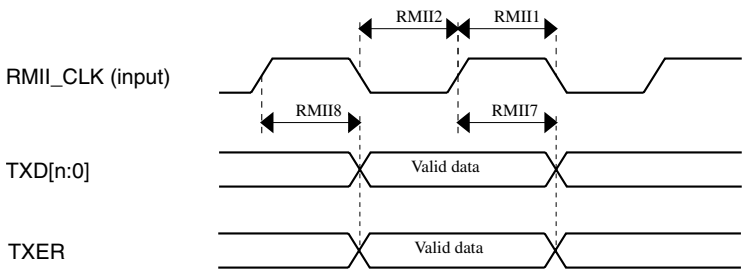


Figure 12. RMII transmit signal timing diagram

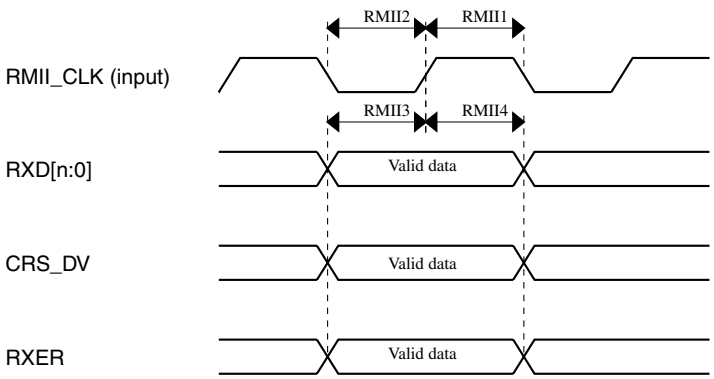


Figure 13. RMII receive signal timing diagram

9.1.3 RGMII signal switching specifications

The RGMII interface works at 3.3 V compatible levels as mentioned in RGMII pad DC electrical characteristics.

The following timing specs meet the requirements for RGMII style interfaces for a range of transceiver devices.

- Measurements are with input transition of 0.750 ns and output load of 10 pF.

Table 35. RGMII signal switching specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
—	Input Duty cycle (Clock from external PHY)	48	—	52	%	
Tcyc	Clock cycle duration	7.2	8.0	8.8	ns	1
TskewT	Data to clock output skew at transmitter	-500	0	500	ps	2
TskewR	Data to clock input skew at receiver	1	1.8	2.6	ns	2

Table continues on the next page...

Table 35. RGMII signal switching specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Notes
Duty_G	Duty cycle for Gigabit	45	50	55	%	3
Duty_T	Duty cycle for 10/100T	40	50	60	%	3
Tr/Tf	Rise/fall time (20–80%)	—	—	1.5	ns	

1. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
2. For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100 the Max value is unspecified.
3. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

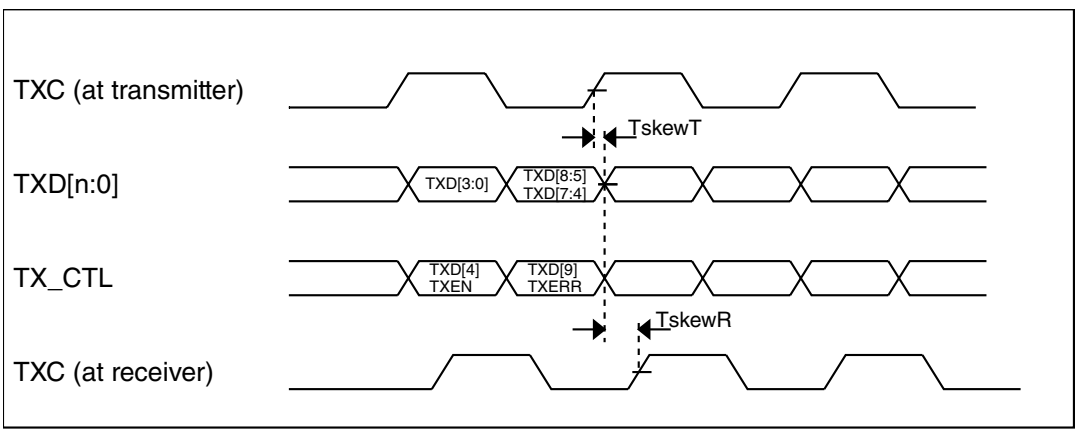


Figure 14. RGMII transmit signal timing diagram

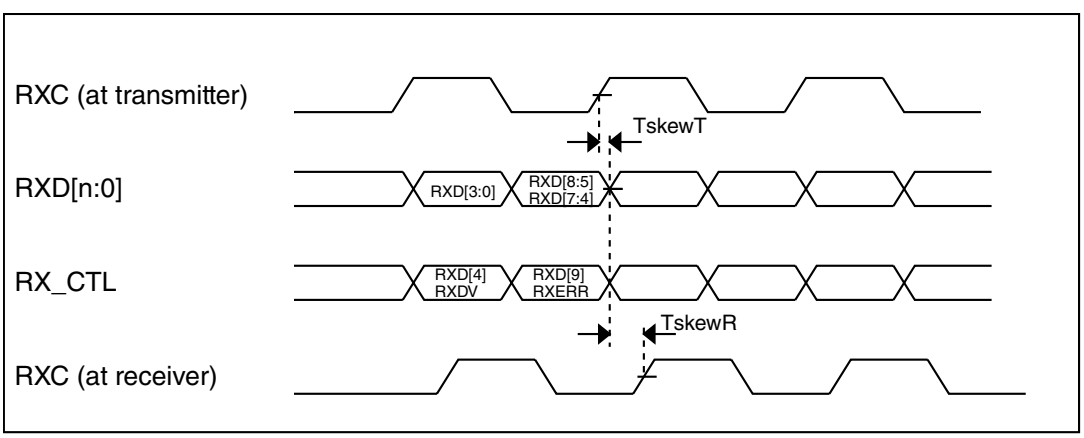


Figure 15. RGMII receive signal timing diagram

9.1.4 MII/RMII Serial Management channel timing (MDC/MDIO)

The MDC/MDIO interface works at 3.3V compatible levels as mentioned in CMOS input (vih/vil/voh/vol/)values in I/O pad DC electrical characteristics .

Ethernet works with maximum frequency of MDC at 2.5 MHz. Output pads configured with SRC=11. MDIO pin must have external pull-up. Measurements are with input transition of 1.0 ns and output load of 50 pF.

Table 36. Ethernet MDIO timing table

Num	Description	Min.	Max.	Unit
MDC00	MDC clock frequency	—	2.5	MHz
MDC10	MDC falling edge to MDIO output invalid (minimum propagation delay)	(-0.8 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))	—	ns
MDC11	MDC falling edge to MDIO output valid (maximum propagation delay)	—	(13 + (ENET_MSCR[HOLDTIME] +1)*(PBRIDGE_n_CLK period in ns))	ns
MDC12	MDIO (input) to MDC rising edge setup	13	—	ns
MDC13	MDIO (input) to MDC rising edge hold	0	—	ns
MDC14	MDC pulse width high	40%	60%	MDC Period
MDC15	MDC pulse width low	40%	60%	MDC Period

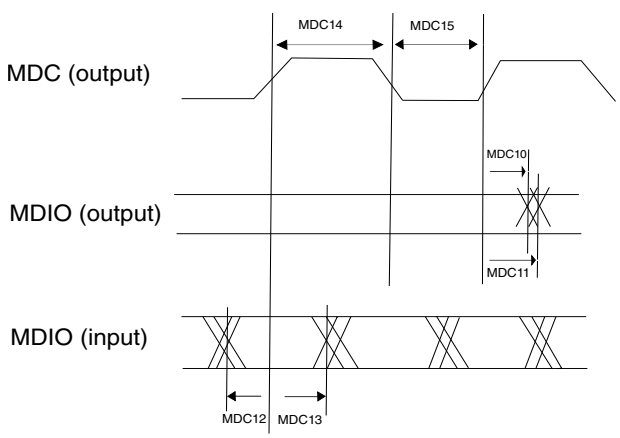


Figure 16. RMII/MII serial management channel timing diagram

9.2 FlexRay timing parameters

This section provides the FlexRay interface timing characteristics for the input and output signals. These numbers are recommended per the FlexRay Electrical Physical Layer Specification, Version 3.0.1, and subject to change per the final timing analysis of the device.

9.2.1 TxEN

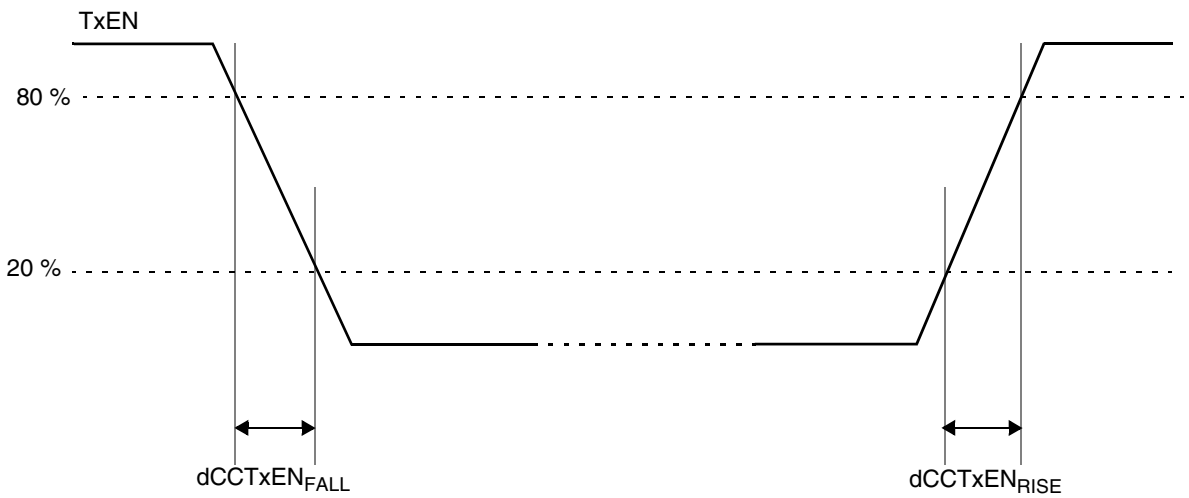


Figure 17. FlexRay TxEN signal

Table 37. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +10%, T_J = –40 °C / 150 °C, TxEN pin load maximum 25 pF.

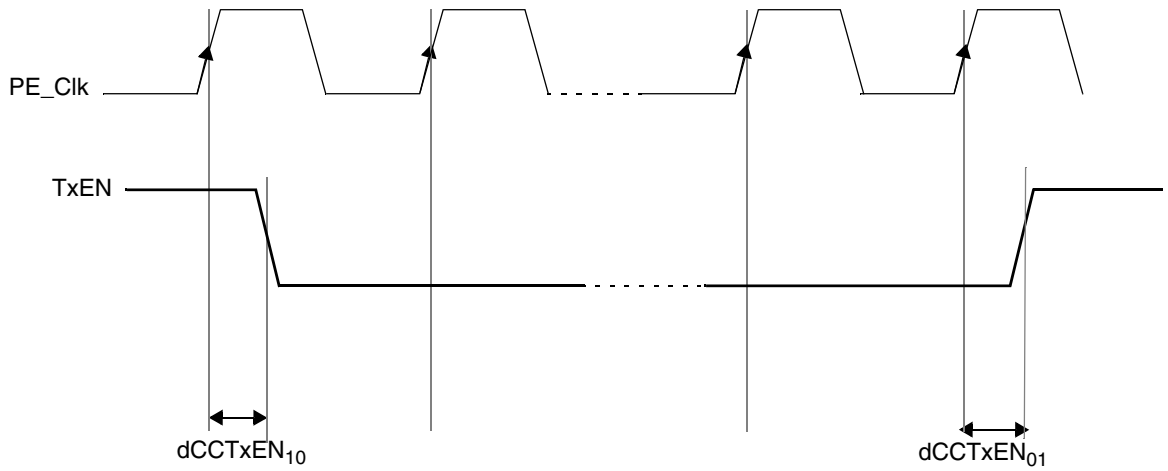


Figure 18. FlexRay TxEN signal propagation delays

9.2.2 TxD

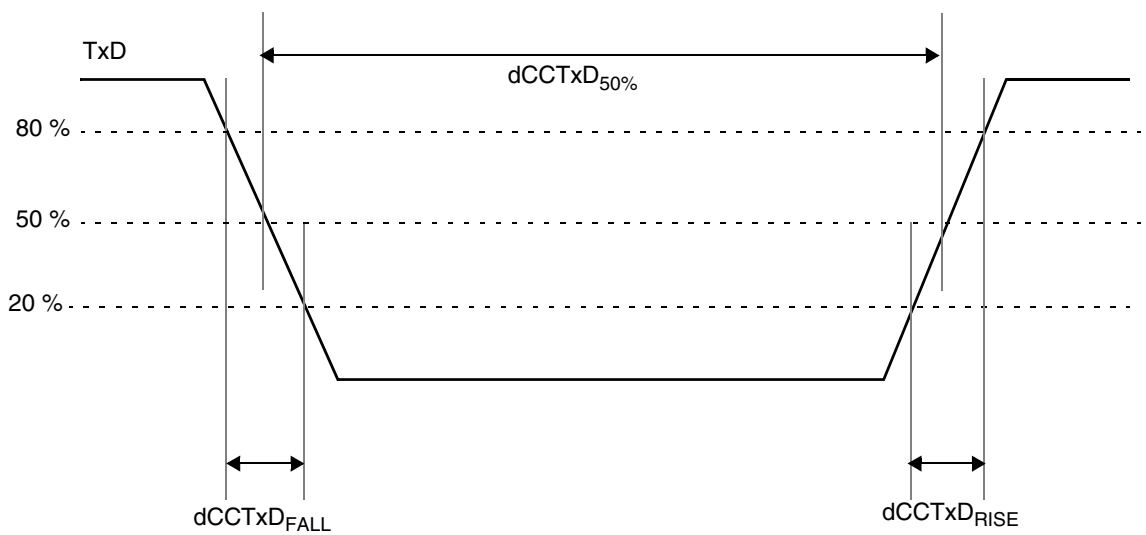


Figure 19. FlexRay TxD signal

- Measurements are with output load of 25 pF and pad configured as SRE =11.

Table 38. TxD output characteristics

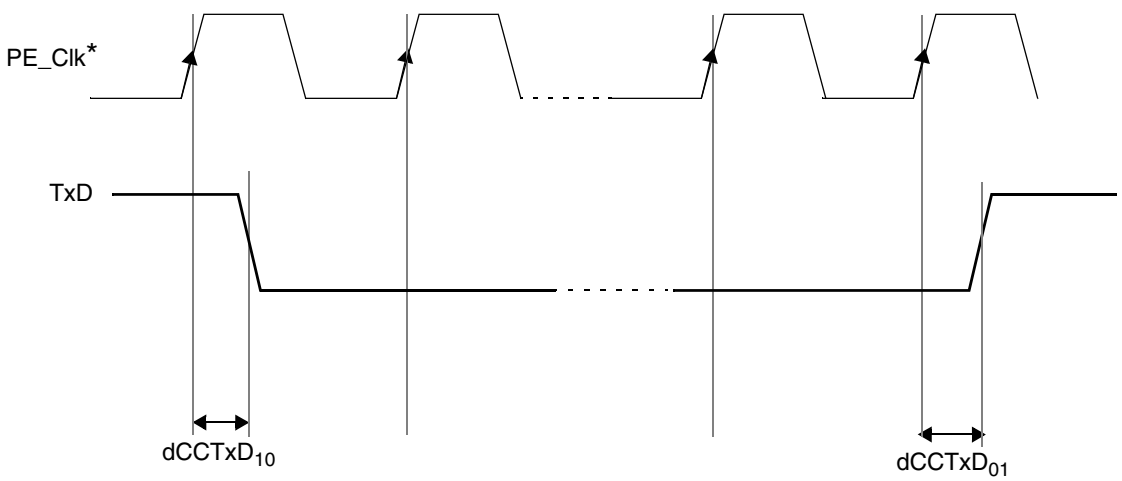
Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load	–2.45	2.45	ns

Table continues on the next page...

Table 38. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
	(=$dCCTxD_{50\%}$ - 100 ns)			
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9	ns
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +10%, T_J = –40 °C / 150°C, TxD pin load maximum 25 pF



*FlexRay Protocol Engine Clock

Figure 20. FlexRay TxD signal propagation delays

9.2.3 RxD

Table 39. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +10%, T_J = –40 / 150 °C

9.2.4 Receiver asymmetry

Table 40. Receiver asymmetry

Name	Description	Min	Max	Unit
$dCCRxAsymAccept_{15}$	Acceptance of asymmetry at receiving CC with 15 pF load (*)	–31.5	+44.0	ns
$dCCRxAsymAccept_{25}$	Acceptance of asymmetry at receiving CC with 25 pF load (*)	–30.5	+43.0	ns

9.3 LVDS Fast Asynchronous Transmission (LFAST) electrical characteristics

The following table provides output driver characteristics for LFAST I/Os.

Table 41. LFAST output buffer electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
$\lvert\Delta_{VO_L}\rvert$	Absolute value for differential output voltage swing (terminated)	—	100	200	285	mV
V_{ICOM_L}	Common mode voltage	—	1.08	1.2	1.32	V
T_{tr_L}	Transition time output pin LVDS configuration	—	0.2	—	1.5	ns

1. $V_{DD_HV_IOx}$ = 3.3 V (–5%, +10%), T_J = –40 / 150 °C, unless otherwise specified.

NOTE

Fast IOs must be specified only as fast (and not as high current). See GPIO DC electrical specification.

9.3.1 LFAST interface timing diagrams

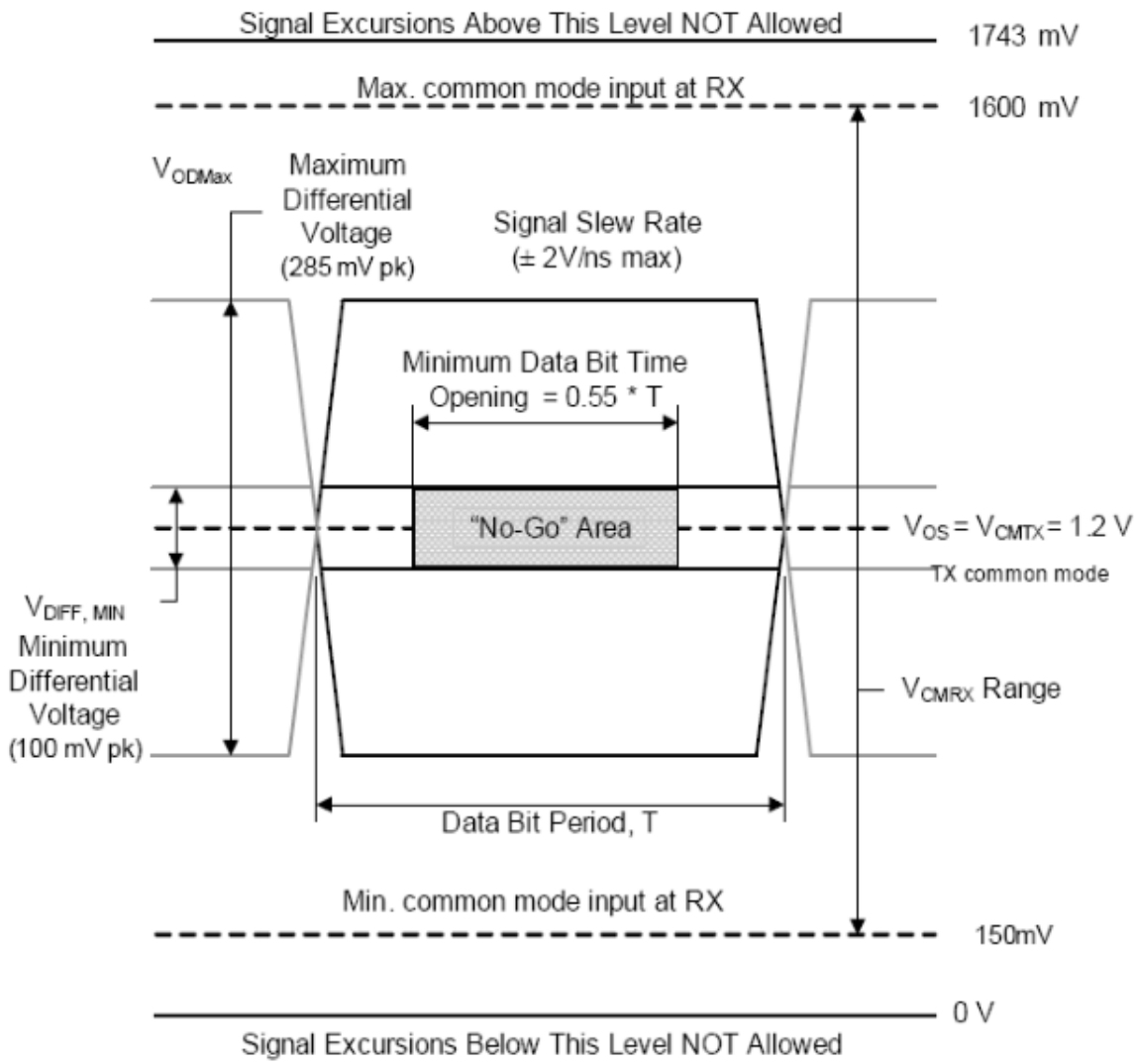


Figure 21. LFAST timing definition

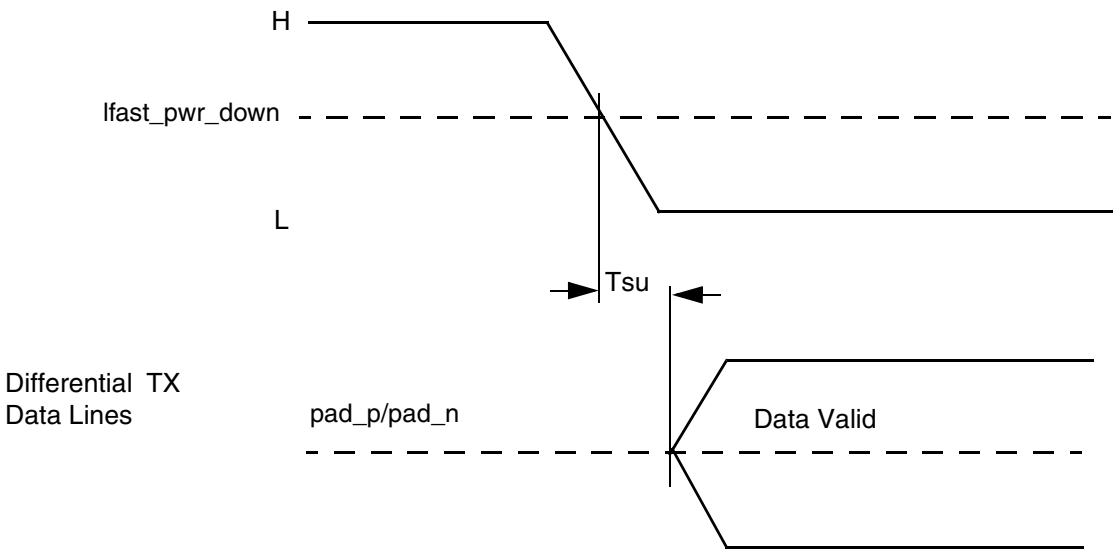


Figure 22. Power-down exit time

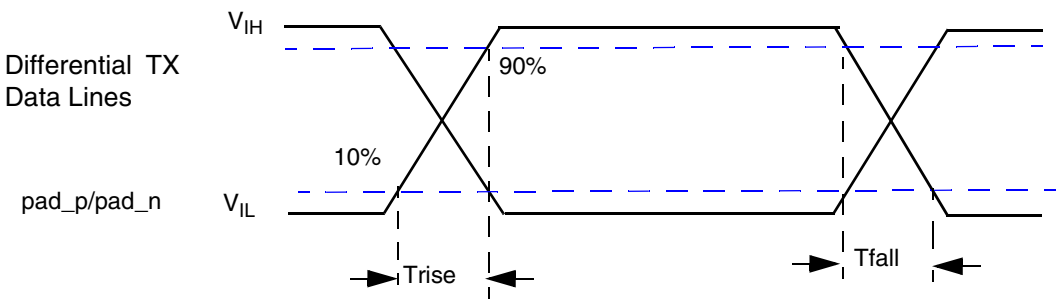


Figure 23. Rise/fall time

9.3.2 LFAST interface electrical characteristics

NOTE

While LFAST is operating and 'Ready' (nex_rdy_b) signal is used by the debugger on PAD_132, the recommended SRE settings are ‘00' and ‘01'. TCK should be used with low frequency (preferably less than 10 MHz).

Table 42. LFAST electrical characteristics

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
Data Rate						
DATARATE	Data rate	—	—	312/320	Typ+0.1%	Mbps
STARTUP						
T_{STRT_BIAS}	Bias startup time[2]	—	—	0.5	3	µs

Table continues on the next page...

Table 42. LFAST electrical characteristics (continued)

Symbol	Parameter	Conditions[1]	Value			Unit
			Min	Typ	Max	
T_{PD2NM_TX}	Transmitter startup time (power down to normal mode)[3]	—	—	0.2	2	µs
T_{SM2NM_TX}	Transmitter startup time (sleep mode to normal mode)[4]	—	—	0.2	0.5	µs
T_{PD2NM_RX}	Receiver startup time[5] (Power down to Normal mode)	—	—	20	40	ns
T_{PD2SM_RX}	Receiver startup time[4] (Power down to Sleep mode)	—	—	20	50	ns
TRANSMITTER						
V_{OS_DRF}	Common mode voltage	—	1.08	—	1.32	V
$\lvert\Delta V_{OD_DRF}\rvert$	Differential output voltage swing (terminated)	—	±100	±200	± 285	mV
T_{TR_DRF}	Rise/Fall time (10% - 90% of swing)	—	0.26	—	1.5	ns
R_{OUT_DRF}	Terminating resistance		67	—	198	Ω
C_{OUT_DRF}	Capacitance[6]	—	—	—	5	pF
RECEIVER						
V_{ICOM_DRF}	Common mode voltage	—	0.15[7]	—	1.6[8]	V
$\lvert D_{VI_DRF}\rvert$	Differential input voltage	—	100	—	—	mV
V_{HYS_DRF}	Input hysteresis	—	25	—	—	mV
R_{IN_DRF}	Terminating resistance		80	115	150	Ω
C_{IN_DRF}	Capacitance[9]	—	—	3.5	6	pF
L_{IN_DRF}	Parasitic Inductance[10]	—	—	5	10	nH
TRANSMISSION LINE CHARACTERISTICS (PCB Track)						
Z_0	Transmission line characteristic impedance	—	47.5	50	52.5	Ω
Z_{DIFF}	Transmission line differential impedance	—	95	100	105	Ω

1. $V_{DD_VH_IOx}$ = 3.3 V -5%,+10%, T_J = –40 / 150 °C, unless otherwise specified
2. Startup time is defined as the time taken by LFAST current reference block for settling bias current after its pwr_down (power down) has been deasserted. LFAST functionality is guaranteed only after the startup time.
3. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
4. Startup time is defined as the time taken by LFAST transmitter for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.
5. Startup time is defined as the time taken by LFAST receiver for settling after its pwr_down (power down) has been deasserted. Here it is assumed that current reference is already stable. LFAST functionality is guaranteed only after the startup time.

6. Total lumped capacitance including silicon, package pin and bond wire. Application board simulation is needed to verify LFAST template compliancy.
7. Absolute min = 0.15 V – (285 mV / 2) = 0 V
8. Absolute max = 1.6 V + (285 mV / 2) = 1.743 V
9. Total capacitance including silicon, package pin and bond wire
10. Total inductance including silicon, package pin and bond wire

9.4 Serial Peripheral Interface (SPI) timing specifications

The following table describes the SPI electrical characteristics.

MTEF=1 Mode timing values given below are only applicable when external SPI is in classic mode. Slave mode timing values given below are applicable when device is in MTFE=0.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured as SRE = 11.

Table 43. SPI timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	SPI cycle time	Master (MTFE = 0)	50	—	ns
			Master (MTFE = 1)	50	—	
			Slave (MTFE = 0)	50	—	
			Slave Receive Only mode[1]	16	—	
2	t_{CSC}	PCS to SCK delay	Master	63.8[2]	—	ns
3	t_{ASC}	After SCK delay	Master	68.8[3]	—	ns
4	t_{SDC}	SCK duty cycle	Master[4]	$t_{SCK}/2 - 1$	$t_{SCK}/2 + 1$	ns
			Slave[5]	—	—	ns
			Slave Receive only mode[6]	tSCK/2 – 0.750	tSCK/2 + 0.750	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	25	ns
6	t_{DIS}	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	25	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13 [7]	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13 [8]	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	15	—	ns
			Slave	2	—	
			Slave Receive Mode	2	—	
			Master (MTFE = 1, CPHA = 0)[9]	15-N x SPI IPG clock period[10]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	–2	—	ns
			Slave	4	—	
			Slave Receive Mode	4	—	

Table continues on the next page...

Table 43. SPI timing (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
			Master (MTFE = 1, CPHA = 0)[9]	-2 + N x SPI IPG clock period [10]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	7 [11]	ns
			Slave	—	23	
			Master (MTFE = 1, CPHA = 0)[12]	—	7 + SPI IPG Clock Period	
			Master (MTFE = 1, CPHA = 1)	—	7	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	–4 [11]	—	ns
			Slave	3.8	—	
			Master (MTFE = 1, CPHA = 0) [12]	-4 + SPI IPG Clock Period	—	
			Master (MTFE = 1, CPHA = 1)	–4	—	

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50. Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters (t_{SUI}, t_HI, t_{SUO} and t_{HO}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters (t_{SUI} and t_{HI}) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below t_{sdc}(min) corresponding to the t_{sdc}(min) for the slave receive mode.
7. In the master mode, this is governed by t_{PCSSCK}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by t_{PASC}. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SPI_MCR[SMPL_PT] should be set to 1.

NOTE

For numbers shown in the following figures, see Table 43.

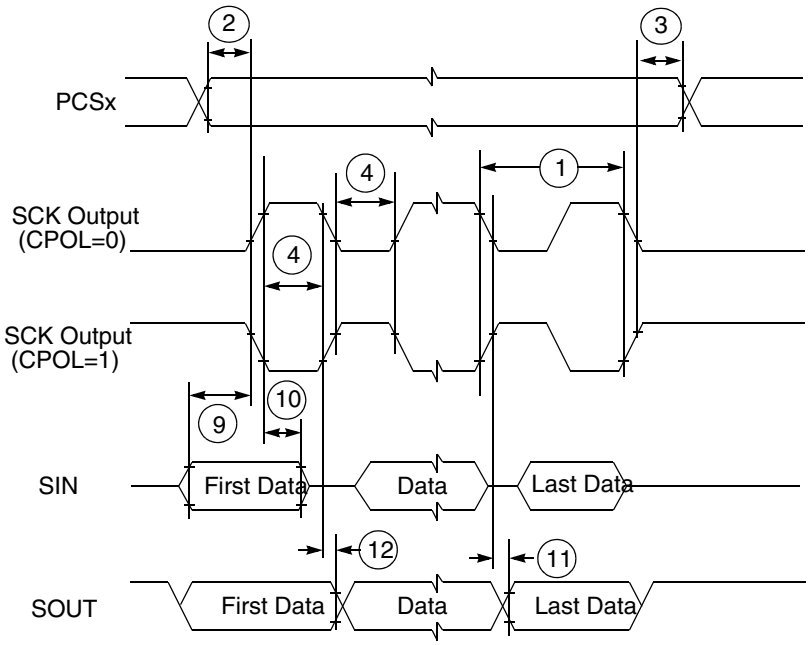


Figure 24. SPI classic SPI timing — master, CPHA = 0

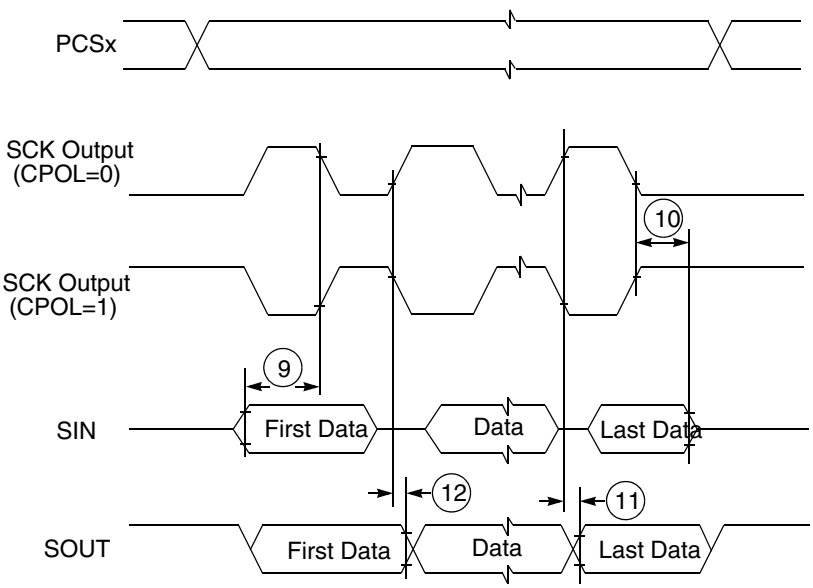


Figure 25. SPI classic SPI timing — master, CPHA = 1

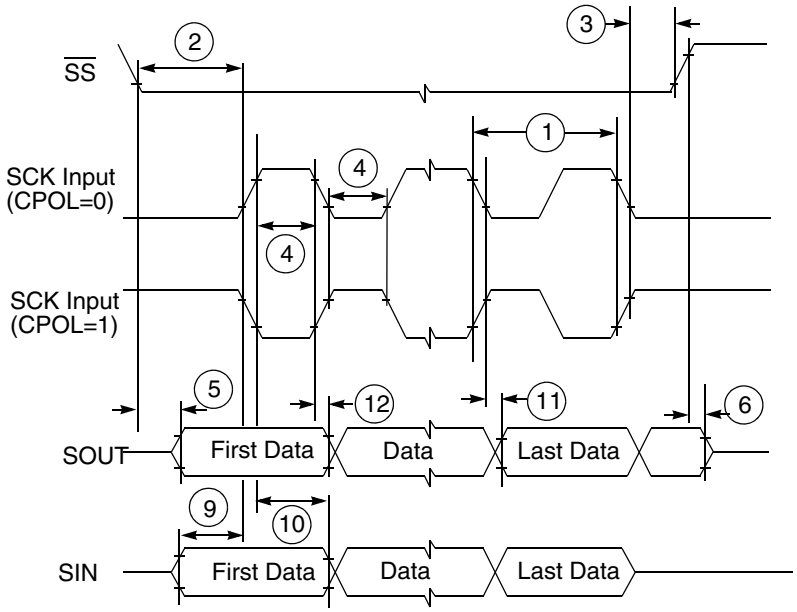


Figure 26. SPI classic SPI timing — slave, CPHA = 0

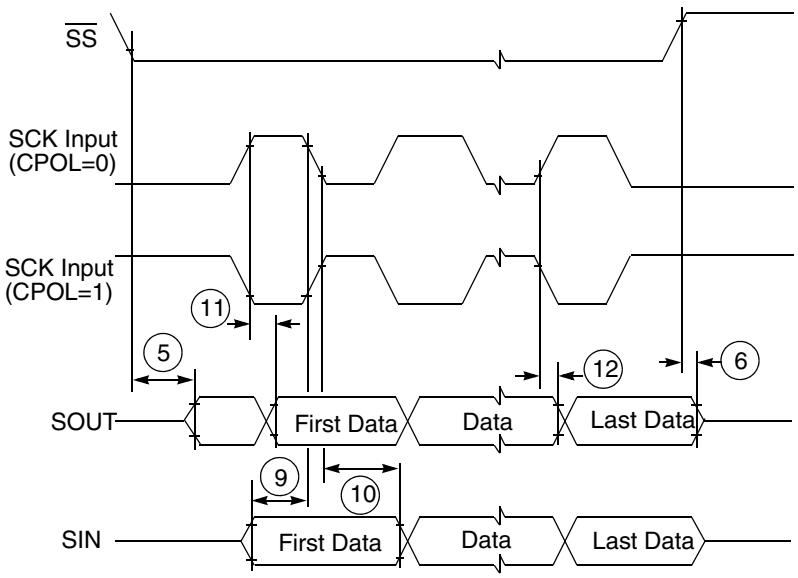


Figure 27. SPI classic SPI timing — slave, CPHA = 1

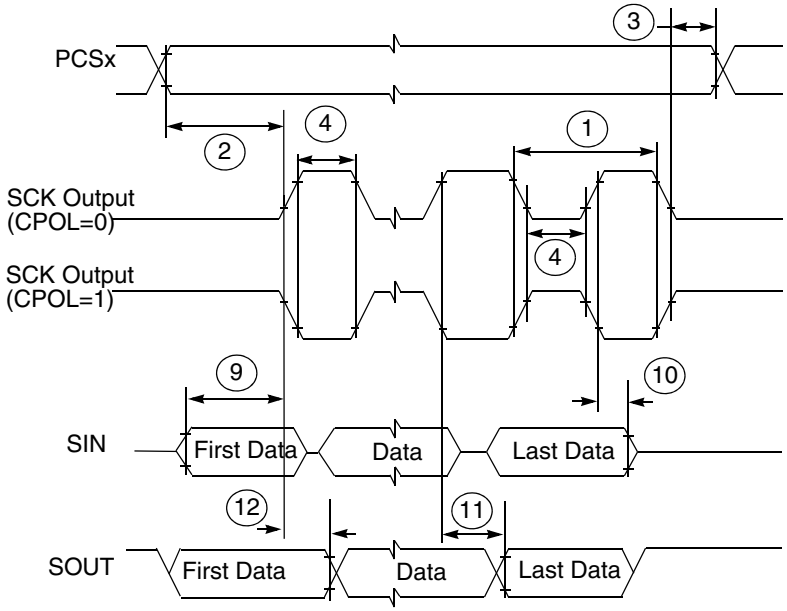


Figure 28. SPI modified transfer format timing — master, CPHA = 0

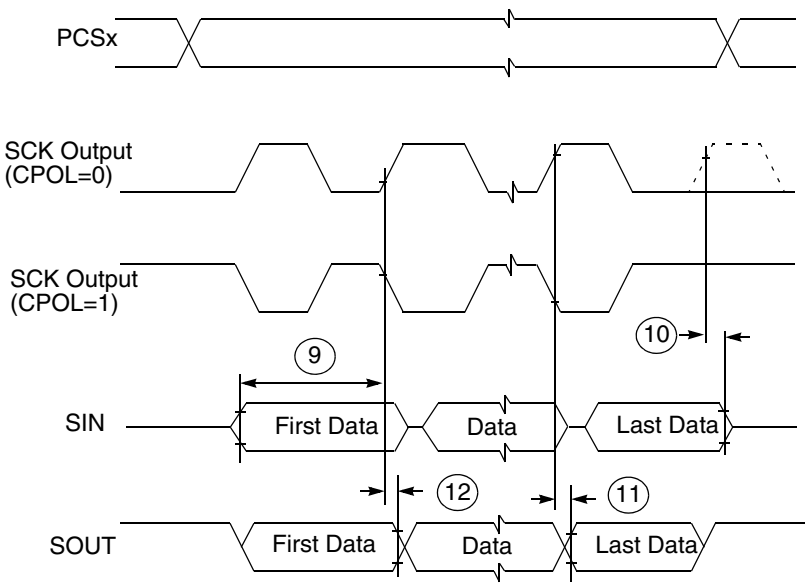


Figure 29. SPI modified transfer format timing — master, CPHA = 1

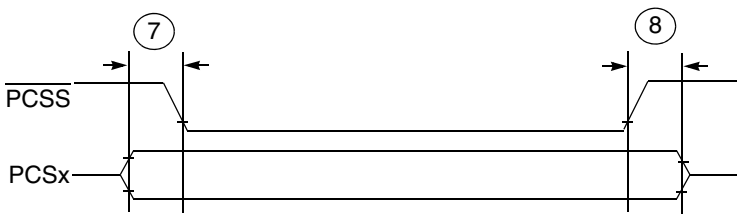


Figure 30. SPI PCS strobe (PCSS) timing

9.5 LINFlexD timing specifications

The maximum bit rate is 1.875 MBit/s.

9.6 I²C timing

Table 44. I²C SCL and SDA input timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	I_tHD:STA	Start Condition hold time	2	-	Peripheral clock
2	I_t_LOW	Clock low time	8	-	
3	I_tHD:DAT	Data hold time	2	-	
4	I_tHIGH	Clock high time	4	-	
5	I_tSU:DAT	Data setup time	4	-	
6	I_tSU:STA	Start condition setup time (for repeated start condition only)	2	-	
7	I_tSU:STOP	Stop condition setup time	2	-	

Table 45. I²C SCL and SDA output timing specifications

Number	Symbol	Parameter	Value		Unit
			Min	Max	
1	O_tHD:STA	Start condition hold time[1]	6	-	Peripheral clock
2	O_t_LOW	Clock low time[1]	10	-	
3	O_tHD:DAT	Data hold time[1]	7	-	
4	O_t_HIGH	Clock high time[1]	10	-	
5	O_tSU:DAT	Data setup time[1]	2	-	
6	O_tSU:STA	Start condition setup time (for repeated start condition only)[1]	20	-	
7	O_tSU:STOP	Stop condition setup time[1]	10	-	
8	O_tr	SCL/SDA rise time[2]	-	99.6	ns
9	O_tf	SCL/SDA fall time[1]	-	99.6	

1. Programming IBFD (I²C Bus Frequency Divider Register) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR (I²C Bus Data I/O Register).
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

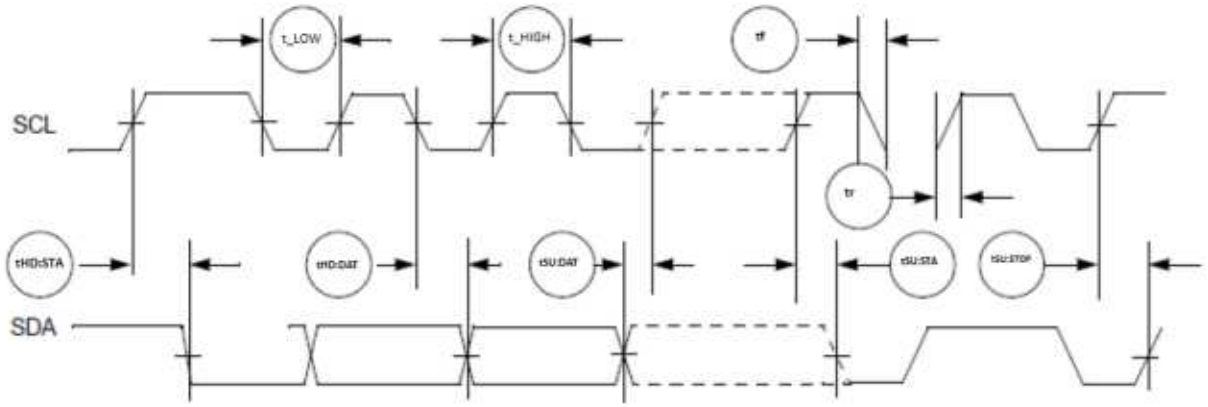


Figure 31. I²C input/output timing

10 Debug modules

10.1 JTAG/CJTAG interface timing

The following table lists JTAGC/CJTAG electrical characteristics.

- Measurements are with input transition of 1 ns, output load of 50 pF and pads configured with SRE=11.

Table 46. JTAG/CJTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}[2]	TCK Cycle Time (JTAG)	36	—	ns
		TCK Cycle Time (CJTAG)	50		
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO/TMS Data Valid [3]	—	15[4]	ns
7	t_{TDOI}	TCK Low to TDO/TMS Data Invalid[3]	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO/TMS High Impedance[3]	—	22	ns
9	t_{JCMPPW}	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[5]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns

Table continues on the next page...

Table 46. JTAG/CJTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency.
3. TMS timing is applicable only in CJTAG mode
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

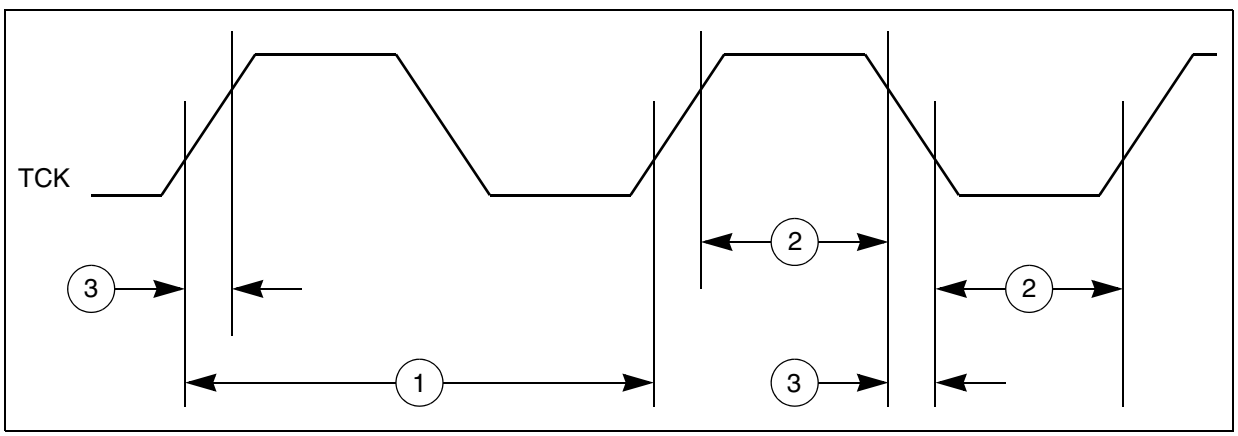


Figure 32. JTAG test clock input timing

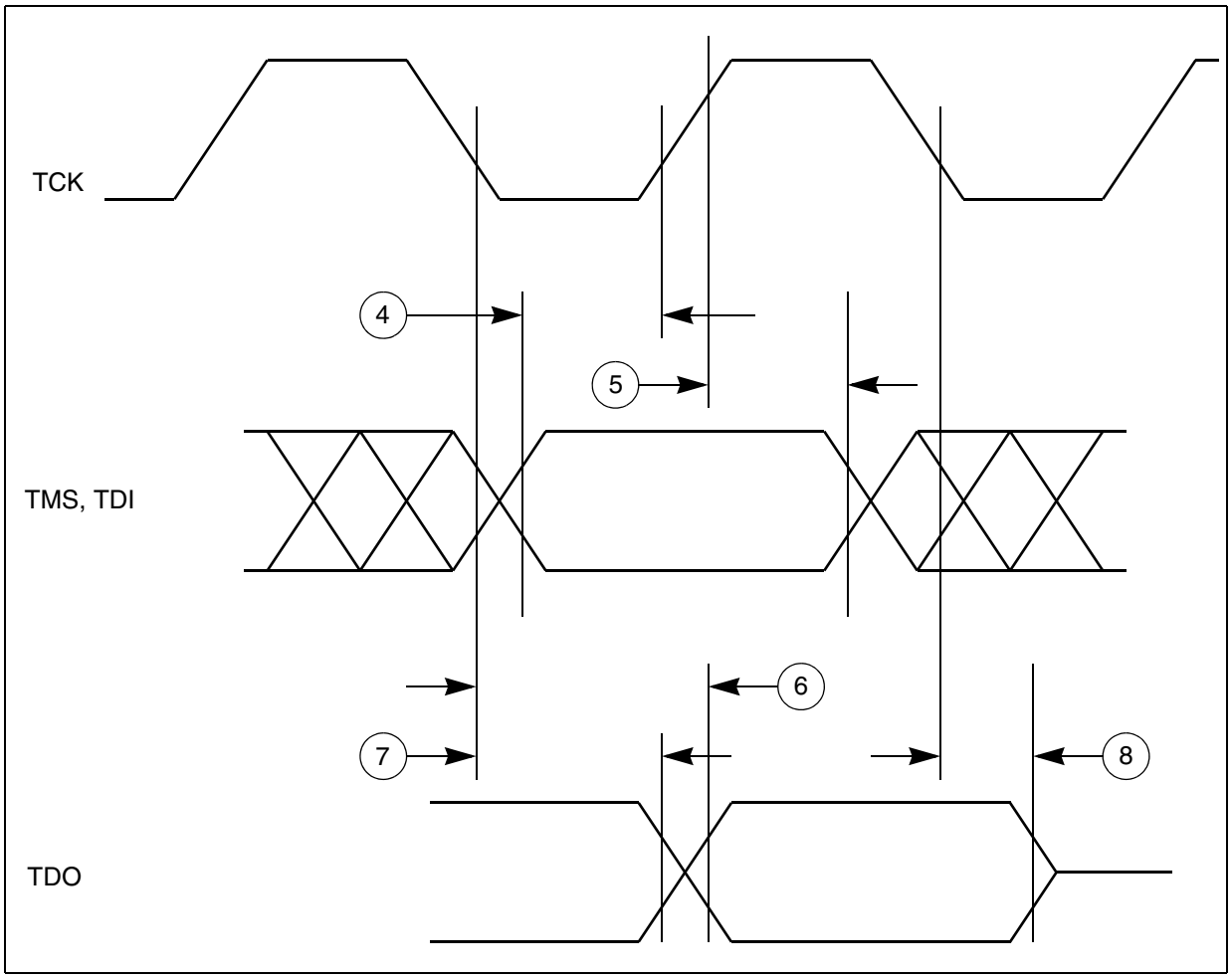


Figure 33. JTAG test access port timing

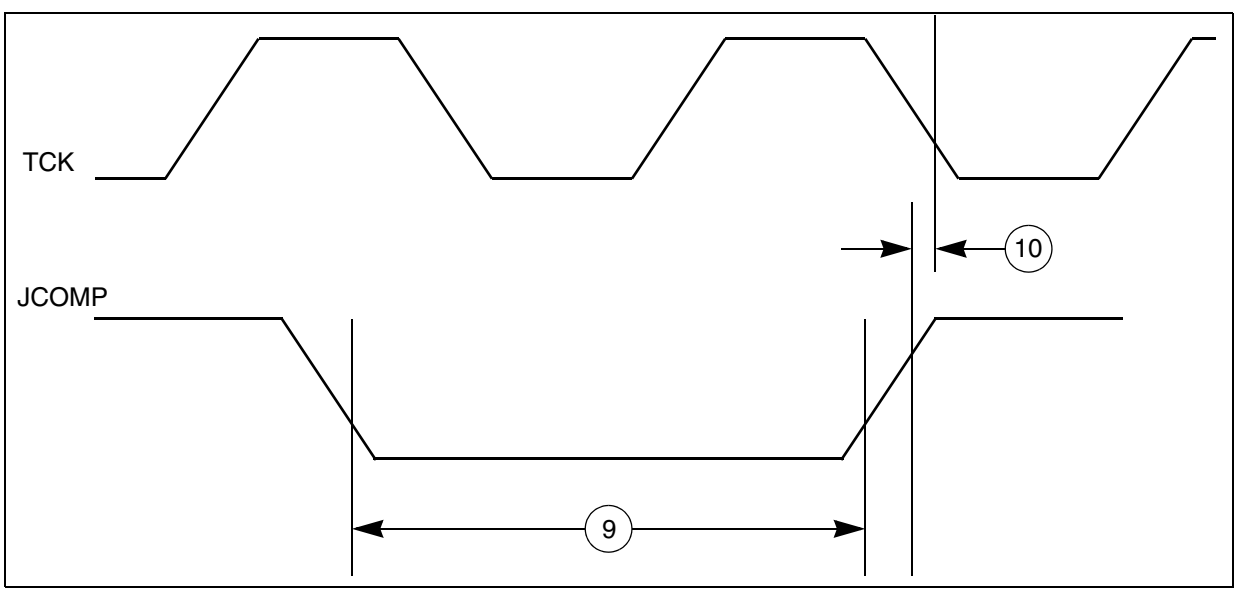


Figure 34. JTAG JCOMP timing

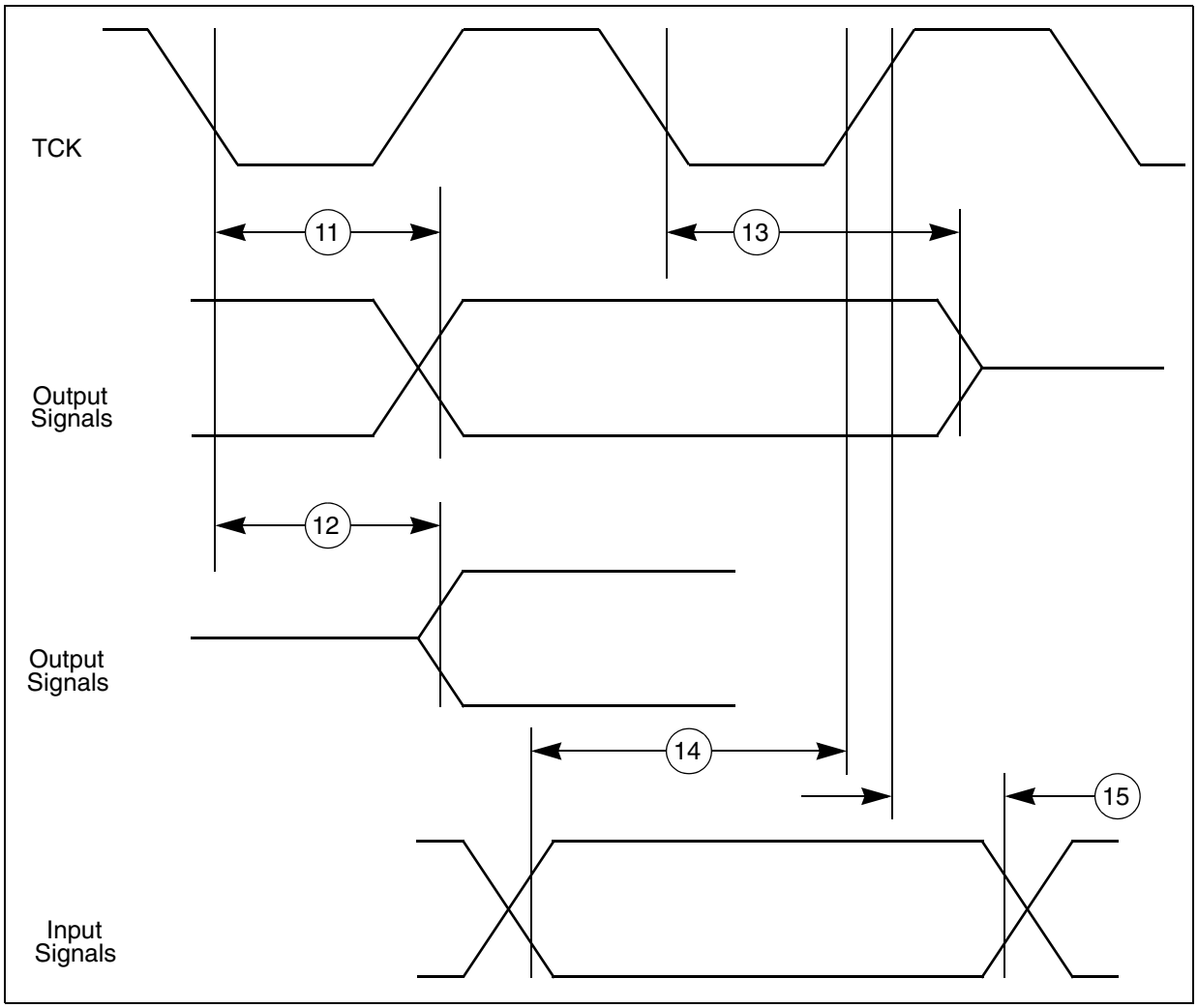


Figure 35. JTAG boundary scan timing

10.2 Nexus Aurora debug port timing

Table 47. Nexus Aurora debug port timing

#	Symbol	Characteristic	Min	Max	Unit
1	t_{REFCLK}	Reference clock frequency	625	1250	MHz
1a	t_{MCYC}	Reference Clock rise/fall time	—	400	ps
2	t_{RCDC}	Reference Clock Duty Cycle	45	55	%
3	J_{RC}	Reference Clock jitter	—	40	ps
4	$t_{STABILITY}$	Reference Clock Stability	50	—	PPM
5	BER	Bit Error Rate	—	10^{-12}	—
6	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}
7	J_D	Transmit lane Deterministic Jitter	—	0.17	OUI
8	J_T	Transmit lane Total Jitter	—	0.35	OUI

Table continues on the next page...

Table 47. Nexus Aurora debug port timing (continued)

#	Symbol	Characteristic	Min	Max	Unit
9	S_O	Differential output skew	—	20	ps
10	S_{MO}	Lane to lane output skew	—	1000	ps
11	OUI	Aurora lane Unit Interval	800	800	ps

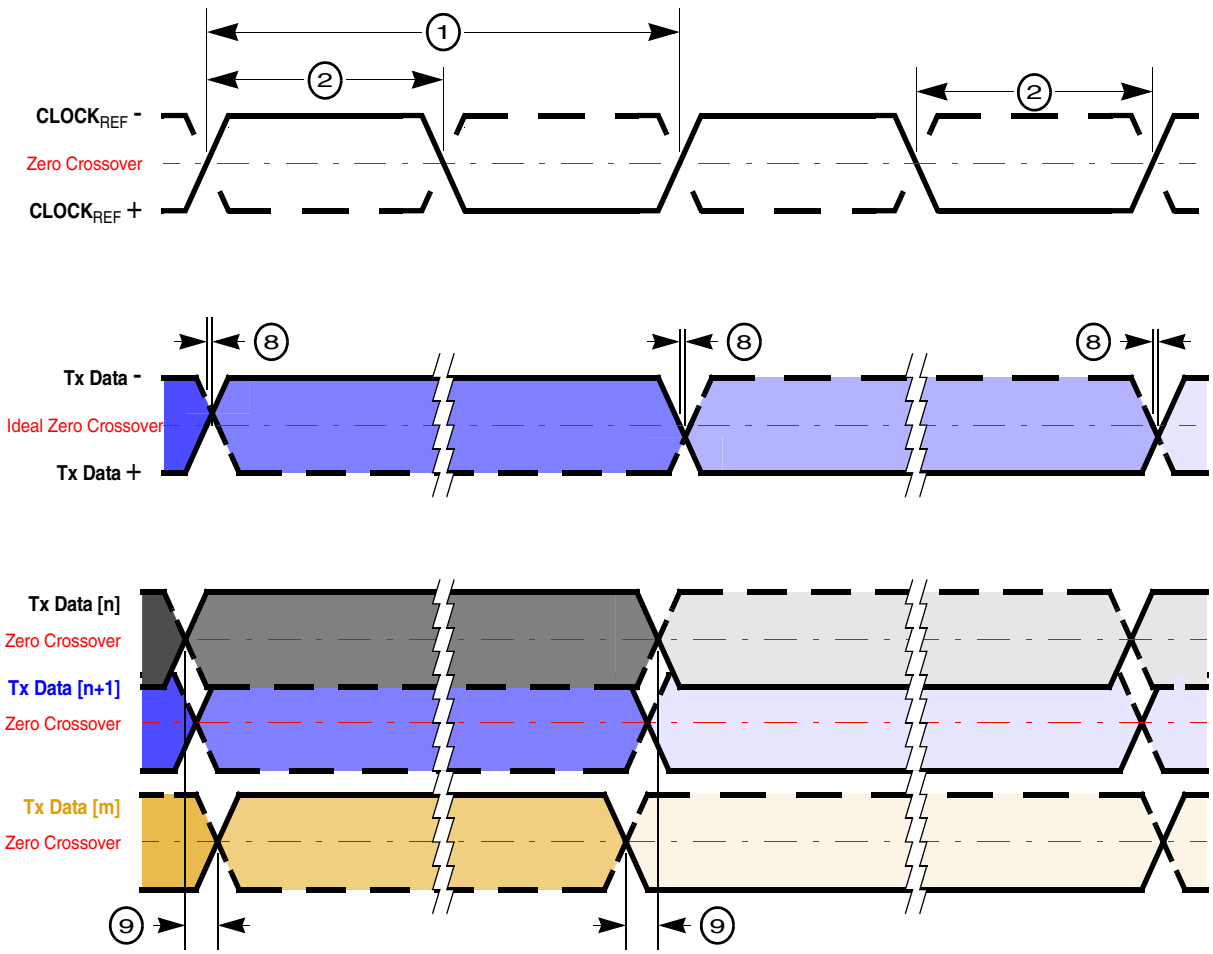


Figure 36. Nexus Aurora timings

11 WKUP/NMI timing specifications

Table 48. WKUP/NMI glitch filter

Symbol	Parameter	Min	Typ	Max	Unit
W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
W_{NFNMI}	NMI pulse width that is passed	400	—	—	ns

12 External interrupt timing (IRQ pin)

Table 49. External interrupt timing

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time[1]	—	6	—	t_{CYC}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

NOTE

tCYC is equivalent to TCK (prescaled filter clock period) which is the IRC clock prescaled to the Interrupt Filter Clock Prescaler (IFCP) value. TCK = T(IRC) x (IFCP + 1) where T(IRC) is the internal oscillator period. Refer SIUL2 chapter of the device reference manual for details.

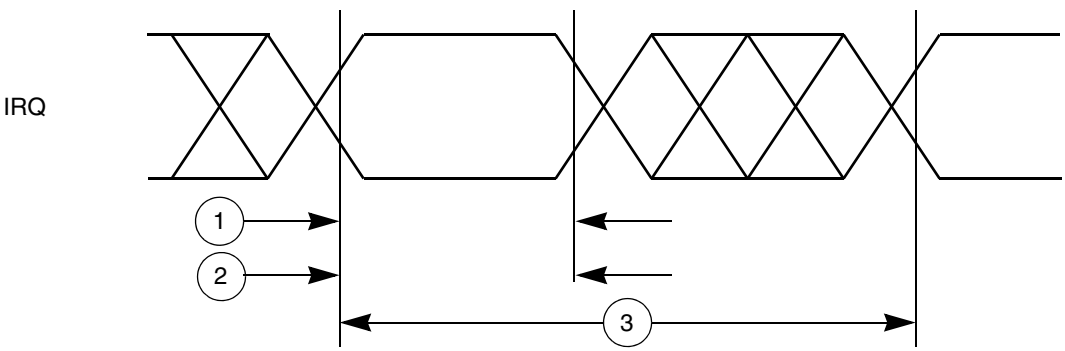


Figure 37. External interrupt timing

13 Temperature sensor electrical characteristics

The following table describes the temperature sensor electrical characteristics.

Table 50. Temperature sensor electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
—	Temperature monitoring range		-40	—	150	°C
T_{SENS}	Sensitivity		—	5.18	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 to 150°C	5	—	5	°C

14 Radar module

14.1 MIPICSI2 D-PHY electrical and timing specifications

This section describes MIPICSI2[1] D-PHY electrical specifications, compliant with MIPICSI2 version 1.1, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes).

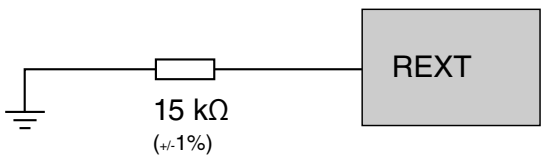


Figure 38. MIPICSI2 circuit

Table 51. Calibrator specifications

Symbol	Parameters	Min	Typ	Max	Unit
R_{EXT}	External reference resistor, 1% accuracy (or better), for auto calibration	-	15	-	kΩ
T_{cal}	Time from when PD signal goes low to when CALCOMPL goes high	-	2	2.5	µs

14.1.1 Electrical and timing information

Table 52. Electrical and timing information

Symbol	Parameters	Min	Typ	Max	Unit
HS Line Receiver DC Specifications					
V_{IDTH}	Differential input high voltage threshold	-	-	70	mV
V_{IDTL}	Differential input low voltage threshold	-70	-	-	mV
V_{IHHS}	Single ended input high voltage	-	-	460	mV
V_{ILHS}	Single ended input low voltage	-40	-	-	mV
V_{CMRXDC}	Input common mode voltage	70	-	330	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
Z_{ID}	Differential input impedance	80	-	125	ohm
LP Line Receiver DC Specifications					
V_{ILLP}	Input low voltage	-	-	550	mV

Table continues on the next page...

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Table 52. Electrical and timing information (continued)

Symbol	Parameters	Min	Typ	Max	Unit
V_{IHLP}	Input high voltage	880	-	-	mV
V_{HYST}	Input hysteresis	25	-	-	mV

14.1.2 D-PHY signaling levels

The signal levels are different for differential HS mode and single-ended LP mode. The figure below shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

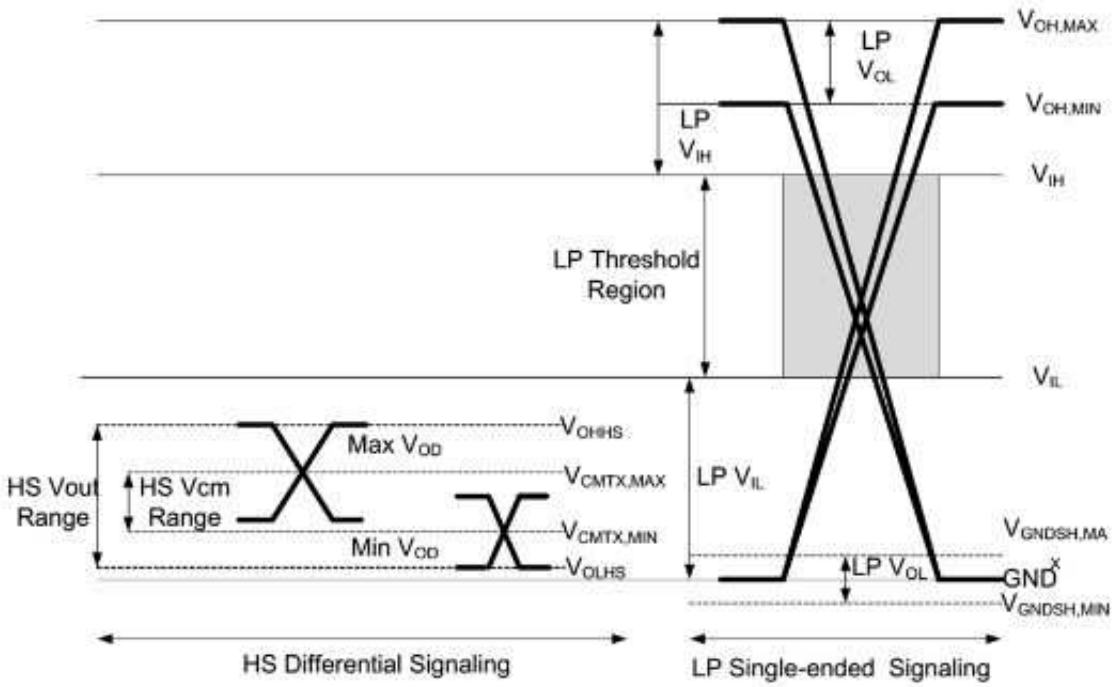


Figure 39. D-PHY signaling levels

14.1.3 D-PHY switching characteristics

Table 53. D-PHY switching characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HS Line Receiver AC Specifications						
-	Maximum serial data rate	On DATAP/N inputs. 80 Ohm<= RL <= 125 Ohm	80	-	1000	Mbps

Table continues on the next page...

Table 53. D-PHY switching characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔVCMRX(HF)	Common mode interference beyond 450 MHz		-	-	100	mVpp
ΔVCMRX(LF)	Common mode interference between 50 MHz and 450 MHz		-50	-	50	mVpp
CCM	Common mode termination		-	-	60	pF
LP Line Receiver AC Specification						
e_{SPIKE}	Input pulse rejection		-	-	300	Vps
T_{MIN}	Minimum pulse response		20	-	-	ns
V_{INT}	Pk-to-Pk interference voltage		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

14.1.4 Low-power receiver timing

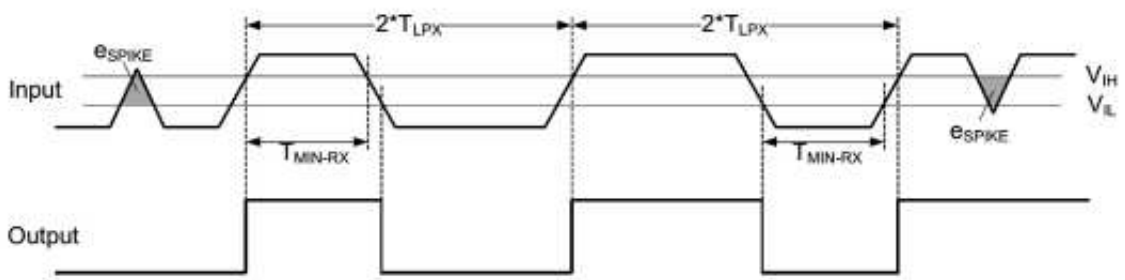


Figure 40. Input Glitch Rejection of Low-Power Receivers

14.1.5 Data to clock timing

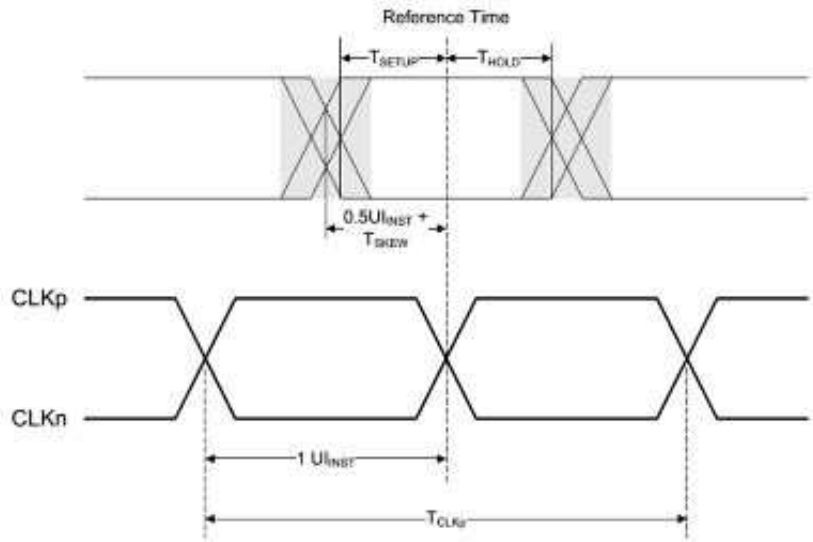


Figure 41. Definition

Table 54. Data to clock timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{CLKP}	Clock Period	40	-	500	MHz
UI_{INST}	UI Instantaneuous	1	-	12.5	ns
T_{SETUP}	Data to Clock Setup Time	0.15	-	-	UIINST
T_{HOLD}	Clock to Data Hold Time	0.15	-	-	UIINST

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15 Thermal Specifications

15.1 Thermal characteristics

Table 55. 257MAPBGA package thermal characteristics

Symbol	Parameter	Conditions	257MAPBGA	Unit
$R_{\theta JA}$	Thermal resistance, junction-to-ambient natural convection [1, 2]	Single layer board - 1s	41.8	°C/W
		Four layer board - 2s2p[3]	22.3	
$R_{\theta JMA}$	Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1, 3]	Single layer board - 1s	29.8	°C/W
		Four layer board - 2s2p	17.7	
$R_{\theta JB}$	Thermal resistance junction-to-board[4]	—	7.6	°C/W
$R_{\theta JC}$	Thermal resistance junction-to-case[5]	—	5.2	°C/W
Ψ_{JT}	Junction-to-package-top natural convection[6]	—	0.2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

15.1.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

$$T_J = T_{BRD} + (R_{\theta JB} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JB}$ = junction to board thermal resistance (°C/W)
- $T_{\theta BRD}$ = average board temperature just outside the package periphery (°C)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard parameter that provides a quick and easy estimation of thermal performance. However, junction to board thermal resistance is more appropriate for tight enclosure spaces where board temperature should be used as reference temperature. Using 2s2p board with natural convection conditions, junction temperature is found to be less than 150°C . There are two parameters in common usage: the value determined on a single layer board and the value obtained on a board with two inner planes. For packages such as PBGA, these values can significantly differ. For customer board design with different number of layers and copper percentage content, these values must be appropriately interpolated in order to evaluate junction temperature. In general, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the

package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

15.1.2 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

16 Packaging

The S32R274 is offered in the following package types.

If you want the drawing for this package	Then use this document number
257-ball MAPBGA	98ASA00081D

NOTE

For detailed information regarding package drawings, refer to www.nxp.com.

17 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

17.1 Reset sequence duration

Table 57 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 57. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ	Max[1]	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	15		50[2]	ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	400		2000	µs
3	T_{ERLB}	External Reset Sequence Long, BIST enabled	15		50	ms
4	T_{FRL}	Functional Reset Sequence Long, BIST disabled	400		2000	µs
5	T_{FRS}	Functional Reset Sequence Short[3]	1		500	µs

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.
2. Max time is based on STCU BIST configuration execution time + max RESET time (TDR). For default STCU BIST configuration execution time, refer to EB834. Contact your NXP sales representative for details.
3. BIST is not executed on short functional reset

17.2 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 57.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The SMPS self test is always triggered during Phase3 after a destructive reset so that duration is included into Phase3 below.

In external regulation mode, the VREG_POR_B pin should be de-asserted only when all the design supplies are in operating range. Deassertion of VREG_POR_B pin triggers the start of reset sequence in internal as well as external regulation modes.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only

be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 57 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

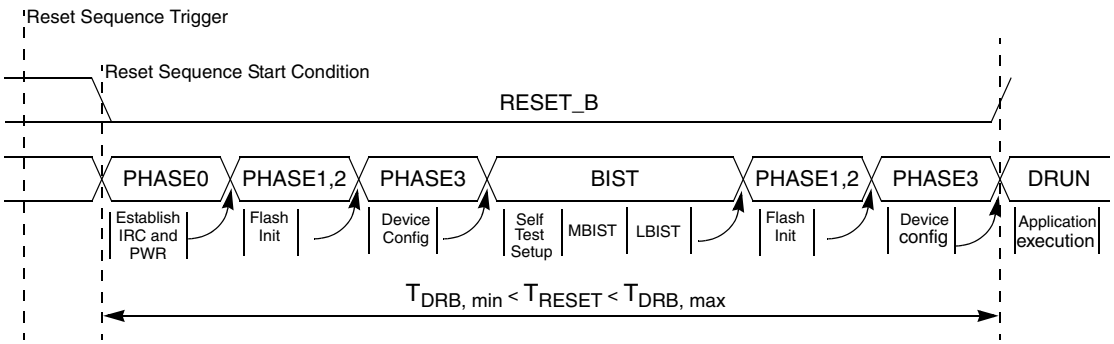


Figure 42. Destructive reset sequence, BIST enabled

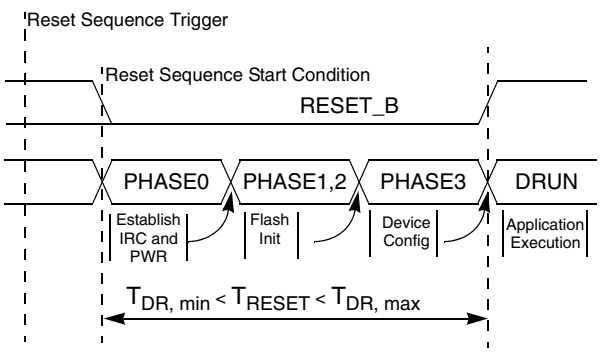


Figure 43. Destructive reset sequence, BIST disabled

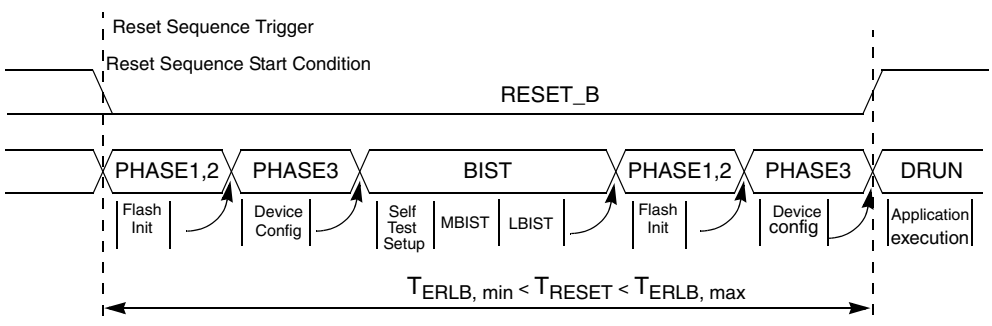


Figure 44. External reset sequence long, BIST enabled

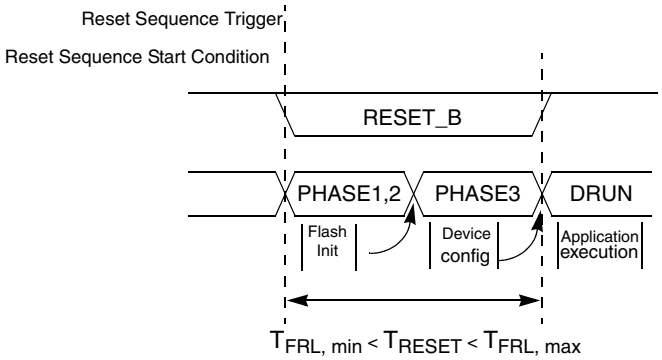


Figure 45. Functional reset sequence long

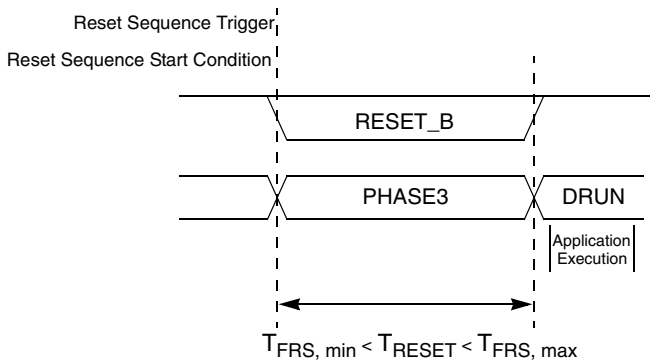


Figure 46. Functional reset sequence short

The reset sequences shown in Figure 45 and Figure 46 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

18 Power sequencing requirements

The device does not require any specific power sequencing as far as user follows recommendations in this section.

Either ramp $V_{DD_HV_IO}$ and $V_{DD_HV_PMU}$ together or ramp $V_{DD_HV_IO}$ before $V_{DD_HV_PMU}$ such that the two supplies always maintain 100 mV or less difference, when using internal regulation mode. $V_{DD_LV_DPHY}$ and $V_{DD_LV_CORE}$ are to be driven from same source. $V_{DD_HV_IO}$, $V_{DD_HV_IO_RGMII}$, $V_{DD_HV_IO_PWM}$ and $V_{DD_HV_IO_LFAST}$ supplies should be treated as a single supply from board perspective.

As mentioned in the previous section, it is expected that the external ASIC which powers up the device in external regulation mode deasserts VREG_POR_B pin only when all the power supplies to the design are in operating range.

It should be noted that LVD and HVD detectors on VDD supply are disabled by default in external regulation mode for preventing a conflict with external regulator operation but they can be enabled by software once design is powered up.

While designing the system, it is important to ensure that AFE supplies are powered up before data is sent on its input pads.

19 Pinouts

19.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

20 Revision History

Table 58. Revision History

Revision	Date	Description

Rev 4	May, 2018	• Removed section "4.1 Introduction".
		• Removed section "3.2 Format".
		• In Fields, removed figure "Commercial product code structure".
		• In Nexus Aurora debug port timing, added t_{EVTIPW} row.
		• In Ethernet switching specifications changed the following:
		  • Updated the figure RMII/MII serial management channel timing diagram.
		  • In Ethernet MDIO timing table changed MDC10 Min value and MDC11 Max value.
		• Extensively updated Table 32.
		• In Table 7, changed $V_{inxosccllkvih}$ Max value from 1.2 to 1.23.
		• In Table 25, added rows for the symbols $t_{sampleC}$, $t_{sampleS}$,$t_{sampleBG}$, and $t_{sampleTS}$.
		• In Table 6, changed V_{INA} maximum value to 6.0.
		• Added the following footnotes in Absolute maximum ratings :
		  • The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
		  • The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.
		• In Table 7, changed V_{INA} maximum value to $V_{DD_HV_ADCREFx}$.
		• In Table 2 :
		  • Changed part from FS32R274KBK2MMM to FS32R274KSK2MMM and changed configuration from "B" to "S"
		  • Changed part from FS32R274KBK2VMM to FS32R274KSK2VMM and changed configuration from "B" to "S"
		  • Added "B or S" to Table 3

Rev 5	July 03, 2018	• In Table 6, Removed footnote on I_{INJPAD}.
Rev 5	April 30, 2019	• In Table 1, added information for 266 MHz frequency parts . • In Table 2, added the rows for "FS32R274JSK2MMM", "FS32R264KBK0MMM", "FS32R264KCK0MMM", "FS32R264JBK0MMM" and "FS32R264JCK0MMM". • Added the feature changes for S32R264 with respect to S32R274 in Feature list.

Table continues on the next page...

Table 58. Revision History (continued)

Revision	Date	Description
		• In Table 4, added the row for 266MHz frequency performance. • In Table 8, added the Conditions and Max value in I_{DD_CORE} for 266 MHz frequency. • Added note "S32R264 devices support AFE PLL while S32R274 devices support SDPLL", in Block diagram. • In Operating conditions, changed the footnote from "Full performance means Core0 running @ 120 MHz, Core1/2 running @ 240 MHz, SPT running @ 200 MHz, rich set of peripherals used" to "Full performance means full frequency".
Rev 6	May 24, 2021	• In Table 26, removed the $IMD_{SDA_MM_OFF}$, $SNDR_{SDA_MM_OFF}$ and $SNR_{SDA_MM_OFF}$ symbols.

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