# S-5716 Series

## LOW CURRENT CONSUMPTION OMNIPOLAR / UNIPOLAR DETECTION TYPE HALL EFFECT SWITCH IC

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Rev.1.7_00

This IC, developed by CMOS technology, is a high-accuracy Hall effect switch IC that operates with low current consumption.
The output voltage changes when this IC detects the intensity level of magnetic flux density. Using this IC with a magnet makes it possible to detect the open / close in various devices.
High-density mounting is possible by using the small SOT-23-3 package or the super small SNT-4A package.
Due to its high-accuracy magnetic characteristics, this IC can make operation's dispersion in the system combined with magnet smaller.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales representatives.

## ■ Features

- Pole detection*1: Detection of omnipolar, S pole or N pole
- Output logic*1: Active "L", active "H"
- Output form*1: Nch open-drain output, CMOS output
- Magnetic sensitivity*1: $B_{OP}$ = 1.8 mT typ.
  $B_{OP}$ = 3.0 mT typ.
  $B_{OP}$ = 3.4 mT typ.
  $B_{OP}$ = 4.5 mT typ.
  $B_{OP}$ = 7.0 mT typ.
- Operating cycle (current consumption): Product with omnipolar detection
  $t_{CYCLE}$ = 50.50 ms ($I_{DD}$ = 4.0 μA) typ.
  Product with S pole or N pole detection
  $t_{CYCLE}$ = 50.85 ms ($I_{DD}$ = 2.6 μA) typ.
- Power supply voltage range: $V_{DD}$ = 2.7 V to 5.5 V
- Operation temperature range: Ta = –40°C to +85°C
- Lead-free (Sn 100%), halogen-free

***1**. The option can be selected.

## ■ Applications

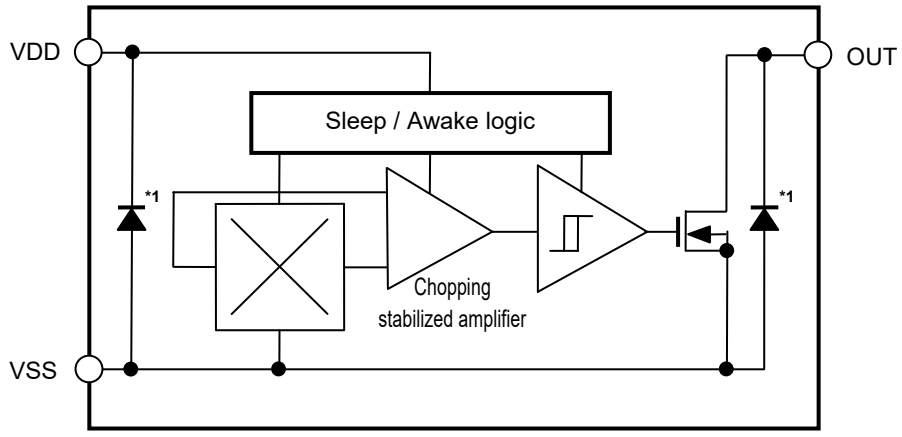
- Plaything, portable game
- Home appliance
- Housing equipment
- Industrial equipment

## ■ Packages

- SOT-23-3
- SNT-4A

## ■ Block Diagrams

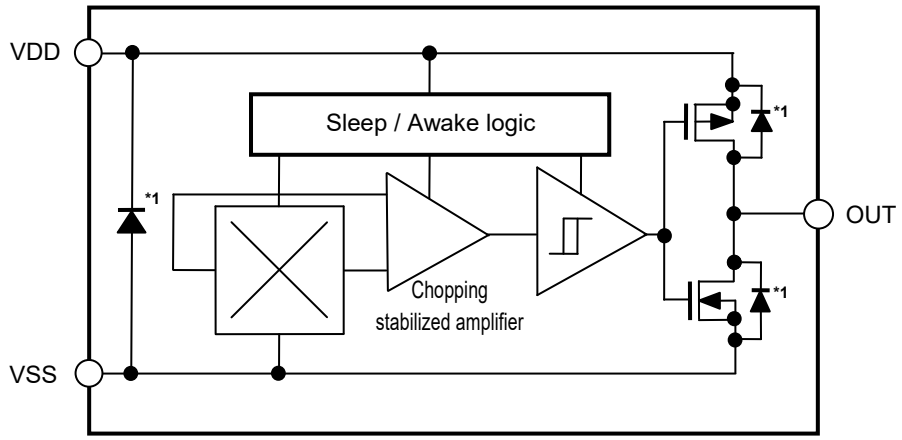
### 1. Nch open-drain output product




***1.** Parasitic diode

**Figure 1**

### 2. CMOS output product




***1.** Parasitic diode

**Figure 2**

## ■ Product Name Structure

### 1. Product name

**S-5716 A x x x x - xxxx U**

Environmental code
- U : Lead-free (Sn 100%), halogen-free

Package name (abbreviation) and packing specifications*1
- M3T1 : SOT-23-3, Tape
- I4T1 : SNT-4A, Tape

Magnetic sensitivity
- 0 : $B_{OP}$ = 1.8 mT typ.
- 1 : $B_{OP}$ = 3.0 mT typ.
- 7 : $B_{OP}$ = 3.4 mT typ.
- 2 : $B_{OP}$ = 4.5 mT typ.
- 3 : $B_{OP}$ = 7.0 mT typ.

Output logic
- L : Active "L"
- H : Active "H"

Pole detection
- D : Detection of both poles
- S : Detection of S pole
- N : Detection of N pole

Output form
- N : Nch open-drain output
- C : CMOS output

Operating cycle
- A : $t_{CYCLE}$ = 50.50 ms typ.
  (Product with both poles detection)
  $t_{CYCLE}$ = 50.85 ms typ.
  (Product with S pole or N pole detection)

***1.*** Refer to the tape drawing.

### 2. Packages

**Table 1 Package Drawing Codes**

| Package name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| SOT-23-3 | MP003-C-P-SD | MP003-C-C-SD | MP003-Z-R-SD | – |
| SNT-4A | PF004-A-P-SD | PF004-A-C-SD | PF004-A-R-SD | PF004-A-L-SD |

## 3. Product name list

### 3. 1 SOT-23-3

#### 3. 1. 1 Nch open-drain output product

**Table 2**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Output Form | Pole Detection | Output Logic | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|
| S-5716ANDL0-M3T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 1.8 mT typ. |
| S-5716ANDL1-M3T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 3.0 mT typ. |
| S-5716ANDL2-M3T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 4.5 mT typ. |
| S-5716ANDL3-M3T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 7.0 mT typ |
| S-5716ANSL0-M3T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 1.8 mT typ. |
| S-5716ANSL1-M3T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 3.0 mT typ. |
| S-5716ANSL2-M3T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 4.5 mT typ. |
| S-5716ANSL3-M3T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 7.0 mT typ. |
| S-5716ANNL1-M3T1U | 50.85 ms typ. | Nch open-drain output | N pole | Active "L" | 3.0 mT typ. |

**Remark** Please contact our sales representatives for products other than the above.

#### 3. 1. 2 CMOS output product

**Table 3**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Output Form | Pole Detection | Output Logic | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|
| S-5716ACDL0-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 1.8 mT typ. |
| S-5716ACDL1-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 3.0 mT typ. |
| S-5716ACDL7-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 3.4 mT typ. |
| S-5716ACDL2-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 4.5 mT typ. |
| S-5716ACDL3-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 7.0 mT typ |
| S-5716ACDH0-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 1.8 mT typ. |
| S-5716ACDH1-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 3.0 mT typ. |
| S-5716ACDH2-M3T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 4.5 mT typ. |
| S-5716ACSL0-M3T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 1.8 mT typ. |
| S-5716ACSL1-M3T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 3.0 mT typ. |
| S-5716ACSL2-M3T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 4.5 mT typ. |
| S-5716ACSL3-M3T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 7.0 mT typ. |

**Remark** Please contact our sales representatives for products other than the above.

### 3. 2 SNT-4A

#### 3. 2. 1 Nch open-drain output product

**Table 4**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Output Form | Pole Detection | Output Logic | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|
| S-5716ANDL0-I4T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 1.8 mT typ. |
| S-5716ANDL1-I4T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 3.0 mT typ. |
| S-5716ANDL2-I4T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "L" | 4.5 mT typ. |
| S-5716ANDH0-I4T1U | 50.50 ms typ. | Nch open-drain output | Omnipolar | Active "H" | 1.8 mT typ. |
| S-5716ANSL0-I4T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 1.8 mT typ. |
| S-5716ANSL1-I4T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 3.0 mT typ. |
| S-5716ANSL2-I4T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 4.5 mT typ. |
| S-5716ANSL3-I4T1U | 50.85 ms typ. | Nch open-drain output | S pole | Active "L" | 7.0 mT typ. |

**Remark** Please contact our sales representatives for products other than the above.

#### 3. 2. 2 CMOS output product

**Table 5**

| Product Name | Operating Cycle ($t_{CYCLE}$) | Output Form | Pole Detection | Output Logic | Magnetic Sensitivity ($B_{OP}$) |
|---|---|---|---|---|---|
| S-5716ACDL0-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 1.8 mT typ. |
| S-5716ACDL1-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 3.0 mT typ. |
| S-5716ACDL2-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 4.5 mT typ. |
| S-5716ACDL3-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "L" | 7.0 mT typ. |
| S-5716ACDH0-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 1.8 mT typ. |
| S-5716ACDH1-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 3.0 mT typ. |
| S-5716ACDH2-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 4.5 mT typ. |
| S-5716ACDH3-I4T1U | 50.50 ms typ. | CMOS output | Omnipolar | Active "H" | 7.0 mT typ. |
| S-5716ACSL0-I4T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 1.8 mT typ. |
| S-5716ACSL1-I4T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 3.0 mT typ. |
| S-5716ACSL2-I4T1U | 50.85 ms typ. | CMOS output | S pole | Active "L" | 4.5 mT typ. |
| S-5716ACSH0-I4T1U | 50.85 ms typ. | CMOS output | S pole | Active "H" | 1.8 mT typ. |
| S-5716ACNL0-I4T1U | 50.85 ms typ. | CMOS output | N pole | Active "L" | 1.8 mT typ. |

**Remark** Please contact our sales representatives for products other than the above.

## ■ Pin Configurations

### 1. SOT-23-3

Top view

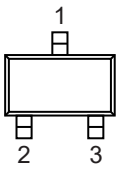



**Figure 3**

**Table 6**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VSS | GND pin |
| 2 | VDD | Power supply pin |
| 3 | OUT | Output pin |

### 2. SNT-4A

Top view

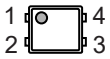



**Figure 4**

**Table 7**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VDD | Power supply pin |
| 2 | VSS | GND pin |
| 3 | NC*1 | No connection |
| 4 | OUT | Output pin |

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

## ■ Absolute Maximum Ratings

**Table 8**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{DD}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 7.0 | V |
| Output current | | $I_{OUT}$ | ±2.0 | mA |
| Output voltage | Nch open-drain output product | $V_{OUT}$ | $V_{SS}$ – 0.3 to $V_{SS}$ + 7.0 | V |
| | CMOS output product | | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Operation ambient temperature | | $T_{opr}$ | –40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | –40 to +125 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Thermal Resistance Value

**Table 9**

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Junction-to-ambient thermal resistance*1 | $\theta_{JA}$ | SOT-23-3 | Board A | – | 200 | – | °C/W |
| | | | Board B | – | 165 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |
| | | SNT-4A | Board A | – | 300 | – | °C/W |
| | | | Board B | – | 242 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

## ■ Electrical Characteristics

### 1. Product with omnipolar detection

#### 1. 1 S-5716AxDxx

**Table 10**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 4.0 | 8.0 | μA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT} = 2$ mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT} = 2$ mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT} = -2$ mA | $V_{DD}$ – 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product Output transistor Nch, $V_{OUT} = 5.5$ V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.10 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 50.40 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW} + t_{SL}$ | | – | 50.50 | 100.00 | ms | – |

### 2. Product with S pole or N pole detection

#### 2. 1 S-5716AxSxx, S-5716AxNxx

**Table 11**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | – | | 2.7 | 5.0 | 5.5 | V | – |
| Current consumption | $I_{DD}$ | Average value | | – | 2.6 | 5.0 | μA | 1 |
| Output voltage | $V_{OUT}$ | Nch open-drain output product | Output transistor Nch, $I_{OUT} = 2$ mA | – | – | 0.4 | V | 2 |
| | | CMOS output product | Output transistor Nch, $I_{OUT} = 2$ mA | – | – | 0.4 | V | 2 |
| | | | Output transistor Pch, $I_{OUT} = -2$ mA | $V_{DD}$ – 0.4 | – | – | V | 3 |
| Leakage current | $I_{LEAK}$ | Nch open-drain output product Output transistor Nch, $V_{OUT} = 5.5$ V | | – | – | 1 | μA | 4 |
| Awake mode time | $t_{AW}$ | – | | – | 0.05 | – | ms | – |
| Sleep mode time | $t_{SL}$ | – | | – | 50.80 | – | ms | – |
| Operating cycle | $t_{CYCLE}$ | $t_{AW} + t_{SL}$ | | – | 50.85 | 100.00 | ms | – |

## ■ Magnetic Characteristics

### 1. Product with omnipolar detection

#### 1. 1 Product with $B_{OP}$ = 1.8 mT typ.

**Table 12**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 0.9 | 1.8 | 2.7 | mT | 5 |
| | N pole | $B_{OPN}$ | – | –2.7 | –1.8 | –0.9 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 0.3 | 1.2 | 2.2 | mT | 5 |
| | N pole | $B_{RPN}$ | – | –2.2 | –1.2 | –0.3 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.6 | – | mT | 5 |
| | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.6 | – | mT | 5 |

#### 1. 2 Product with $B_{OP}$ = 3.0 mT typ.

**Table 13**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 1.4 | 3.0 | 4.0 | mT | 5 |
| | N pole | $B_{OPN}$ | – | –4.0 | –3.0 | –1.4 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 1.1 | 2.2 | 3.7 | mT | 5 |
| | N pole | $B_{RPN}$ | – | –3.7 | –2.2 | –1.1 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.8 | – | mT | 5 |
| | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.8 | – | mT | 5 |

#### 1. 3 Product with $B_{OP}$ = 3.4 mT typ.

**Table 14**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 2.0 | 3.4 | 5.6 | mT | 5 |
| | N pole | $B_{OPN}$ | – | –5.6 | –3.4 | –2.0 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 1.5 | 2.6 | 4.2 | mT | 5 |
| | N pole | $B_{RPN}$ | – | –4.2 | –2.6 | –1.5 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.8 | – | mT | 5 |
| | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.8 | – | mT | 5 |

#### 1. 4 Product with $B_{OP}$ = 4.5 mT typ.

**Table 15**

(Ta = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 2.5 | 4.5 | 6.0 | mT | 5 |
| | N pole | $B_{OPN}$ | – | –6.0 | –4.5 | –2.5 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 2.0 | 3.5 | 5.5 | mT | 5 |
| | N pole | $B_{RPN}$ | – | –5.5 | –3.5 | –2.0 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 1.0 | – | mT | 5 |
| | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 1.0 | – | mT | 5 |

### 1. 5 Product with $B_{OP}$ = 7.0 mT typ.

**Table 16**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 5.0 | 7.0 | 8.5 | mT | 5 |
| | N pole | $B_{OPN}$ | – | –8.5 | –7.0 | –5.0 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 3.7 | 5.2 | 7.2 | mT | 5 |
| | N pole | $B_{RPN}$ | – | –7.2 | –5.2 | –3.7 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 1.8 | – | mT | 5 |
| | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 1.8 | – | mT | 5 |

## 2. Product with S pole detection

### 2. 1 Product with $B_{OP}$ = 1.8 mT typ.

**Table 17**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 0.9 | 1.8 | 2.7 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 0.3 | 1.2 | 2.2 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.6 | – | mT | 5 |

### 2. 2 Product with $B_{OP}$ = 3.0 mT typ.

**Table 18**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 1.4 | 3.0 | 4.0 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 1.1 | 2.2 | 3.7 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.8 | – | mT | 5 |

### 2. 3 Product with $B_{OP}$ = 3.4 mT typ.

**Table 19**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 2.0 | 3.4 | 5.6 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 1.5 | 2.6 | 4.2 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 0.8 | – | mT | 5 |

### 2. 4 Product with $B_{OP}$ = 4.5 mT typ.

**Table 20**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 2.5 | 4.5 | 6.0 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 2.0 | 3.5 | 5.5 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 1.0 | – | mT | 5 |

### 2. 5 Product with $B_{OP}$ = 7.0 mT typ.

**Table 21**

($Ta$ = +25°C, $V_{DD}$ = 5.0 V, $V_{SS}$ = 0 V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | S pole | $B_{OPS}$ | – | 5.0 | 7.0 | 8.5 | mT | 5 |
| Release point*2 | S pole | $B_{RPS}$ | – | 3.7 | 5.2 | 7.2 | mT | 5 |
| Hysteresis width*3 | S pole | $B_{HYSS}$ | $B_{HYSS} = B_{OPS} - B_{RPS}$ | – | 1.8 | – | mT | 5 |

## 3. Product with N pole detection

### 3. 1 Product with $B_{OP}$ = 1.8 mT typ.

**Table 22**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | N pole | $B_{OPN}$ | – | –2.7 | –1.8 | –0.9 | mT | 5 |
| Release point*2 | N pole | $B_{RPN}$ | – | –2.2 | –1.2 | –0.3 | mT | 5 |
| Hysteresis width*3 | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.6 | – | mT | 5 |

### 3. 2 Product with $B_{OP}$ = 3.0 mT typ.

**Table 23**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | N pole | $B_{OPN}$ | – | –4.0 | –3.0 | –1.4 | mT | 5 |
| Release point*2 | N pole | $B_{RPN}$ | – | –3.7 | –2.2 | –1.1 | mT | 5 |
| Hysteresis width*3 | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.8 | – | mT | 5 |

### 3. 3 Product with $B_{OP}$ = 3.4 mT typ.

**Table 24**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | N pole | $B_{OPN}$ | – | –5.6 | –3.4 | –2.0 | mT | 5 |
| Release point*2 | N pole | $B_{RPN}$ | – | –4.2 | –2.6 | –1.5 | mT | 5 |
| Hysteresis width*3 | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 0.8 | – | mT | 5 |

### 3. 4 Product with $B_{OP}$ = 4.5 mT typ.

**Table 25**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | N pole | $B_{OPN}$ | – | –6.0 | –4.5 | –2.5 | mT | 5 |
| Release point*2 | N pole | $B_{RPN}$ | – | –5.5 | –3.5 | –2.0 | mT | 5 |
| Hysteresis width*3 | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 1.0 | – | mT | 5 |

### 3. 5 Product with $B_{OP}$ = 7.0 mT typ.

**Table 26**

($Ta = +25°C$, $V_{DD} = 5.0$ V, $V_{SS} = 0$ V unless otherwise specified)

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Operation point*1 | N pole | $B_{OPN}$ | – | –8.5 | –7.0 | –5.0 | mT | 5 |
| Release point*2 | N pole | $B_{RPN}$ | – | –7.2 | –5.2 | –3.7 | mT | 5 |
| Hysteresis width*3 | N pole | $B_{HYSN}$ | $B_{HYSN} = \|B_{OPN} - B_{RPN}\|$ | – | 1.8 | – | mT | 5 |

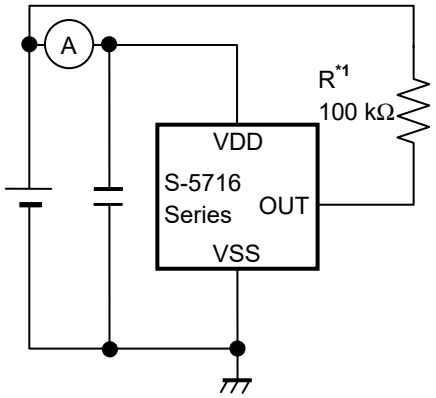
***1.** $B_{OPN}$, $B_{OPS}$: Operation points
$B_{OPN}$ and $B_{OPS}$ are the values of magnetic flux density when the output voltage ($V_{OUT}$) is inverted after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds $B_{OPN}$ or $B_{OPS}$, $V_{OUT}$ retains the status.

***2.** $B_{RPN}$, $B_{RPS}$: Release points
$B_{RPN}$ and $B_{RPS}$ are the values of magnetic flux density when the output voltage ($V_{OUT}$) is inverted after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below $B_{RPN}$ or $B_{RPS}$, $V_{OUT}$ retains the status.

***3.** $B_{HYSN}$, $B_{HYSS}$: Hysteresis widths
$B_{HYSN}$ and $B_{HYSS}$ are the difference between $B_{OPN}$ and $B_{RPN}$, and $B_{OPS}$ and $B_{RPS}$, respectively.

**Remark** The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

## ■ Test Circuits




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 5 Test Circuit 1**

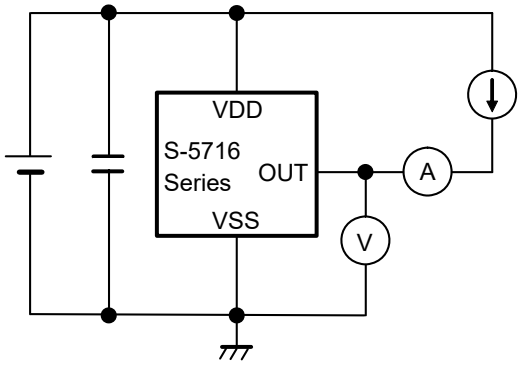



**Figure 6 Test Circuit 2**

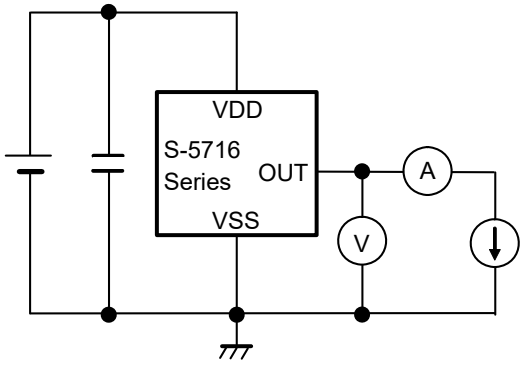



**Figure 7 Test Circuit 3**

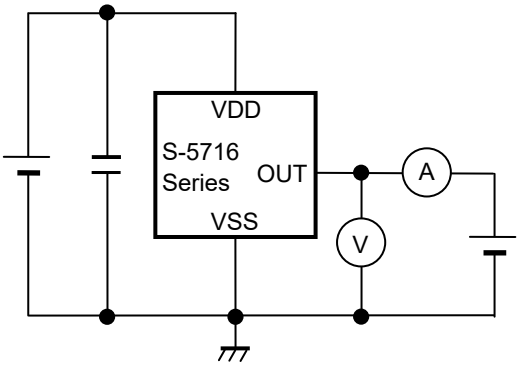
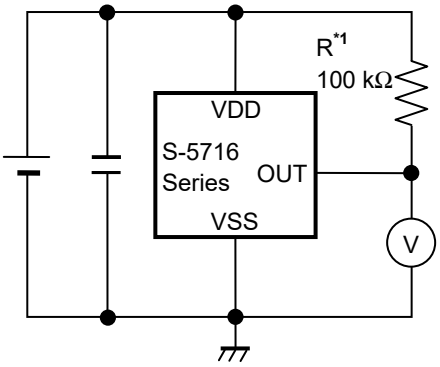


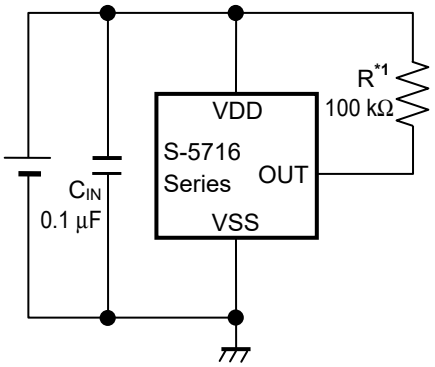

**Figure 8 Test Circuit 4**




***1.*** Resistor (R) is unnecessary for the CMOS output product.

**Figure 9 Test Circuit 5**

## ■ Standard Circuit




***1.** Resistor (R) is unnecessary for the CMOS output product.

**Figure 10**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Operation

### 1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is vertical to the marking surface.
In product with omnipolar detection, the output voltage ($V_{OUT}$) is inverted when the S pole or N pole is moved closer to the marking surface.
In product with S pole detection, $V_{OUT}$ is inverted when the S pole is moved closer to the marking surface.
In product with N pole detection, $V_{OUT}$ is inverted when the N pole is moved closer to the marking surface.
**Figure 11** and **Figure 12** show the direction in which magnetic flux is being applied.

**1. 1 SOT-23-3**

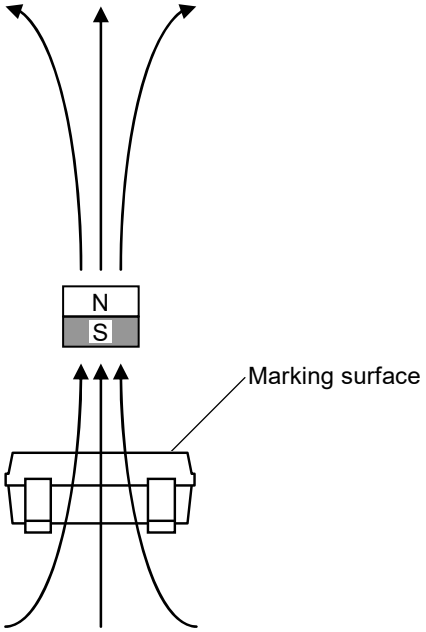



**Figure 11**

**1. 2 SNT-4A**

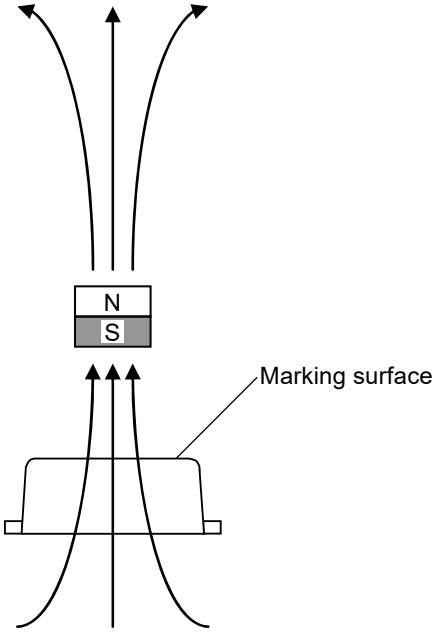



**Figure 12**

### 2. Position of Hall sensor

**Figure 13** and **Figure 14** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

**2. 1 SOT-23-3**

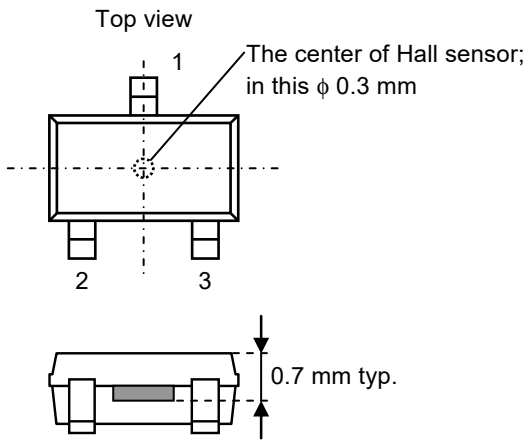



**Figure 13**

**2. 2 SNT-4A**

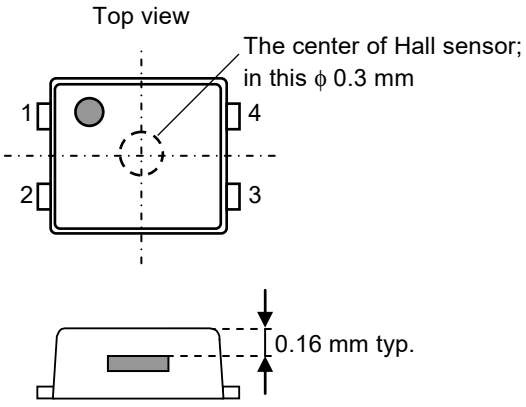



**Figure 14**

## 3. Basic operation

This IC changes the output voltage level ($V_{OUT}$) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.
The following explains the operation when the output logic is active "L".

### 3. 1 Product with omnipolar detection

When the magnetic flux density vertical to the marking surface exceeds the operation point ($B_{OPN}$ or $B_{OPS}$) after the S pole or N pole of a magnet is moved closer to the marking surface of this IC, $V_{OUT}$ changes from "H" to "L". When the S pole or N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point ($B_{RPN}$ or $B_{RPS}$), $V_{OUT}$ changes from "L" to "H".
**Figure 15** shows the relationship between the magnetic flux density and $V_{OUT}$.

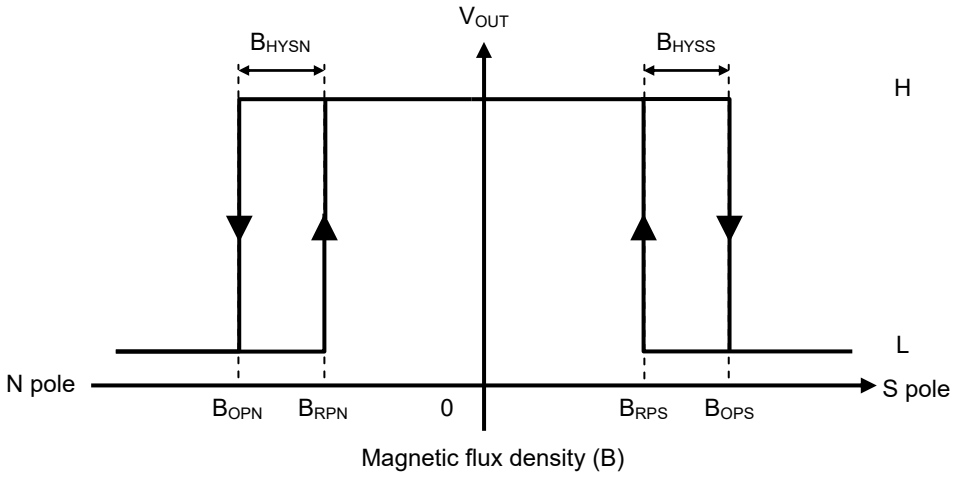



**Figure 15**

### 3. 2 Product with S pole detection

When the magnetic flux density vertical to the marking surface exceeds $B_{OPS}$ after the S pole of a magnet is moved closer to the marking surface of this IC, $V_{OUT}$ changes from "H" to "L". When the S pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than $B_{RPS}$, $V_{OUT}$ changes from "L" to "H".
**Figure 16** shows the relationship between the magnetic flux density and $V_{OUT}$.

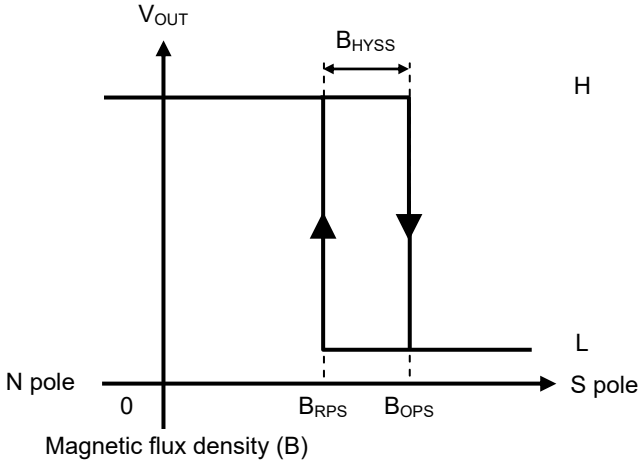



**Figure 16**

### 3. 3 Product with N pole detection

When the magnetic flux density vertical to the marking surface exceeds $B_{OPN}$ after the N pole of a magnet is moved closer to the marking surface of this IC, $V_{OUT}$ changes from "H" to "L". When the N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than $B_{RPN}$, $V_{OUT}$ changes from "L" to "H".
**Figure 17** shows the relationship between the magnetic flux density and $V_{OUT}$.

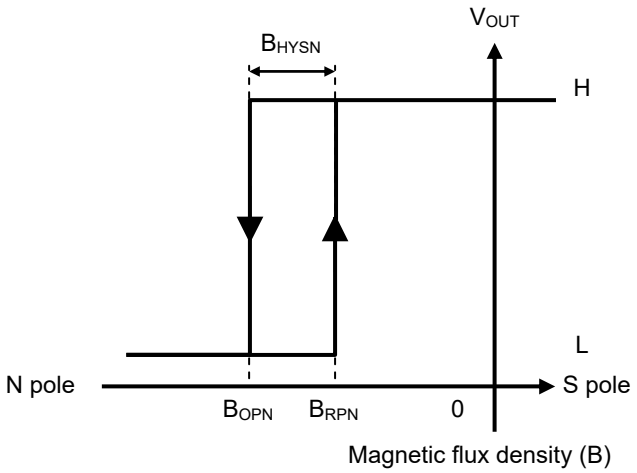


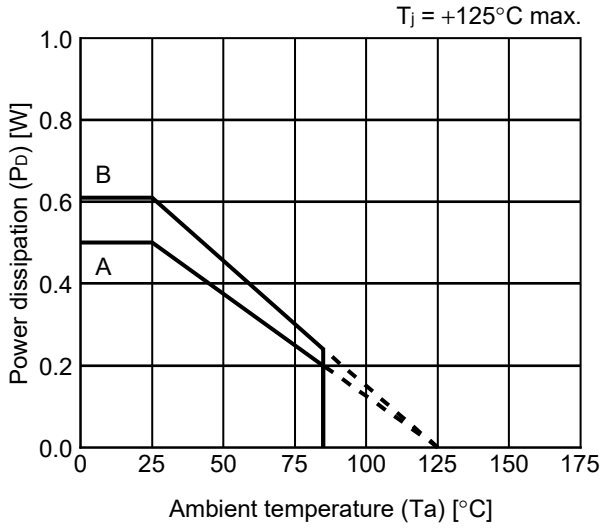

**Figure 17**

## ■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by bend and distortion during mounting the IC on a board or handle after mounting.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

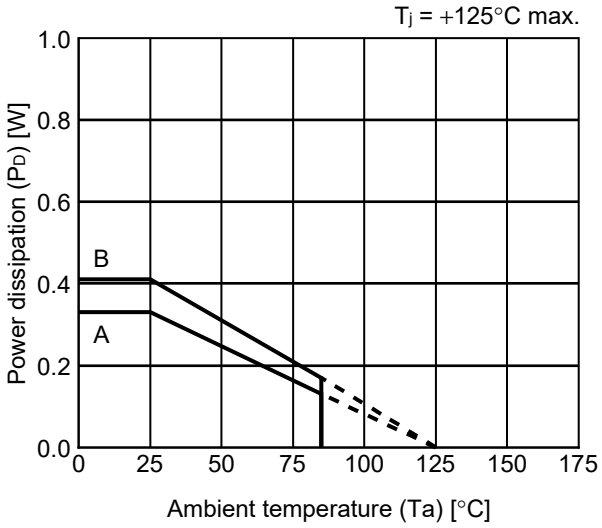
## ■ Power Dissipation

**SOT-23-3**




| Board | Power Dissipation ($P_D$) |
|---|---|
| A | 0.50 W |
| B | 0.61 W |
| C | – |
| D | – |
| E | – |

**SNT-4A**

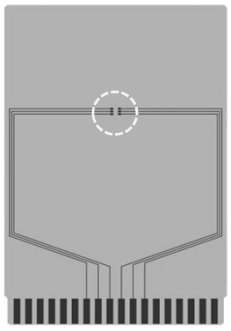



| Board | Power Dissipation ($P_D$) |
|---|---|
| A | 0.33 W |
| B | 0.41 W |
| C | – |
| D | – |
| E | – |

# SOT-23-3/3S/5/6 Test Board

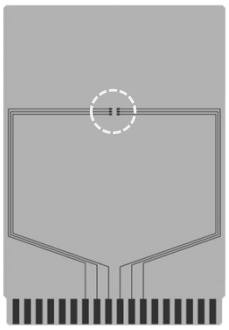
IC Mount Area

**(1) Board A**



| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(2) Board B**



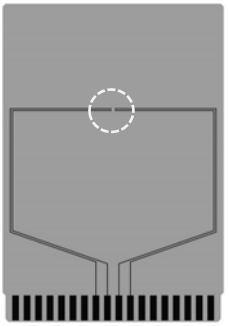
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. SOT23x-A-Board-SD-2.0

# SNT-4A Test Board

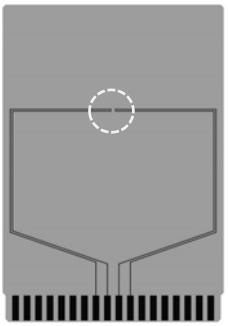
IC Mount Area

**(1) Board A**



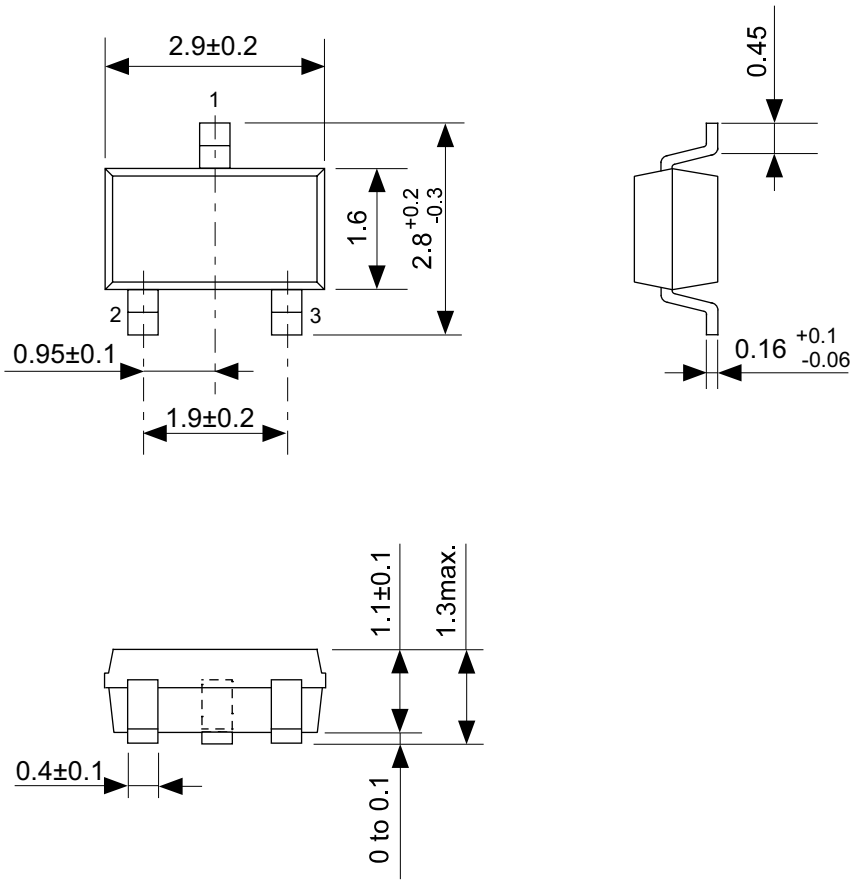
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

**(2) Board B**



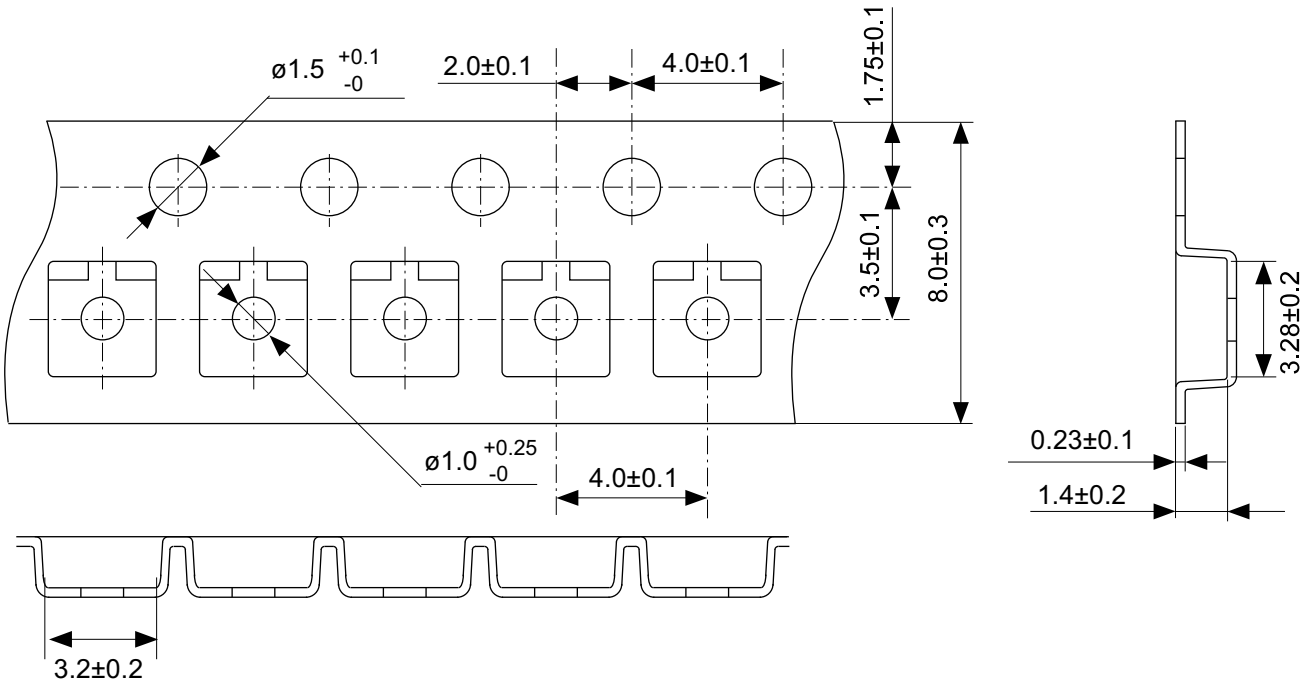
| Item | | Specification |
|---|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

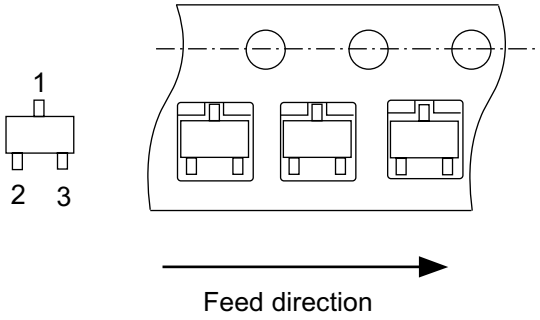
No. SNT4A-A-Board-SD-1.0




No. MP003-C-P-SD-1.1

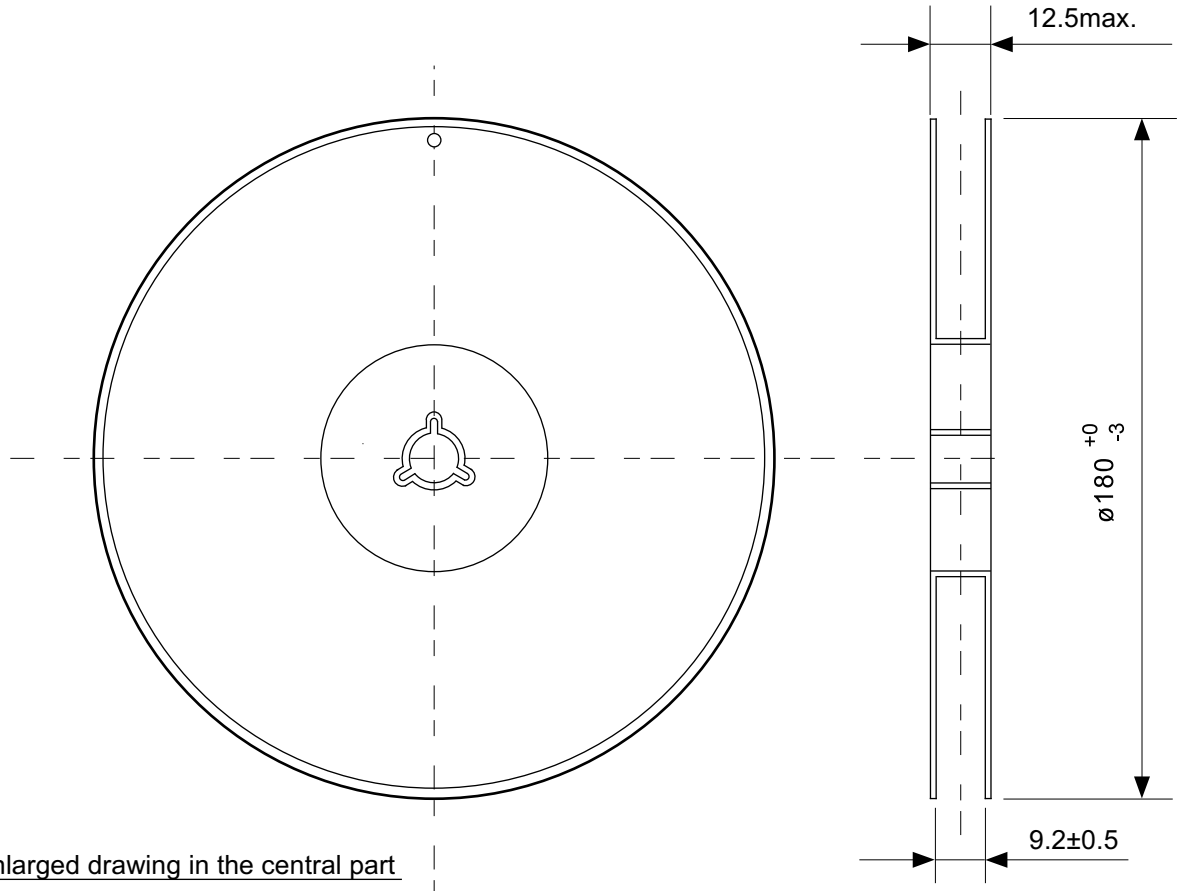
| | |
|---|---|
| TITLE | SOT233-C-PKG Dimensions |
| No. | MP003-C-P-SD-1.1 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |



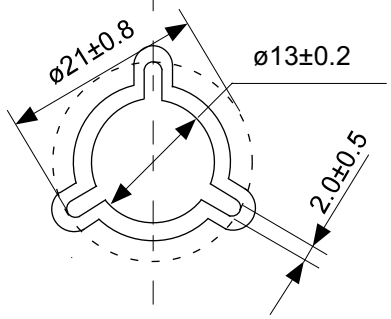




No. MP003-C-C-SD-2.0

| | |
|---|---|
| TITLE | SOT233-C-Carrier Tape |
| No. | MP003-C-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

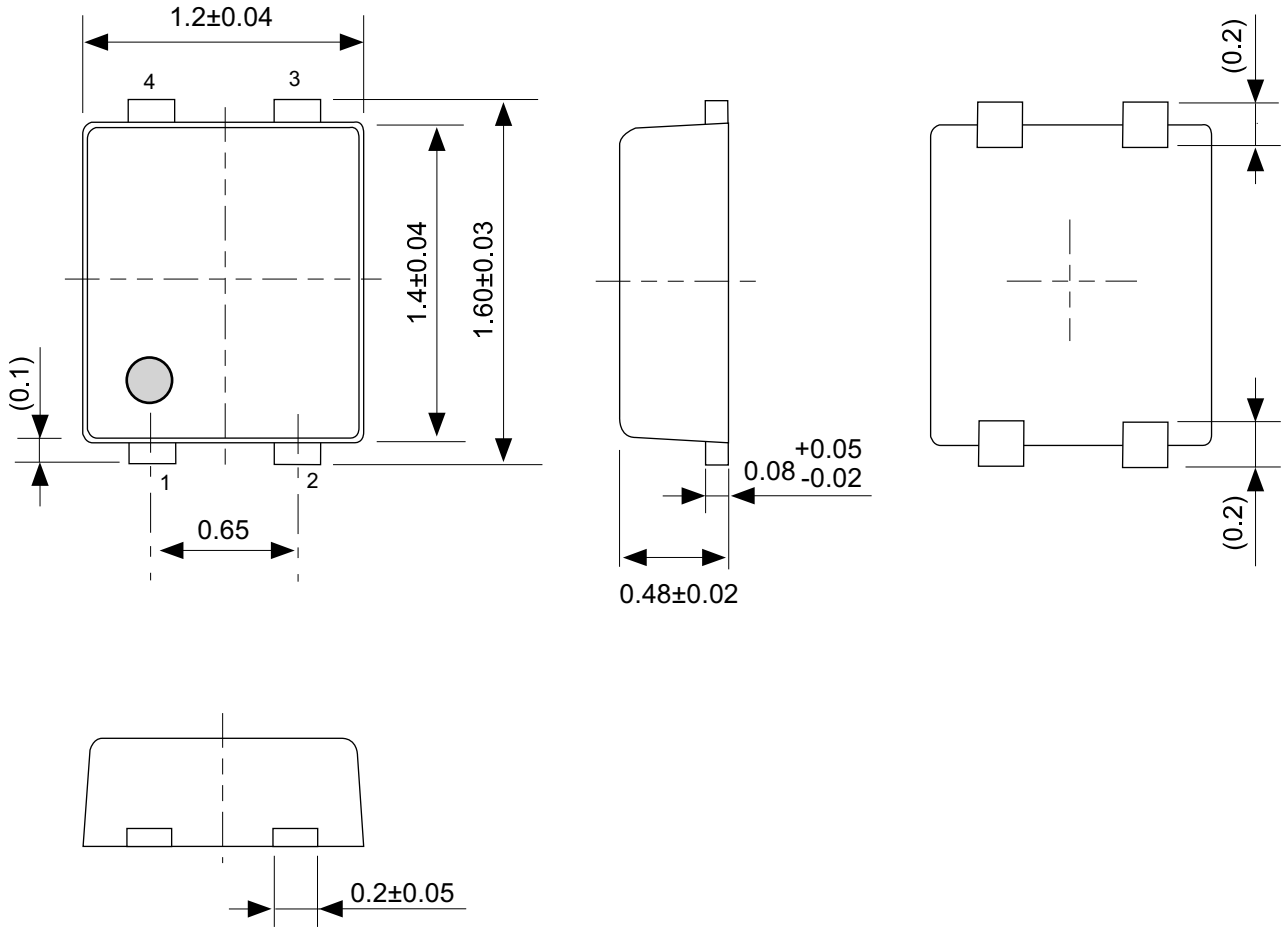



Enlargement drawing in the central part



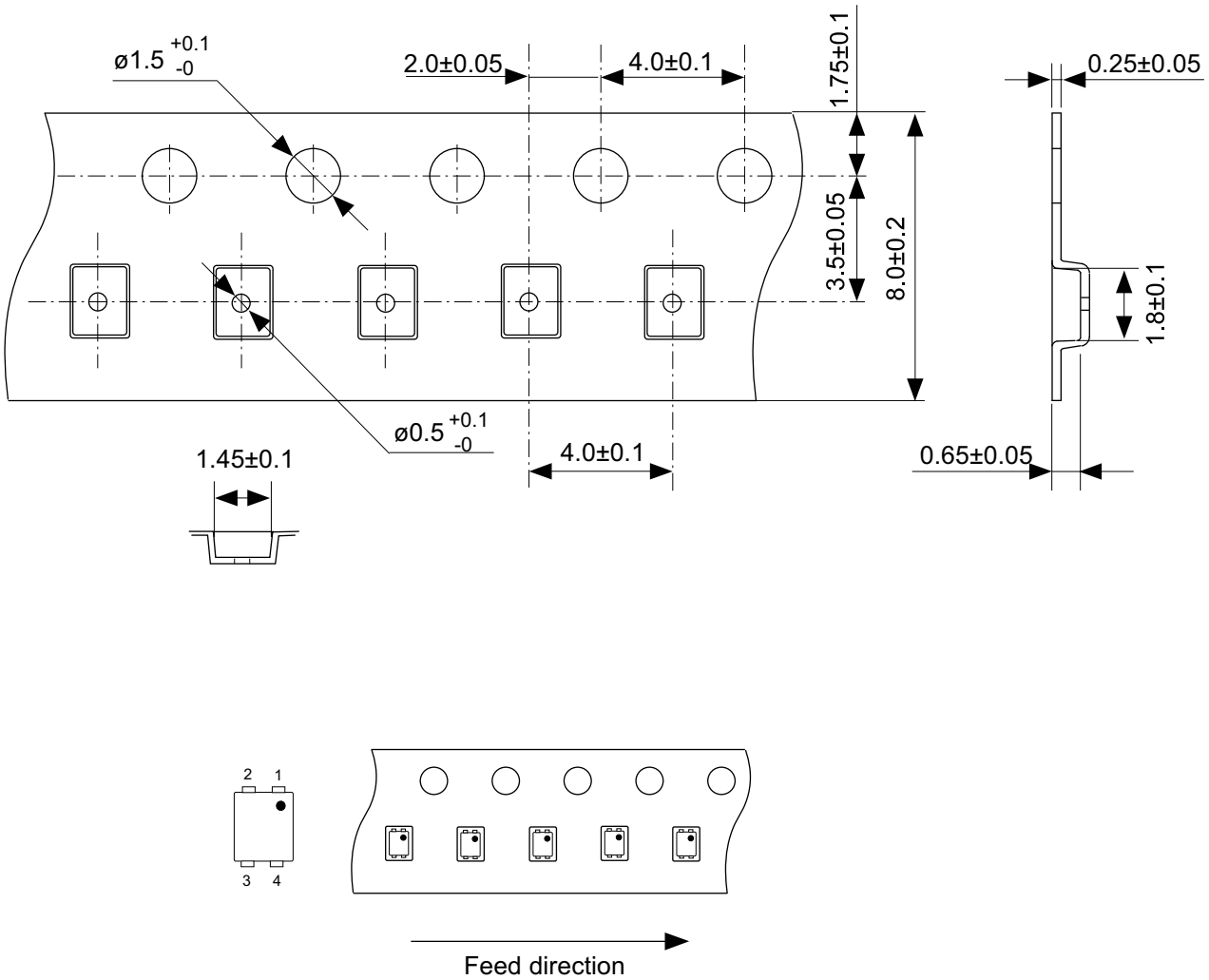

No. MP003-Z-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SOT233-C-Reel | | |
| No. | MP003-Z-R-SD-1.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |



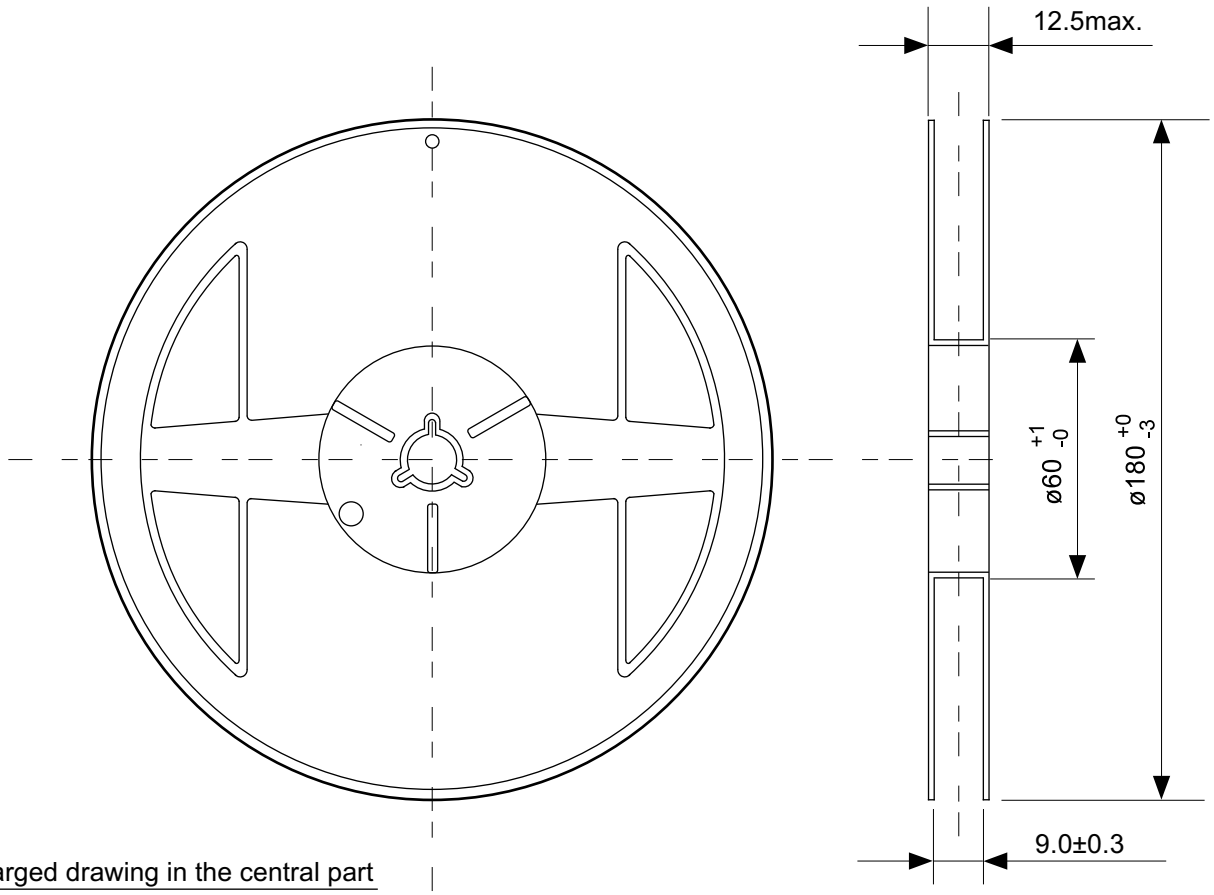

No. PF004-A-P-SD-6.0

| | |
|---|---|
| TITLE | SNT-4A-A-PKG Dimensions |
| No. | PF004-A-P-SD-6.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

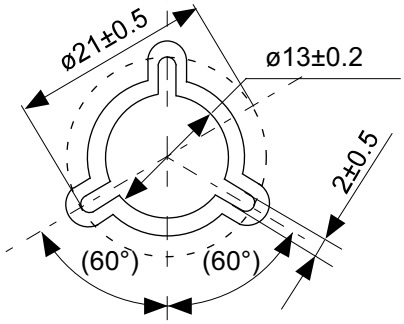



No. PF004-A-C-SD-2.0

| | |
|---|---|
| TITLE | SNT-4A-A-Carrier Tape |
| No. | PF004-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

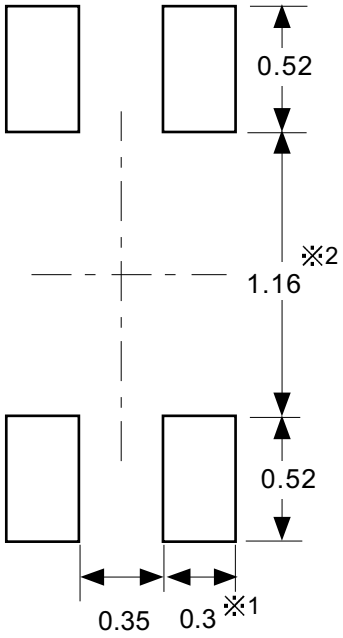



Enlarged drawing in the central part




No. PF004-A-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SNT-4A-A-Reel | | |
| No. | PF004-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |




※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.10 mm ~ 1.20 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.10 mm to 1.20 mm).

**Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.**
**2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
**3. Match the mask aperture size and aperture position with the land pattern.**
**4. Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.10 mm ~ 1.20 mm)。

**注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。**
**2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
**3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。**
**4. 详细内容请参阅 "SNT 封装的应用指南"。**

No. PF004-A-L-SD-4.1

| | |
|---|---|
| TITLE | SNT-4A-A<br>-Land Recommendation |
| No. | PF004-A-L-SD-4.1 |
| ANGLE | |
| UNIT | mm |
| | |
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