S-8821 Series

VOLTAGE REGULATION BOOST CHARGE PUMP DC-DC CONVERTER

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Rev.5.2_00

The S-8821 series is a CMOS boost charge pump DC-DC converter with a voltage regulation function.
The S-8821 series consists of an oscillation circuit, a controller, a reference voltage circuit, an error amplifier circuit, and an output switching transistor, and can regulate the output voltage by PFM control.
Since small ceramic capacitors can be used for the pump capacitor, input capacitor, and output capacitor, the mounting area can be minimized.

■ Features

- PFM control CMOS boost charge pump
- Power supply voltage: 1.6 to 5.0 V
- Output voltage: 2.5 to 5.5 V, selectable in 0.1 V steps.
- Output voltage accuracy: ±2 % max.
- Built-in soft start circuit: 1.0 ms typ.
- Output current 25 mA (V_{IN}=($V_{OUT(S)}$ × 0.80) V)
- Oscillation frequency: 1.0 MHz typ.
- ON/OFF function: During standby: 1 μA max.
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Lithium ion battery driven applications
- Local power supply
- Power supply for white LED display backlights

■ Packages

- SOT-23-6W
- SNT-8A

■ Block Diagram

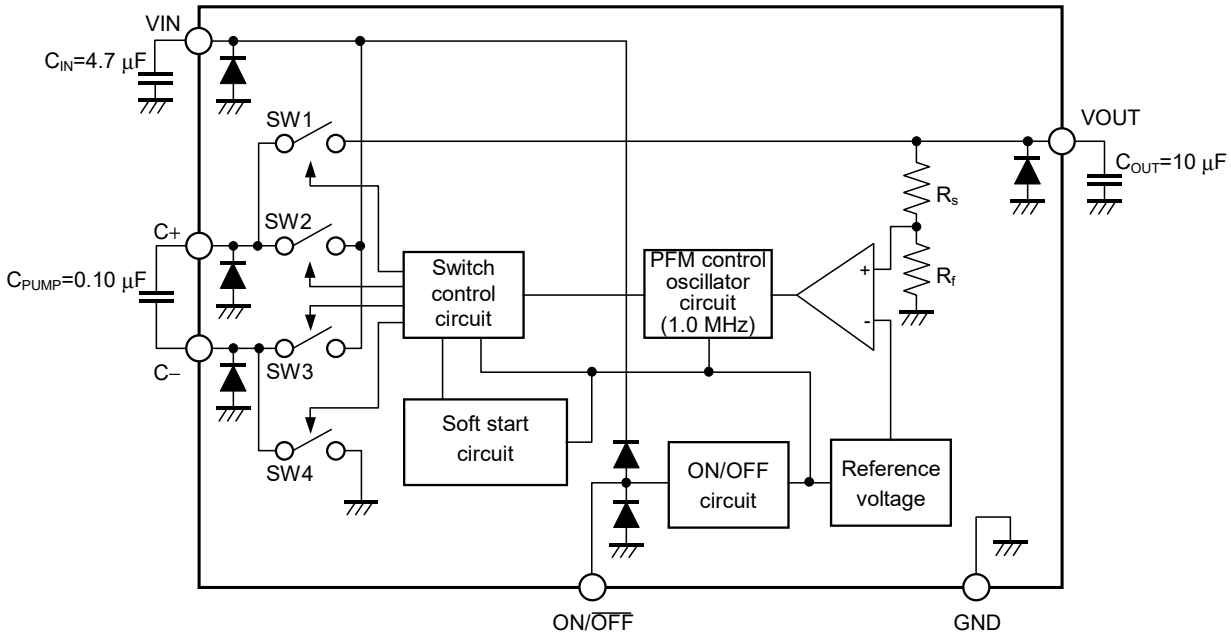


Figure 1

■ Product Name Structure

- The output voltage and packages for the S-8821 Series can be selected at the user's request. Refer to the "Product name" for the meanings of the characters in the product name, "Package" regarding the package drawings and "Product name list" for the full product names.

1. Product name

(1) SOT-23-6W

S-8821 xx A MH - xxx TF x

- x: Environmental code
  - S: Lead-free, halogen-free
  - G: Lead-free (Contact our sales representatives for details)
  - U: Lead-free (Sn 100%), halogen-free
- TF: IC direction in tape specifications*1
- xxx: Product name (abbreviation)*2
- MH: Package name (abbreviation)
  - MH: SOT-23-6W
- xx: Output voltage
  - 25 to 55
  - (E.g., when the output voltage is 2.5 V, it is expressed as 25.)

***1.** Refer to the tape specifications at the end of this book.
***2.** Refer to the product name list.

(2) SNT-8A

S-8821 xx A PH - xxx TF U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- TF: IC direction in tape specifications*1
- xxx: Product name (abbreviation)*2
- PH: Package name (abbreviation)
  - PH: SNT-8A
- xx: Output voltage
  - 25 to 55
  - (E.g., when the output voltage is 2.5 V, it is expressed as 25.)

***1.** Refer to the tape specifications at the end of this book.
***2.** Refer to the product name list.

2. Package

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SOT-23-6W	MP006-B-P-SD	MP006-B-C-SD	MP006-B-R-SD	—
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

Table 1

Output Voltage	SOT-23-6W	SNT-8A
2.5 V	S-882125AMH-M2ATF□	S-882125APH-M2ATFU
3.0 V	S-882130AMH-M2FTF□	—
3.3 V	S-882133AMH-M2ITF□	—
3.5 V	S-882135AMH-M2KTF□	—
3.6 V	S-882136AMH-M2LTF□	—
4.0 V	S-882140AMH-M2PTF□	—
4.5 V	S-882145AMH-M2UTF□	—
5.0 V	S-882150AMH-M2ZTF□	S-882150APH-M2ZTFU
5.2 V	S-882152AMH-M3BTF□	—
5.5 V	S-882155AMH-M3ETF□	—

Remark 1. Please contact our sales representatives for products other than the above.
2. □: G, S or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configurations

SOT-23-6W
Top view

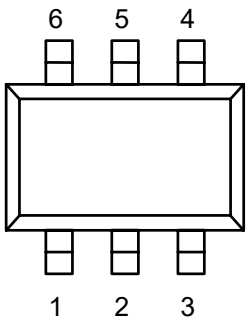


Figure 2

Table 2

Pin No.	Symbol	Pin Description
1	VIN	Voltage input pin
2	C+	Charge-pump pump capacitor connection pin (positive pin)
3	C–	Charge-pump pump capacitor connection pin (negative pin)
4	$\overline{\text{ON/OFF}}$	Shutdown pin High level (H): normal operation (boost) Low level (L) : boost halt (all circuit halt)
5	GND	GND pin
6	VOUT	Voltage output pin

SNT-8A
Top view

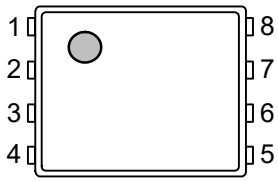


Figure 3

Table 3

Pin No.	Symbol	Pin Description
1	C+	Charge-pump pump capacitor connection pin (positive pin)
2	VIN	Voltage input pin
3	NC*1	No connection
4	VOUT	Voltage output pin
5	$\overline{\text{ON/OFF}}$	Shutdown pin High level (H): normal operation (boost) Low level (L) : boost halt (all circuit halt)
6	GND	GND pin
7	NC*1	No connection
8	C–	Charge-pump pump capacitor connection pin (negative pin)

***1.** The NC pin is electrically open.
The NC pin can be connected to VIN or GND.

■ Absolute Maximum Ratings

Table 4

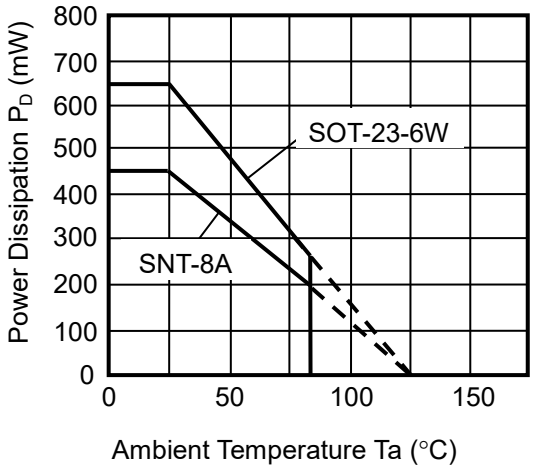
(Ta=25°C unless otherwise specified)

Items		Symbols	Absolute Maximum Ratings	Units
C+ pin voltage		V_{C+}	V_{GND}–0.3 to V_{GND}+7.5	V
C– pin voltage		V_{C-}	V_{GND}–0.3 to V_{GND}+7	V
VIN pin voltage		V_{IN}	V_{GND}–0.3 to V_{GND}+5.5	V
VOUT pin voltage		V_{OUT}	V_{GND}–0.3 to V_{GND}+7	V
ON/$\overline{OFF}$ pin voltage		$V_{ON/\overline{OFF}}$	V_{GND}–0.3 to V_{IN}+0.3	V
Power dissipation	SOT-23-6W	P_D	300 (When not mounted on board)	mW
			650*1	mW
	SNT-8A		450*1	mW
Operating ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

(1) When mounted on board



(2) When not mounted on board

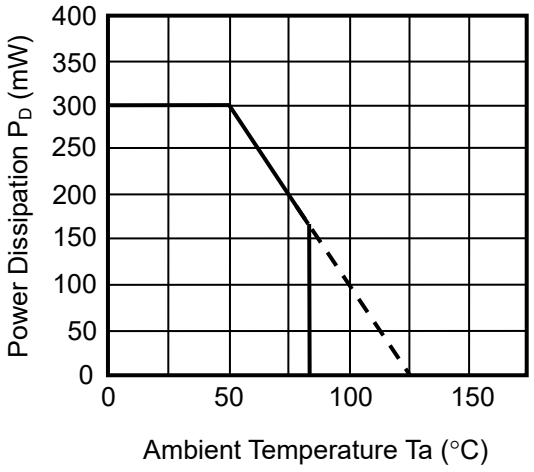


Figure 4 Power Dissipation of Package

■ Electrical Characteristics

Table 5

(V_{IN}=($V_{OUT(S)}$ × 0.60) V*1, Ta=25°C unless otherwise specified)

Items	Symbols	Conditions	Min.	Typ.	Max.	Units	Test circuits
Operation input voltage	V_{IN}	$V_{OUT(S)}$ ≤ 2.9 V	1.6	—	5.0	V	2
		$V_{OUT(S)}$ > 2.9 V	$V_{OUT(S)}$ × 0.54	—	5.0	V	2
Output voltage*2	$V_{OUT(E)}$	I_{OUT}=10 mA	$V_{OUT(S)}$ × 0.98	$V_{OUT(S)}$	$V_{OUT(S)}$ × 1.02	V	2
Output current*3	I_{OUT}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6	5	—	—	mA	2
		V_{IN}=($V_{OUT(S)}$ × 0.60) V*1	15	—	—	mA	2
		V_{IN}=($V_{OUT(S)}$ × 0.80) V	25	—	—	mA	2
Line regulation	ΔV_{OUT1}	V_{IN}=($V_{OUT(S)}$ × 0.60) V*1 to ($V_{OUT(S)}$ − 0.10) V, I_{OUT}=10 mA	—	50	100	mV	2
Load regulation	ΔV_{OUT2}	I_{OUT}=0.1 mA to 10 mA	—	40	80	mV	2
Ripple voltage*4	V_{RIP}	I_{OUT}=10 mA	—	70	—	mV_{p-p}	2
Maximum oscillation frequency	f_{osc}	V_{OUT}=($V_{OUT(S)}$ × 0.60) V, Measure waveform at C− pin	800	1000	1200	kHz	2
Efficiency*5	η	V_{IN}=($V_{OUT(S)}$ × 0.54) V, $V_{OUT(S)}$ ≥ 3.0 V, I_{OUT}=5 mA	—	90	—	%	1
Operation consumption current	I_{SS1}	V_{IN}=$V_{OUT(S)}$, V_{OUT}=($V_{OUT(S)}$ + 0.5) V	—	35	60	μA	2
Standby consumption current	I_{SSS}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6 to 5.0 V, $V_{ON/\overline{OFF}}$=0 V	—	0.3	1.0	μA	1
ON/$\overline{\text{OFF}}$ pin input voltage (high level)	V_{SH}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6 to 5.0 V	1.5	—	—	V	1
ON/$\overline{\text{OFF}}$ pin input voltage (low level)	V_{SL}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6 to 5.0 V	—	—	0.3	V	1
ON/$\overline{\text{OFF}}$ pin input current (high level)	I_{SH}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6 to 5.0 V	−0.1	—	0.1	μA	1
ON/$\overline{\text{OFF}}$ pin input current (low level)	I_{SL}	V_{IN}=($V_{OUT(S)}$ × 0.54) V*6 to 5.0 V	−0.1	—	0.1	μA	1
Soft start time	t_{SS}	I_{OUT}=10 mA	0.2	1.0	4.0	ms	1

***1.** In case of V_{OUT} ≤ 3.3 V, V_{IN}=2.0 V

***2.** $V_{OUT(E)}$: Actual output voltage
$V_{OUT(S)}$: Specified output voltage

***3.** The output current at which the output voltage becomes 97 % of $V_{OUT(E)}$ after gradually increasing the output current.

***4.** Design assurance

***5.** The ideal efficiency is indicated by the following expression.
Efficiency (η)=(V_{OUT} × I_{OUT}) / (2.0 × V_{IN} × I_{OUT})

***6.** In case of V_{OUT} ≤ 2.9 V, V_{IN}=1.6 V

■ Test Circuits

1.

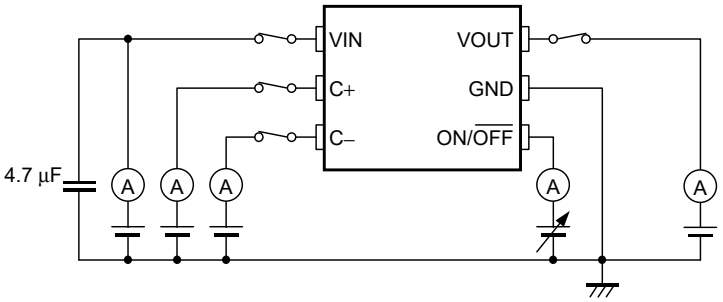


Figure 5

2.

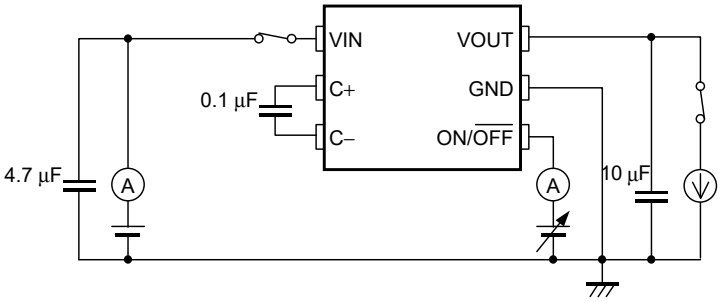


Figure 6

■ Operation

1. Basic operation

Figure 7 shows the block diagram of the S-8821 Series.
The S-8821 series controls the output voltage by using the pulse frequency modulation (PFM) method. The SW1 to SW4 switching transistors are switched ON/OFF with the clock generated by the internal oscillator circuit, and operates the boost charge pump.
The output voltage is fed back and the voltage split by feedback resistances R_s and R_f and reference voltage (V_{ref}) are compared by a comparator. This comparator signal is used to modulate the oscillation pulse frequency in order to keep the output voltage constant.

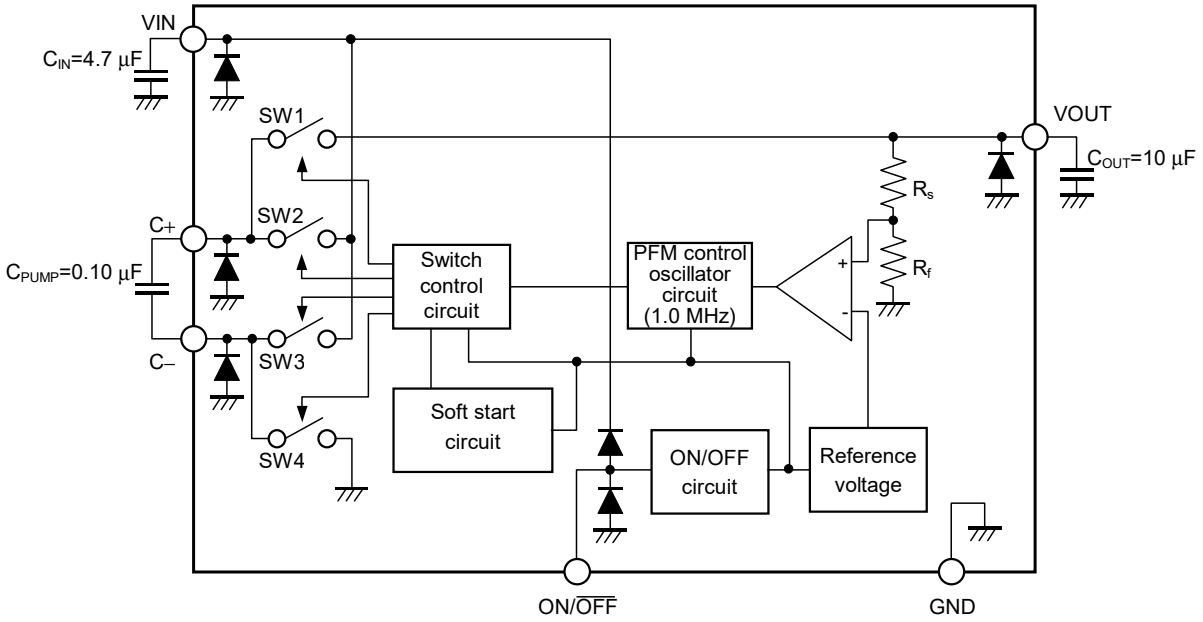


Figure 7

2. Boost Charge Pump

The boost charge pump boosts the voltage by switching ON/OFF of the SW1 to SW4 switching transistors.
First, in order to charge the pump capacitance (C_{PUMP}), set SW1 to OFF, SW2 to ON, SW3 to OFF, and SW4 to ON (charge cycle). Following charging the electricity, in order to discharge the charged electricity to the output capacitance (C_{OUT}), SW1 set the switches as to ON, SW2 to OFF, SW3 to ON, and SW4 to OFF (discharge cycle).
The input voltage can be boosted to a constant voltage value by repeating this charge cycle and discharge cycle.
Figure 8 shows the charge cycle, and **Figure 9** shows the discharge cycle.

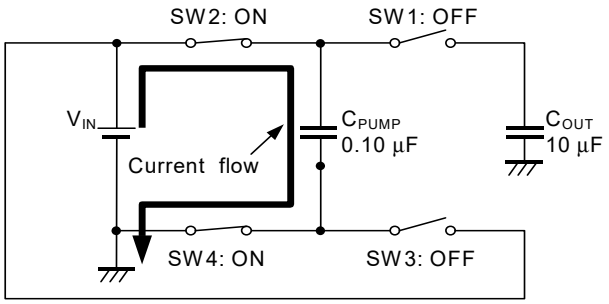


Figure 8

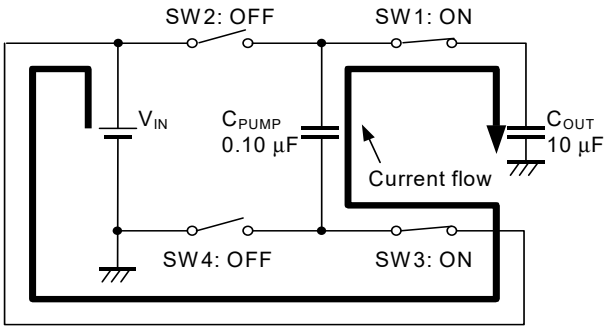


Figure 9

3. Shutdown Pin (ON/$\overline{\text{OFF}}$ Pin)

Setting the ON/$\overline{\text{OFF}}$ pin to the Low level ("L") causes the voltage of the VOUT pin to change to the GND level and simultaneously the operation of all the internal circuit to stop. At this time, the consumption current is largely reduced, to a level of approximately 0.3 μA.
The structure of the ON/$\overline{\text{OFF}}$ pin is as shown in **Figure 10**. Since the ON/$\overline{\text{OFF}}$ pin is neither pulled down nor pulled up internally, do not use it in the floating state.
When the ON/$\overline{\text{OFF}}$ pin is not used, connect it to the VIN pin.

Table 6

ON/$\overline{\text{OFF}}$ pin	Internal circuit	VOUT pin voltage
"H": Power on	Operating	Set value
"L": Power off	Stop	V_{GND} level

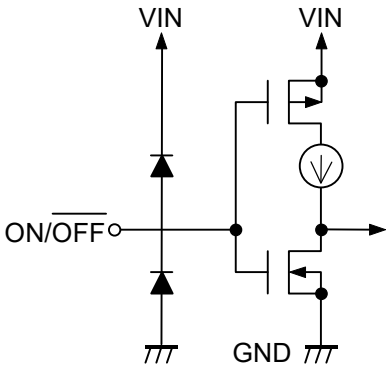


Figure 10

4. Soft Start Function

The S-8821 Series features a built-in soft start circuit. Upon power application or when the ON/$\overline{\text{OFF}}$ pin is switched from "L" to "H", the output voltage gradually rises over the soft start time, and the output current is gradually output as a result. This soft start function reduces the input current rush.

■ External Capacitor Selection

1. Input and Output Capacitors (C_{IN}, C_{OUT})

The input capacitor (C_{IN}) lowers the power supply impedance and averages the input current.
The C_{IN} value is selected according to the impedance of the power supply that is used. Select a ceramic capacitor with a small equivalent series resistance (ESR). Although this figure varies according to the impedance of the power supply that is used as well as the load current value, it is generally in the range of 4.7 μF to 10 μF.
For the output capacitor (C_{OUT}), select a ceramic capacitor with a small ESR for smoothing the ripple voltage. A value of 10 μF is recommended for the capacitance value. Use of a capacitor with a capacitance lower than 10 μF results in a larger ripple voltage. Conversely, use of a capacitor with a capacitance greater than 10 μF results in the output voltage not being able to rise up to setting value and the impossibility to obtain the desired output current.

2. Pump Capacitor (C_{PUMP})

The pump capacitor (C_{PUMP}) is required for boosting the voltage. Select a ceramic capacitor with a small ESR. A capacitance value of 0.10 μF is recommended. Use of a capacitor with a capacitance greater than 0.10 μF results in a larger ripple voltage. Conversely, use of a capacitor with a capacitance lower than 0.10 μF results in the output voltage not being able to raise up to setting value and the impossibility to obtain the desired output current.

■ Precautions

- Regarding the wiring to the VIN pin, VOUT pin, C+ pin, C– pin and GND pin, be careful to perform pattern wiring so as to obtain low impedance.

- Always connect a capacitor to the VOUT pin, C+ pin, and C– pin.

- Connect C_{IN} and C_{OUT} in the vicinity of the IC and sufficiently strengthen the wiring for GND pin and VIN pin in order to lower the impedance of the wiring resistance, etc. High impedance may cause unstable operation.
  Moreover, in selecting C_{IN} and C_{OUT}, perform a full evaluation of the actual usage conditions.

- Connect C_{PUMP} in the vicinity of the IC and sufficiently strengthen the wiring for the C+ pin and C– pin in order to lower the impedance of the wiring resistance, etc. High impedance may cause instable operation.
  Moreover, in selecting C_{PUMP}, perform a full evaluation of the actual usage conditions.

- The ON/$\overline{\text{OFF}}$ pin is configured as shown in **Figure 9** and is neither pulled up or down internally, so do not use this pin in a floating state. When not using the ON/$\overline{\text{OFF}}$ pin, connect it to the VIN pin.
  Moreover, please do not apply voltage higher than VIN + 0.3 V to an ON/$\overline{\text{OFF}}$ pin. Current flows for a VIN pin through the protection diode inside IC.

- Since this IC consists of double boost circuits, it cannot set more than twice voltage of V_{IN} to $V_{OUT(S)}$.

- Be careful about the usage conditions for the input/output voltages and output current to make sure that dissipation within the IC does not exceed the allowable power dissipation of the package.
  For reference, the calculation of the power consumption in this IC is shown below.
  $P_D=(V_{IN} \times 2.0 - V_{OUT}) \times (I_{OUT})$

  Reference: V_{IN}=4.2 V, V_{OUT}=5.5 V, I_{OUT}=10 mA
  $P_D=(4.2 \times 2.0 - 5.5) \times 0.010$=29 mW

- Since the information described herein is subject to change without notice, confirm that this is the latest one before using.

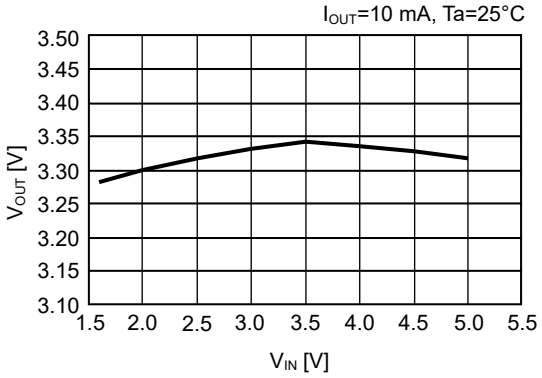
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

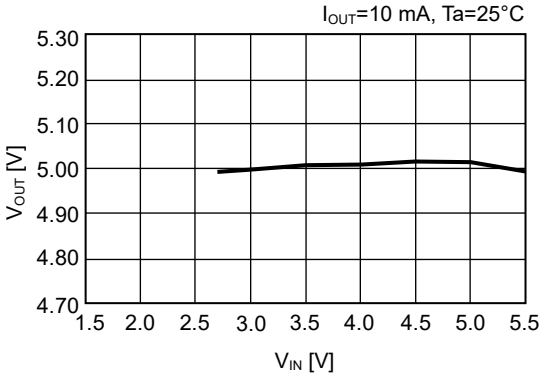
■ Characteristics (Typical Data)

(1) Output voltage vs. Operation input voltage

S-882133A

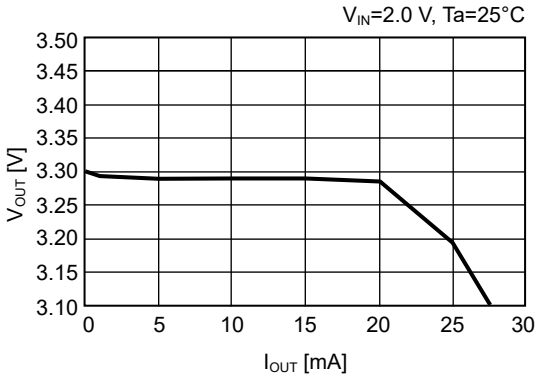


S-882150A

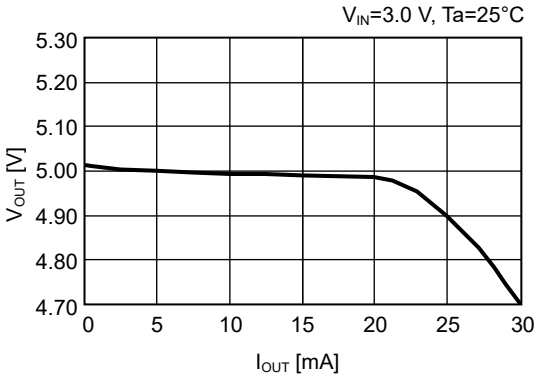


(2) Output voltage vs. Output current

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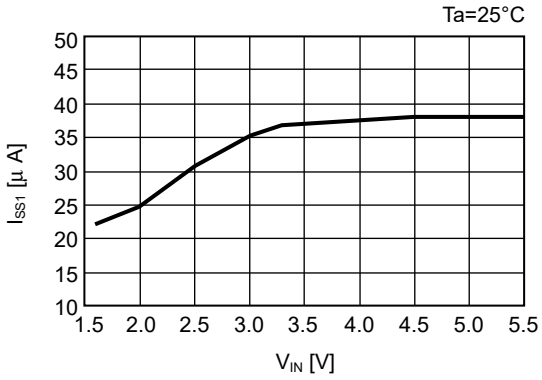


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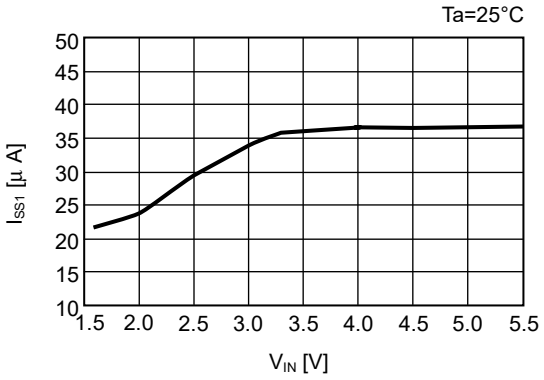


(3) Operation consumption vs. Operation input voltage

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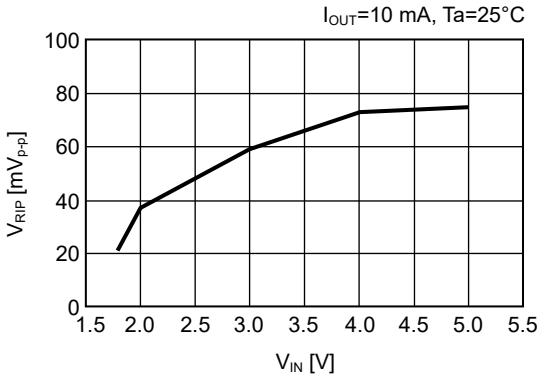


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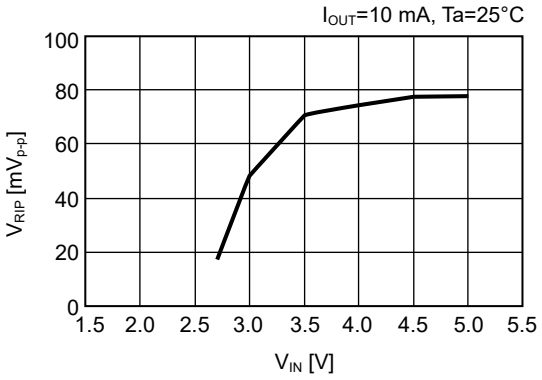


(4) Ripple voltage vs. Operation input voltage

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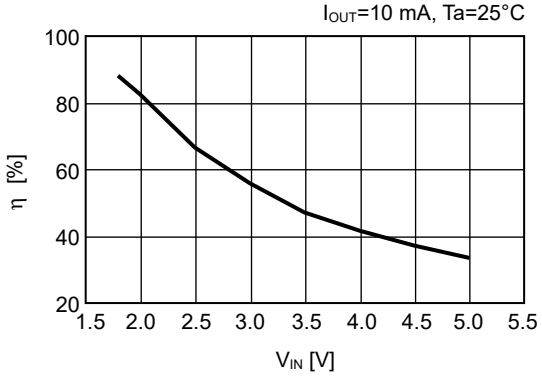


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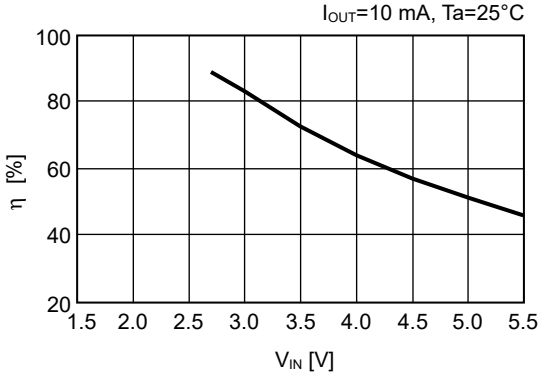


(5) Efficiency*1 vs. Operation input voltage

S-882133A



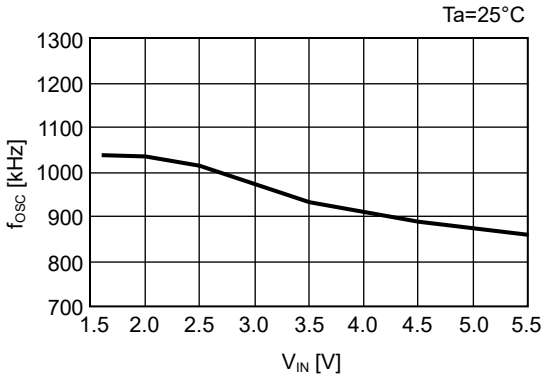
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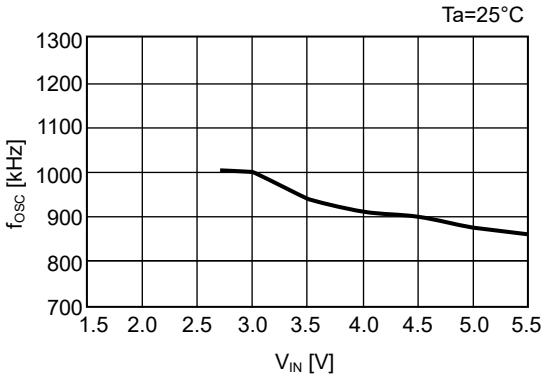
***1.** The ideal efficiency is indicated by the following expression.
Efficiency (η)=($V_{OUT} \times I_{OUT}$) / ($2.0 \times V_{IN} \times I_{OUT}$)

(6) Maximum oscillation frequency vs. Operation input voltage

S-882133A

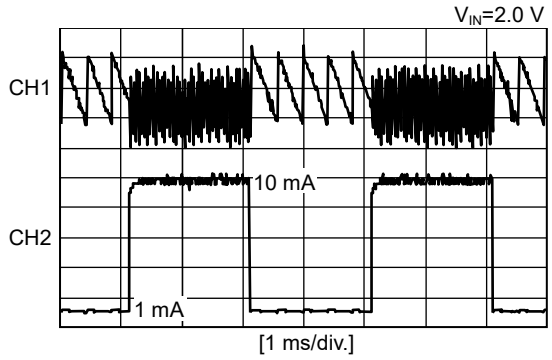


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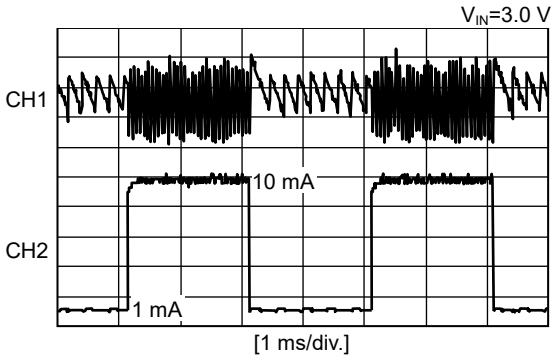
(7) Load fluctuation

S-882133A



CH1: V_{OUT} [20 mV/div.]
CH2: I_{OUT} [2 mA/div.]

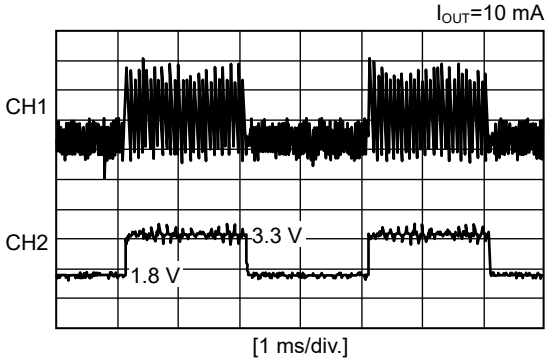
S-882150A



CH1: V_{OUT} [20 mV/div.]
CH2: I_{OUT} [2 mA/div.]

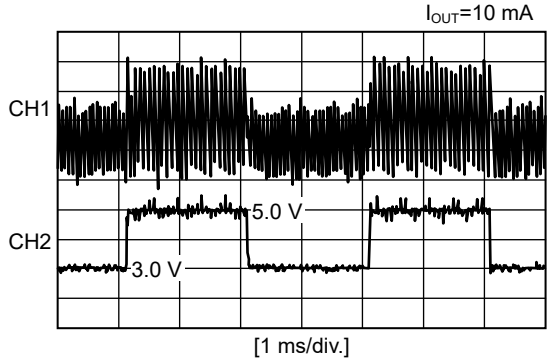
(8) Input voltage fluctuation

S-882133A

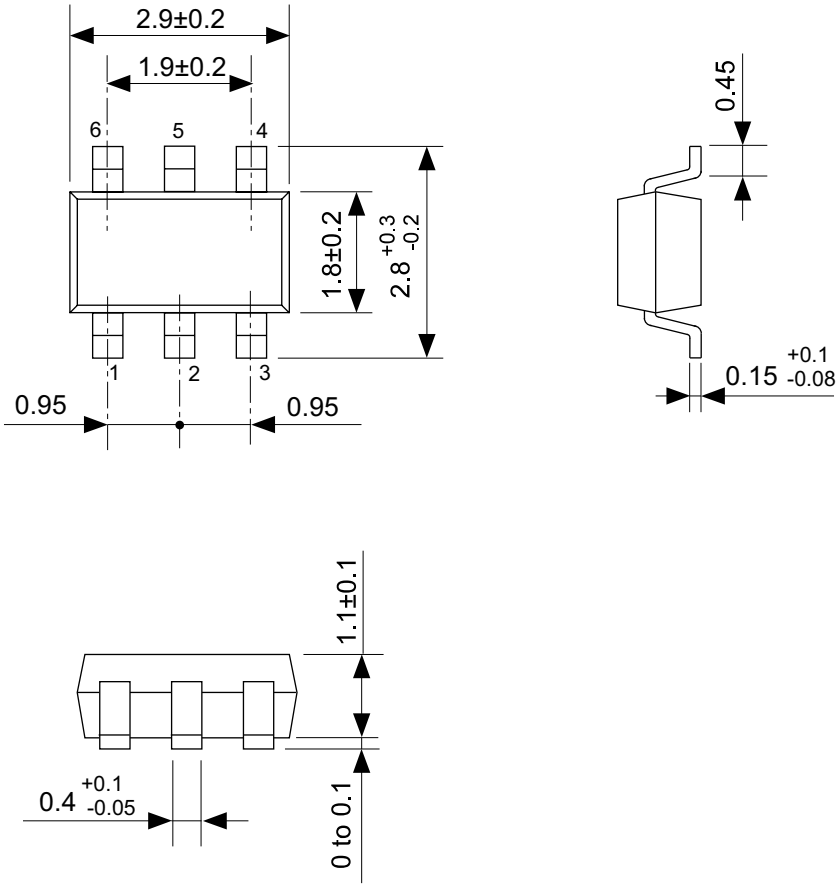


CH1: V_{OUT} [20 mV/div.]
CH2: V_{IN} [1 V/div.]

S-882150A

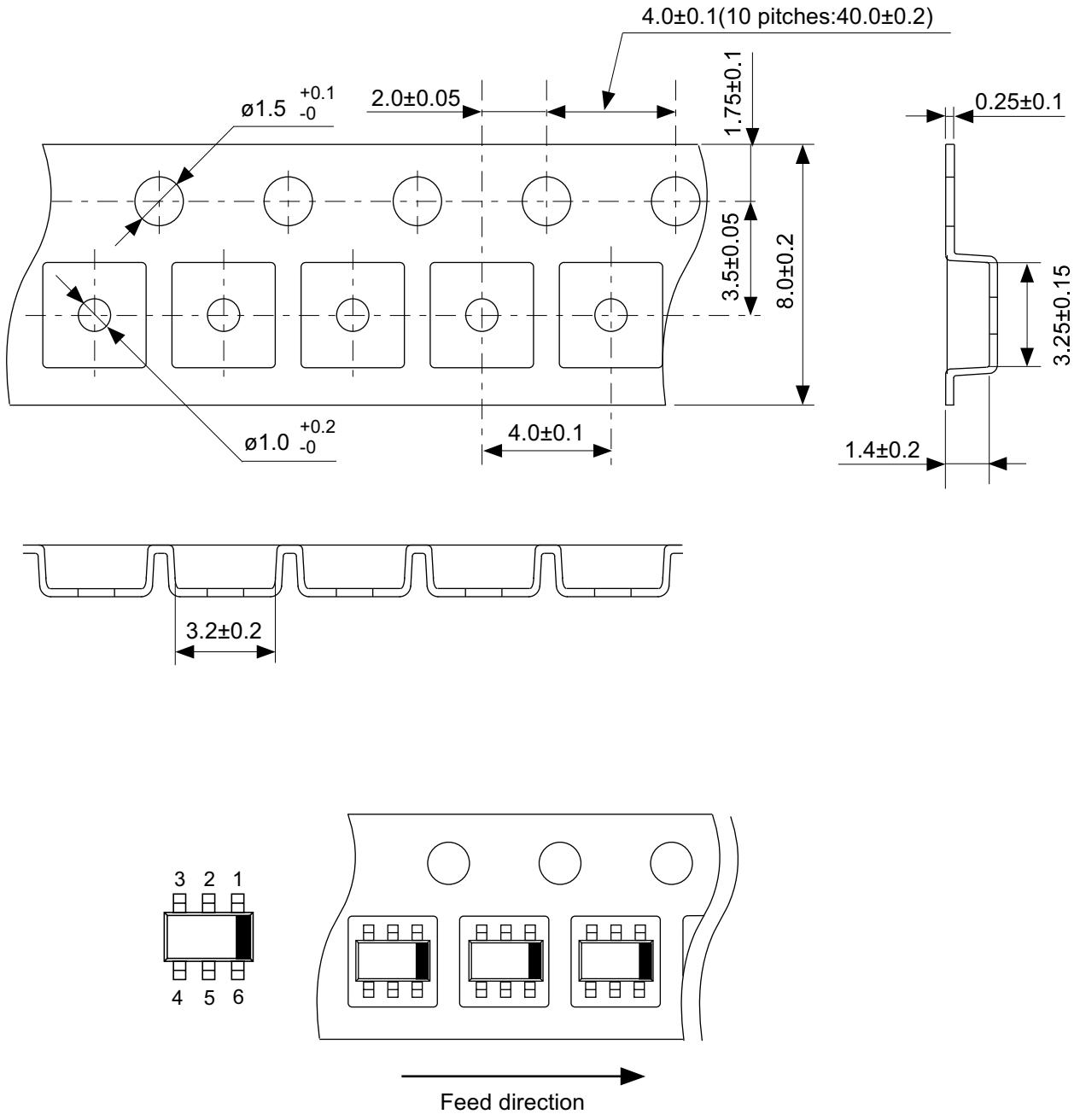


CH1: V_{OUT} [20 mV/div.]
CH2: V_{IN} [1 V/div.]



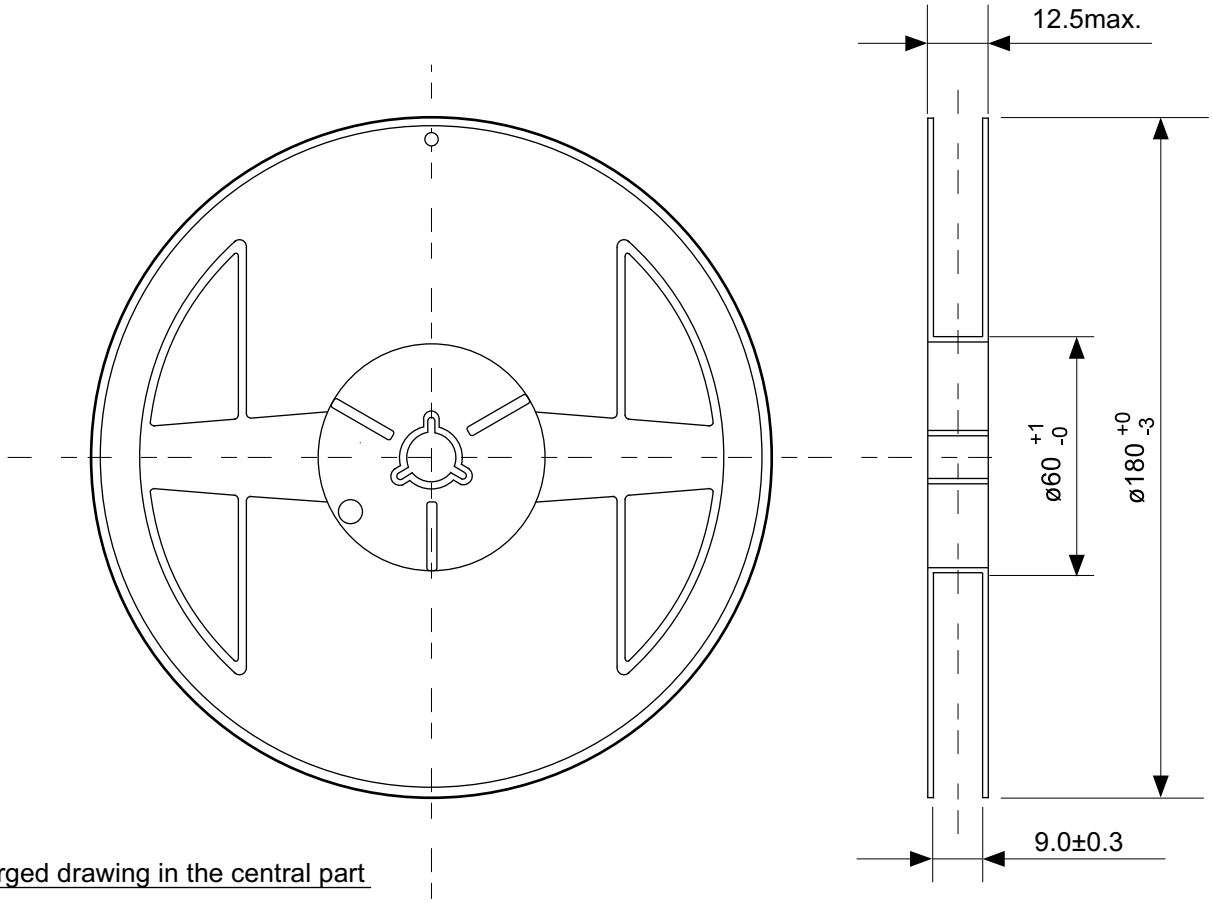
No. MP006-B-P-SD-2.1

TITLE	SOT236-B-PKG Dimensions
No.	MP006-B-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

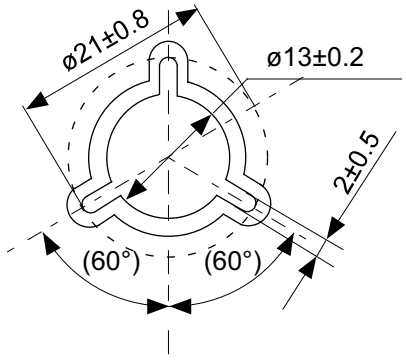


No. MP006-B-C-SD-1.0

TITLE	SOT236-B-Carrier Tape
No.	MP006-B-C-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.

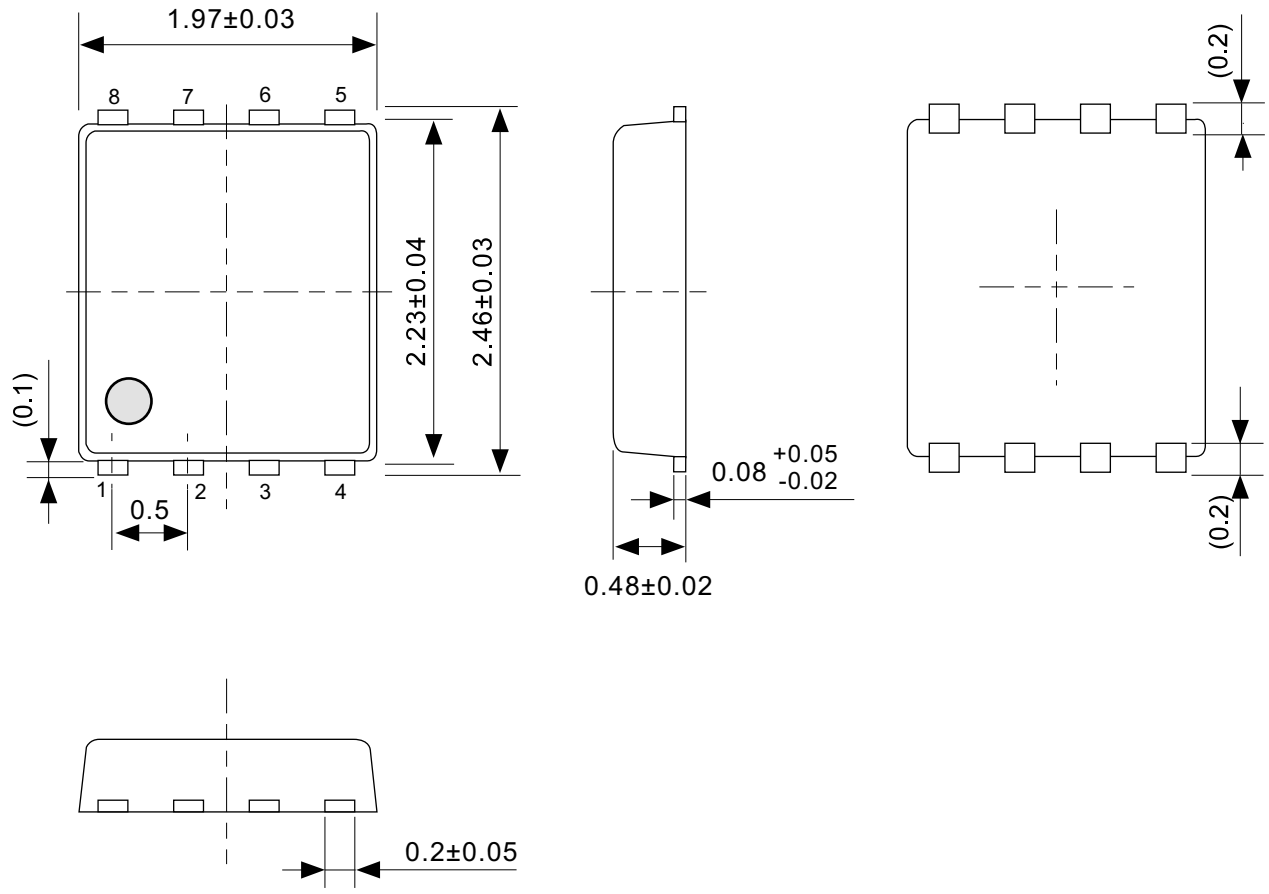


Enlarged drawing in the central part



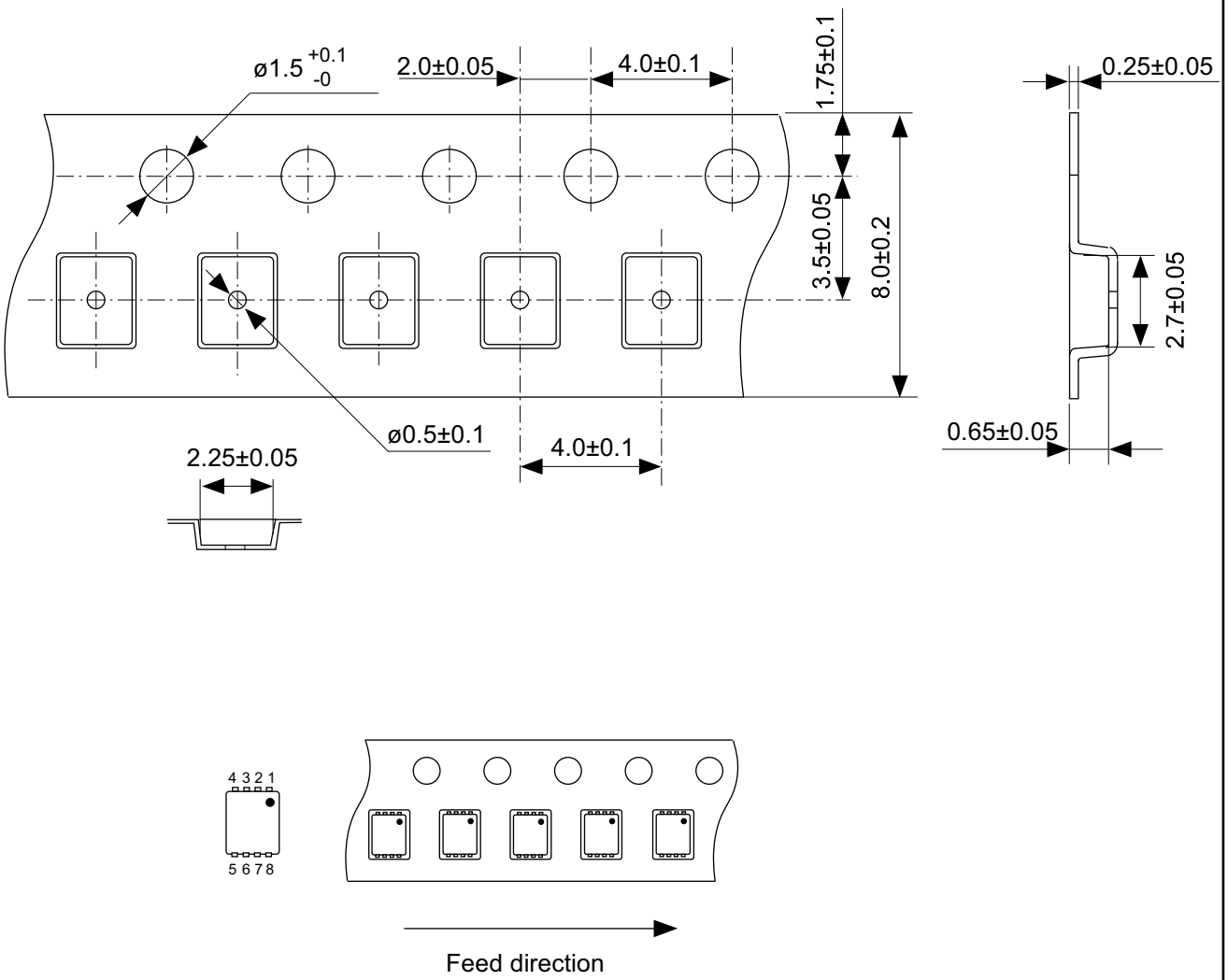
No. MP006-B-R-SD-1.0

TITLE	SOT236-B-Reel		
No.	MP006-B-R-SD-1.0		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			



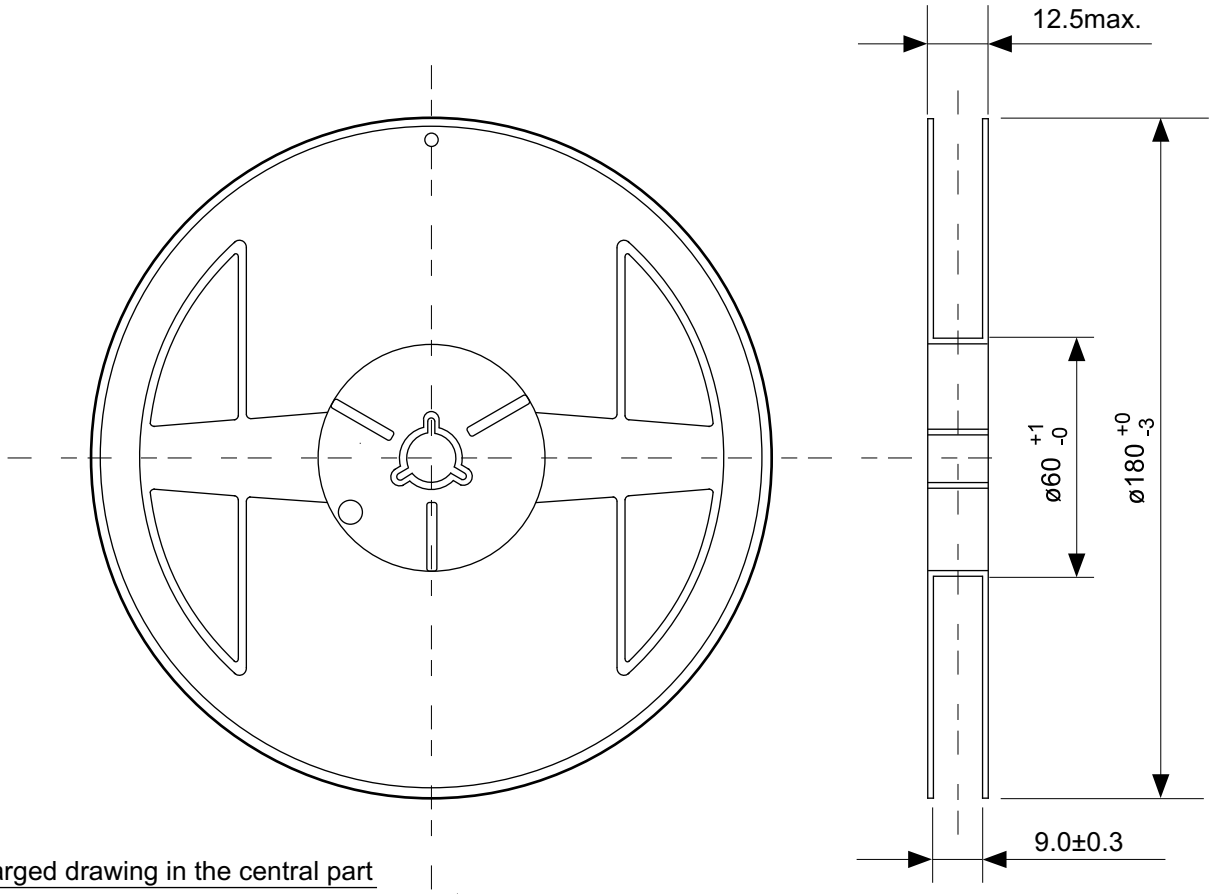
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

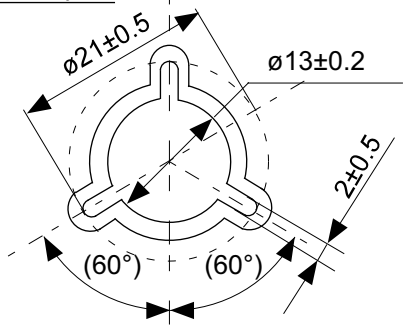


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

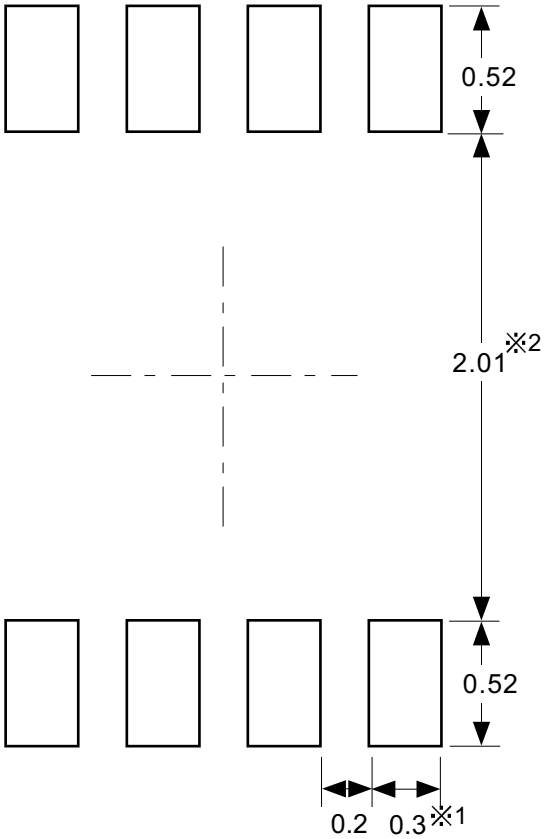


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意　1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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2.4-2019.07