SA604A

High-performance low-power FM IF system

Rev. 4.3 — 13 July 2016 Product data sheet

1. General description

The SA604A is an improved monolithic low-power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic received signal strength indicator, and voltage regulator. The SA604A features higher IF bandwidth (25 MHz) and temperature compensated RSSI and limiters providing wide RSSI dynamic range, high IF/limiter gain and overall stability. The SA604A is available in an SO16 (surface-mounted miniature) and HXQFN16 package.

2. Features and benefits

- Low power consumption: 3.3 mA typical
- Temperature compensated logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90 dB
- Two audio outputs — muted and un-muted
- Low external component count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5 μV across input pins (0.22 μV into 50 Ω matching network) for 12 dB SINAD (Signal-to-Noise and Distortion ratio) at 455 kHz
- SA604A meets cellular radio specifications

3. Applications

- Cellular radio FM IF
- High-performance communications receivers
- Intermediate frequency amplification and detection up to 25 MHz
- RF level meter
- Spectrum analyzer
- Instrumentation
- FSK and ASK data receivers

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
SA604AD/01	SA604AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
SA604AD/02	SA604AD	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
SA604AHR	04A	HXQFN16	plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.5 mm	SOT1039-2

4.1 Ordering options

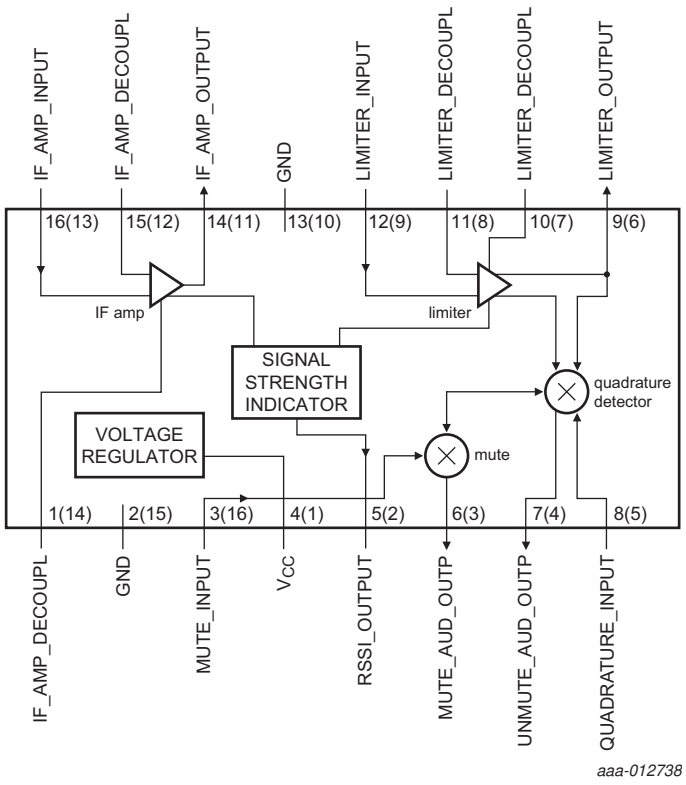
Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
SA604AD/01	SA604AD/01,112	SO16	Standard marking * IC's tube - DSC bulk pack	1000	T_{amb} = −40 °C to +85 °C
	SA604AD/01,118	SO16	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
SA604AD/02	SA604AD/02J	SO16	Reel 13" Q1/T1 *Standard mark SMD	2500	T_{amb} = −40 °C to +85 °C
SA604AHR	SA604AHRZ	HXQFN16	Reel 7" Q2/T3 *Standard mark SMD	1500	T_{amb} = −40 °C to +85 °C

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5. Block diagram



Pin numbers for SO16; HXQFN16 pins shown in parentheses

Fig 1. Block diagram of SA604A

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6. Pinning information

6.1 Pinning

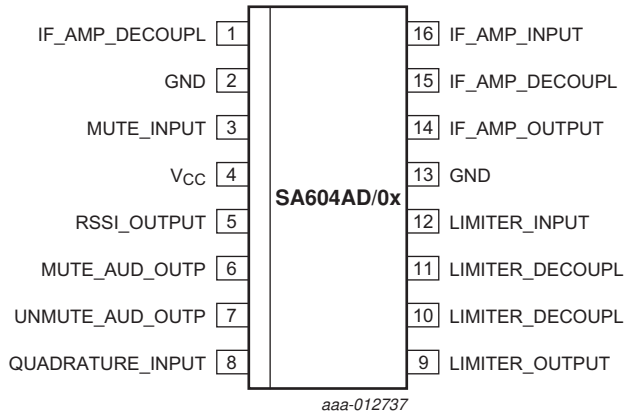
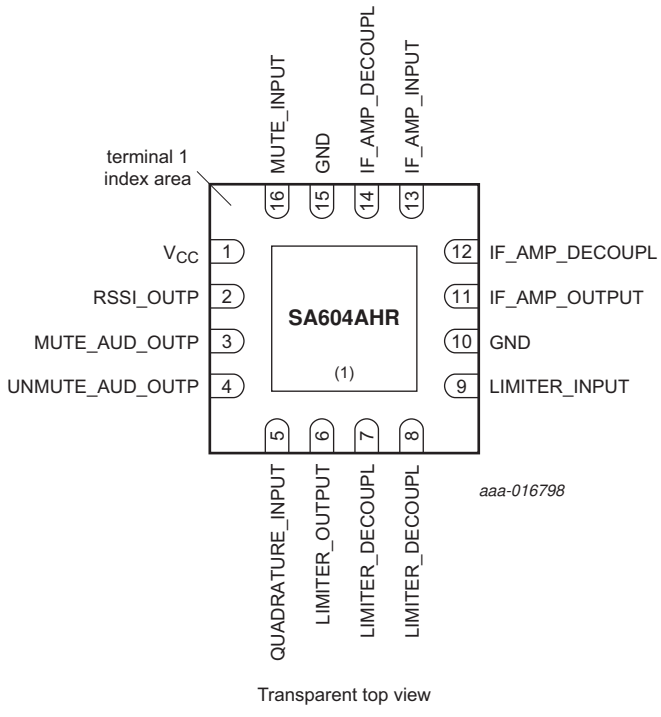


Fig 2. Pin configuration for SO16



(1) Die Attach Paddle (DAP).

Fig 3. Pin configuration for HXQFN16

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6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16	HXQFN16	
IF_AMP_DECOUPL	1	14	IF amplifier decoupling
GND	2	15	ground
MUTE_INPUT	3	16	mute input
V_{CC}	4	1	supply voltage
RSSI_OUTPUT	5	2	RSSI output
MUTE_AUD_OUTP	6	3	mute audio output
UNMUTE_AUD_OUTP	7	4	unmute audio output
QUADRATURE_INPUT	8	5	quadrature input
LIMITER_OUTPUT	9	6	limiter output
LIMITER_DECOUPL	10	7	limiter decoupling
LIMITER_DECOUPL	11	8	limiter decoupling
LIMITER_INPUT	12	9	limiter input
GND	13	10[1]	ground
IF_AMP_OUTPUT	14	11	IF amplifier output
IF_AMP_DECOUPL	15	12	IF amplifier decoupling
IF_AMP_INPUT	16	13	IF amplifier input
-	-	DAP	exposed Die Attach Paddle

[1] HXQFN16 package supply ground is connected to both GND pin and exposed center pad. GND pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board. For proper heat conduction through the board, thermal vias must be incorporated in the PCB in the thermal pad region.

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7. Functional description

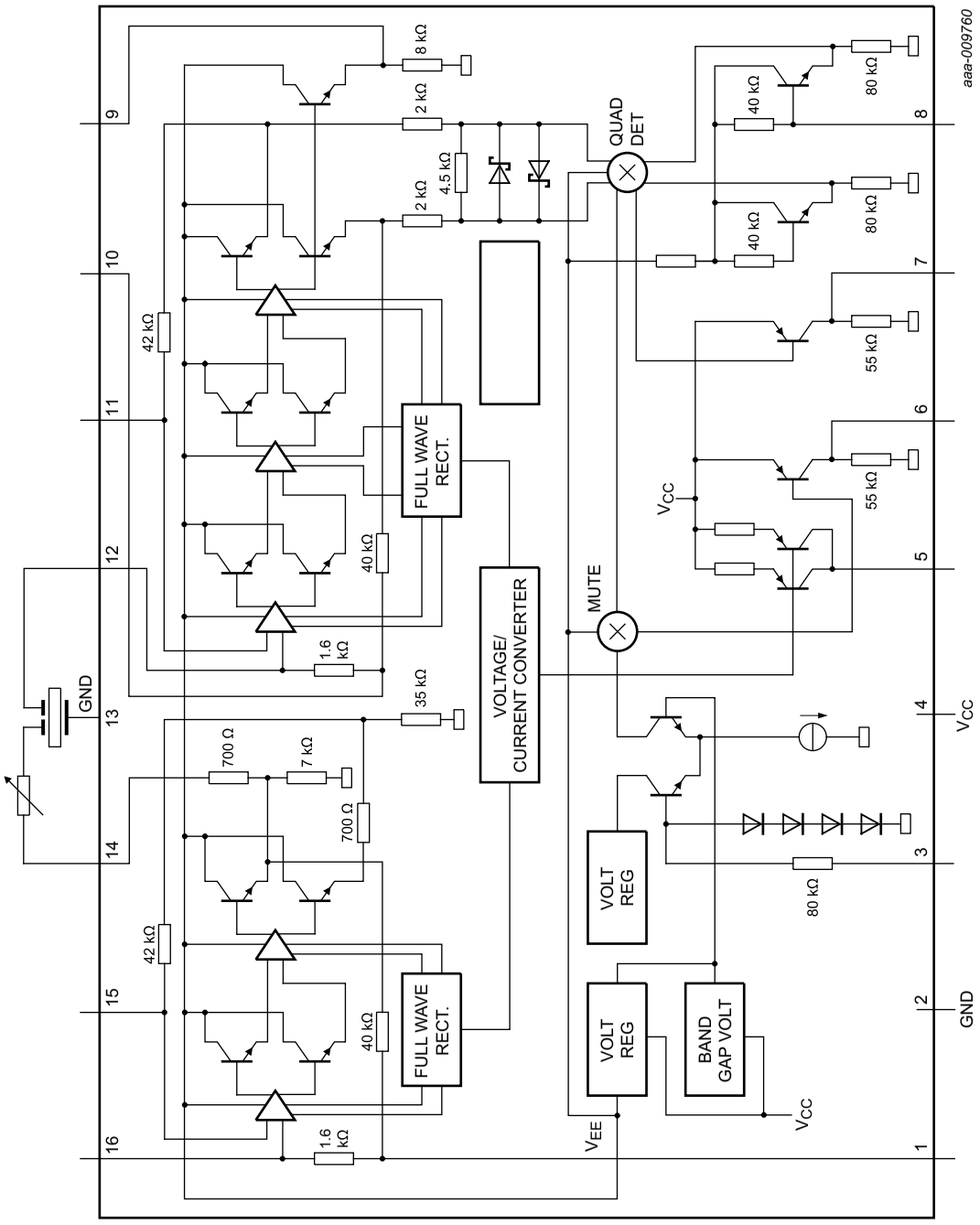


Fig 4. Equivalent circuit

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8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	9	V
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-a)}$	transient thermal impedance from junction to ambient	SO16 package	90	K/W
		HXQFN16 package	75	K/W

10. Static characteristics

Table 6. Static characteristics

V_{CC} = 6 V; T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	8.0	V
I_{CC}	supply current		2.5	3.3	4.0	mA
V_{th}	threshold voltage	mute switch-on	1.7	-	-	V
		mute switch-off	-	-	1.0	V

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11. Dynamic characteristics

Table 7. Dynamic characteristics

Typical reading at T_{amb} = 25 °C; V_{CC} = 6 V, unless specified otherwise. IF frequency = 455 kHz; IF level = −47 dBm; FM modulation = 1 kHz with ±8 kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor. Test circuit Figure 14. The parameters listed below are tested using automatic test equipment to assure consistent electrical characteristics. The limits do not represent the ultimate performance limits of the device. Use of an optimized RF layout will improve many of the listed parameters.

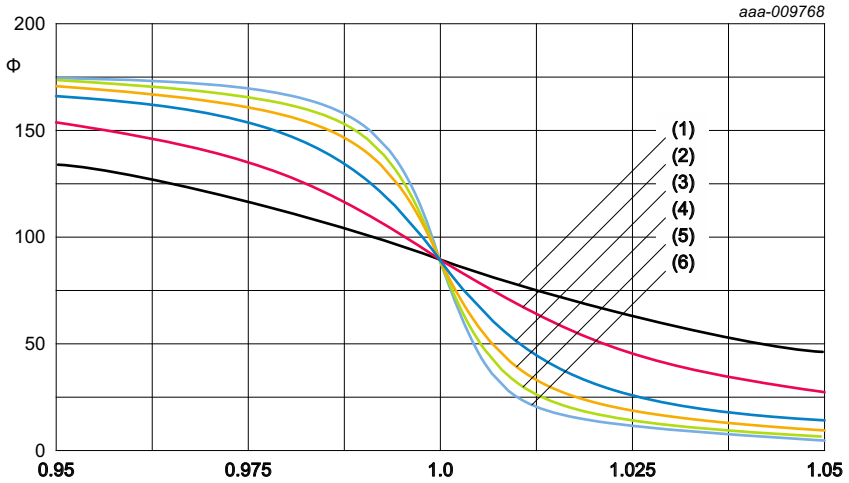
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	input limiting −3 dB	test at pin IF_AMP_INPUT; per 50 Ω	-	−92	-	dBm
α_{AM}	AM rejection	80 % AM 1 kHz	30	34	-	dB
	recovered audio level	15 nF de-emphasis; RMS value	80	175	260	mV
		150 pF de-emphasis; RMS value	-	530	-	mV
THD	total harmonic distortion		−34	−42	-	dB
S/N	signal-to-noise ratio	no modulation for noise	-	73	-	dB
$V_{o(RSSI)}$	RSSI output voltage	IF level = −118 dBm [1]	0	160	650	mV
		IF level = −68 dBm (SA604AD/01, SA604AHR) [1]	1.9	2.65	3.1	V
		IF level = −68 dBm (SA604AD/02) [1]	2.1	2.65	3.1	V
		IF level = −18 dBm [1]	4.0	4.85	5.6	V
$\alpha_{RSSI(range)}$	RSSI range	R4 = 100 kΩ (pin RSSI_OUTPUT)	-	90	-	dB
	RSSI accuracy	R4 = 100 kΩ (pin RSSI_OUTPUT)	-	±1.5	-	dB
$Z_{i(IF)}$	IF input impedance		1.4	1.6	-	kΩ
$Z_{o(IF)}$	IF output impedance		0.85	1.0	-	kΩ
$Z_{i(lim)}$	limiter input impedance		1.4	1.6	-	kΩ
R_o	output resistance	unmuted audio	-	58	-	kΩ
		muted audio	-	58	-	kΩ

[1] IF level is referenced to level at IF pin which is at 1.5 kΩ input impedance.

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12. Performance curves



Normalized IF frequency: $\frac{\omega}{\omega_1} = 1 + \frac{\Delta\omega}{\omega_1}$

(1) Q = 10
(2) Q = 20
(3) Q = 40
(4) Q = 60
(5) Q = 80
(6) Q = 100

Fig 5. Phase as a function of normalized IF frequency

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13. Application information

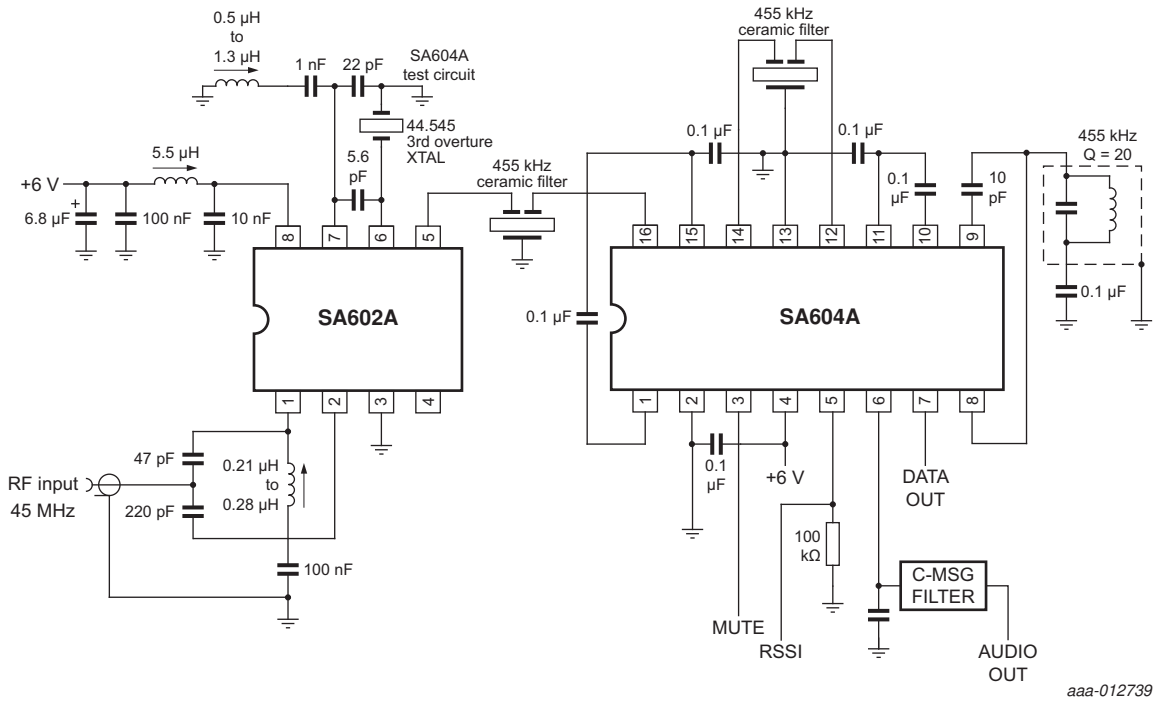
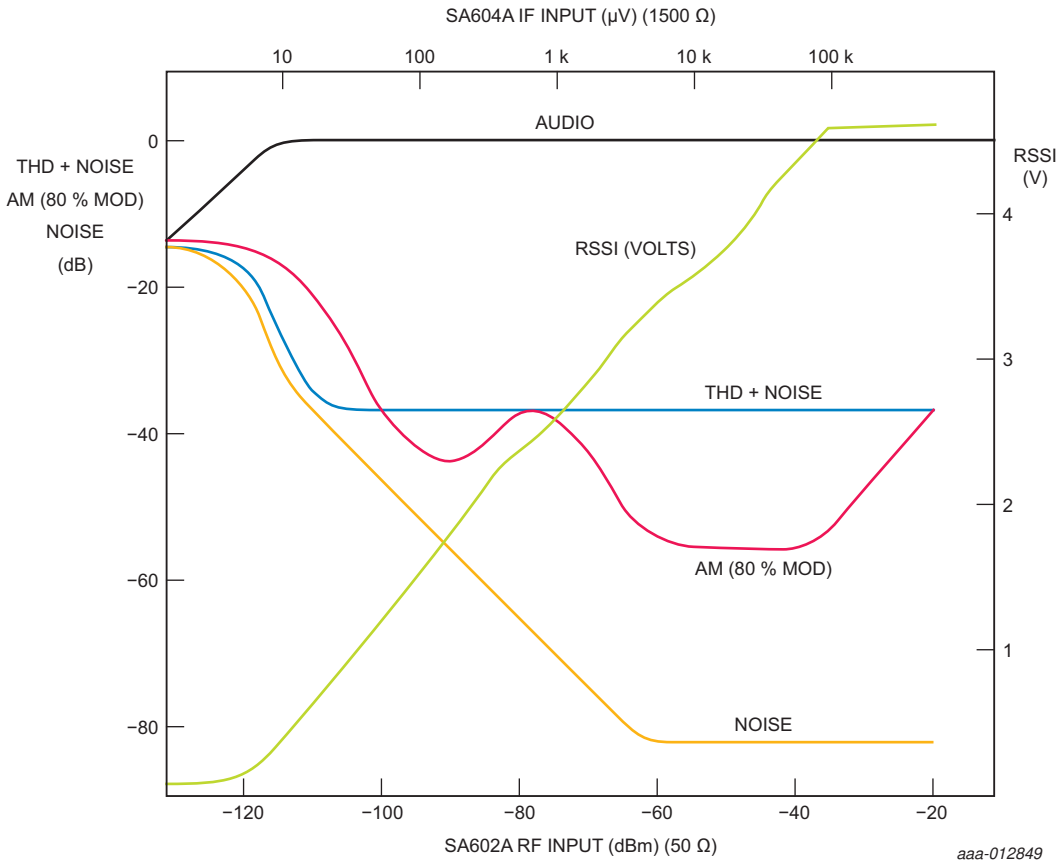


Fig 6. Typical application cellular radio (45 MHz RF input and 455 kHz IF)

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Audio output: C message weighted; 0 dB reference = recovered audio for 8 kHz peak deviation (dB)

Fig 7. Performance of the typical cellular radio application

13.1 Circuit description

The SA604A is a very high gain, high frequency device. Correct operation is not possible if good RF layout and gain stage practices are not used. The SA604A cannot be evaluated independent of circuit, components, and board layout. A physical layout which correlates to the electrical limits is shown in Figure 17. This configuration can be used as the basis for production layout.

The SA604A is an IF signal processing system suitable for IF frequencies as high as 21.4 MHz. The device consists of two limiting amplifiers, quadrature detector, direct audio output, muted audio output, and signal strength indicator (with log output characteristic). The equivalent circuit is shown in Figure 4.

Figure 7 is the performance of the typical cellular radio application shown in Figure 6 with 45 MHz RF input and 455 kHz IF.

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13.2 IF amplifiers

The IF amplifier section consists of two log-limiting stages. The first consists of two differential amplifiers with 39 dB of gain and a small signal bandwidth of 41 MHz (when driven from a 50 Ω source). The output of the first limiter is a low-impedance emitter follower with 1 kΩ of equivalent series resistance. The second limiting stage consists of three differential amplifiers with a gain of 62 dB and a small signal AC bandwidth of 28 MHz. The outputs of the final differential stage are buffered to the internal quadrature detector. One of the outputs is available at pin LIMITER_OUTPUT to drive an external quadrature capacitor and L/C quadrature tank.

Both of the limiting amplifier stages are DC biased using feedback. The buffered output of the final differential amplifier is fed back to the input through 42 kΩ resistors. As shown in Figure 4, the input impedance is established for each stage by tapping one of the feedback resistors 1.6 kΩ from the input. It requires one additional decoupling capacitor from the tap point to ground.

Because of the very high gain, bandwidth and input impedance of the limiters, there is a very real potential for instability at IF frequencies above 455 kHz. The basic phenomenon is shown in Figure 10. Distributed feedback (capacitance, inductance and radiated fields) forms a divider from the output of the limiters back to the inputs (including RF input). If this feedback divider does not cause attenuation greater than the gain of the forward path, then oscillation or low-level regeneration is likely. If regeneration occurs, two symptoms may be present:

1. The RSSI output is high with no signal input (should nominally be 250 mV or lower).
2. The demodulated output demonstrates a threshold. Above a certain input level, the limited signal begins to dominate the regeneration, and the demodulator begins to operate in a normal manner.

There are three primary ways to deal with regeneration:

1. Minimize the feedback by gain stage isolation.
2. Lower the stage input impedances, thus increasing the feedback attenuation factor.
3. Reduce the gain. Gain reduction can effectively be accomplished by adding attenuation between stages, which can also lower the input impedance. Examples of impedance/gain adjustment are shown in Figure 11. Reduced gain results in reduced limiting sensitivity.

A feature of the SA604A IF amplifiers, which is not specified, is low phase shift. The SA604A is fabricated with a 10 GHz process with very small collector capacitance. It is advantageous in some applications that the phase shift changes only a few degrees over a wide range of signal input amplitudes.

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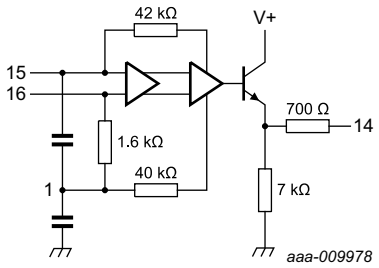


Fig 8. First limiter bias

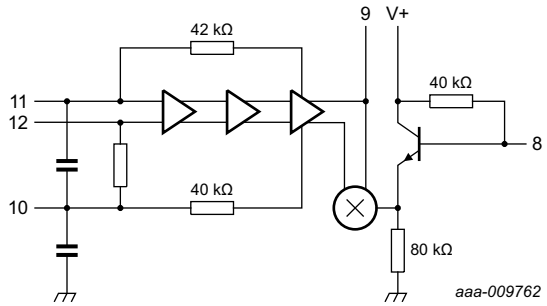


Fig 9. Second limiter and quadrature detector

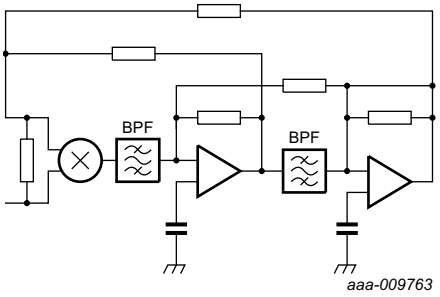
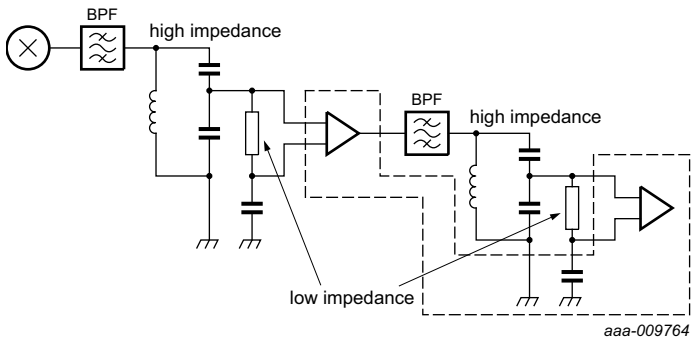
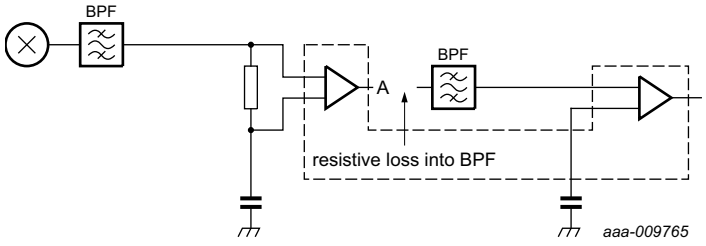


Fig 10. Feedback paths



a. Terminating HIGH impedance filters with transformation to LOW impedance



b. LOW impedance termination and gain reduction

Fig 11. Practical termination

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13.3 Stability considerations

The high gain and bandwidth of the SA604A in combination with its very low currents permit circuit implementation with superior performance. However, stability must be maintained and, to do that, every possible feedback mechanism must be addressed. These mechanisms are:

- supply lines and ground
- stray layout inductances and capacitances
- radiated fields
- phase shift

As the system IF increases, so must the attention to fields and strays. However, ground and supply loops cannot be overlooked, especially at lower frequencies. Even at 455 kHz, if the supply line is not decoupled, using the test layout in Figure 17, instability occurs. To decouple, use two high-quality RF capacitors, a 0.1 μF monolithic on the V_{CC} pin, and a 6.8 μF tantalum on the supply line. An electrolytic is not an adequate substitute. At 10.7 MHz, a 1 μF tantalum has proven acceptable with this layout. Every layout must be evaluated on its own merit, but do not underestimate the importance of good supply bypass.

At 455 kHz, if the layout of Figure 17 or one substantially similar is used, ceramic filters can be connected directly to the input and between limiter stages with no special consideration. At frequencies above 2 MHz, some input impedance reduction is usually necessary. Figure 11 demonstrates a practical means.

As illustrated in Figure 12, 430 Ω external resistors are applied in parallel to the internal 1.6 kΩ load resistors, thus presenting approximately 330 Ω to the filters. The input filter is a crystal type for narrowband selectivity. The filter is terminated with a tank which transforms to 330 Ω. The interstage filter is a ceramic type which does not contribute to system selectivity, but does suppress wideband noise and stray signal pickup. In wideband 10.7 MHz IFs the input filter can also be ceramic, directly connected to pin IF_AMP_INPUT.

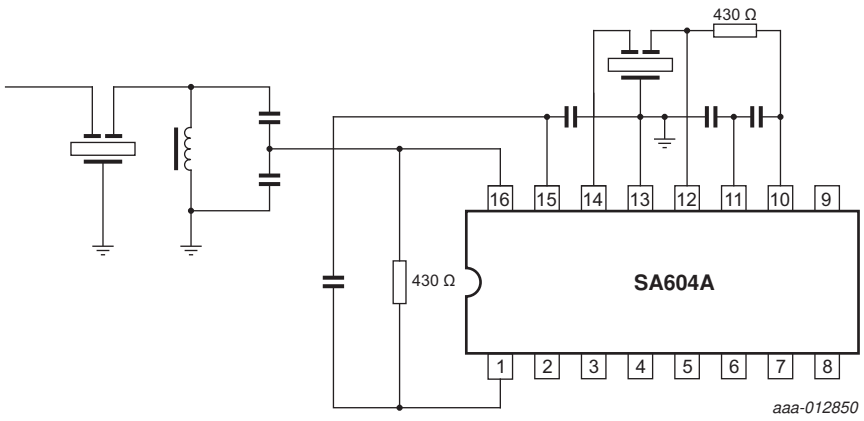


Fig 12. Crystal input filter with ceramic interstage filter

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In some products, it may be impractical to utilize shielding, but this mechanism may be appropriate to 10.7 MHz and 21.4 MHz IF. One of the benefits of low current is lower radiated field strength, but lower does not mean non-existent. A spectrum analyzer with an active probe clearly shows IF energy with the probe held in the proximity of the second limiter output or quadrature coil. No specific recommendations are provided, but mechanical shielding should be considered if layout, bypass, and input impedance reduction do not solve a stubborn instability.

The final stability consideration is phase shift. The phase shift of the limiters is very low, but there is phase shift contribution from the quadrature tank and the filters. Most filters demonstrate a large phase shift across their passband (especially at the edges). If the quadrature detector is tuned to the edge of the filter passband, the combined filter and quadrature phase shift can aggravate stability. It is not usually a problem, but should be kept in mind.

13.4 Quadrature detector

Figure 9 shows an equivalent circuit of the SA604A quadrature detector. It is a multiplier cell similar to a mixer stage. Instead of mixing two different frequencies, it mixes two signals of common frequency but different phase. Internal to the device, a constant amplitude (limited) signal is differentially applied to the lower port of the multiplier. The same signal is applied single-ended to an external capacitor at pin LIMITER_OUTPUT. There is a 90° phase shift across the plates of this capacitor. The phase shifted signal applied to the upper port of the multiplier is at pin QUADRATURE_INPUT. A quadrature tank (parallel L/C network) permits frequency selective phase shifting at the IF frequency. This quadrature tank must be returned to ground through a DC blocking capacitor.

The loaded Q of the quadrature tank impacts three fundamental aspects of the detector: distortion, maximum modulated peak deviation, and audio output amplitude. Typical quadrature curves are illustrated in Figure 5. The phase angle translates to a shift in the multiplier output voltage.

Thus a small deviation gives a large output with a high Q tank. However, as the deviation from resonance increases, the non-linearity of the curve increases (distortion). With too much deviation, the signal is outside the quadrature region (limiting the peak deviation which can be demodulated). If the same peak deviation is applied to a lower Q tank, the deviation remains in a region of the curve which is more linear (less distortion). However, it creates a smaller phase angle (smaller output amplitude). Thus the Q of the quadrature tank must be tailored to the design. Basic equations and an example for determining Q are shown in Section 13.5. This explanation includes first-order effects only.

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13.5 Frequency discriminator design equations

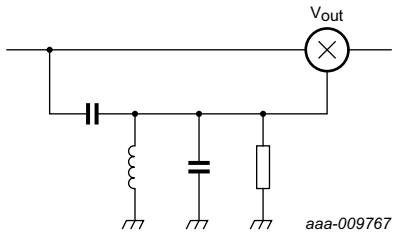


Fig 13. Frequency discriminator

$$V_O = \frac{C_S}{C_P + C_S} \bullet \frac{1}{1 + \frac{\omega_1}{Q_1 S} + \left(\frac{\omega_1}{S}\right)^2} \bullet V_{IN} \quad (1)$$

where: $\omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}}$ and $Q_1 = R(C_P + C_S)\omega_1$

From Equation 1, the phase shift between nodes 1 and 2, or the phase across C_S will be:

$$\phi = \angle V_O - \angle V_{IN} = (t_g)^{-1} \bullet \left[\frac{\frac{\omega_1}{Q_1 \omega}}{1 - \left(\frac{\omega_1}{\omega}\right)^2}\right] \quad (2)$$

Figure 5 is the plot of ϕ as a function of $\left(\frac{\omega_1}{\omega}\right)$. It is notable that at $\omega = \omega_1$, the phase shift is $\frac{\pi}{2}$ and the response is close to a straight line with a slope of $\frac{\Delta\phi}{\Delta\omega} = \frac{2Q_1}{\omega_1}$.

The signal V_O would have a phase shift of $\frac{\pi}{2} - \frac{2Q_1}{\omega_1}\omega$ with respect to the V_{IN}.

If V_{IN} = A sin(ωt) =>

$$V_O = A\sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1} \cdot \omega\right] \quad (3)$$

Multiplying the two signals in the mixer, and low pass filtering yields:

$$V_{IN} \bullet V_O = A^2 \sin\omega t \cdot \sin\left[\omega t + \frac{\pi}{2} - \frac{2Q_1}{\omega_1} \cdot \omega\right] \quad (4)$$

After low pass filtering =>

$$V_O = \frac{1}{2}A^2 \cos\left[\frac{\pi}{2} - \frac{2Q_1}{\omega_1} \cdot \omega\right] = \frac{1}{2}A^2 \sin\left[\frac{2Q_1}{\omega_1} \cdot \omega\right] \quad (5)$$

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$$V_O \propto 2Q_1\frac{\omega}{\omega_1} = 2Q_1\left(\frac{\omega_1 + \Delta\omega}{\omega_1}\right) \quad (6)$$

For $2Q_1\frac{\omega}{\omega_1} << \frac{\pi}{2}$ which is discriminated FM output. Note that $\Delta\omega$ is the deviation frequency from the carrier ω_1 [1]. Example: at 455 kHz IF, with ±5 kHz FM deviation, the maximum normalized frequency is (455 ± 5)/455 kHz = 1.010 or 0.990.

Go to the frequency as a function of normalized frequency curves (Figure 5) and draw a vertical straight line at $\frac{\omega}{\omega_1}$ = 1.01.

The curves with Q = 100, Q = 40 are not linear, but Q = 20 and less shows better linearity for this application. Too small Q decreases the amplitude of the discriminated FM signal. Equation 6 => Choose a Q = 20.

The internal resistance of the SA604A is 40 kΩ. From $Q_1 = R(C_P + C_S)\omega_1$, and then $\omega_1 = \frac{1}{\sqrt{L(C_P + C_S)}}$, it results that $C_P + C_S$ = 174 pF and L = 0.7 mH.

A more exact analysis including the source resistance of the previous stage shows a series and a parallel resonance in the phase detector tank. To make the parallel and series resonances close, and to get maximum attenuation of higher harmonics at 455 kHz IF, a C_S = 10 pF and C_P = 164 pF provided the best results. For commercial purposes, values of 150 pF or 180 pF may be practical. A variable inductor which can be adjusted around 0.7 mH should be chosen and optimized for minimum distortion. (For 10.7 MHz, a value of C_S = 1 pF is recommended.)

13.6 Audio outputs

Two audio outputs are provided. Both are PNP current-to-voltage converters with 55 kΩ nominal internal loads. The unmuted output is always active to permit the use of signaling tones in systems such as cellular radio. The other output can be muted with 70 dB typical attenuation. The two outputs have an internal 180° phase difference.

The nominal frequency response of the audio outputs is 300 kHz. This response can be increased with the addition of external resistors between the output pins and ground. The resistors are placed in parallel with the internal 55 kΩ resistors and they lower the output time constant. The output structure is a current-to-voltage converter where current is driven into the resistance, creating a voltage drop. By adding external parallel resistance, it also lowers the output audio amplitude and DC level.

This technique of audio bandwidth expansion can be effective in many applications such as SCA receivers and data transceivers. Because the two outputs have a 180° phase relationship, FSK demodulation can be accomplished by applying the two outputs differentially across the inputs of an op amp or comparator. Once the threshold of the reference frequency (or no-signal condition) has been established, the two outputs shift in opposite directions (higher or lower output voltage) as the input frequency shifts. The

1. Ref. Krauss, Raab, Bastian: Solid-State radio Eng.; Wiley, 1980, p.311.

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output of the comparator is logic output. The choice of op amp or comparator depends on the data rate. With high IF frequency (10 MHz and above), and wide IF bandwidth (L/C filters) data rates in excess of 4 MBd are possible.

13.7 RSSI

The Received Signal Strength Indicator (RSSI), of the SA604A demonstrates monotonic logarithmic output over a range of 90 dB. The signal strength output is derived from the summed stage currents in the limiting amplifiers. It is independent of the IF frequency. Thus, unfiltered signals at the limiter inputs, spurious products, or regenerated signals manifest themselves as RSSI outputs. An RSSI output of greater than 250 mV with no signal (or a very small signal) applied, is an indication of possible regeneration or oscillation.

To achieve optimum RSSI linearity, there must be a 12 dB insertion loss between the first and second limiting amplifiers. With a typical 455 kHz ceramic filter, there is a nominal 4 dB insertion loss in the filter. An additional 6 dB is lost in the interface between the filter and the input of the second limiter. A small amount of additional loss must be introduced with a typical ceramic filter. In the test circuit used for cellular radio applications (Figure 6), the optimum linearity was achieved with a 5.1 kΩ resistor. The resistor was placed between the output of the first limiter (pin IF_AMP_OUTPUT) and the input of the interstage filter. With this resistor from pin IF_AMP_OUTPUT to the filter, sensitivity of 0.25 μV for 12 dB SINAD was achieved. With the 3.6 kΩ resistor, sensitivity was optimized at 0.22 μV for 12 dB SINAD with minor change in the RSSI linearity.

Any application requiring optimized RSSI linearity, such as spectrum analyzers, cellular radio, and certain types of telemetry, requires careful attention to limiter interstage component selection. This is especially true with high IF frequencies which require insertion loss or impedance reduction for stability.

At low frequencies, the RSSI makes an excellent logarithmic AC voltmeter.

For data applications, the RSSI is effective as an Amplitude Shift Keyed (ASK) data slicer. If a comparator is applied to the RSSI and the threshold set slightly above the no signal level, when an in-band signal is received the comparator is sliced. Unlike FSK demodulation, the maximum data rate is limited. An internal capacitor limits the RSSI frequency response to approximately 100 kHz. At high data rates, the rise and fall times are not symmetrical.

The RSSI output is a current-to-voltage converter similar to the audio outputs. However, an external resistor is required. With a 91 kΩ resistor, the output characteristic is 0.5 V for a 10 dB change in the input amplitude.

13.8 Additional circuitry

Internal to the SA604A are voltage and current regulators which have been temperature compensated to maintain the performance of the device over a wide temperature range. These regulators are not accessible to the user.

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14. Test information

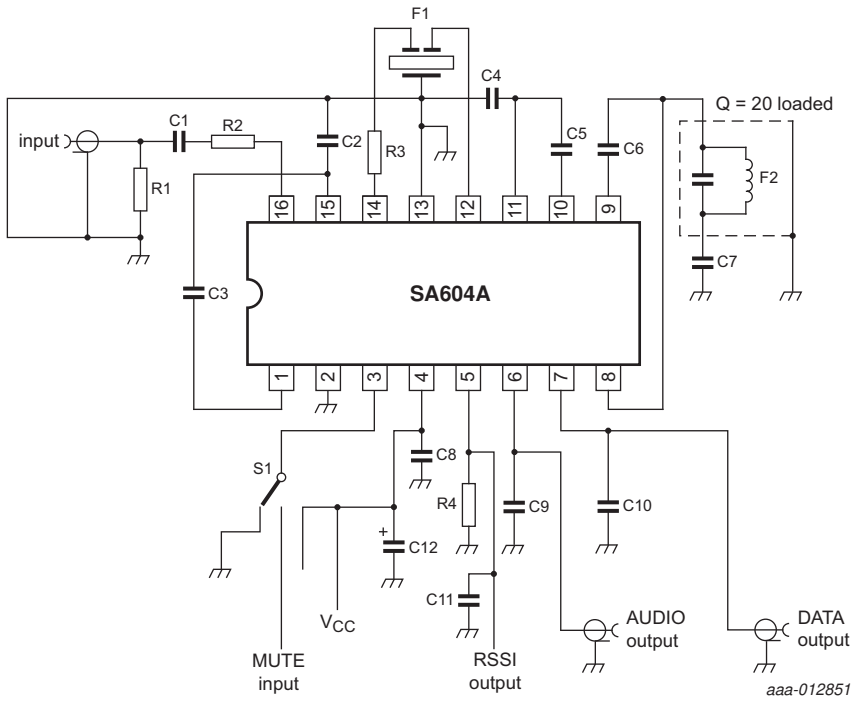


Fig 14. SA604A test circuit

Table 8. SA604AD/01 demo board component list

Component	Value	Description
C1	100 nF, +80 %, −20 %,63 V	K10000-25V ceramic
C2	100 nF, +10 %, 50 V	-
C3	100 nF, ±10 %, 50 V	-
C4	100 nF, +10 %, 50 V	-
C5	100 nF, ±10 %, 50 V	-
C6	10 pF, ±2 %, 100 V	NPO ceramic
C7	100 nF, ±10 %, 50 V	-
C8	100 nF, ±10 %, 50 V	-
C9	15 nF, ±10 %, 50 V	-
C10	150 pF ±2 %, 100 V	N1500 ceramic
C11	1 nF, ±10 %, 100 V	K2000-Y5P ceramic
C12	6.8 μF ±20 %, 25 V	tantalum
F1	455 kHz	ceramic filter Murata SFG455A3
F2	455 kHz, Ce = 180 pF	Toko RMC 2A6597H
R1	51 Ω, ±1 %, 1/4 W	metal film
R2	1500 Ω, ±1 %, 1/4 W	metal film
R3	1500 Ω, ±5 %, 1/8 W	carbon composition
R4	100 kΩ, ±1 %, 1/4 W	metal film

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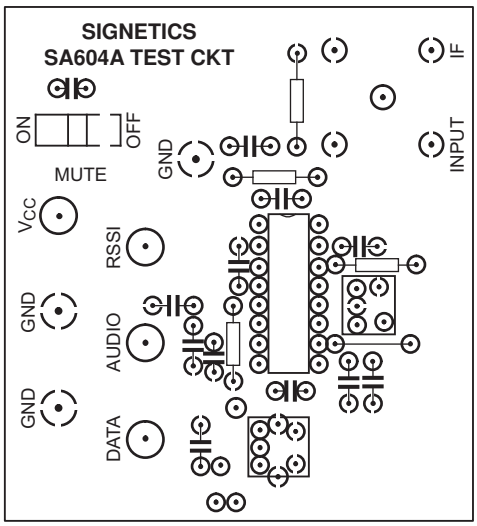


Fig 15. Components layout (viewed from the top)

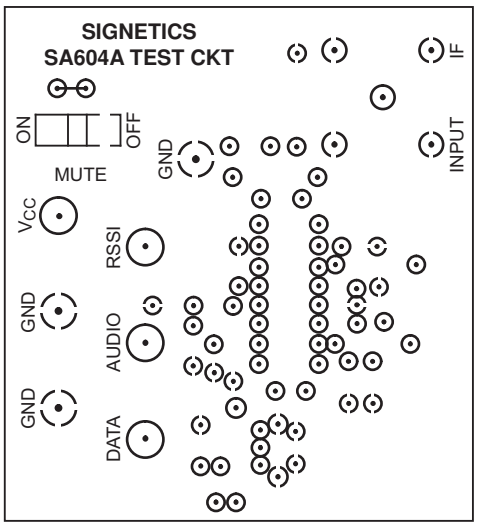


Fig 16. Bottom layout (viewed from the top)

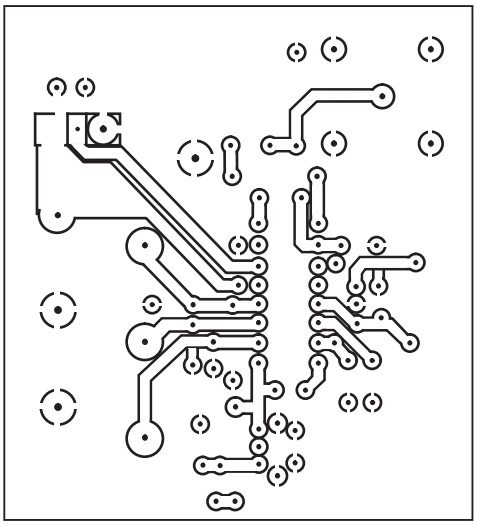


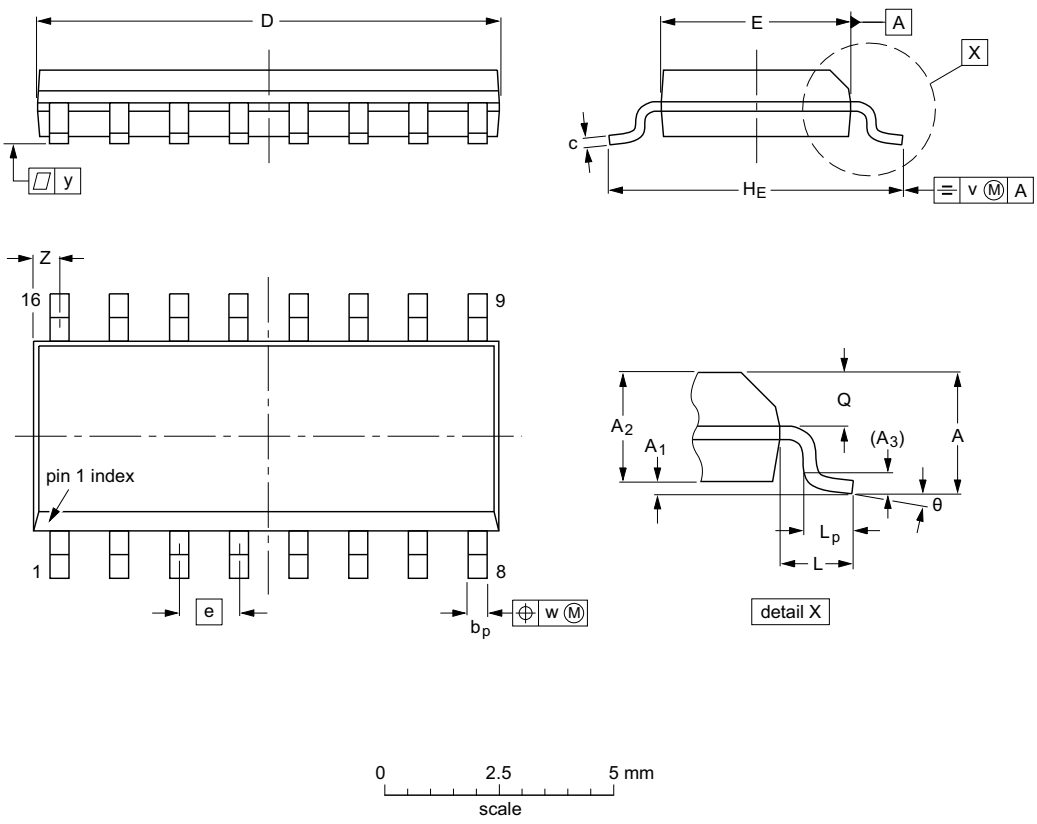
Fig 17. Print layout (viewed from the top)

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15. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

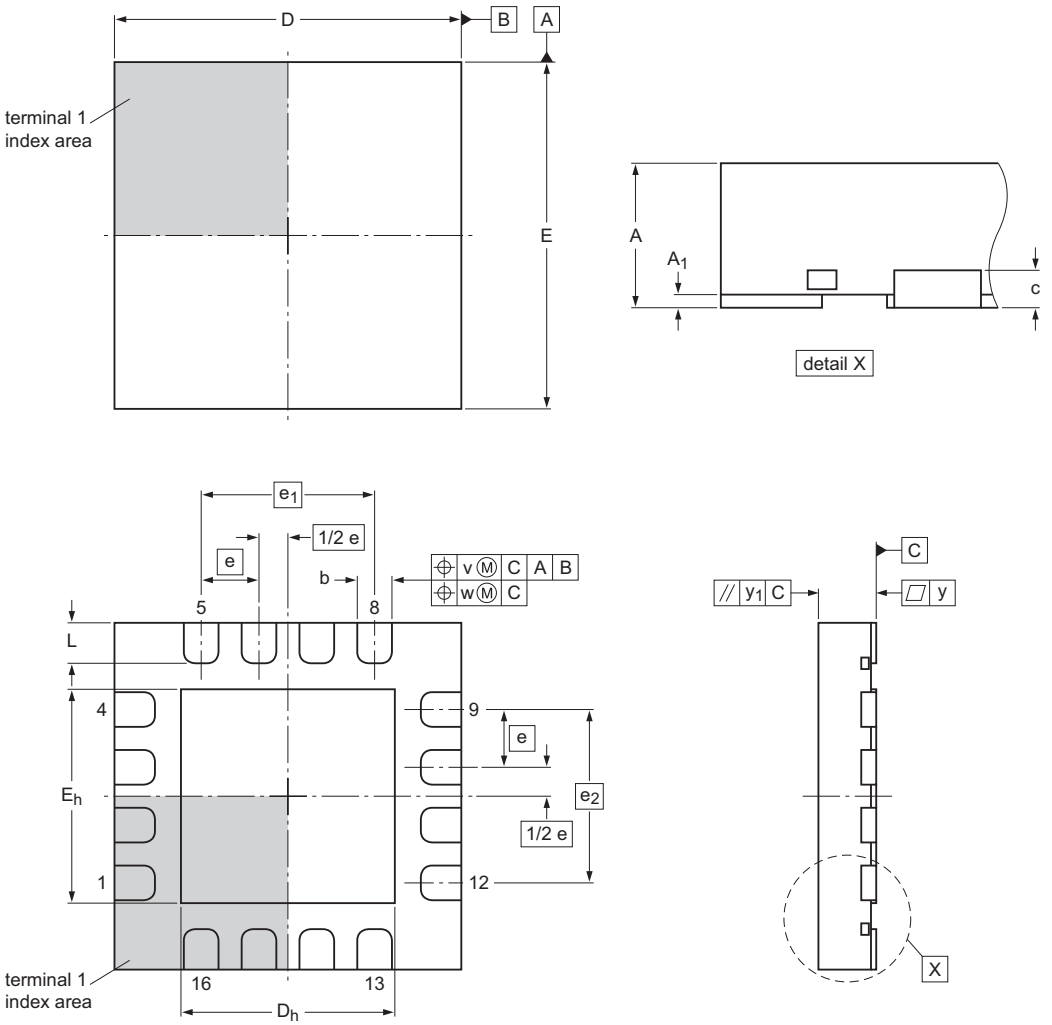
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 18. Package outline SOT109-1 (SO16)

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HXQFN16: plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.5 mm **SOT1039-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	0.5	0.05	0.35	0.127	3.1	1.95	3.1	1.95	0.5	1.5	1.5	0.40	0.1	0.05	0.05	0.1
	nom			0.30		3.0	1.85	3.0	1.85				0.35				
	min		0.00	0.25		2.9	1.75	2.9	1.75				0.30				

sot1039-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1039-2	- - -		- - -			~~10-07-29~~ 11-03-30

Fig 19. Package outline SOT1039-2 (HXQFN16)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

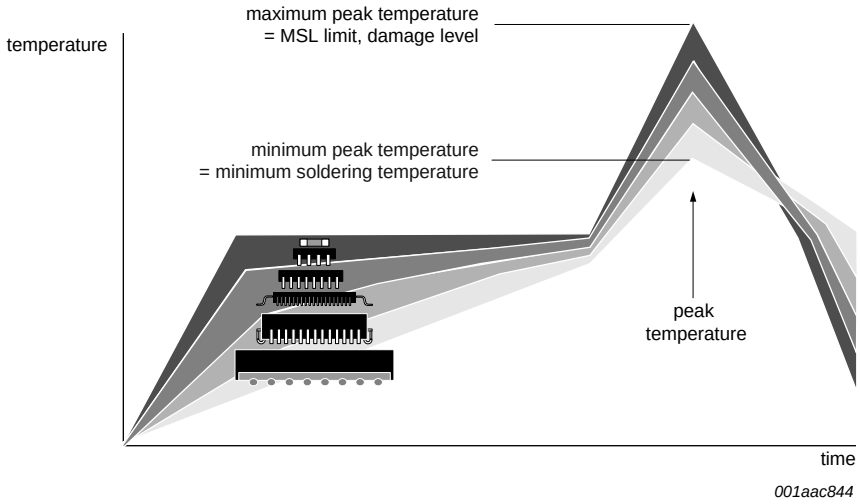
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.

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MSL: Moisture Sensitivity Level

Fig 20. Temperature profiles for large and small components

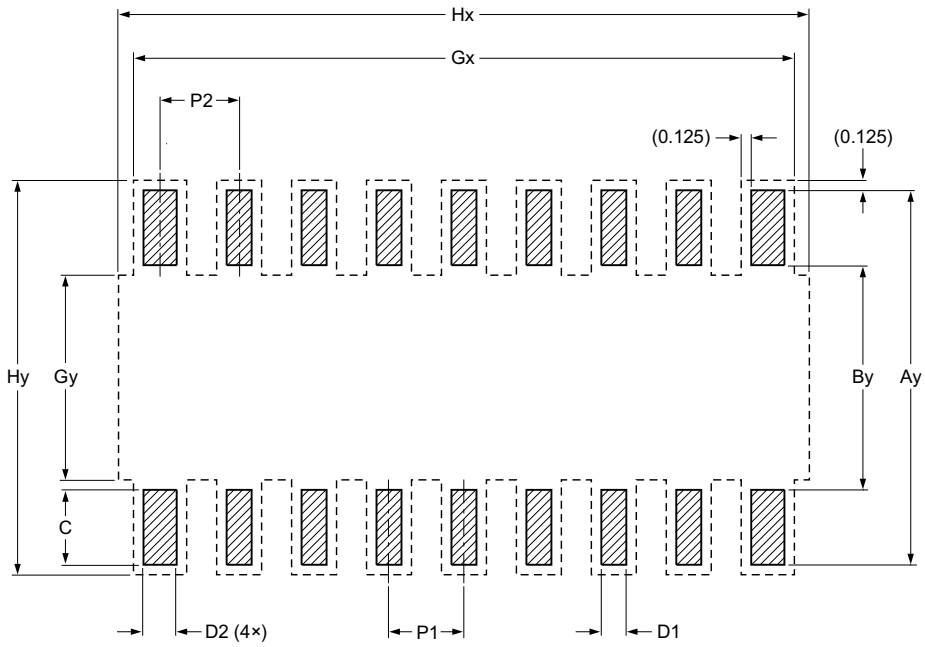
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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17. Soldering: PCB footprints

Footprint information for reflow soldering of SO16 package **SOT109-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
1.270	1.320	7.400	3.900	1.750	0.700	0.800	10.040	5.200	11.900	7.650

Fig 21. PCB footprint for SOT109-1 (SO16); reflow soldering

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Footprint information for reflow soldering of HXQFN16 package **SOT1039-2**

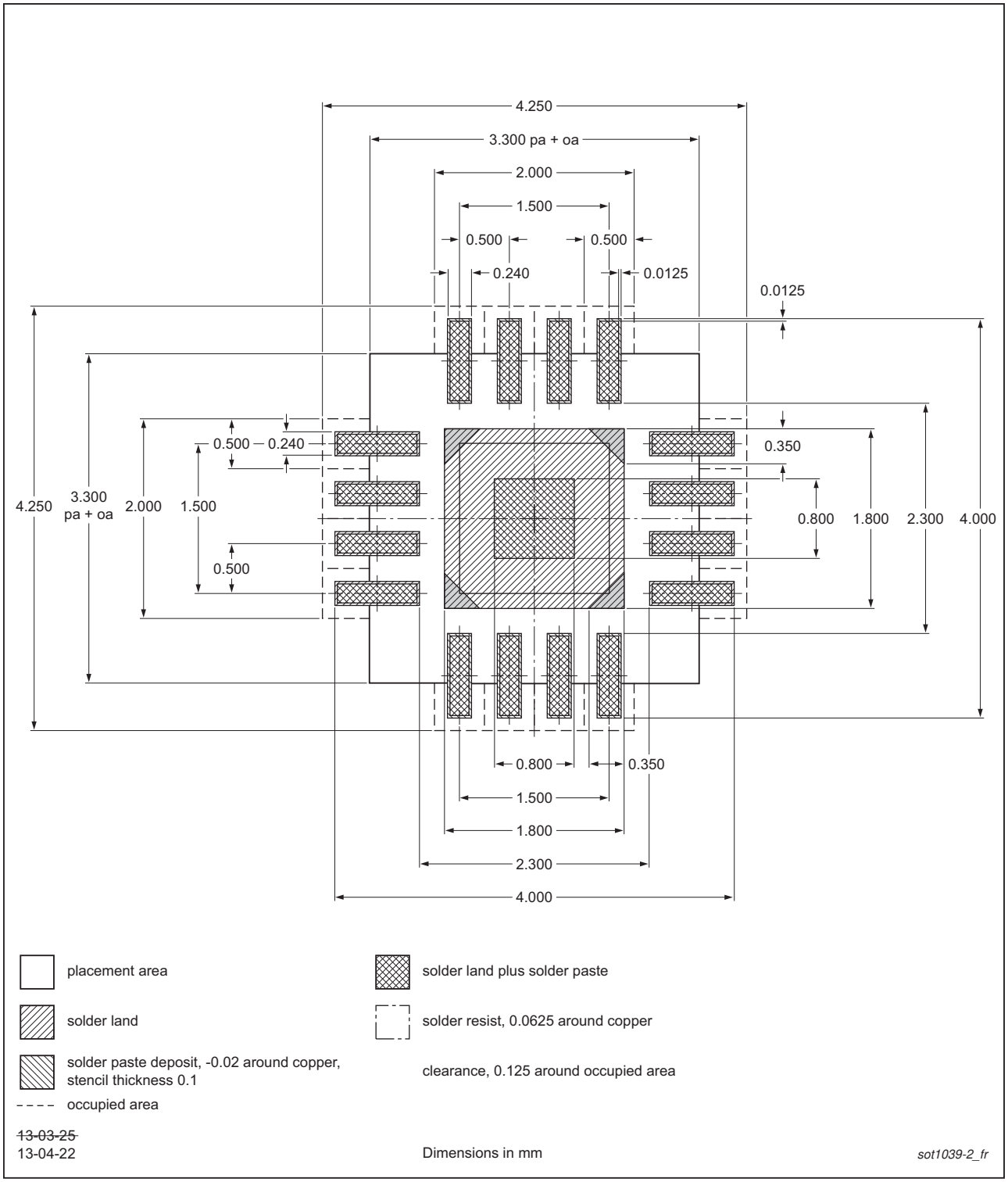


Fig 22. PCB footprint for SOT1039-2 (HXQFN16); reflow soldering

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18. Abbreviations

Table 11. Abbreviations

Acronym	Description
AM	Amplitude Modulation
ASK	Amplitude Shift Keying
BPF	Band-Pass Filter
FM	Frequency Modulation
FSK	Frequency Shift Keying
IF	Intermediate Frequency
PCB	Printed-Circuit Board
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
SCA	Subsidiary Communications Authorization
SINAD	Signal-to-Noise-And-Distortion ratio

19. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA604A v.4.3	20160713	Product data sheet	-	SA604A v.4.2
Modifications:	• Table 2 “Ordering options”: Changed orderable part number from SA604AD/02,118 to SA604AD/02J. • Table 7 “Dynamic characteristics”, $V_{o(RSSI)}$: removed SA604AD/01 from −118 dBm and −18 dBm; added SA604AHR to IF level = −68 dBm for 1.9 V min.			
SA604A v.4.2	20160513	Product data sheet	-	SA604A v.4.1
Modifications:	• Added SA604AD/02 • Table 7 “Dynamic characteristics”, $V_{o(RSSI)}$: added row for SA604AD/02; changed “RF” to “IF”; updated Table note 1. • Deleted Table 8 “SA604 versus SA604A RSSI output voltage”.			
SA604A v.4.1	20150330	Product data sheet	-	SA604A v.4
Modifications:	• Table 2, SA604AHR: Changed orderable part number from “SA604AHRX” to “SA604AHRZ”; corrected packing method from “Q1/T1” to “Q2/T3”.			
SA604A v.4	20150220	Product data sheet	-	SA604A v.3
SA604A v.3	20140418	Product data sheet	-	SA604A v.2
SA604A v.2	19971107	Product specification	ECN 853-1431 18663	SA604A v.1
SA604A v.1	19941215	Product specification	-	-

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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 13 July 2016
Document identifier: SA604A