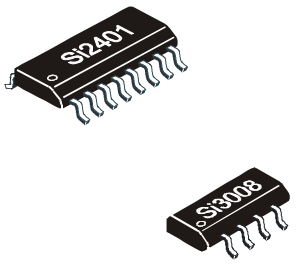
Si2401/Si3008

V.22BIS ISOMODEM® WITH LOW-COST DAA

Features

- Data modem formats
  - 2400 bps: V.22bis
  - 1200 bps: V.22, V.23, Bell 212A
  - 300 bps: V.21, Bell 103
  - Fast connect and V.23 reversing
  - SIA and other security protocols
- 27 MHz CLKIN support
- Caller ID detection and decode
- UART with flow control
- Integrated DAA
  - Over 6000 V capacitive isolation
  - Parallel phone detection
  - Compliant with FCC, China, JATE, and 31 other PTTs
  - Line-in-use detection
- AT command set support
- Call progress support
- 3.3 V Power
- Lead-free and RoHS-compliant packages



Ordering Information

See page 66.

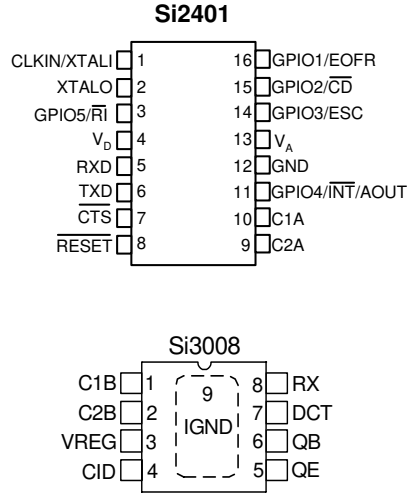
Applications

- Set-top boxes
- Point-of-sale
- ATM terminals
- Security systems
- Medical monitoring
- Power meters

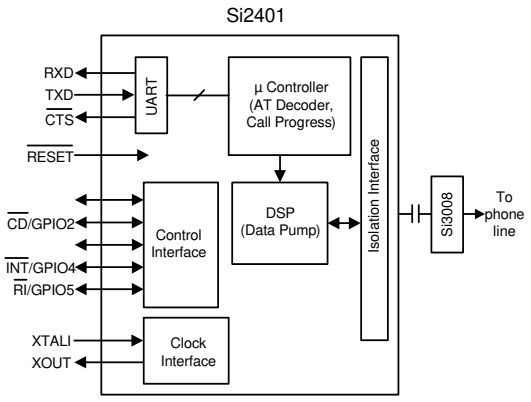
Description

The Si2401 ISOmodem® is a complete, two-chip, 2400 bps modem integrating Silicon Laboratories' fourth-generation direct access arrangement (DAA), which provides a globally-programmable telephone line interface with an unprecedented level of integration. Available in two small packages, this compact solution eliminates the need for a separate DSP data pump, modem controller, codec, isolation transformer, relay, opto-isolators, and 2–4 wire hybrid. The Si2401 provides conventional data formats at connect rates of up to 2400 bps with full-duplex operation over the Public Switched Telephone Network (PSTN). This device is ideal for embedded modem applications due to its small size, minimal external component count, and low power consumption.

Pin Assignments



Functional Block Diagram



U.S. Patent #5,870,046
U.S. Patent #6,061,009
Other patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F-Grade	0	25	70	°C
Si2401 Supply Voltage, Digital[3]	V_D		3.0	3.3	3.6	V

Notes:
1. The Si2401 specifications are guaranteed when the typical application circuit (including component tolerance) and Si2401 and Si3008 are used. See "2. Typical Application Schematic" on page 9.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The digital supply, V_D, operates from 3.0 to 3.6 V. The Si2401 interface supports 5 V logic (CLKIN/XTALI supports 3.3 V logic only).

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA	9	—	—	V
On-Hook Leakage Current	I_{LK}	V_{TR} = –100 V	—	—	12	µA
Operating Loop Current	I_{LP}		15	—	120	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}		10	15	35	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to be undetected below the minimum. The ring signal is guaranteed to be detected above the maximum.

Table 3. DC Characteristics*

(V_D = 3.0 to 3.6 V, T_A = 0 to 70°C for F-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 1 mA	—	—	0.35	V
Low Level Output Voltage, GPIO1–4	V_{OL}	I_O = 10 mA	—	—	0.6	V
Input Leakage Current	I_L		–10	—	10	µA
Pullup Resistance Pins 5,7,11,14	R_{PU}		50	100	200	kΩ
Power Supply Current, Digital	I_D	V_D pin	—	10	15	mA
Power Supply Current, DSP Powerdown	I_D	SEB[3] = 1	—	8	12	mA
Power Supply Current, Wake-On-Ring	I_D	ATZ	—	7	10	mA
Power Supply Current, Total Powerdown	I_D	SF1[5] =1, SF1[6] =1	—	100	—	µA

***Note:** Measurements are taken with inputs at rails and no loads on outputs.

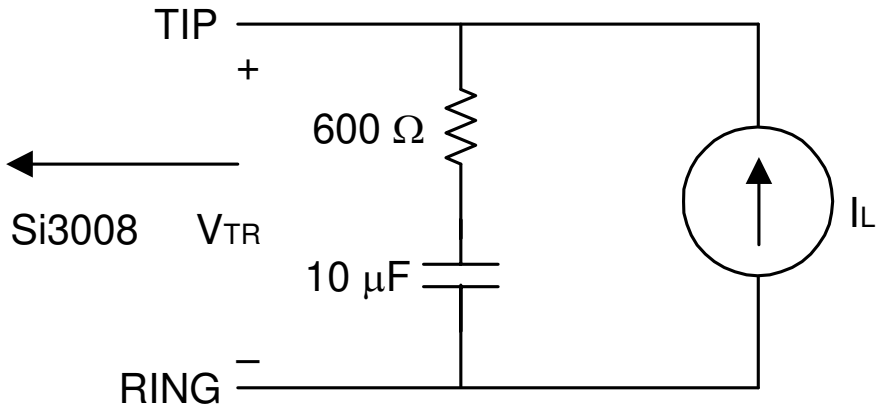


Figure 1. Test Circuit for Loop Characteristics

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for K-Grade, Fs = 8 kHz)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		—	8	—	kHz
Clock Input Frequency	F_{XTL}	default	—	4.9152	—	MHz
Clock Input Frequency	F_{XTL}	≤10 kΩ resistor between pin 11 and GND	—	27	—	MHz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}	–1 dBm	—	0.98	—	V_{PEAK}
Receive Full Scale Level[1,2]	V_{FS}	–1 dBm	—	0.98	—	V_{PEAK}
Dynamic Range[3,4,5]	DR	I_L = 100 mA	—	80	—	dB
Dynamic Range[3,4,5]	DR	I_L = 20 mA	—	80	—	dB
Transmit Total Harmonic Distortion[5,6]	THD	I_L = 20 mA	—	75	—	dB
Dynamic Range (Caller ID Mode)[7]	DR_{CID}	VIN = 1 kHz, –13 dBm	—	50	—	dB

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
2. Receive full-scale level produces –0.9 dBFS.
3. DR = 20 x log (rms V_{FS}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise, excluding harmonics). V_{FS} is the –1 dBm full-scale level.
4. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
5. V_{IN} = 1 kHz, –3 dBFS
6. THD = 20 x log (rms distortion / rms signal).
7. DR_{CID} = 20 x log (rms V_{CID}/rms V_{IN})+ 20 x log (rms V_{IN}/rms noise). V_{CID} is the 6 V full-scale level.

Table 5. Absolute Maximum Ratings

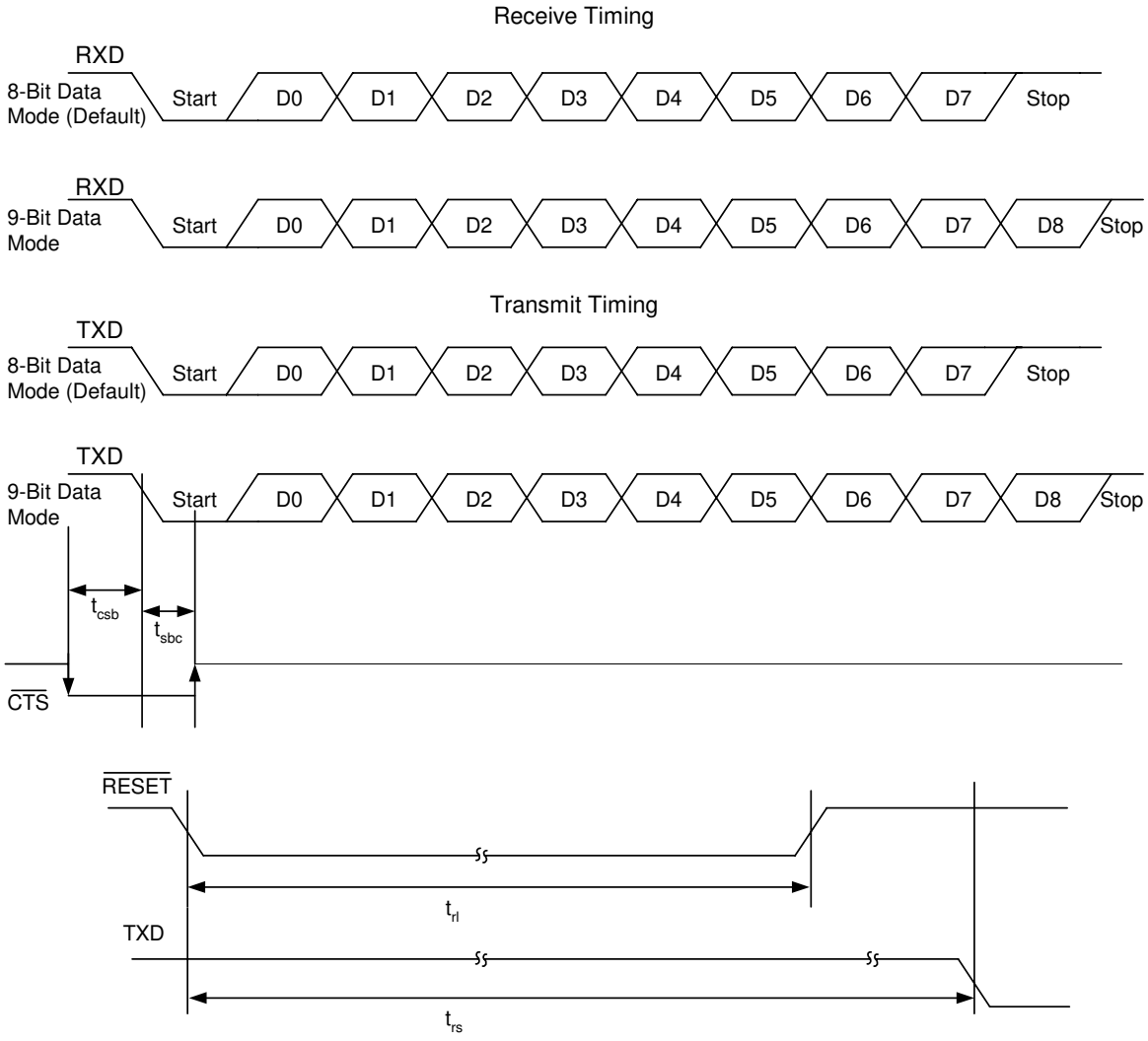
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	4.1	V
Input Current, Si2401 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to 5.3	V
CLKIN/XTALI Input Voltage	V_{XIND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–10 to 100	°C
Storage Temperature Range	T_{STG}	–40 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Switching Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F-Grade)

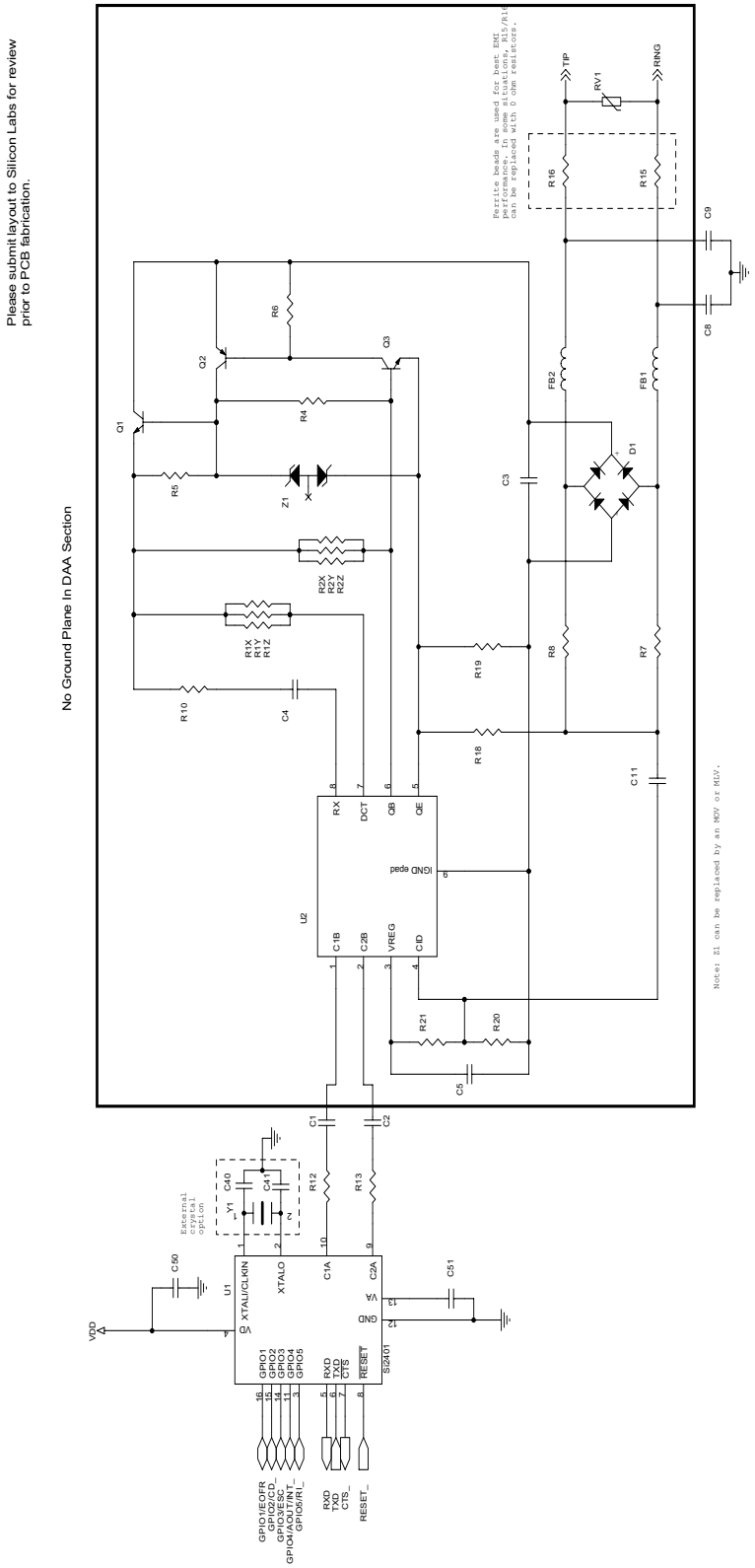
Parameter	Symbol	Min	Typ	Max	Unit
Baud Rate Accuracy		–1	—	1	%
$\overline{CTS}$ ↓ Active to Start Bit↓	t_{csb}	10	—	—	ns
$\overline{RESET}$ Pulse Width	t_{rl}	1	—	—	ms
$\overline{RESET}$ ↑ to TXD ↓	t_{rs}	3	—	—	ms
Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = 2.0 V, V_{IL} = 0.8 V					



Note: Baud rates (programmed through register SE0) are as follows: 300,1200, 2400, 9600, 19200, 38400, 115200, and 307200 Hz.

Figure 2. Asynchronous UART Serial Interface Timing Diagram

2. Typical Application Schematic



3. Bill of Materials: Si2401/08 Chipset

Component	Value	Supplier(s)
C1, C2	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 25 V, X7R, ±20%	Venkel, SMEC
C5, C50	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C11[1]	330 pF, 50 V, X7R, ±20%	Venkel, SMEC
C40, C41[2]	33 pF, 16 V, NPO, ±5%	Venkel, SMEC
C51	0.22 µF, 16 V, X7R, ±20%	Venkel, SMEC
D1, D2[3]	Dual Diode, 225 mA, 300 V, CMPD2004S	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM18AG601SN1B	Murata
Q1, Q3	NPN, 300 V, MMBTA42	OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Protek, ST Micro
R1[4]	205 Ω, 1 W, ±1%	Venkel, SMEC, Panasonic
R2[5]	243 Ω, 1 W, ±1%	Venkel, SMEC, Panasonic
R4	3.9 kΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R7, R8[6]	10 MΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R10	1 kΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R12, R13	56 Ω, 1/16 W, ±1%	Venkel, SMEC, Panasonic
R15, R16[7]	0 Ω, 1/16 W	Venkel, SMEC, Panasonic
R18	1.5 MΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R19	180 kΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R20, R21[1]	3 MΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
U1	Si2401	Silicon Labs
U2	Si3008	Silicon Labs
Y1[2,8]	4.9152 MHz, 20 pF, 100 ppm, 150 Ω ESR	ECS Inc., Siward
Z1[9]	Dual Zener Diode, 20 V, 1/4 W	Vishay

Notes:

1. In applications that do not require caller ID, C11, R20, and R21 can be removed.
2. In STB applications, C40, C41, and Y1 can be removed by using the 27 MHz clock input feature.
3. Several diode bridge configurations are acceptable. For example, a single DF04S or four 1N4004 diodes may be used.
4. Three parallel 619 Ω, 1/4 W, resistors may be used instead of R1.
5. Three parallel 732 Ω, 1/4 W, resistors may be used instead of R2.
6. The package size on R7 and R8 must be at least 0805.
7. Murata BLM18AG601SN1 may be substituted for R15–R16 (0 Ω) to decrease emissions.
8. To ensure compliance with ITU specifications, frequency tolerance must be less than 100 ppm including initial accuracy, 5-year aging, 0 to 70 °C, and capacitive loading. 50 ppm initial accuracy crystals typically satisfy this requirement.
9. Two series Zener diodes may be used instead of Z1.

4. Functional Description

The Si2401 ISOmodem utilizing the Si3008 line-side device is a complete embedded modem chipset with integrated direct access arrangement (DAA). Available in two small packages, this solution includes a DSP data pump, modem controller, on-chip RAM and ROM, codec, DAA, analog output, and 27 MHz clock input.

The modem accepts simple modem AT commands and provides connect rates up to 2400 bps full-duplex over the Public Switched Telephone Network (PSTN) with V.42 hardware support through HDLC framing. To minimize handshake times, the Si2401 can implement a V.22-based fast connect. The modem also supports the V.23 reversing protocol and standard alarm formats including SIA.

This device is ideal for embedded modem applications due to its flexibility, small footprint, and minimal external component count. The Si2401 solution integrates a silicon DAA using Silicon Laboratories' proprietary fourth-generation DAA technology. This highly-integrated DAA can be programmed using the Si3008 to meet international requirements and is compliant with FCC, JATE, and other country-specific PTT specifications as shown in Table 7.

The Si2401 is designed for rapid assimilation into existing modem applications. The device interfaces directly through a UART to a microcontroller. The Si2401URT-EVB evaluation board connects directly to a standard RS-232 or USB interface. This allows for evaluation of the modem immediately upon powerup via HyperTerminal or any standard terminal software.

In addition, the Si2401 has been designed to meet the most stringent worldwide requirements for out-of-band energy, billing-tone immunity, high-voltage surges, and safety requirements.

Table 7. Country-Specific PTT Specifications

Country	
Argentina	Kyrgyzstan
Armenia	Macao
Bahamas	Mexico
Bangladesh	Moldova
Belarus	New Zealand[2]
Bermuda	Paraguay
Brunei	Peru
Canada	Puerto Rico
Caribbean	Russia
Chile	Saudi Arabia
China	Singapore
Colombia	South Korea[3]
Costa Rica	Sri Lanka
Dominican Republic	Taiwan
Ecuador	Thailand
El Salvador	Tunisia
Georgia	UAE
Guam	Ukraine
Hong Kong	Uruguay
India	Uzbekistan
Indonesia	USA
Japan[1]	Venezuela
Kazakhstan	Vietnam
Kuwait	Yemen

Notes:

1. DCR exceeds 300 Ω; disclaimer required in product documentation.
2. 600 Ω ac termination used; disclaimer required in product documentation.
3. Additional components required to pass ringer impedance specifications.

Table 8. Selectable Configurations

Configuration	Modulation	Carrier Frequency (Hz)	Data Rate (bps)	Standard Compliance
V.21	FSK	1080/1750	300	Full
V.22*	DPSK	1200/2400	1200	Full
V.22bis*	QAM	1200/2400	2400	No retrain
V.23	FSK	1300/2100	1200/75	Full; plus reversing (Europe)
V.23		1300/1700	600/75	
Bell 103	FSK	1170/2125	300	Full
Bell 212A	DPSK	1200/2400	1200	Full
Security	DTMF	—	40	Full
SIA—Pulse	Pulse	—	Low	Full
SIA Format	FSK	1170/2125	300 half-duplex	300 bps only

***Note:** The Si2401 only adjusts its DCE rate from 2400 bps to 1200 bps if it is connecting to a V.22-only (1200 bps only) modem. Since the V.22bis specification does not outline a fallback procedure, the host should implement a fallback mechanism consisting of hanging up and connecting at a lower baud rate. Retraining to accommodate changes in line conditions that occur during a call must be implemented by terminating the call and redialing.

4.1. Serial Interface

The Si2401 has a universal asynchronous receiver/transmitter (UART) serial interface compatible with standard microcontroller serial interfaces. After powerup or reset, the speed of the serial (Data Terminal Equipment—DTE) interface is set by default to 2400 bps with the 8-bit, no parity, and one-stop bit (8N1) format described below.

The serial interface DTE rate can be modified by writing SE0[2:0] (SD) with the value corresponding to the desired DTE rate. (See Table 9.) This is accomplished with the command, ATSE0=xx, where xx is the hexadecimal value of the SE0 register.

Table 9. DTE Rates

DTE Rate (bps)	SE0[2:0] (SD)
300	000
1200	001
2400	010
9600	011
19200	100
38400	101
115200	110
307200	111

Immediately after the ATSE0=xx string is sent, the host UART must be reprogrammed to the new DTE rate in order to communicate with the Si2401.

The carriage return character following the ATSE0=xx string must be sent at the new DTE rate to observe the “O” response code. See Table 12 on page 20 for the response code summary.

4.2. Configurations and Data Rates

The Si2401 can be configured to any of the Bell and CCITT operation modes listed in Table 10. When configured for V.22bis, the modem connects at 1200 bps if the far end modem is configured for V.22. This device also supports SIA and other protocols for the security industry. Table 8 provides the modulation method, carrier frequencies, data rate, baud rate, and notes on standard compliance for each modem configuration of the Si2401. Table 10 shows example register settings (S07) for some of the modem configurations.

Table 10. Modem Configuration Examples (S07[7] (HDEN) = 0, S07[6] (BD) = 0)

Modem Protocol	Register S07 Values
V.22bis	0x06
V.22	0x02
V.21	0x03
Bell 212A	0x00
Bell 103	0x01
V.23 (1200 tx, 75 rx)	0x14
V.23 (75 tx, 1200 rx)	0x24
V.23 (600 tx, 75 rx)	0x10
V.23 (75 tx, 600 rx)	0x20

As shown in Figure 3, 8-bit and 9-bit data modes refer to the DTE format over the UART. Line data formats are configured through registers S07 (MF1) and S15 (MLC). If the number of bits specified by the format differs from the number of bits specified by the DCE data communications equipment or line (DTE) format, the MSBs are either dropped or bit-stuffed, as appropriate. For example, if the DTE format is 9 data bits (9N1) and the line data format is 8 data bits (8N1), the MSB from the DTE is dropped as the 9-bit word is passed from the DTE side to the DCE (line) side. In this case, the dropped ninth bit can then be used as an escape mechanism. However, if the DTE format is 8N1 and the line data format is 9N1, an MSB equal to 0 is added to the 8-bit word as it is passed from the DTE side to the DCE side.

The Si2401 UART does not continuously check for stop bits on the incoming digital data. Therefore, if the TXD pin is not high, the RXD pin may echo meaningless characters to the host UART. This requires the host UART to flush its receiver FIFO upon initialization.

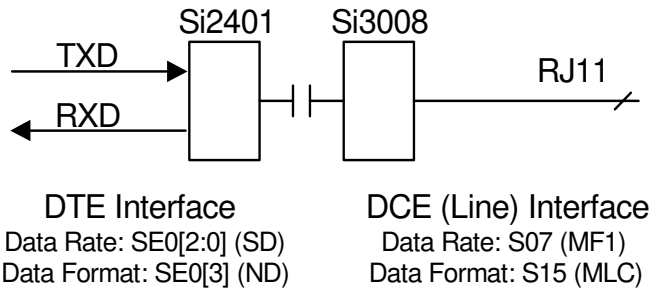


Figure 3. Link and Line Data Formats

4.2.1. Command/Data Mode

Upon reset, the modem is in command mode and accepts AT-style commands. An outgoing modem call can be made using the “ATDT#” (tone dial) or “ATDP#” (pulse dial) command after the device is configured. If the handshake is successful, the modem responds with the “c”, “d”, or “v” string and enters data mode. (The byte following the “c”, “d”, or “v” is the first data byte.) At this point, AT-style commands are not accepted. There are three methods that may be used to return the Si2401 to command mode:

- Use the ESC pin—To program the GPIO3 pin to function as an ESCAPE input, set GPIO3 SE2[5:4] = 11. In this setting, a positive edge detected on this pin returns the modem to command mode. The “ATO” string can be used to reenter data mode.
- Use 9-bit data mode—If 9-bit data format with escape is programmed, a 1 detected on bit 9 returns the modem to command mode. (See Figure 2 on page 8.) This is enabled by setting SE0[3] (ND) = 1 and S15[0] (NBE) = 1. The ATO string can be used to reenter data mode. Ninth bit escape does not work in the security modes.
- Use “+++”—The escape sequence is a sequence of three escape characters that are set in S-register S0F (“+” characters by default). If the ISOmodem® chipset detects the “+++” sequence and detects no activity on the UART before or after the “+++” sequence for a time period set by S-register S10, it returns to command mode. To disable this escape sequence, set S-register S10=FF. To remove the time-dependent behavior, set S-register S10=00.

Whether using an escape method or not, when the carrier is lost, the modem automatically returns to command mode and reports “N”.

4.2.2. 8-Bit Data Mode (8N1)

8-bit data mode is the default mode after powerup or reset and is set by SE0[3] (ND) = 0_b. It is asynchronous, full duplex, and uses a total of 10 bits including a start bit (logic 0), eight data bits, and a stop bit (logic 1). Data received from the remote modem is transferred from the Si2401 to the host on the RXD pin. Data transfer to the host begins when the Si2401 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2401 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the remote modem is shifted to the Si2401 on TXD beginning with a start bit, LSB first at the DTE rate determined by the SE0[2:0] setting and terminates with a stop bit.

After the middle of the stop bit time, the Si2401 begins looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

4.2.3. 9-Bit Data Mode (9N1)

The 9-bit data mode is set by SE0[3] (ND) = 1. It is asynchronous, full duplex, and uses a total of 11 bits including a start bit (logic 0), 9 data bits, and a stop bit (logic 1). Data received from the line (remote modem) is transferred from the Si2401 to the host on the RXD pin. Data transfer to the host begins when the Si2401 asserts a logic 0 start bit on RXD. Data is shifted out of the Si2401 LSB first at the DTE rate determined by the SE0[2:0] (SD) setting and terminates with a stop bit. Data from the host for transmission to the line (remote modem) is shifted to the Si2401 on TXD beginning with a start bit (LSB first at the DTE rate determined by the S-Register SE0[2:0] (SD) setting) and terminates with a stop bit. After the middle of the stop bit time, the Si2401 begins looking for a logic 1 to logic 0 transition signaling the start of the next character on TXD to be sent to the line (remote modem).

The ninth data bit may be used to indicate an escape by setting S15[0] (NBE) = 1. In this mode, the ninth data bit is normally set to 0 when the modem is online. When the ninth data bit is set to 1, the modem goes offline into command mode, and the next frame is interpreted as an AT command. Data mode can be reentered using the ATO command.

4.2.4. Flow Control

No flow control is needed if the DTE rate and DCE rate are the same. If the serial link (DTE) data rate is set higher than the line (DCE) rate of the modem, flow control is required to prevent loss of data to the transmitter.

To control data flow, the clear-to-send (CTS) pin is used. When CTS is asserted, the Si2401 is ready to accept a character. While CTS is negated, no data should be sent to the Si2401 on TXD. To simplify flow control, the Si2401 has an integrated ten character transmit FIFO and allows for two different CTS reporting methods. By default, the CTS pin is negated as soon as a start bit is detected on the TXD pin and remains negated until the modem is ready to accept another character (see Figure 2 on page 8.) By setting SFC7[7]=1 (CTSM), CTS is negated when the FIFO is 70% full and is reasserted when the FIFO is 30% full.

4.3. Low Power Modes

The Si2401 has three low-power modes:

- DSP Powerdown. The DSP processor can be powered down by setting register SEB[3] (PDDE) = 1.
  In this mode, the serial interface still functions, and the modem detects ringing and intrusion. However, no modem modes or tone detection features function.
- Wake-Up-On-Ring. By issuing the ATZ command, the Si2401 goes into a low-power mode where both the microcontroller and DSP are powered down. Only an incoming ring, a low TXD signal, or a total reset will power up the chip again. Return from wake-on-ring triggers the $\overline{INT}$ pin if S09[6] (WOR) = 1 (WOR = 0_b by default).
- Total Powerdown. Setting SF1[5] = 1 and SF1[6] = 1 places the Si2401 into a total powerdown mode. All logic is powered down including the crystal oscillator and clock-out pin. Only a hardware reset can restart the Si2401.

4.4. Parallel Phone Detection

The ISOmodem® chipset is able to detect when another telephone, modem, or other device is using the phone line. This allows the host to avoid interrupting another phone call when the phone line is already in use and to intelligently handle an interruption when the ISOmodem chipset is using the phone line.

4.4.1. On-Hook Intrusion Detection

When the ISOmodem chipset is sharing the telephone line with other devices, it is important that it not interrupt a call in progress. To detect when another device is using the shared telephone line, the host can use the ISOmodem chipset to monitor the TIP-RING dc voltage with the LVS[7:0] bits (SDB). The LVS[7:0] bits have a resolution of 1 V per bit with an accuracy of approximately ±10%. Bits 0 through 6 of this 8-bit signed 2s complement number indicate the value of the line voltage, and the sign bit (bit 7) indicates the polarity of TIP and RING.

When all devices on a particular telephone line are on-hook, there is no loop current flowing through TIP and RING. Therefore, the voltage across TIP and RING is at a maximum. (On most telephone lines, this on-hook voltage is a minimum of 40 V.) Once a device goes off-hook, current flows through TIP and RING on that device, and the TIP-RING voltage drops appreciably. (On most telephone lines, this off-hook voltage is a maximum of 20 V.)

If the host checks the TIP-RING voltage via LVS before causing the ISOmodem chipset to dial out or go off-hook, the host can determine if another device is using the telephone line. One way to do this is to verify that the voltage represented in LVS is above some fixed threshold, such as 30 V.

4.4.2. Off-Hook Intrusion Detection

After it is determined that it is safe to use the phone line without interrupting a call, the host can instruct the ISOmodem chipset to begin a call or go off-hook. However, once the call has begun and the ISOmodem chipset is in data mode, the serial port is used for modem data, making it difficult for the host to monitor registers. Therefore, when the ISOmodem chipset is off-hook, an algorithm is implemented to automatically monitor the TIP-RING loop current via the LCS register (SF3). Because the TIP-RING voltage drops significantly when off-hook, TIP-RING current is a better indicator of another device using the phone line. The LCS[7:0] bits have a resolution of 1.1 mA per bit. An LCS register value of 0x00 indicates that less than the required loop current is present, and a value of 0xFF indicates excessive current draw. The user can read these bits directly through the LCS register. Upon detecting an intrusion, an "i" result code is sent to the host if it is in the call negotiation stage or command mode. Otherwise, the modem can be programmed to generate an interrupt to notify the host of the intrusion.

The off-hook intrusion algorithm monitors the value of LCS (SF3) at a sample rate determined by the DGSR (SDF, bits 6:0) register (40 ms units). The algorithm compares each LCS sample to the reference value in the ACL register (S12). If LCS is lower than ACL by an amount greater than DCL (S11, bits 4:0), the algorithm waits for another LCS sample, and if the next LCS sample is also lower than ACL by an amount greater than DCL, an interrupt occurs. This helps the ISOmodem chipset avoid a false parallel phone detection (PPD) interrupt due to glitches on the phone line. The ACL is continually updated with the value of LCS as outlined below. The algorithm can be outlined as follows:

If LCS(t) = LCS(t – 40 ms x DGSR)
and
LCS(t) – ACL > DCL

then ACL = LCS(t)

If (ACL – LCS[t – 40 ms x DGSR]) > DCL)
and
(ACL – LCS[t]) > DCL),

an intrusion is sent to the host.

The very first sample of LCS the algorithm uses after going off-hook does not have any previous samples for comparison. If LCS was measured during a previous call, this value of LCS may be used as an initial reference. ACL may be written by the host with this known value of LCS. If ACL is non-zero, the ISOmodem chipset uses ACL as the first valid LCS sample in the off-hook intrusion algorithm. If ACL is 0 (default after reset), the ISOmodem chipset ignores the register and does not begin operating the algorithm until two LCS samples have been received. Additionally, immediately after a modem call, ACL is updated automatically with the last valid LCS value before a parallel phone detection (PPD) intrusion or going back on-hook.

The off-hook intrusion algorithm does not begin to operate immediately after going off-hook. This is to avoid triggering an interrupt due to transients resulting from the ISOmodem chipset itself going from on-hook to off-hook. The time that elapses between the ISOmodem chipset going off-hook and the intrusion algorithm starting defaults to one second and may be adjusted via the IST register (S82, bits 7:4). If ACL is written to a non-zero value before going off-hook, a parallel phone intrusion that occurs during this IST interval and sustains through the end of the interval triggers an interrupt.7

The off-hook intrusion algorithm may, additionally, be disabled for a period of time after dialing begins via the IB register (S82, bits 2:1). This avoids triggering an interrupt due to pulse dialing, open-switch intervals, or line transients from central office switching. Intrusion may be disabled from the start of dialing to the end of dialing (IB = DI_b), from the start of dialing to the timeout of the IS (S29, bits 7:0) by setting IB = 10_b(IB = 2) or from the start of dial to carrier detect by setting IB = 11. The off-hook intrusion algorithm is only suspended (not disabled) during this IB interval. Therefore, any intrusion that occurs during the IB interval and sustains through the end of the interval triggers a PPD interrupt.

4.5. Interrupt Detection

The $\overline{INT}$ interrupt pin can be programmed to alert the host of loss-of-carrier, loss-of-phone-line voltage/current, parallel phone detection, and other interrupts listed in the interrupt status mask (S08). After the host receives an interrupt via the $\overline{INT}$ pin, the host should issue the AT:I command. This command causes a read-clear of the WOR, PPD, NLD, RI, OCD, and REV bits of the S09 register and raises (deactivates) the $\overline{INT}$ pin. All the interrupt status bits in register S09 remain high after being set until cleared by the AT:I command.

4.5.1. Loop Current Detection

In addition to monitoring parallel phone intrusion, it is possible to monitor the loss of loop current. This feature can be enabled by setting S08[4] (NLDM) = 1. This feature is disabled by default. If the loop current is too low for normal DAA operation, S09[4] (NLD) is set. During this event, if the NLR result code is enabled by setting S62[1](NLR) = 1, the “l” result code is sent. Once the loop current returns to a normal current state, the “L”

result code is sent. The $\overline{INT}$ pin is also asserted if enabled.

4.5.2. Loss-of-Carrier Detection

The Si2401 has two methods of implementing a loss-of-carrier function. If GPIO4 is programmed as $\overline{INT}$ and if S08[7](CDM) = 1, $\overline{INT}$ asserts in data mode when a loss-of-carrier is detected. The carrier detect function may also be implemented on GPIO2 by setting SE2[3:2] (GPIO2) = 01 and SOC[7](CDE) = 1.

4.5.3. Caller ID Decoding Operation

The Si2401 supports full caller ID detection and decode for US Bellcore and UK standards. To use the caller ID decoding feature, the following configuration is necessary:

1. Set SE0[3] (ND) = 0_b (set modem to 8N1 configuration).
2. Set S0C[6:5] (CIDM) = 01 (set modem to Bellcore type caller ID) or S13[2] (CIDB) = 1 (set modem to UK type caller ID).

4.5.4. Caller ID Monitor/Bellcore Caller ID

The Si2401 continuously monitors the phone line for the caller ID mark signals. This can be useful in systems that require detection of caller ID data before the ring signal, voice mail indicator signals, and Type II caller ID monitor support. To force the Si2401 into caller ID monitor mode, set SOC[6:5] (CIDM) = 11.

Note: CIDM should be disabled before going off-hook.

4.5.5. UK Caller ID Operation

The Si2401 starts searching for the Idle State Tone Alert Signal. When this signal has been detected, the Si2401 transmits an “a” to the host. After the Idle State Tone Alert Signal is completed, the Si2401 applies the wetting pulse for the required 15 ms by quickly going off-hook and on-hook. From this point on, the algorithm is identical to that of Bellcore in that it searches for the channel seizure signal and the marks before echoing an “m” and then reports the decoded caller ID data.

4.6. V.23 Operation/V.23 Reversing

The Si2401 supports full V.23 operation including the V.23 reversing procedure. V.23 operation is enabled by setting S07 (MF1) = $xx10xx00_b$ or $xx01xx00_b$. If S07[5] (V23R) = 1, the Si2401 transmits data at 75 bps and receives data at 600 or 1200 bps. If S07[4] (V23T) = 1, the Si2401 receives data at 75 bps and transmits data at 600 or 1200 bps. S07[2] (BAUD) is the 1200 or 600 bps indicator. BAUD = 1 enables the 1200/600 V.23 channel to run at 1200 bps, while BAUD = 0_b enables 600 bps operation.

When a V.23 connection is successfully established, the modem responds with a “c” character if the connection is made with the modem transmitting at 1200/600 bps and receiving at 75 bps. The modem responds with a “v” character if a V.23 connection is established with the modem transmitting at 75 bps and receiving at 1200/600 bps.

The Si2401 supports the V.23 turnaround procedure. This allows a modem that is transmitting at 75 bps to initiate a “turnaround” procedure so that it can begin transmitting data at 1200/600 bps and receiving data at 75 bps. The modem is defined as being in V.23 master mode if it is transmitting at 75 bps, and it is defined as being in slave mode if the modem is transmitting at 1200/600 bps. The following paragraphs give a detailed description of the V.23 turnaround procedure.

4.6.1. Modem in Master Mode

To perform a direct turnaround once a modem connection is established, the master host goes into online command mode by sending an escape command (Escape pin activation, TIES, or ninth bit escape) to the master modem.

Note: The host can initiate a turnaround only if the Si2401 is the master.

The host then sends the ATRO command to the Si2401 to initiate a V.23 turnaround and return to the online (data) mode.

The Si2401 then changes its carrier frequency (from 390 Hz to 1300 Hz) and waits to detect a 390 Hz carrier for 440 ms. If the modem detects more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it echoes the “c” response character. If the modem does not detect more than 40 ms of a 390 Hz carrier in a time window of 440 ms, it hangs up and echoes the “N” (no carrier) character as a response.

4.6.2. Modem in Slave Mode

Configure GPIO4 as $\overline{INT}$ (SE2[7:6] [GPIO4] = 11). The Si2401 performs a reverse turnaround when it detects a carrier drop longer than 20 ms. The Si2401 then reverses (changes its carrier from 1300 Hz to 390 Hz) and waits to detect a 1300 Hz carrier for 400 ms. If the Si2401 detects more than 40 ms of a 1300 Hz carrier in a time window of 400 ms, it sets the S09[7] bit, and the next character echoed by the Si2401 is a “v”.

If the Si2401 does not detect more than 40 ms of the 1300 Hz carrier in a time window of 400 ms, it reverses again and waits to detect a 390 Hz carrier for 440 ms. Then, if the Si2401 detects more than 40 ms of a 390 Hz carrier in a time window of 220 ms, it sets the S09[7] bit, and the next character echoed by the Si2401 is a “c”.

At this point, if the Si2401 does not detect more than 40 ms of the 390 Hz carrier in a time window of 440 ms, it hangs up, sets the S09[7] bit, and the next character

echoed by the Si2401 is an “N” (no carrier).

Successful completion of a turnaround procedure in master or slave mode automatically updates S07[4] (V23T) and S07[5] (V23R) to indicate the new status of the V.23 connection.

To avoid using the $\overline{INT}$ pin, the host may also be notified of the $\overline{INT}$ condition by using 9-bit data mode. Setting S15[0] (NBE) = 1 and S0C[3] (9BF) = 0_b configures the ninth bit on the Si2401 TXD path to function exactly as the $\overline{INT}$ pin has been described.

4.7. V.42 HDLC Mode

The Si2401 supports V.42 through hardware HDLC framing in all modem data modes. Frame packing and unpacking including opening and closing flag generation and detection, CRC computation and checking, zero insertion and deletion, and modem data transmission and reception are all performed by the Si2401. V.42 error correction and V.42bis data compression must be performed by the host.

The digital link interface in this mode uses the same UART interface (8-bit data and 9-bit data formats) as in the asynchronous modes, and the ninth data bit may be used as an escape by setting S15[0] (NBE) = 1. When using HDLC in 9-bit data mode, if the ninth bit is not used as an escape, it is ignored.

To use the HDLC feature on the Si2401, the host must enable HDLC operation by setting S13[1] (HDEN) = 1. The host may initiate the call or answer the call using either the “ATDT#”, the “ATA” command or the auto-answer mode. (The auto-answer mode is implemented by setting register S00 (NR) to a non-zero value.) When the call is connected, a “c”, “d”, or “v” is echoed to the host controller. The host may now send/receive data across the UART using either the 8-bit or 9-bit data formats with flow control.

At this point, the Si2401 begins framing data into the HDLC format. On the transmit side, if no data is available from the host, the HDLC flag pattern is sent repeatedly. When data is available, the Si2401 computes the CRC code throughout the frame, and the data is sent with the HDLC zero-bit insertion algorithm.

HDLC flow control operates in a manner similar to normal asynchronous flow control across the UART and is shown in Figure 4. To operate flow control (using the $\overline{CTS}$ pin to indicate when the Si2401 is ready to accept a character), a DTE rate higher than the line rate should be selected. The method of transmitting HDLC frames is as follows:

1. After the call is connected, the host should begin sending the frame data to the Si2401 using the $\overline{CTS}$ flow control to ensure data synchronicity.
2. When the frame is complete, the host should simply stop sending data to the Si2401. Since the Si2401 does not yet recognize the end-of-frame, it expects an extra byte and assert $\overline{CTS}$ as shown in Figure 4A. If $\overline{CTS}$ is used to cause a host interrupt, this final interrupt should be ignored by the host.
3. When the Si2401 is ready to send the next byte, if it has not yet received any data from the host, it recognizes this as an end-of-frame, raise $\overline{CTS}$, calculates the final CRC code, transmits the code, and begins transmitting stop flags.
4. After transmitting the first stop flag, the Si2401 lowers $\overline{CTS}$, indicating that it is ready to receive the next frame from the host. At this point, the process repeats as in Step 1.

The method of receiving HDLC frames is as follows:

1. After the call is connected, the Si2401 searches for flag data. Then, once the first non-flag word is detected, the CRC is continuously computed, and the data is sent across the UART (8-bit data or 9-bit data mode) to the host after removing the HDLC zero-bit insertion. The DTE rate of the host must be at least as high as that of data transmission. HDLC mode only works with 8-bit data words; the ninth bit is used only for escape on TXD and end-of-frame received (EOFR) on RXD.
2. When the Si2401 detects the stop flag, it sends the last data word in the frame as well as the two CRC bytes and determines if the CRC checksum matches. Thus, the last two bytes are not frame data but are the CRC bytes, which can be discarded by the host. If the checksum matches, the Si2401 echoes “G” (good). If the checksum does not match, the Si2401 echoes “e” (error). Additionally, if the Si2401 detects an abort (seven or more contiguous ones), it echoes an “A”.
   When the “G”, “e”, or “A” (referred to as a frame result word) is sent, the Si2401 raises the EOFR (end of frame receive) pin (see Figure 4B). The GPIO1 pin must be configured as EOFR by setting SE4[3] (GPE) = 1. In addition to using the EOFR pin to indicate that the byte is a frame result word, if in 9-bit data mode (set S15[0] (NBE) = 1), the ninth bit is raised if the byte is a frame result word. To program this mode, set S0C[3] (9BF) = 1 and SE0[3] (ND) = 1.
3. When the next frame of data is detected, EOFR is lowered, and the process repeats at Step 1.

To summarize, when receiving HDLC frames, the host begins receiving data asynchronously from the Si2401. When each byte is received, the host should check the EOFR pin (or the ninth bit). If the EOFR pin (or the ninth bit) is low, the data is valid frame data. If the EOFR pin (or the ninth bit) is high, the data is a frame result word.

4.8. Fast Connect

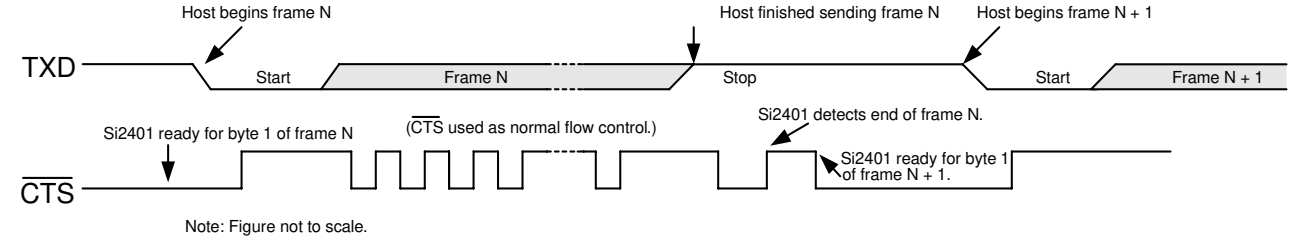
In modem applications that require fast connection times, it is possible to reduce the length of the handshake.

Additional modem handshaking control can be adjusted through the registers shown in Table 11. These registers are most useful if the user has control of both the originating and answering modems.

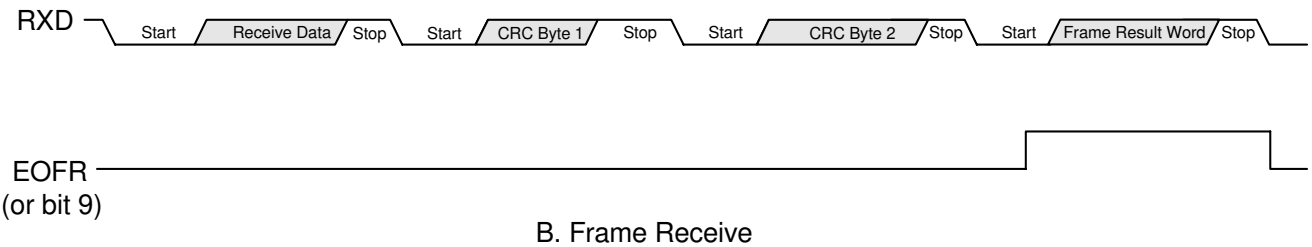
When the fast connect settings are used, there may be unintended data received initially.The host must tolerate these bytes.

4.9. Clock Generation Subsystem

The Si2401 contains an on-chip clock generator. Using a single master clock input, the Si2401 can generate all modem sample rates necessary to support V.22bis, V.22/Bell212A, and V.21/Bell103 standards and a 9.6 kHz rate for audio playback. Either a 27 MHz or 4.9152 MHz clock on XTALI or a 4.9152 MHz crystal across XTALI and XTALO form the master clock for the Si2401. This clock source is sent to an internal phase-locked loop (PLL) that generates all necessary internal system clocks. The PLL has a settling time of ~1 ms. Data on RXD should not be sent to the device prior to settling of the PLL. By default, the Si2401 assumes a 4.9152 MHz clock input. If a 27 MHz clock on XTALI is used, a pulldown resistor $\leq$10 kΩ must be placed between GPIO4 (Si2401, pin 11) and GND.



A. Frame Transmit



B. Frame Receive

Figure 4. HDLC Timing

Table 11. V.22/Bell212 Handshaking Control Registers

Register	Name	Function	Units	Default	Fast Connect
S1E	TATL	Transmit Answer Tone Length	1 s	0x03	00
S1F	ATTD	Answer Tone to Transmit Delay	5/3 ms	0x2D	00
S20	UNL	Unscrambled Ones Length—V.22	5/3 ms	0x5D	00
S21	TSOD	Transmit Scrambled Ones Delay—V.22	53.3 ms	0x09	00
S22	TSOL	Transmit Scrambled Ones Length—V.22	5/3 ms	0xA2	00
S23	VDDL	V.22/22b Data Delay Low	5/3 ms	0xCB	00
S24	VDDH	V.22/22b Data Delay High	(256) 5/3 ms	0x08	00
S34	TASL	Answer Tone Length (only used in S1E [TATL] = 0x00)	5/3 ms	0x5A	F0
S35	RSOL	Receive V.22 Scrambled Ones Length	5/3 ms	0xA2	00

5. AT Command Set

The controller provides several vital functions including AT command parsing, DAA control, connect sequence control, DCE protocol control, intrusion detection, parallel phone off-hook detection, escape control, caller ID control and formatting, ring detect, DTMF control, call progress monitoring, and HDLC framing. The controller also writes to the control registers that configure the modem. Virtually all interaction between the host and the modem is done via the controller. The controller uses AT (ATtention) commands and S-Registers to configure and control the modem.

The modem has two modes of operation: command mode and data mode. The Si2401 is asynchronous in both command mode and data mode. The modem is in command mode at powerup, after a reset, before a connection is made, after a connection is dropped, and during a connection after successfully "Escaping" from the data mode back to the command mode using one of the methods previously described. The following section describes the AT command set available in command mode.

The Si2401 supports a subset of the typical modem AT command set since it is intended for use with a dedicated microcontroller instead of general terminal applications. AT commands begin with the letters AT and are followed directly (no space) by the command. These commands are also case-sensitive. All AT commands *must* be entered in upper case including AT except w##, r#, m#, q#, and z (wakeup-on-ring).

AT commands can be divided into two groups: control commands and configuration commands. Control commands, such as ATD, cause the modem to perform an action (going off-hook and dialing). The value of this type of command is changed at a particular time to perform a particular action. For example, the ATDT1234<CR> command causes the modem to go off hook and dial the number, 1234, via DTMF. This action exists only during a connection attempt. No enduring change in the modem configuration exists after the connection or connection attempt has ended.

Configuration commands change modem characteristics until they are modified or reversed by a subsequent configuration command or the modem is reset. Modem configuration status can be determined with the use of "ATSR?<CR>" Where R is the two-character hexadecimal address of an S-register.

A command line is defined as a string of characters starting with AT and ending with an end-of-line character, <CR> (13 decimal). Command lines may contain several commands one after the other. If there are no characters between AT and <CR>, the modem responds with "O" after the carriage return.

5.1. Command Line Execution

The characters in a command line are executed one-at-a-time. Unexpected command characters are ignored, but unexpected data characters may be interpreted incorrectly.

After the modem has executed a command line, the result code corresponding to the last command executed is returned to the terminal or host. In addition to the "ATH" and "ATZ" commands, the commands that warrant a response (e.g., "ATSR?" or "ATI") must be the last in the string and followed by a <CR>. All other commands may be concatenated on a single line. To echo command line characters, set the Si2401 to Echo mode using the E1 command.

All numeric arguments, including the address and value of an S-register, are in hexidecimal format, and two digits must always be entered.

5.2. <CR> End-Of-Line Character

This character is typed to end a command line. The value of the <CR> character is 13 in decimal, the ASCII carriage return character. When the <CR> character is entered, the modem executes the commands in the command line.

Note: Commands that do not require a response are executed immediately and do not need a <CR>.

Table 12. AT Command Set Summary

Command	Function
A	Answer line immediately with modem
DT#	Tone dial number
DP#	Pulse dial number
E	Local echo on/off
H0	Go on-hook (hang up modem)
H1	Go off-hook
I	Chip revision
:I	Interrupt read and clear
M	Speaker control options
O	Return online
RO	V.23 reverse
S	Read/write S-Registers
w##	Write S-Register in binary
r#	Read S-Register in binary
m#	Monitor S-Register in binary

Table 12. AT Command Set Summary

q#	Read S-Register in binary
V0	Result code with no carriage return
V1	Result code with added carriage returns
Z	Software reset
z	Wakeup on ring

5.3. AT Command Set Description

A Answer

The "A" command makes the modem go off-hook and respond to an incoming call. This command is to be executed after the Si2401 has indicated a ring has occurred. (The Si2401 indicates an incoming ring by echoing an "R".)

This command is aborted if any other character is transmitted to the Si2401 before the answer process is completed.

Auto answer mode is entered by setting S00 (NR) to a non-zero value. NR indicates the number of rings before answering the line.

Upon answering, the modem communicates by whatever protocol has been determined via the modem control registers in S07 (MF1).

If no transmit carrier signal is received from the calling modem within the time specified in S39 (CDT), the modem hangs up and enters the idle state.

D Dial

DT# Tone Dial Number.

DP# Pulse Dial Number.

The D commands make the modem dial a telephone call according to the digits and dial modifiers in the dial string following the command. A maximum of 64 digits is allowed. A DT command performs tone dialing, and a DP command performs pulse dialing.

The ATH1 command can be used to go off-hook without detecting a dial tone or dialing.

The dial string must contain only the digits "0–9", "*", "#", "A", "B", "C", "D", or the modifiers "**;**", "/", or "**,**". Other characters are interpreted incorrectly. The modifier "**,**" causes a two-second delay (added to the spacing value in S04) in dialing. The modifier "/" causes a 125 ms delay (added to the spacing value in S04) in dialing. The modifier "**;**" returns the device to command mode after dialing and must be the last character.

If any character is received by the Si2401 between the ATDT#<CR> (or ATDP#<CR>) command and when the connection is made ("c" or "d" is echoed), the extra character is interpreted as an abort, and the Si2401 returns to command mode ready to accept AT commands. A line feed character immediately following the <CR> is treated as an "extra character" and aborts the call.

If the modem does not have to dial (i.e., "ATDT<CR>" or "ATDP<CR>" with no dial string), the Si2401 assumes the call was manually established and attempts to make a connection.

5.3.1. Automatic Tone/Pulse Dialing

The Si2401 can be configured to attempt DTMF dialing and automatically revert to pulse dialing if it determines that the line is not DTMF-capable. This feature is best explained by the following example:

If it is desired that the telephone number, 12345, be dialed, it is normally accomplished through either the ATDT12345 or the ATDP12345 command. In the force pulse dialing mode of operation, the following string should be issued instead:

ATDT1,p12345

A result code of "t," indicates that the dialing was accomplished using DTMF dialing. If the result code returned is "tt,", this indicates that the dialing was accomplished using pulse dialing.

In the above example, the Si2401 dials the first digit "1" using DTMF dialing. The "," is used to pause in order to ensure that the central office has had time to accept the DTMF digit "1". When the Si2401 processes the "p" command, it attempts to detect a dial tone. If a dial tone is detected, the DTMF digit "1" was not effective, hence, the line does not support DTMF dialing. Conversely, if the dial tone is not detected, the DTMF digit "1" was effective, and the line supports DTMF dialing. The character after the "p" may or may not be dialed depending on whether the DTMF digit "1" was effective or not. If the "1" was effective (DTMF mode), the character after the "p" is skipped. The next DTMF digit to be dialed is "2". Subsequent digits are all DTMF. If the "1" was not effective, the first character after the "p" (the "1") is pulse dialed, and subsequent digits are all pulse dialed.

E Command Mode Echo

Tells the Si2401 whether or not to echo characters sent from the terminal.

EO

Does not echo characters sent from the terminal.

E1

Echoes characters sent from the terminal.

H0 Hangup

Hang up and go into command mode (go offline).

H1 Off-hook

Go off-hook.

I Chip Identification

This command causes the modem to echo the chip revision for the Si2401 device.

A = Revision A

B = Revision B

C = Revision C, etc.

I6

Display the ISOmodem® model number.

"2401" = Si2401.

:I Interrupt Read

This command causes the ISOmodem chipset to report the contents of the interrupt status register (S09). The WOR, PPD, NLD, RI, OCD, and REV bits are also cleared, and the INT is deactivated on this read.

M Speaker On/Off Options

These options are used to control AOUT for use with a call progress monitor speaker.

M0

Speaker always off.

M1

Speaker on until carrier established. The modem sets SF4[3:2] (ARL) = 11 and SF4[1:0] (ATL) = 11 after a connection is established.

M2

Speaker always on.

M3

Speaker on after last digit dialed, off at carrier detect.

O Return to Online Mode

This command returns the modem to the online mode. It is frequently used after an escape sequence to resume communication with the remote modem.

RO Turn-Around

This command initiates a V.23 "direct turnaround" sequence and returns online.

S S Register Control

SR=N

Write an S register. This command writes the value "N" to the S-register specified by "R". "R" is a hexidecimal number, and "N" must also be a hexadecimal number from 00–FF. This command does not wait for a carriage return <CR> before taking effect.

Note: Two digits must always be entered for both "R" and "N".

SR?

Read an S register. This command causes the Si2401 to echo the value of the S-register specified by R in hex format. R must be a hexidecimal number.

Note: Two digits must always be entered for R.

w## Write S Register in Binary

This command writes a register in binary format. The first byte following the "w" is the address in binary format and the second byte is the data in binary format. This is a more rapid method to write registers than the "SR=N" command and is recommended for use by a host microcontroller.

r# Read S Register in Binary

This command reads a register in binary format. The byte following the "r" is the address in binary format. The modem echoes the contents of this register in binary format. This is a more rapid method to read registers than the "SR?" command and is recommended for use by a host microcontroller.

Notes:

1. w## and r# are not required to be on separate lines (i.e., no <CR> between them). Also, the result of an r# is returned immediately without waiting for a <CR> at the end of the AT command line.
2. Once a <CR> is encountered, "AT" is again required to begin the next "AT" command.

m# Monitor S Register in Binary

This command monitors a register in binary format. The byte following the "m" is the address in binary format. The Si2401 constantly transmits the contents of the register at the set baud rate until a new byte is transmitted to the device. The new byte is ignored and viewed as a stop command. The modem result codes should be disabled (as described above in r#) before using this command.

q# Read S Register in Binary

This command is exactly the same as the r# command; however, the response from the Si2401 is formatted as 0x55 followed by the contents of the register in binary. This guarantees that the register contents are always preceded by 0x55 and allows the result codes to remain enabled.

V Result Code Options

V0

Result codes reported according to Table 14.

V1

Result codes reported with an additional carriage return and line feeds (default).

Z Software Reset

The "Z" command initiates a software reset causing all registers, with the exception of E0, which controls the DTE settings, to default to their powerup value.

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The hardware reset pin, $\overline{\text{RESET}}$ (Si2401, pin 8), is used to reset the Si2401 to factory default settings.

z Wakeup on Ring (lower-case z)

The Si2401 enters a low-power mode in which the DSP and microcontroller are powered down. In this mode, only the line-side device (Si3008) and the isolation capacitor communication link are functional. An incoming ring signal or line transient causes the Si2401 to power up and echo an "R". Any character received on the RXD pin also causes the Si2401 to exit the wakeup-on-ring state. Return from wake-on-ring can also be set to trigger the $\overline{\text{INT}}$ pin by setting S08[6] (WORM) = 1.

5.4. Alarm Industry AT Commands

The Si2401 supports a complete set of commands necessary for making connections in security industry systems. The Si2401 is configurable in two modes for these applications. The first mode uses DTMF messaging and is selected with the "!1" command. The second mode uses FSK transmit with a tone acknowledgement and is selected with "!2".

The following are a few general comments about the use of "!" commands. Specific details for each command are given below. The first instance of the "!" must be on the same line as the ATDT or ATDP command. DRT must be set to data mode (SE4[5:4] (DRT) = 0_b) before attempting to send tones after a "!" command. The three data-mode escape sequences ("+++", "escape" pin and "ninth-bit") only function in "!2" mode. However, using the "+++" or "ninth-bit" is not recommended because characters could be sent to and misinterpreted by the remote modem. Only the "escape pin" (Si2401, pin 14) is recommended for use in the "!2" mode. The "!1" mode has a special escape provision described below. The AT commands for Alarm Industry applications are described in Table 13.

Table 13. AT Command Set Extensions for the Alarm Industry

Command	Function
!1	Dial and switch to DTMF security mode
!2	Dial and switch to "SIA Format"
X1	SIA half-duplex mode search
X2	SIA half-duplex return online as transmitter
X3	SIA half-duplex return online as receiver

5.4.1. !1

Dial number and follow the DTMF security protocol.

The format for this command is as follows:

ATDT<phone number>!1<message 1><CR>

K

!<message 2><CR>

K

!<message 3><CR>

K

K

!<message n><CR>

The modem dials the phone number and echoes "r" (ring), "b" (busy), and "c" (connect) as appropriate. "c" echoes only after the Si2401 detects the Handshake Tone. After a 250 ms delay, the modem sends the DTMF tones containing the first message data and listens for a Kissoff Tone. If a Kissoff Tone shorter than or equal to the value stored in S36(KTL) (default = 1 second) is detected, the Si2401 echoes a "K". A "k" is echoed if the length of the Kissoff Tone is longer than the S36(KTL) value. The controller can then send the next message. All messages must be preceded by a "!" and followed by a <CR> and received by the Si2401 within 250 ms after the "K" is echoed. Setting S0C[0] (MCH) = 1 causes a "." to be echoed when the DTMF tone is turned on and a "/" character to be echoed when the DTMF tone is turned off. This helps the host monitor the status of the message being sent. The previous message can be resent if the host responds with a "~" after the Si2401 echoes a "K". Any character other than a "!" or a "~" sent to the modem immediately after the "K" causes the modem to escape to the command mode and remain off-hook. Any character except "!" and "~" sent during the transmission of a message causes the message to be aborted and the modem to return to the command mode.

If the Kissoff Tone is not received within 1.25 seconds, the modem echoes a "^". A "~" from the host causes the last message to be resent. Any character other than a "!" or a "~" sent to the modem immediately after the "^" causes the modem to escape to the command mode and remain off-hook.

5.4.2. !2

Dial the number and follow the "SIA Format" protocol for Alarm System Communications.

The modem dials the phone number and echoes "r" (ring), "b" (busy), and "c" (connect) as appropriate. "c" echoes only after the Si2401 detects the Handshake Tone and the speed synchronization signal is sent. The signaling is at 300 bps, half-duplex FSK. The host can send the first SIA block after the "c" is received. Once

the block is transmitted, the modem can monitor for the acknowledge tone by completing the following sequence:

1. Place the Si2401 in the command mode by pulsing the ESCAPE pin (Si2401 pin 14). The “+++” and “ninth-bit” escape modes operate in the “!2” mode but are not recommended because they can send unwanted characters to the remote modem.
2. Issue the “ATX1” command to turn the modem transmitter off and begin monitoring for the acknowledgment tones.
3. Monitor for a positive (negative) acknowledgment “P” (“N”) after the tone has been detected for at least 400 ms.
4. The modem, still in command mode, can be placed online as a transmitter by issuing the “ATX2” command or as a receiver by issuing the “ATX3” command. If tonal acknowledgement is not used, the host can toggle the ESCAPE pin to place the Si2401 in the command mode and issue an “ATX2” or an “ATX3” command to reverse data direction.

This sequence can be repeated for long messages.

5.5. Modem Result Codes and Call Progress

Table 14 shows the modem result codes that can be used in call progress monitoring. All result codes are a single character to speed up communication and ease host processing.

Table 14. Modem Result Codes

Command	Function
a	British Telecom Caller ID Idle Tone Alert Detected
b	Busy Tone Detected
c	Connect
d	Connect 1200 bps (when programmed as V.22bis modem)
f	Hookswitch Flash or Battery Reversal Detected
H	Modem Automatically Hanging Up in !2, !1
I	Intrusion Completed (parallel phone back on-hook)
i	Intrusion Detected (parallel phone off-hook on the line)
K	Kissoff Tone Detected
k	Contact ID Kissoff Tone too long (!1)
L	Phone Line Detected
l	No Phone Line Detected
m	Caller ID Mark Signal Detected
N	No Carrier Detected
n	No Dial tone (time-out set by CW [S02])
O	Modem OK Response
R	Incoming Ring Signal Detected
r	Ringback Tone Detected
t	Dial Tone
v	Connect 75 bps TX (V.23 originate only)
x	Overcurrent State Detected After an Off-Hook Event
^	Kissoff tone detection required
,	Dialing Complete

5.5.1. Automatic Call Progress Detection

The Si2401 has the ability to detect dial, busy, and ringback tones automatically. The following is a description of the algorithms that have been implemented for these three tones.

- **Dial Tone**. The dial tone detector looks for a dial tone after going off-hook and before dialing is initiated. This can be bypassed by enabling blind dialing (set S07[6] (BD) = 1). After going off-hook, the Si2401 waits the number of seconds in S01 (DW) before searching for the dial tone.
  In order for a dial tone to be detected, it must be present for the length of time programmed in S1C (DTT). Once the dial tone is detected, dialing commences. If a dial tone is not detected within the time programmed in S02 (CW), the Si2401 hangs up and echoes an "n" to the user.
- **Busy/Ringback Tone**. After dialing has completed, the Si2401 monitors for Busy/Ringback and modem answer tones. The busy and ringback tone detectors both use the call progress energy detector. The registers that set the cadence for busy and ringback are listed in Table 15. Si2401 register settings for global cadences for busy and ringback tones are listed in Table 16.

Table 15. Busy and Ringback Cadence Registers

Register	Name	Function	Units
S16	BTON	Busy tone on time	10 ms
S17	BTOF	Busy tone off time	10 ms
S18	BTOD	Busy tone delta time	10 ms
S19	RTON	Ringback tone on time	53.333 ms
S1A	RTOF	Ringback tone off time	53.333 ms
S1B	RTOD	Ringback tone delta time	53.333 ms

5.5.2. Manual Call Progress Detection

Because other call progress tones beyond those described may exist, the Si2401 supports manual call progress. This requires the host to read and write the low-level DSP registers and may require real-time control by the host. Manual call progress may be required for detection of application-specific ringback, dial tone, and busy signals. The section on DSP low-level control should be read before attempting manual call progress detection.

The call progress biquad filters can be programmed to have a custom frequency response and detection level (as described in "6. Low Level DSP Control").

Four dedicated user-defined frequency detectors can be programmed to search for individual tones. The four detectors have center frequencies that can be set by registers UDFD1–4 (see Table 18). SE5[6] [TDET] [SE8 = 0x02] Read Only Definition can be monitored, along with TONE, to detect energy at these user-defined frequencies. The default trip-threshold for UDFD1–4 is –43 dBm but can be modified with the DSP register, UDFSL.

By issuing the "ATDT;" command, the modem goes off-hook and returns to command mode. The user can then put the DSP into call progress monitoring by first setting SE8 = 0x02. Next, set SE5 (DSP2) = 0x00 so no tones are transmitted, and set SE6 (DSP3) to the appropriate code, depending on which types of tones are to be detected.

Table 16. Si2401 Global Ringer and Busy Tone Cadence Settings

Country	RTON	RTOF	RTOD	BTON	BTOF	BTOD
	S19	S1A	S1B	S16	S17	S18
China	0x12	0x4B	0x08	0x23	0x23	0x04
Hong Kong	0x07	0x03	0x01	0x32	0x32	0x05
Hungary	0x17	0x46	0x0F	0x1E	0x1E	0x03
India	0x07	0x03	0x01	0x4B	0x4B	0x08
Japan, Korea	0x12	0x25	0x04	0x32	0x32	0x05
Malaysia	0x07	0x03	0x01	0x23	0x41	0x07
Mexico	0x12	0x4B	0x08	0x19	0x19	0x03
Singapore	0x07	0x03	0x01	0x4B	0x4B	0x08
Taiwan	0x12	0x25	0x04	0x32	0x32	0x05
U.S., Canada (default)	0x25	0x4B	0x08	0x32	0x32	0x05

At this point, users may program their own algorithm to monitor the detected tones. If the host wishes to dial, it should do so by blind dialing, setting the dial timeout S01 (DW) to 0 seconds, and issuing an "ATDT<Phone Number>;<CR>" command. This immediately causes the ISOmodem® chipset to dial and return to command mode.

Once the host has detected an answer tone using manual call progress, the host should immediately execute the "ATDT" command in order to make a connection. This causes the Si2401 to search for the modem answer tone and begin the correct connect sequence.

In manual call progress, the DSP can be programmed to detect specific tones. The result of the detection is reported in SE5 (SE8 = 0x2) as explained above. The output is priority-encoded such that if multiple tones are detected, the one with the highest priority whose detection is also enabled is reported (see SE5 [SE8=02] Read Only.)

In manual call progress, the DSP can be programmed to generate specific tones (see SE5[2:0] (TONC) (SE8 = 02) Write Only). For example, setting SE5[2:0] (TONC) = 110_b generates the user-defined tone (as indicated by UFRQ in Table 18) with an amplitude of TGNL.

Table 17 shows the mappings of Si2401 DTMF values, keyboard equivalents, and related dual tones.

Table 17. DTMF Values

DTMF Code	Keyboard Equivalent	Contact ID Digit	Tones	
			Low	High
0	0	0	941	1336
1	1	1	697	1209
2	2	2	697	1336
3	3	3	697	1477
4	4	4	770	1209
5	5	5	770	1336
6	6	6	770	1477
7	7	7	852	1209
8	8	8	852	1336
9	9	9	852	1477
10	D	–	941	1633
11	*	B	941	1209
12	#	C	941	1477
13	A	D	697	1633
14	B	E	770	1633
15	C	F	852	1633

6. Low Level DSP Control

Although not necessary for most applications, the DSP low-level control functions are available for users with very specific applications requiring direct DSP control.

6.1. DSP Registers

Several DSP registers are accessible through the Si2401 microcontroller via S-registers SE5, SE6, and SE8. SE5 and SE6 are used as conduits to write data to specific DSP registers and read status. SE8 defines the function of SE5 and SE6 depending on whether they are being written to or read from. Care must be exercised when writing to DSP registers. DSP registers can only be written while the Si2401 is on-hook and in the command mode. Writing to any register address not listed in Tables 18 and 19 or writing out-of-range values is likely to cause the DSP to exhibit unpredictable behavior.

The DSP register address is 16-bits wide, and the DSP data field is 14-bits wide. DSP register addresses and data are written in hexadecimal. To write a value to a DSP register, the register address is written, and then the data is written. When SE8 = 0x00, SE5(DADL) is written with the low bits [7:0] of the DSP register address, and SE6 (DADH) is written with the high bits [15:8] of the DSP address. When SE8 = 0x01, SE5 (DDL) is written with the low bits [7:0] of the DSP data word corresponding to the previously-written address, and SE6 (DDH) is written with the high bits [15:8] of the data word corresponding to the previously-written address. Example 1 illustrates the proper procedure for writing to DSP registers.

Example1: The user would like to program call progress filter coefficient A2_k0 (0x15) to be 309 (0x135).

Host Command:

ATSE8=00SE6=00SE5=15SE8=01SE6=01SE5=35SE8=00

In this command, ATSE8=00 sets up registers SE5 and SE6 as DSP address registers. SE6=00 sets the high bits of the address, and SE5=15 sets the low bits. SE8=01 sets up registers SE5 and SE6 as DSP data registers for the previously-written DSP address (0x15). SE6=01 sets the six high bits of the 14-bit data word, and SE5=35 sets the eight low bits of the 14-bit data word.

Table 18. Low-Level DSP Parameters

DSP Reg. Addr.	Name	Description	Function	Default (dec)
0x0002	XMTL	DAA modem full-scale transmit level, default = –10 dBm.	Level = $20\log_{10}$ (XTML/4096) –10 dBm	4096
0x0003	DTML	DTMF high-tone transmit level, default = –5.5 dBm.	Level = $20\log_{10}$ (DTML/4868) –5.5 dBm	4868
0x0004	DTMT	DTMF twist ratio (low/high), default = –2 dBm.	Level = $20\log_{10}$ (DTMT/3277) – 2 dB	3277
0x0005	UFRQ	User-defined transmit tone frequency. See register SE5 (SE8=0x02 (Write Only)).	f = (9600/512) UFRQ (Hz)	91
0x0006	CPDL	Call progress detect level (see Figure 5), default = –43 dBm.	Level = $20\log_{10}$ (4096/CPDL) –43 dBm	4096
0x0007	UDFD1	User-defined frequency detector 1. Center frequency for detector 1.	UDFD1 = 8192 cos (2π f/9600)	4987
0x0008	UDFD2	User-defined frequency detector 2. Center frequency for detector 2.	UDFD2 = 8192 cos (2π f/9600)	536
0x0009	UDFD3	User-defined frequency detector 3. Center frequency for detector 3.	UDFD3 = 8192 cos (2π f/9600)	4987
0x000A	UDFD4	User-defined frequency detector 4. Center frequency for detector 4.	UDFD4 = 8192 cos (2π f/9600)	536
0x000B	TGNL	Tone generation level associated with TONC (SE5 (SE8 = 0x02) Write Only Definition), default = –10 dBm.	Level = $20\log_{10}$ (TGNL/2896) – 10 dBm	2896
0x000E	UDFSL	Sensitivity setting for UDFD1–4 detectors, default = –43 dBm.	Sensitivity = $10\log_{10}$(UDFSL/4096) –43 dBm	4096
0x0024	CONL	Carrier ON level. Carrier is valid once it reaches this level.	Level = $20\log_{10}$(2620/CONL) – 43 dBm	2620
0x0025	COFL	Carrier OFF level. Carrier is invalid once it falls below this level.	Level = $20\log_{10}$(3300/COFL) – 45.5 dBm	3300
0x0026	AONL	Answer ON level. Answer tone is valid once it reaches this level.	Level = $10\log_{10}$(AONL/107) – 43 dBm	67
0x0027	AOFL	Answer OFF level. Answer tone is invalid once it falls below this level.	Level = $10\log_{10}$(AOFL/58) – 45.5 dBm	37

Table 19 defines the relationship between SE5, SE6, and SE8.

Table 19. SE5, SE6, and SE8 Relationship

SE8		SE6		SE5	
	R/W	Name	Description	Name	Description
0x00	W	DADH	DSP register address bits [15:8]	DADL	DSP register address bits [7:0]
0x01	W	DDH	DSP register data bits [15:8]	DDL	DSP register data bits [7:0]
0x02	R			DSP1	7 = DSP data available 6 = Tone detected 5 = Reserved 4:0 = Tone type
0x02	W	DSP3	7 = Enable squaring function 6 = Call progress cascade disable 5 = Reserved 4 = User tone 3 and 4 reporting 3 = User tone 1 and 2 reporting 2 = V.23 tone reporting 1 = Answer tone reporting 0 = DTMF tone reporting	DSP2	7 = Reserved 6:3 = DTMF tone to transmit 2:0 = Tone type

6.2. Call Progress Filters

The programmable call progress filter coefficients are located in DSP address locations 0x0010 through 0x0023. There are two independent 4th order filters, A and B, each consisting of two biquads, for a total of 20 coefficients. Coefficients are 14 bits (–8192 to 8191) and are interpreted as, for example, b0 = value/4096, thus giving a floating point value of approximately –2.0 to 2.0. The output of each biquad is calculated as follows:

$$w[n] = k0 \times x[n] + a1 \times w[n-1] + a2 \times w[n-2]$$

$$y[n] = w[n] + b1 \times w[n-1] + b2 \times w[n-2]$$

The output of the filters is input to an energy detector and then compared to a fixed threshold with hysteresis (DSP register CPDL). Defaults shown are a bandpass filter from 290–630 Hz (–3 dB). These registers are located in the DSP and, thus, must be written in the same manner described in “6.1. DSP Registers” .

The filters may be configured in either parallel or cascade through SE6[6] (CPCD) with SE8 = 0x02, and the output of filter B may be squared by selecting SE6[7] (CPSQ) = 1. Figure 5 shows a block diagram of the call progress filter structure.

Table 20. Call Progress Filters

DSP Register Address	Coefficient	Default (dec)
0x0010	A1_k0	256
0x0011	A1_b1	–8184
0x0012	A1_b2	4096
0x0013	A1_a1	7737
0x0014	A1_a2	–3801
0x0015	A2_k0	1236
0x0016	A2_b1	133
0x0017	A2_b2	4096
0x0018	A2_a1	7109
0x0019	A2_a2	–3565
0x001A	B1_k0	256
0x001B	B1_b1	–8184
0x001C	B1_b2	4096
0x001D	B1_a1	7737
0x001E	B1_a2	–3801
0x001F	B2_k0	1236
0x0020	B2_b1	133
0x0021	B2_b2	4096
0x0022	B2_a1	7109
0x0023	B2_a2	–3565

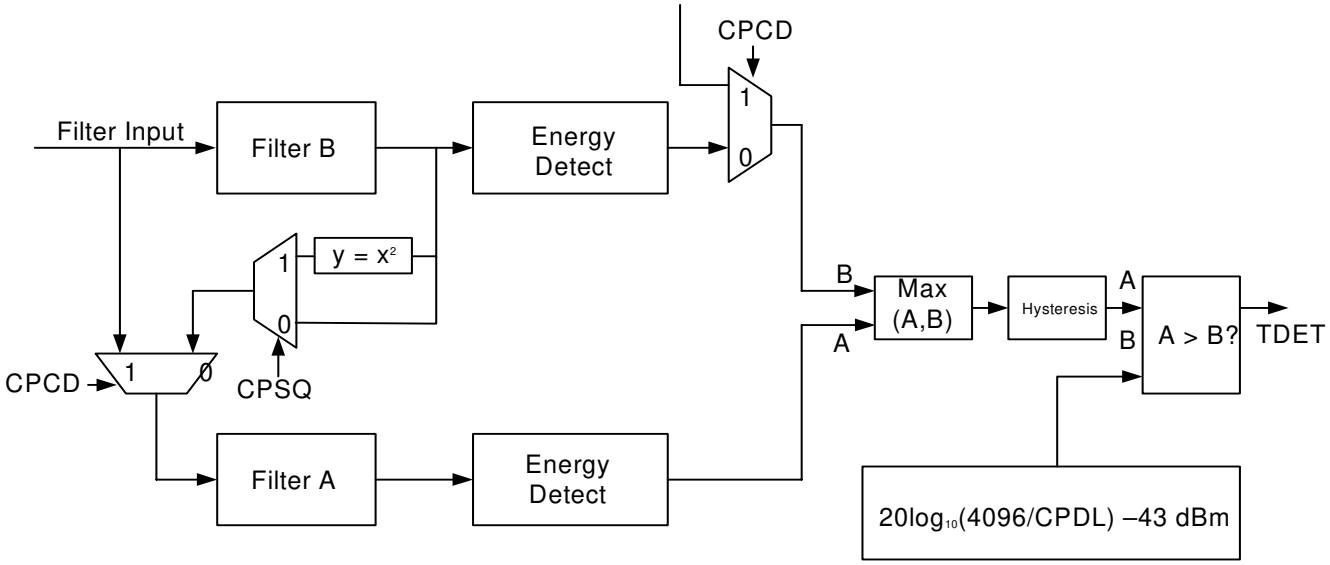


Figure 5. Programmable Call Progress Filter Architecture

7. S Registers

Any register not documented here is reserved and should not be written. Bold selection in bit-mapped registers indicates default values.

Table 21. S-Register Summary

"S" Register	Register Address (hex)	Name	Function	Reset
S00	0x00	NR	Number of rings before answer; 0 suppresses auto answer.	0x00
S01	0x01	DW	Number of seconds modem waits before dialing after going off-hook (maximum of 109 seconds).	0x02
S02	0x02	CW	Number of seconds modem waits for a dial tone before hang-up added to time specified by DW (maximum of 109 seconds).	0x03
S03	0x03	CLW	Duration that the modem waits (53.33 ms units) after loss of carrier before hanging up.	0x0E
S04	0x04	TD	Both duration and spacing (5/3 ms units) of DTMF dialed tones.	0x30
S05	0x05	OFFPD	Duration of off-hook time (5/3 ms units) for pulse dialing.	0x18
S06	0x06	ONPD	Duration of on-hook time (5/3 ms units) for pulse dialing.	0x24
S07	0x07	MF1	This is a bit-mapped register.*	0x06
S08	0x08	INTM	This is a bit-mapped register.*	0x00
S09	0x09	INTS	This is a bit-mapped register.*	0x00
S0C	0x0C	MF2	This is a bit-mapped register.*	0x00
S0D	0x0D	MF3	This is a bit-mapped register.*	0x00
S0E	0x0E	DIT	Pulse dialing Interdigit time (10 ms units added to a minimum time of 64 ms).	0x46
S0F	0x0F	TEC	TIES escape character. Default = +.	0x2B
S10	0x10	TDT	TIES delay time (53.33 ms units).	0x13
S11	0x11	OFHI	This is a bit-mapped register.*	0x04
S12	0x12	ACL	Absolute Current Level. When S13[4] (OFHD) = 0_b, ACL represents the absolute current threshold used by the off-hook intrusion algorithm (1 mA units.)	0x00
S13	0x13	MF4	This is a bit-mapped register.*	0x10
S15	0x15	MLC	This is a bit-mapped register.*	0x04
S16	0x16	BTON	Busy tone on. Time that the busy tone must be on (10 ms units) for busy tone detector.	0x32
S17	0x17	BTOF	Busy tone off. Time that the busy tone must be off (10 ms units) for busy tone detector.	0x32
***Note:** These registers are explained in detail in the following section.				

Table 21. S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S18	0x18	BTOD	Busy tone delta time (10 ms units). A busy tone is detected to be valid if (BTON – BTOD < on time < BTON + BTOD) and (BTOF – BTOD < off time < BTOF + BTOD).	0x0F
S19	0x19	RTON	Ringback tone on. Time that the ringback tone must be on (53.333 ms units) for ringback tone detector.	0x26
S1A	0x1A	RTOF	Ringback tone off. Time that the ringback tone must be off (53.333 ms units) for ringback tone detector.	0x4B
S1B	0x1B	RTOD	Detector time delta (53.333 ms units). A ringback tone is determined to be valid if (RTON – RTOD < on time < RTON + RTOD) and (RTOF – RTOD < off time < RTOF + RTOD).	0x07
S1C	0x1C	DTT	Dial tone detect time. The time that the dial tone must be valid before being detected (10 ms units).	0x0A
S1E	0x1E	TATL	Transmit answer tone length. Answer tone length in seconds when answering a call (1 s units).	0x03
S1F	0x1F	ARM3	Answer tone to transmit delay. Delay between answer tone end and transmit data start (5/3 ms units).	0x2D
S20	0x20	UNL	Unscrambled ones length. Minimum length of time required for detection of unscrambled binary ones during V.22 handshaking by a calling modem (5/3 ms units).	0x5D
S21	0x21	TSOD	Transmit scrambled ones delay. Time between unscrambled binary one detection and scrambled binary one transmission by a call mode V.22 modem (53.3 ms units).	0x09
S22	0x22	TSOL	Transmit scrambled ones length. Length of time scrambled ones are sent by a call mode V.22 modem (5/3 ms units).	0xA2
S23	0x23	VDDL	V.22X data delay low. Delay between handshake complete and data connection for a V.22X call mode modem (5/3 ms units added to the time specified by VDDH).	0xCB
S24	0x24	VDDH	V.22X data delay high. Delay between handshake complete and data connection for a V.22X call mode modem (256 x 5/3 ms units added to the time specified by VDDL).	0x08
S25	0x25	SPTL	S1 pattern time length. Amount of time the unscrambled S1 pattern is sent by a call mode V.22bis modem (5/3 ms units).	0x3C
S26	0x26	VTSO	V.22bis 1200 bps scrambled ones length. Minimum length of time for transmission of 1200 bps scrambled binary ones by a call mode V.22bis modem after the end of pattern S1 detection (53.3 ms).	0x0C
S27	0x27	VTSOL	V.22bis 2400 bps scrambled ones length low. Minimum length of time for transmission of 2400 bps scrambled binary ones by a call mode V.22bis modem (5/3 ms units).	0x78
***Note:** These registers are explained in detail in the following section.				

Table 21. S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S28	0x28	VTSOH	V.22bis 2400 bps scrambled ones length high. Minimum length of time for transmission of 2400 bps scrambled binary ones by a call mode V.22bis modem (256 x 5/3 ms units added to the time specified by VTSOL).	0x08
S29	0x29	IS	Intrusion suspend. When S82[2:1] (IB) = 10_b, this register sets the length of time from when dialing begins that the off-hook intrusion algorithm is blocked (suspended) (500 ms units).	0x00
S2A	0x2A	RSO	Receive scrambled ones V.22bis (2400 bps) length. Minimum length of time required for detection of scrambled binary ones during V.22bis handshaking by the answering modem after S1 pattern conclusion (5/3 ms units).	0xD2
S2B	0x2B	DTL	V.23 direct turnaround carrier length. Minimum length of time that a master mode V.23 modem must detect carrier when searching for a direct turnaround sequence (5/3 ms units).	0x18
S2C	0x2C	DTTO	V.23 direct turnaround timeout. Length of time that the modem searches for a direct turnaround carrier (5/3 ms units added to a minimum time of 426.66 ms).	0x08
S2D	0x2D	SDL	V.23 slave carrier detect loss. Minimum length of time that a slave mode V.23 modem must lose carrier before searching for a reverse turnaround sequence (5/3 ms units).	0x0C
S2E	0x2E	RTCT	V.23 reverse turnaround carrier timeout. Amount of time a slave mode V.23 modem searches for carriers during potential reverse turnaround sequences (5/3 ms units).	0xF0
S2F	0x2F	FCD	FSK connection delay low. Amount of time delay added between end of answer tone handshake and actual modem connection for FSK modem connections (5/3 ms units).	0x3C
S30	0x30	FCDH	FSK connection delay high. Amount of time delay added between end of answer tone handshake and actual modem connection for FSK modem connections (256 x 5/3 ms units).	0x00
S31	0x31	RATL	Receive answer tone length. Minimum length of time required for detection of a CCITT answer tone (5/3 ms units).	0x3C
S32	0x32	OCDT	The time after going off-hook when the loop current sense bits are checked for overcurrent status (5/3 ms units).	0x0C
S34	0x34	TASL	Answer tone length when answering a call (5/3 ms units). This register is only used if TATL (1E) has a value of zero.	0x5A
S35	0x35	RSOL	Receive scrambled ones V.22 length (5/3 ms units). Minimum length of time that an originating V.22 (1200 bps) modem must detect 1200 bps scrambled ones during a V.22 handshake.	0xA2
S36	0x36	ARM1	Second kissoff tone detector length. The security modes, A1 and !1, echo a "k" if a kissoff tone longer than the value stored in SKDTL is detected (10 ms units).	0x30
***Note:** These registers are explained in detail in the following section.				

Table 21. S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
S37	0x37	CDR	Carrier detect return. Minimum length of time that a carrier must return and be detected in order to be recognized after a carrier loss is detected (5/3 ms units).	0x20
S39	0x39	CDT	Carrier detect timeout. Amount of time modem waits for carrier detect before aborting call (1 second units).	0x3C
S3A	0x3A	ATD	Delay between going off-hook and answer tone generation when in answer mode (53.33 ms units).	0x29
S3B	0x3B	RP	Minimum number of consecutive ring pulses per ring burst.	0x03
S3C	0x3C	CIDG	This is a bit mapped register.*	0x01
S62	0x62	RC	This is a bit mapped register.*	0x41
S82	0x82	IST	This is a bit mapped register.*	0x08
SDB	0xDB	LVS	Line Voltage Status. Eight bit signed, 2s complement number representing the tip-ring voltage. Each bit represents 1 volt. Polarity of the voltage is represented by the MSB (sign bit). 0000_0000 = Measured voltage is < 3 V.	
SDF	0xDF	DGSR	This is a bit mapped register.*	0x0C
SE0	0xE0	CF1	This is a bit mapped register.*	0x22
SE1	0xE1	GPIO1	This is a bit mapped register.*	0x04
SE2	0xE2	GPIO2	This is a bit mapped register.*	0x00
SE3	0xE3	GPD	This is a bit mapped register.*	0x00
SE4	0xE4	CF5	This is a bit mapped register.*	0x00
SE5	0xE5	DADL	(SE8 = 0x00) Write only definition. DSP register address lower bits [7:0].*	0x00
SE5	0xE5	DDL	(SE8 = 0x01) Write only definition. DSP data word lower bits [7:0].*	0x00
SE5	0xE5	DSP1	(SE8 = 0x02) Read only definition. This is a bit mapped register.[1]	0x00
SE5	0xE5	DSP2	(SE8 = 0x02) Write only definition. This is a bit mapped register.[1]	0x00
SE6	0xE6	DADH	(SE8 = 0x00) Write only definition. DSP register address upper bits [15:8].	0x00
SE6	0xE6	DDH	(SE8 = 0x01) Write only definition. DSP data word upper bits [13:8]	0x00
SE6	0xE6	DSP3	(SE8 = 0x02) Write only definition. This is a bit mapped register.[1]	0x00
SE8	0xE8	DSPR4	Set the mode to define E5 and E6 for low level DSP control.	0x00

***Note:** These registers are explained in detail in the following section.

Table 21. S-Register Summary (Continued)

"S" Register	Register Address (hex)	Name	Function	Reset
SEB	0xEB	TPD	This is a bit mapped register.*	0x00
SEC	0xEC	RVC1	This is a bit mapped register.*	0x88
SED	0xED	RVC2	This is a bit mapped register.*	0x19
SEE	0xEE	RVC3	This is a bit mapped register.*	0x16
SF0	0xF0	DAA0	This is a bit mapped register.*	0x40
SF1	0xF1	DAA1	This is a bit mapped register.*	0x0C
SF2	0xF2	DAA2	This is a bit mapped register.*	0x00
SF3	0xF3	DAA3	Line Current Status. Eight-bit value returning the loop current. Each bit represents 1.1 mA of loop current. Accuracy is not guaranteed if the loop current is less than required for normal operation.	0x00
SF4	0xF4	DAA4	This is a bit mapped register.*	0x0F
SF5	0xF5	DAA5	This is a bit mapped register.*	0x00
SF6	0xF6	DAA6	This is a bit mapped register.*	0xF0
SF7	0xF7	DAA7	This is a bit mapped register.*	0x00
SF8	0xF8	DAA8	This is a bit mapped register.*	—
SF9	0xF9	DAA9	This is a bit mapped register.*	0x20

***Note:** These registers are explained in detail in the following section.

Table 22. Bit Mapped Register Summary

"S" Register	Register Address (hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Binary
S07	0x07	MF1		BD	V23R	V23T		BAUD	CCITT	FSK	0000_0110
S08	0x08	INTM	CDM	WORM	PPDM	NVDM	RIM	CIDM		REVM	0000_0000
S09	0x09	INTS	CD	WOR	PPD	NVD	RI	CID		REV	0000_0000
S0C	0x0C	MF2	CDE	CIDM[1:0]			9BF	BDL	MLB		0000_0000
S0D	0x0D	MF3		RI	INTP	RBTS	EHR	EHB	EHI	EHE	0000_0000
S11	0x11	OFHI					DCL[3:0]				0000_0100
S13	0x13	MF4		BTID		OFHD		CIDB	HDEN		0001_0000
S15	0x15	MLC	ATPRE	VCTE	FHGE	EHGE	STB	BDA[1:0]		NBE	0000_0100
S3C	0x3C	CIDG						CIDG[2:0]			0000_0001
S62	0x62	RC		OCR				IR	NLR	RR	0100_0001
S82	0x82	IST	IST[3:0]				LCLD	IB[1:0]			0000_1000
SDF	0xDF	DGSR		DGSR[6:0]							0000_1100
SE0	0xE0	CF1			ICTS		ND	SD[2:0]			0010_0010
SE1	0xE1	GPIO1							GPD5	GPIO5	0000_0000
SE2	0xE2	GPIO2	GPIO4[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]		0000_0000
SE3	0xE3	GPD					GPD4	GPD3	GPD2	GPD1	0000_0000
SE4	0xE4	CF5	NBCK	SBCK	DRT		GPE				0000_0000
SE5	0xE5	DSP1	DDAV	TDET		TONE[4:0]					0000_0000
SE5	0xE5	DSP2		DTM[3:0]				TONC[2:0]			0000_0000
SE6	0xE6	DSP3	CPSQ	CPCD		USEN2	USEN1	V23E	ANSE	DTMFE	0000_0000
SEB	0xEB	TPD					PDDE				0000_0000
SEC	0xEC	RVC1	RNGV	RDLY[2:0]			RCC[2:0]				1000_1000
SED	0xED	RVC2			RAS[5:0]						0001_1001
SEE	0xEE	RVC3	RTO[3:0]				RMX[3:0]				0001_0110
SF0	0xF0	DAA0	FOH[1:0]						LM[1:0]		0100_0000
SF1	0xF1	DAA1		PDN	PDL	LVFD		HBE			0000_1100
SF2	0xF2	DAA2					FDT				0000_0000

Table 22. Bit Mapped Register Summary (Continued)

"S" Register	Register Address (hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Binary
SF4	0xF4	DAA4					ARL[1:0]		ATL[1:0]		0000_1111
SF5	0xF5	DAA5								RT	0000_0000
SF8	0xF8	DAA8	LRV[3:0]								—
SF9	0xF9	DAA9						OVL	ROV		0010_0000
SFC	0xFC	DAAFC	CTSM								0000_0000

S07 (MF1). Modem Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		BD	V23R	V23T		BAUD	CCITT	FSK
Type		R/W	R/W	R/W		R/W	R/W	R/W

Reset settings = 0000_0110 (0x06)

Bit	Name	Function
7	Reserved	Read returns zero.
6	BD	**Blind Dialing.** **0** = **Disable.** 1 = Enable (Blind dialing occurs immediately after “ATDT#” command).
5	V23R	**V.23 Receive.*** V.23 75 bps send/600 (BAUD = 0) or 1200 (BAUD = 1) bps receive. **0** = **Disable.** 1 = Enable.
4	V23T	**V.23 Transmit.*** V.23 600 (BAUD = 0) or 1200 (BAUD = 1) bps send/75 bps receive. **0** = **Disable.** 1 = Enable.
3	Reserved	Read returns zero.
2	BAUD	**2400/1200 Baud Select.*** 2400/1200 baud select (V23R = 0 and V23T = 0). 0 = 1200 **1** = **2400** 600/1200 baud select (V23R = 1 and V23T = 1). 0 = 600 **1** = **1200**
1	CCITT	**CCITT/Bell Mode.*** 0 = Bell. **1** = **CCITT.**
0	FSK	**300 bps FSK.*** **0** = **Disable.** 1 = Enable.
***Note:** See Table 10 on page 13 for proper setting of modem protocols.		

S08 (INTM). Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDM	WORM	PPDM	NVDM	RIM	CIDM		REVM
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	CDM	**Carrier Detect Mask.** **0** = **Change in CD does not affect INT.** 1 = A high to low transition in CD (S09, bit 7), which indicates loss of carrier, activates INT.
6	WORM	**Wake-on-Ring Mask.** **0** = **Change in CD does not affect INT.** 1 = A low to high transition in WOR (S09, bit 6) activatesINT.
5	PPDM	**Parallel Phone Detect Mask.** **0** = **Change in PPD does not affect INT.** 1 = A low to high transition in PPD (S09, bit 5) activates INT.
4	NVDM	**No Phone Line Detect Mask.** **0** = **Change in NLD does not affect INT.** 1 = A low to high transition in NLD (S09, bit 4) activates INT.
3	RIM	**Ring Indicator Mask.** **0** = **Change in RI does not affect INT.** 1 = A low to high transition in RI (S09, bit 3) activates INT.
2	CIDM	**Caller ID Mask.** **0** = **Change in CID does not affect INT.** 1 = A low to high transition in CID (S09, bit 2) activates INT.
1	Reserved	Read returns zero.
0	REVM	**V.23 Reversal Detect Mask.** **0** = **Change in REV does not affect INT.** 1 = A low to high transition in REV (S09, bit 0) activates INT.

S09 (INTS). Interrupt Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CD	WOR	PPD	NVD	RI	CID		REV
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	CD	**Carrier Detect (sticky).** Active high bit indicates carrier detected (equivalent to inverse of CD pin). Clears on :1 read.
6	WOR	**Wake-on-Ring (sticky).** Wake-on-ring has occurred. Clears on :I read.
5	PPD	**Parallel Phone Detect (sticky).** Parallel phone detected since last off-hook event. Clears on :I read.
4	NVD	**No Phone Line Detect (sticky).** No line phone detected. Clears on :I read.
3	RI	**Ring Indicator (sticky).** Active high bit when the Si2401 is on-hook, indicates ring event has occurred. Clears on :I read.
2	CID	**Caller ID (sticky).** Caller ID preamble has been detected; data soon follows. Clears on :I read.
1	Reserved	Read returns zero.
0	REV	**V.23 Reversal Detect (sticky).** V.23 reversal condition has occurred. Clears on :I read.

S0C (MF2). Modem Functions 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CDE	CIDM[1:0]			9BF	BDL	MLB	
Type	R/W	R/W			R/W	R/W	R/W	

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	CDE	**Carrier Detect Enable.** **0** = **Disable.** 1 = Enable GPI02 as an active low carrier detect pin (must also set SE2[3:2] [GPIO2] = 01).
6:5	CIDM[1:0]	**Caller ID Monitor.** **00** = **Caller ID monitor disabled.** 01 = Caller ID monitor enabled. Si2401 must detect channel seizure signal followed by marks in order to report caller ID data. (Normal Bellcore caller ID) 10 = Reserved. 11 = Caller ID monitor enabled. Si2401 must only detect marks in order to report caller ID data.
4	Reserved	Read returns zero.
3	9BF	**Ninth Bit Function.** Only valid if the ninth bit escape is set S15[0] (NBE). **0** = **Ninth bit equivalent to ALERT.** 1 = Ninth bit equivalent to HDLC EOFR.
2	BDL	**Blind Dialing.** **0** = **Blind dialing disabled.** 1 = Enables blind dialing after dial timeout register S02 (CW) expires.
1	MLB	**Modem Loopback.** **0** = **Not swapped.** 1 = Swaps frequency bands in modem algorithm to do a loopback in a test mode.
0	Reserved	Read returns zero.

SOD (MF3). Modem Functions 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RI	INTP	RBTS	EHR	EHB	EHI	EHE
Type		R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	Reserved	Read returns zero.
6	RI	**Ring Indicator Control.** Specifies the functionality of pin3. **0** = **Pin 3 functions as GPIO5 controlled by register SE1.** 1 = Pin 3 functions as $\overline{RI}$. $\overline{RI}$ asserts during a ring and negates when no ring is present.
5	INTP	**$\overline{INT}$ Polarity.** Specifies the polarity of the $\overline{INT}$ function on pin 11. **0** = **An interrupt forces pin 11 low.** 1 = An interrupt forces pin 11 high.
4	RBTS	**Ringback Tone Selector.** Controls the unit step size for registers S19, S1A and S1B. **0** = **53.33 ms units. Necessary for detecting a ringback tone.** 1 = 10 ms units. Necessary for detecting a reorder tone.
3	EHR	**Enable Hangup on Reorder.** Modem is placed on-hook if a ringback or reorder tone is detected. See S0D[4]. **0** = **Disable.** 1 = Enable.
2	EHB	**Enable Hangup on Busy.** Modem is placed on-hook if a busy signal is detected. **0** = **Disable.** 1 = Enable.
1	EHI	**Enable Hangup on Intrusion.** Modem is placed on-hook if parallel intrusion is detected. **0** = **Disable.** 1 = Enable.
0	EHE	**Enable Hangup on Escape.** Modem is placed on-hook if a ESC signal is detected. **0** = **Disable.** 1 = Enable.

S11 (OFHI). Off-Hook Intrusion

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					DCL[3:0]			
Type	R/W							

Reset settings = 0000_0100 (0x04)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	DCL[3:0]	**Differential Current Level.** Differential current level to detect intrusion event (1 mA units).

S13 (MF4). Modem Functions 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		BTID		OFHD		CIDB	HDEN	
Type		R/W	R/W	R/W		R/W	R/W	

Reset settings = 0001_0000 (0x10)

Bit	Name	Function
7	Reserved	Read returns zero.
6	BTID	**BT Caller ID Wetting Pulse.** **0** = **Enable.** 1 = Disable.
5	Reserved	Read returns zero.
4	OFHD	**Off-Hook Intrusion Detect Method.** 0 = Absolute. **1** = **Differential.**
3	Reserved	Read returns zero.
2	CIDB	**British Telecom Caller ID Decode.** **0** = **Disable.** 1 = Enable. When set, SOC[6:5] is overwritten by the modem, as needed.
1	HDEN	**HDLC Framing.** **0** = **Disable.** 1 = Enable.
0	Reserved	Read returns zero.

S15 (MLC). Modem Link Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATPRE	VCTE	FHGE	EHGE	STB	BDA[1:0]		NBE
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Reset settings = 0000_0100 (0x04)

Bit	Name	Function
7	ATPRE	**Answer Tone Phase Reversal.** **0** = **Disable.** 1 = Enable answer tone phase reversal.
6	VCTE	**V.25 Calling Tone.** **0** = **Disable.** 1 = Enable V.25 calling tone.
5	FHGE	**550 Hz Guardtone.** **0** = **Disable.** 1 = Enable 550 Hz guardtone.
4	EHGE	**1800 Hz Guardtone.** **0** = **Disable.** 1 = Enable 1800 Hz guardtone.
3	STB	**Stop Bits.** **0** = **1 stop bit.** 1 = 2 stop bits.
2:1	BDA[1:0]	**Bit Data.** 00 = 6 bit data. 01 = 7 bit data. **10** = **8 bit data.** 11 = 9 bit data.
0	NBE	**Ninth Bit Enable.** **0** = **Disable.** 1 = Enable ninth bit as Escape and ninth bit function (register C).

S3C (CIDG). Caller ID Gain

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						CIDG[2:0]		
Type	R/W							

Reset settings = 0000_0001 (0x01)

Bit	Name	Function
7:3	Reserved	Read returns 0.
2:0	CIDG[2:0]	**Caller ID Gain.** The Si2401 dynamically sets the On-Hook Analog Receive Gain SF4[6:4] (ARG) to CIDG during a caller ID event (or continuously if S0C[6:5] (CIDM = 11). This field should be set prior to caller ID operation. **000 = 0 dB** 001 = 3 dB 010 = 6 dB 011 = 9 dB 100 = 12 dB

S62 (RC). Result Codes Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		OCR				IR	NLR	RR
Type	R/W					R/W	R/W	R/W

Reset settings = 0100_0001 (0x41)

Bit	Name	Function
7	Reserved	Read returns zero.
6	OCR	**Overcurrent Result Code ("x").** 0 = Enable. **1 = Disable.**
5:3	Reserved	Read returns zero.
2	IR	**Intrusion Result Code ("I" and "i").** **0 = Disable.** 1 = Enable.
1	NLR	**No Phone Line Result Code ("L" and "l").** **0 = Disable.** 1 = Enable.
0	RR	**Ring Result Code ("R").** 0 = Disable. **1 = Enable.**

S82 (IST). Intrusion

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	IST[3:0]				LCLD	IB[1:0]		
Type	R/W				R/W	R/W		

Reset settings = 0000_1000 (0x08)

Bit	Name	Function
7:4	IST[3:0]	**Intrusion Settling Time.** **0000 = IST equals 1 second.** Delay between when the ISOmodem® chipset goes off-hook and the off-hook intrusion algorithm begins (250 ms units).
3	LCLD	**Loop Current Loss Detect.** 0 = Disable. **1 = Enables the reporting of "l" and "L" result codes while off-hook. Asserts $\overline{\text{INT}}$ if GPIO4 (SE2[7:6]) is enabled as $\overline{\text{INT}}$.**
2:1	IB[1:0]	**Intrusion Blocking.** This feature only works when SDF ≠ 0x00. Defines the method used to block the off-hook intrusion algorithm from operating after dialing has begun. **00 = No intrusion blocking.** 01 = Intrusion disabled from start of dial to end of dial. 10 = Intrusion disabled from start of dial to register S29 time out. 11 = Intrusion disabled from start of dial to carrier detect or to "N" or "n" result code.
0	Reserved	Read returns zero.

SDF (DGSR). Intrusion Deglitch

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DGSR[6:0]						
Type	R/W							

Reset settings = 0000_1100 (0x0C)

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	DGSR[6:0]	**Deglitch Sample Rate.** Sets the sample rate for the deglitch algorithm and the off-hook intrusion algorithm (40 ms units). 0000000 = Disables the deglitch algorithm, and sets the off-hook intrusion sample rate to 200 ms and delay between compared samples to 800 ms.

SE0 (CF1). Chip Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			ICTS		ND	SD[2:0]		
Type	R/W				R/W	R/W		

Reset settings = 0010_0010 (0x22)

Bit	Name	Function
7:6	Reserved	Read returns zero.
5	ICTS	**Invert $\overline{\text{CTS}}$ pin.** 0 = Inverted (CTS). **1 = Normal (CTS).**
4	Reserved	Read returns zero.
3	ND	**0 = 8N1.** 1 = 9N1 (hardware UART only).
2:0	SD[2:0]	**Serial Dividers.** 000 = 300 bps serial link. 001 = 1200 bps serial link. **010 = 2400 bps serial link.** 011 = 9600 bps serial link. 100 = 19200 bps serial link. 101 = 38400 bps serial link 110 = 115200 bps serial link. 111 = 307200 bps serial link.

SE1 (GPIO1). General Purpose Input/Output 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							GPD5	GPIO5
Type							R/W	R/W

Reset settings = 0000_0000 (0x04)

Bit	Name	Function
7:2	Reserved	Read returns zero.
1	GPD5	**GPIO5 Data.** Data = 0. Data = 1.
0	GPIO5	**GPIO5.** **0 = Digital input.** 1 = Digital output (relay drive).

SE2 (GPIO2). General Purpose Input/Output 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	GPIO4[1:0]		GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7:6	GPIO4[1:0]	**GPIO4.** **00** = **Digital input.** 01 = Digital output (relay drive). 10 = $\overline{\text{AOUT}}$. 11 = $\overline{\text{INT}}$ function defined by S08.
5:4	GPIO3[1:0]	**GPIO3.** **00** = **Digital input.** 01 = Digital output (relay drive). 10 = Reserved. 11 = ESC function (digital input).
3:2	GPIO2[1:0]	**GPIO2.** **00** = **Digital input.** 01 = Digital output (relay drive; also used for $\overline{\text{CD}}$ function). 10 = Reserved. 11 = Digital input.
1:0	GPIO1[1:0]	**GPIO1*.** **00** = **Digital input.** 01 = Digital output (relay drive). 10 = Reserved. 11 = Reserved.
***Note:** To be used as a GPIO pin; SE4[3] (GPE) must equal zero.		

SE3 (GPD). GPIO Data

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					GPD4	GPD3	GPD2	GPD1
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	GPD4	**GPIO4 Data.** Data = 0 Data = 1
2	GPD3	**GPIO3 Data.** Data = 0 Data = 1
1	GPD2	**GPIO2 Data.** Data = 0 Data = 1
0	GPD1	**GPIO1 Data.** Data = 0 Data = 1

SE4 (CF5). Chip Functions 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NBCK	SBCK	DRT		GPE			
Type	R	R	R/W		R/W			

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	NBCK	**9600 Baud Clock (Read Only).**
6	SBCK	**600 Baud Clock (Read Only).**
5	DRT	**Data Routing.** **0** = **Data mode, DSP output transmitted to line, line received by DSP input.** 1 = Loopback mode, TXD through microcontroller (DSP) to RXD.
4	Reserved	Read returns zero.
3	GPE	**GPIO1 Enable.** **0** = **Disable.** 1 = Enable GPIO1 to be HDLC end-of-frame flag.
2:0	Reserved	Read returns zero.

SE5 (DSP1). (SE8 = 0x02) Read Only Definition

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DDAV	TDET		TONE[4:0]				
Type	R	R		R				

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	DDAV	**DSP Data Available.**
6	TDET	**Tone Detected.** Indicates a TONE (any of type 0–25 below) has been detected. **0** = **Not detected.** 1 = Detected.
5	Reserved	Read returns zero.
4:0	TONE[4:0]	**Tone Type Detected.** When TDET goes high, TONE indicates which tone has been detected from the following: **TONE** — **Tone Type** — **Priority** 00000–01111 — DTMF 0–15 (DTMFE = 1)[1] See Table 17 on page 26. — 1 10000 — Answer tone detected 2100 Hz (ANSE = 1)[2] — 2 10001 — Bell 103 answer tone detected 2225 Hz (ANSE = 1) — 2 10010 — V.23 forward channel mark 1300 Hz (V23E = 1)[3] — 3 10011 — V.23 backward channel mark 390 Hz (V23E = 1) — 3 10100 — User defined frequency 1 (USEN1 = 1)[4] — 4 10101 — User defined frequency 2 (USEN1 = 1) — 4 10110 — Call progress filter A detected — 6 10111 — User defined frequency 3 (USEN2 = 1)[5] — 5 11000 — User defined frequency 4 (USEN2 = 1) — 5 11001 — Call progress filter B detected — 6

Notes:
1. SE6[0] (DTMFE) SE8 = 0x02.
2. SE6[1] (ANSE) SE8 = 0x02.
3. SE6[2] (V23E) SE8 = 0x02.
4. SE6[3] (USEN1) SE8 = 0x02.
5. SE6[4] (USEN2) SE8 = 0x02.

SE5 (DSP2). (SE8 = 0x02) Write Only Definition

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DTM[3:0]				TONC[2:0]		
Type	W					W		

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	Reserved	Always write this bit to zero.
6:3	DTM[3:0]	**Tone Type Generated.** DTMF tone (0–15) to transmit when selected by TONC = 001. See Table 17 on page 26.
2:0	TONC[2:0]	**DTMF Tone Selector.** **Tone** — **Tone Type** **000** — **Mute** 001 — DTMF 010 — 2225 Hz Bell mode answer tone with phase reversal 011 — 2100 Hz CCITT mode answer tone with phase reversal 100 — 2225 Hz Bell mode answer tone without phase reversal 101 — 2100 Hz CCITT mode answer tone without phase reversal 110 — User-defined programmable frequency tone (UFRQ) (see Table 18 on page 28, default = 1700 Hz) 111 — 1300 Hz V.25 calling tone

SE6 (DSP3). (SE8 = 0x02) Write Only Definition

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CPSQ	CPCD		USEN2	USEN1	V23E	ANSE	DTMFE
Type	W	W		W	W	W	W	W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	CPSQ	**Call Progress Squaring Filter.** **0 = Disable.** 1 = Enables a squaring function on the output of filter B before the input to A (cascade only).
6	CPCD	**Call Progress Cascade Disable.** **0 = Call progress filter B output is input into call progress filter A. Output from filter A is used in the detector.** 1 = Cascade disabled. Two independent fourth order filters available (A and B). The largest output of the two is used in the detector.
5	Reserved	Do not modify.
4	USEN2	**User Tone Reporting Enable 2.** **0 = Disable.** 1 = Enable the reporting of user defined frequency tones 3 and 4 through TONE.
3	USEN1	**User Tone Reporting Enable 1.** **0 = Disable.** 1 = Enable the reporting of user defined frequency tones 1 and 2.
2	V23E	**V.23 Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of V.23 tones, 390 Hz and 1300 Hz.
1	ANSE	**Answering Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of answer tones.
0	DTMFE	**DTMF Tone Reporting Enable.** **0 = Disable.** 1 = Enable the reporting of DTMF tones.

SEB (TPD). Timer and Powerdown

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					PDDE			
Type	R/W							

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	PDDE	**Powerdown DSP Engine.** **0 = Power on.** 1 = Powerdown.
2:0	Reserved	Read returns zero.

SEC (RVC1). Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV	RDLY[2:0]			RCC[2:0]			
Type	R/W	R/W			R/W			

Reset settings = 1000_1000 (0x88)

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. **1 = Ring validation feature is enabled in both normal operating mode and low-power mode.**
6:4	RDLY[2:0]	**Ring Delay.** These bits set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2:0] Delay** **000 0 ms** 001 256 ms 010 512 ms . . . 111 1792 ms
3:1	RCC[2:0]	**Ring Confirmation Count.** These bits set the amount of time that the ring frequency must be within the tolerances set by the RAS[5:0] bits and the RMX[3:0] bits to be classified as a valid ring signal. **RCC[2:0] Ring Confirmation Count Time** 000 100 ms 001 150 ms 010 200 ms 011 256 ms **100 384 ms** 101 512 ms 110 640 ms 111 1024 ms
0	Reserved	This bit must always be written to zero.

SED (RVC2). Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RAS[5:0]					
Type	R/W							

Reset settings = 0001_1001 (0x19)

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out, the frequency of the ring is too low, and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: RAS[5:0] = 1 / (2 x f_min).

SEE (RVC3). Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RTO[3:0]				RMX[3:0]			
Type	R/W				R/W			

Reset settings = 0001_0110 (0x16)

Bit	Name	Function
7:4	RTO[3:0]	**Ring Timeout.** These bits set when a ring signal is determined to be over after the most recent ring threshold crossing. **RTO[3:0] Ring Timeout** 0000 80 ms 0001 128 ms 0010 256 ms . . . 1111 1920 ms
3:0	RMX[3:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[3:0] field, and if it exceeds the value in RMX[3:0], the frequency of the ring is too high, and the ring is invalidated. The difference between RAS[5:0] and RMX[3:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[3:0] value for a frequency range [f_min, f_max], the following equation should be used: RMX[3:0] x 2 ms = RAS[5:0] – 2 ms – (1/(2 x f_max)).

SF0 (DAA0). DAA Low Level Functions 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FOH[1:0]						LM[1:0]	
Type	R/W						R/W	R/W

Reset settings = 0100_0000 (0x40)

Bit	Name	Function
7:6	FOH[1:0]	**Fast Off-Hook Selection.** These bits determine the length of the off-hook counter. The default setting is 128 ms. 00 = 512 ms **01 = 128 ms** 10 = 64 ms 11 = 8 ms
5:2	Reserved	Read returns zero.
1:0	LM[1:0]	**Line Mode.** These bits determine the line status of the Si2401.* 00 = On-hook 01 = Off-hook 10 = On-hook line monitor mode 11 = Reserved
***Note:** Under normal operation, the Si2401 internal microcontroller automatically sets these bits appropriately.		

SF1 (DAA1). DAA Low Level Functions 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		PDN	PDL	LVFD		HBE		
Type		R/W	R/W	R/W		R/W		

Reset settings = 0000_1100 (0x0C)

Bit	Name	Function
7	Reserved	Read returns zero.
6	PDN	**Powerdown.** **0 = Normal operation.** 1 = Powers down the Si2401.
5	PDL	**Powerdown Line-Side Chip (typically only used for board level debug.)** **0 = Normal operation. Program the clock generator before clearing this bit.** 1 = Places the line-side device in lower power mode.
4	LVFD	**Line Voltage Force Disable.** **0 = Normal operation.** 1 = The circuitry that forces the LVS register to all 0s at 3 V or less is disabled. This register may display unpredictable values at voltages between 0 to 2 V. All 0s are displayed if the line voltage is 0 V.
3	Reserved	Do not modify.
2	HBE	**Hybrid Transmit Path Connect.** 0 = Disable. **1 = Enable.**
1:0	Reserved	Do not modify.

SF2 (DAA2). DAA Low Level Functions 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					FDT			
Type	R							

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7:4	Reserved	Read only.
3	FDT	**Frame Detect (Typically only used for board-level debug).** 1 = Indicates isolation capacitor frame lock has been established. **0 = Indicates isolation capacitor frame lock has not been established.**
2:0	Reserved	Reserved

SF4 (DAA4). DAA Low Level Functions 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					ARL[1:0]		ATL[1:0]	
Type	R/W						R/W	

Reset settings = 0000_1111 (0x0F)

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:2	ARL[1:0]	**AOUT Receive—Path Level.** DAA receive path signal AOUT gain. 00 = 0 dB 01 = –6 dB 10 = –12 dB **11 = Mute**
1:0	ATL[1:0]	**AOUT Transmit—Path Level.** DAA transmit path signal AOUT gain. 00 = –18 dB 01 = –24 dB 10 = –30 dB **11 = Mute**

SF5 (DAA5). DAA Low Level Functions 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								RT
Type								R/W

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	RT	**Ringer Threshold Select.** Used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; Signals above the upper level are guaranteed to generated a ring detection. **0 = 13.5 to 16.5 V_{RMS}** 1 = 19.35 to 23.65 V_{RMS}

SF8 (DAA8). DAA Low Level Functions 8

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LRV[3:0]							
Type	R							

Reset settings vary with line-side revision

Bit	Name	Function
7:4	LRV[3:0]	**Line-Side Device Revision Number.** 1001 = Si3008 Rev B
3:0	Reserved	Do not modify.

SF9 (DAA9). DAA Low Level Functions 9 Read Only

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL	ROV	
Type						R	R/W	

Reset settings = 0010_0000 (0x20)

Bit	Name	Function
7:3	Reserved	Do not modify.
2	OVL	**Receive overload.** Same as ROV, except not sticky.
1	ROV	**Receive Overload (sticky).** **0 = No excessive level detected.** 1 = Excessive input level detected.
0	Reserved	Do not modify.

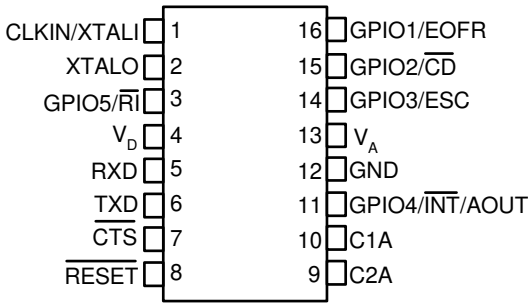
SFC (DAAFC). DAA Low Level Functions

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CTSM							
Type	R/W							

Reset settings = 0000_0000 (0x00)

Bit	Name	Function
7	CTSM	**Clear-to-Send (CTS) Mode.** **0 = $\overline{\text{CTS}}$ pin is negated as soon as a start bit is detected and reasserted when the transmit FIFO is empty.** 1 = $\overline{\text{CTS}}$ pin is negated when the FIFO is $\geq$ 70% full and reasserted when the FIFO is $\leq$ 30% full.
6:0	Reserved	Read returns zero.

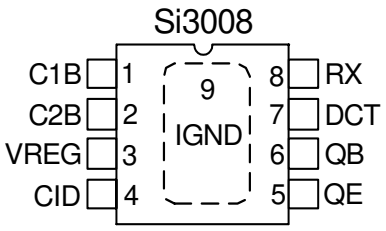
8. Pin Descriptions: Si2401



Pin #	Pin Name	Description
1	CLKIN/XTALI	**XTALI—Crystal Oscillator Pin.** These pins provide support for parallel resonant AT cut crystals. XTALI also acts as an input in the event that an external clock source is used in place of a crystal. A 4.9152 MHz crystal is required or a 4.9152 or 27 MHz clock on XTALI.
2	XTALO	**XTALO—Crystal Oscillator Pin.** Serves as the output of the crystal amplifier.
3	GPI05/$\overline{RI}$	**General Purpose Input/$\overline{RI}$.** This pin can be either a GPIO pin (digital in, digital out) or the $\overline{RI}$ pin. Default is digital in. When programmed as $\overline{RI}$, it indicates the presence of an ON segment of a ring signal on the telephone line.
4	V_D	**Supply Voltage.** Provides the 3.3 V supply voltage to the Si2401.
5	RXD	**Receive Data.** Serial communication data from the Si2401.
6	TXD	**Transmit Data.** Serial communication data to the Si2401.
7	$\overline{CTS}$	**Clear to Send.** Clear to send output used by the Si2401 to signal that the device is ready to receive more digital data on the TXD pin.
8	$\overline{RESET}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si2401 out of sleep mode.
9	C2A	**Isolation Capacitor 2A.** Connects to one side of the isolation capacitor C2.
10	C1A	**Isolation Capacitor 1A.** Connects to one side of the isolation capacitor C1.

Pin #	Pin Name	Description
11	GPIO4/$\overline{\text{INT}}$/ AOUT	**General Purpose Input/$\overline{\text{INT}}$.** This pin can be either a GPIO pin (digital in, digital out) or the $\overline{\text{INT}}$ pin. Default is digital in. When programmed as $\overline{\text{INT}}$, this pin provides five functions. While the modem is connected, it asserts if the carrier is lost, a wake-on ring (using the “ATZ” command) event is detected, a loss of loop current event is detected, V.23 reversal is detected, or if an intrusion event has been detected. The $\overline{\text{INT}}$ pin is sticky and stays asserted until the host clears it by writing to the correct S register. (See register SE2[7:6].)
12	GND	**Ground.** Connects to the system digital ground.
13	V_A	**Regulator Voltage Reference.** This pin connects to an external capacitor and serves as the reference for the internal voltage regulator.
14	GPIO3/ESC	**General Purpose Input/Escape.** This pin can be either a GPIO pin (digital in, digital out) or the ESC pin. Default is digital in. When programmed as ESC, a positive edge on this pin causes the modem to go from online (connected) mode to the offline (command) mode.
15	GPIO2/$\overline{\text{CD}}$	**General Purpose Input/$\overline{\text{CD}}$.** This pin can be either a GPIO pin (digital in, digital out) or the $\overline{\text{CD}}$ pin. Default is digital in. When programmed as $\overline{\text{CD}}$, it is the active low carrier detect pin.
16	GPIO1/EOFR	**General Purpose Input/EOFR.** This pin can be either a GPIO pin (digital in, digital out) or the EOFR pin. Default is digital in. This pin can also be programmed to function as the EOFR (end-of-frame receive) signal for HDLC framing.

9. Pin Descriptions: Si3008



Pin #	Pin Name	Description
1	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1 and communicates with the Si2401.
2	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2 and communicates with the Si2401.
3	VREG	**Voltage regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
4	CID	**Caller ID.** Caller ID input.
5	QE	**Transistor Emitter.** Connects to the emitter of Q3.
6	QB	**Transistor Base.** Connects to the base of transistor Q3. Used to go on- and off-hook.
7	DCT	**DC Termination.** Provides dc termination to the telephone network.
8	RX	**Receive Input.** Serves as the receive side input from the telephone network.
9	IGND	**Isolated Ground (exposed pad).** Connects to ground on the line-side interface.

10. Ordering Guide

Chipset	Description	Power Supply	Digital	Line	Temperature
Si2401	Commercial lead-free	3.3 V	Si2401-FS	Si3008-B-FS	0 to 70 °C

11. Package Outline: 16-Pin SOIC

Figure 6 illustrates the package details for the Si3054 and Si3018. Table 23 lists the values for the dimensions shown in the illustration.

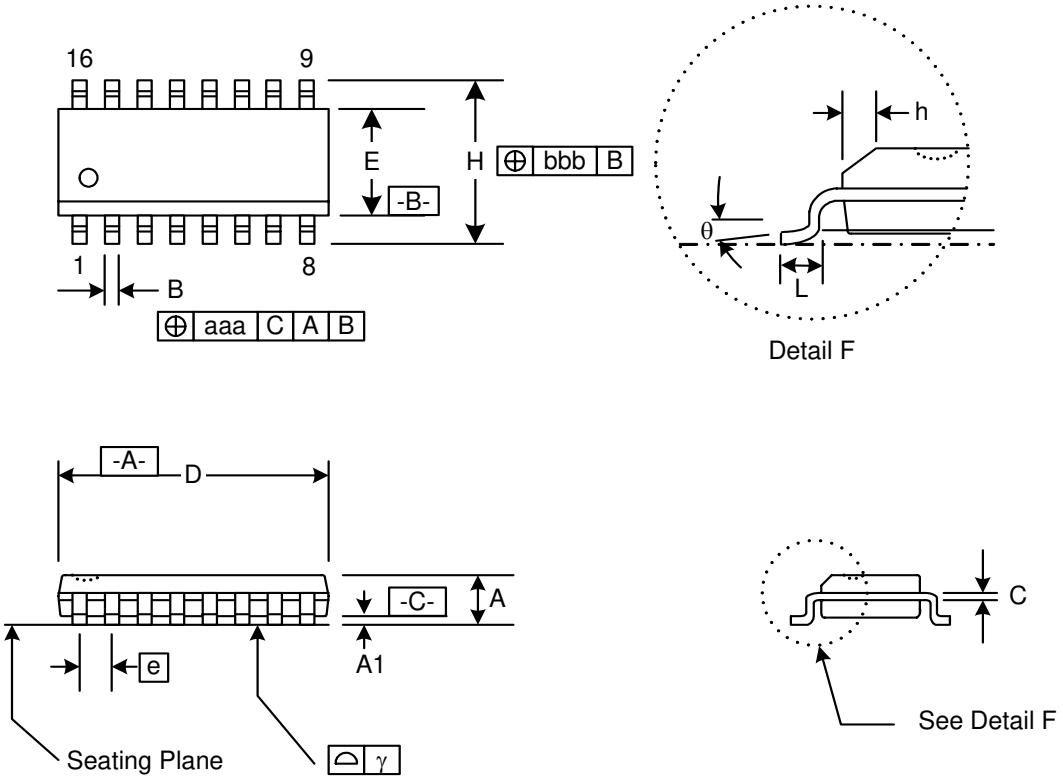


Figure 6. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 23. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
B	.33	.51
C	.19	.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
γ	0.10	
θ	0º	8º
aaa	0.25	
bbb	0.25	

12. Package Outline: 8-Pin Exposed Pad SOIC

Figure 7 illustrates the package details for the Si3008. Table 24 lists the values for the dimensions shown in the illustration.

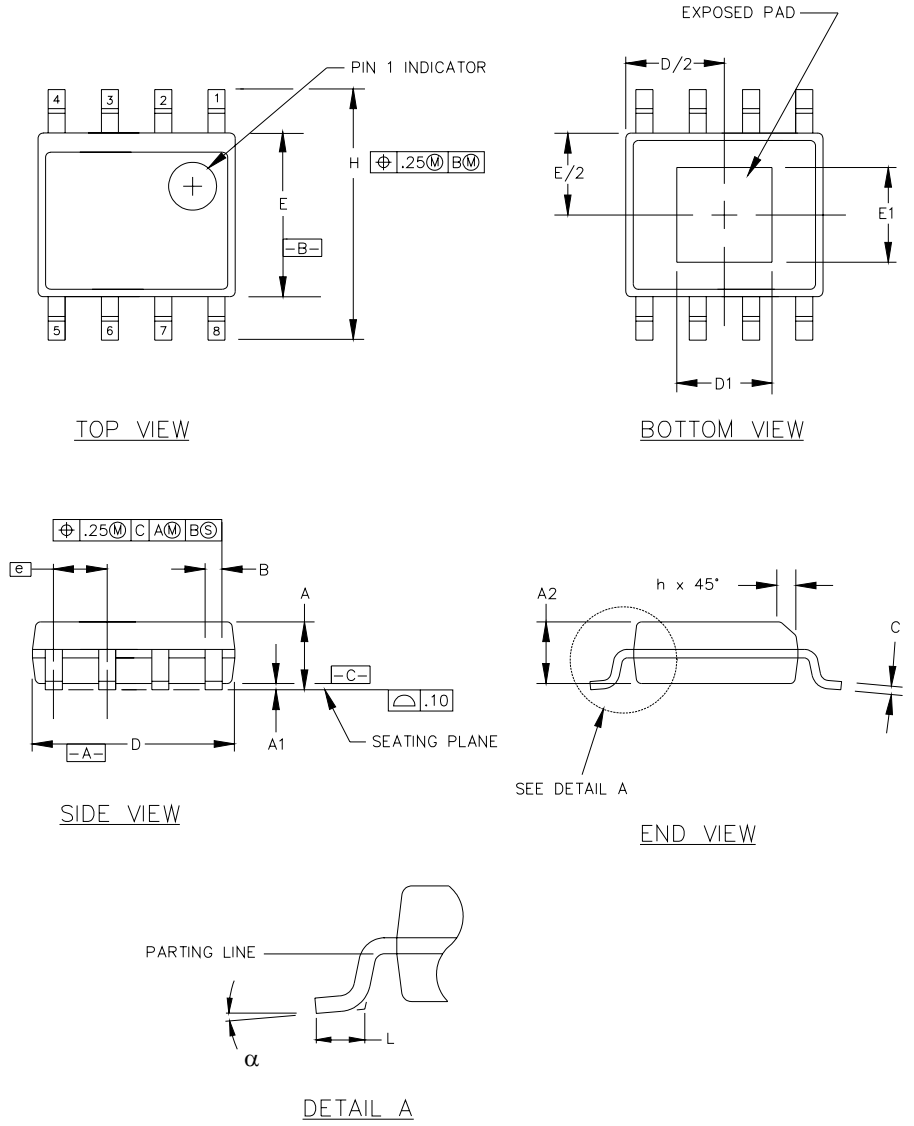


Figure 7. 8-pin Exposed Pad Small Outline Integrated Circuit (SOIC) Package

Table 24. Package Diagram Dimensions

Dimension	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.00	0.15
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
D1	2.14	2.44
E	3.80	4.00
E1	2.14	2.44
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

Notes:
1. All dimensions shown are in millimeters (mm).
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- Updated Table 2, “Loop Characteristics,” on page 4.
- Updated Table 4, “AC Characteristics,” on page 6.
- Updated Table 7, “Country-Specific PTT Specifications,” on page 11.
- Updated "12. Package Outline: 8-Pin Exposed Pad SOIC" on page 68.

Revision 1.0 to Revision 1.1

- Updated Table 7, “Country-Specific PTT Specifications,” on page 11.
  - Removed Brazil listing.

NOTES:

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