SIO1007

LPC Super I/O LPC IrDA Hot Docking Chip with UART

Product Features

- 3.3 Volt Operation (5V tolerant)
- Programmable Wakeup Event Interface (IO_PME# Pin)
- SMI Support (IO_SMI# Pin)
- GPIOs (16)
- Programmable internal pull-up resistors
- Two IRQ Input Pins
- XNOR Chain
- PC99a and ACPI 1.0 Compliant
- 64-Pin STQFP RoHS Compliant Package
- Intelligent Auto Power Management
- One Full Function Serial Port
  - High Speed 16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - Three IR Ports
  - Multi-Protocol Serial Communications Controllers
  - Two IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - One Consumer IR Port with support for NEC PPM and RC5 with PME Wake-up Option
  - Multiple Base I/O Address options, 15 IRQ Options and 3 DMA Options
- LPC Bus Host Interface
  - Supports LPC Bus frequencies of 19.2MHz to 33MHz
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI nCLKRUN Support
  - Power Management Event (IO_PME#) Interface Pin
- LPC PortSwitch™ Interface
  - Secondary Switchable LPC Interface (3.3V only)
  - Trusted cycles blocked
  - Buffered 14 MHz output
  - Switched PCI Clock output

Description

The Microchip SIO1007 is a 3.3V PC 99 and ACPI 1.0 compliant Super I/O Controller. The SIO1007 implements the LPC interface with the LPC PortSwitch Interface. The LPC PortSwitch Interface is a hot-switchable external Docking LPC interface with trusted cycle block. The SIO1007 also features a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI nCLKRUN support, relocatable configuration ports and three DMA channel options. The part also includes 16 GPIO pins.

The SIO1007 incorporates one 8-pin 16C550A compatible UART. In addition, the SIO1007 provides a second UART to support a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats, as well as Consumer IR. There is a second IR port, which supports NEC PPM and RC5, as well as Consumer IR protocols.

The SIO1007 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The SIO1007 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the UARTs.

The SIO1007 supports the ISA Plug-and-Play Standard register set (Version 1.0a) and provides the recommended functionality to support Windows ‘9x, 2K, ME, XP and PC99. The I/O Address, DMA Channel and Hardware IRQ of each device in the SIO1007 may be reprogrammed through the internal configuration registers. There are 192 I/O address location options, a Serialized IRQ interface, and three DMA channels.

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An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

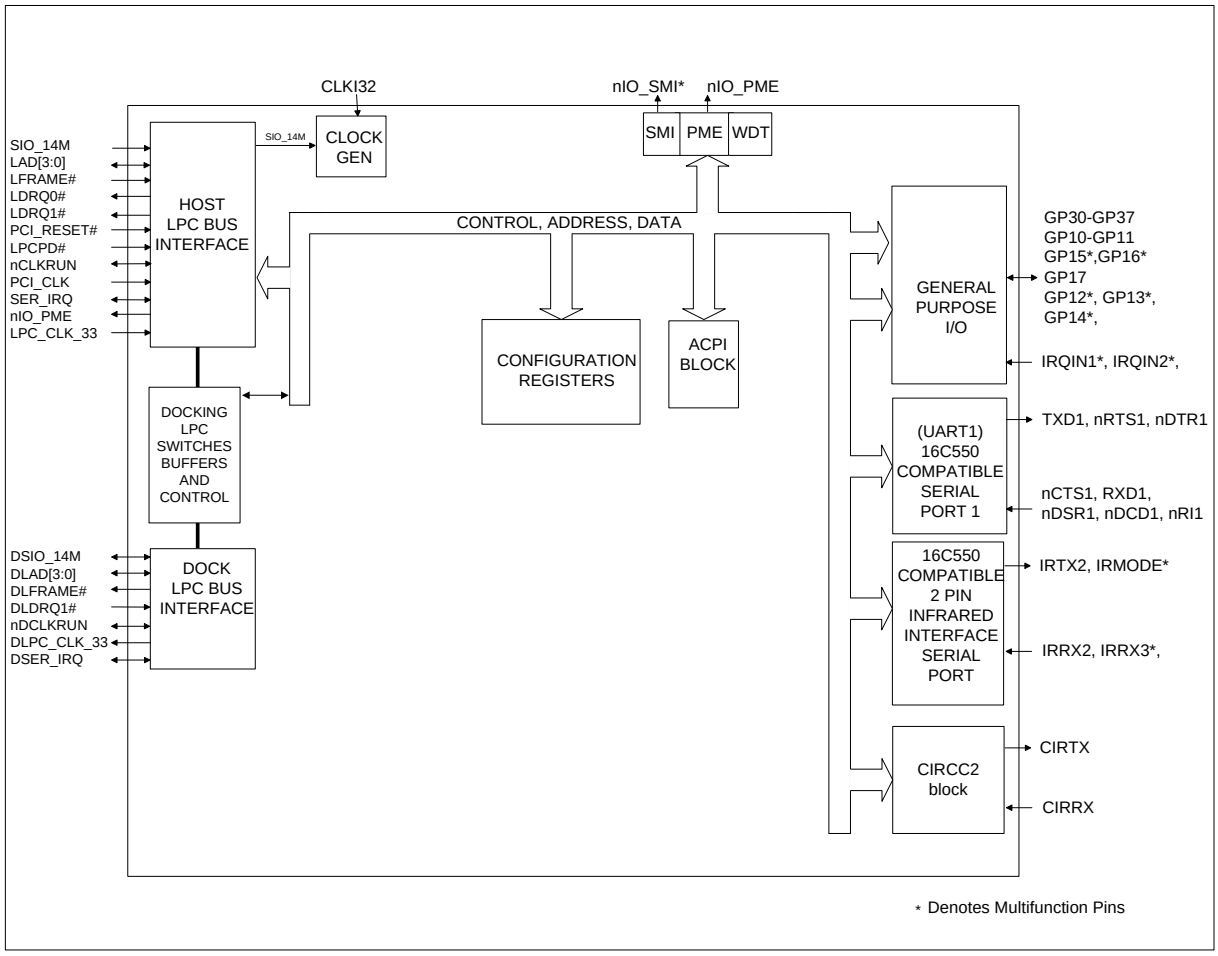
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BLOCK DIAGRAM

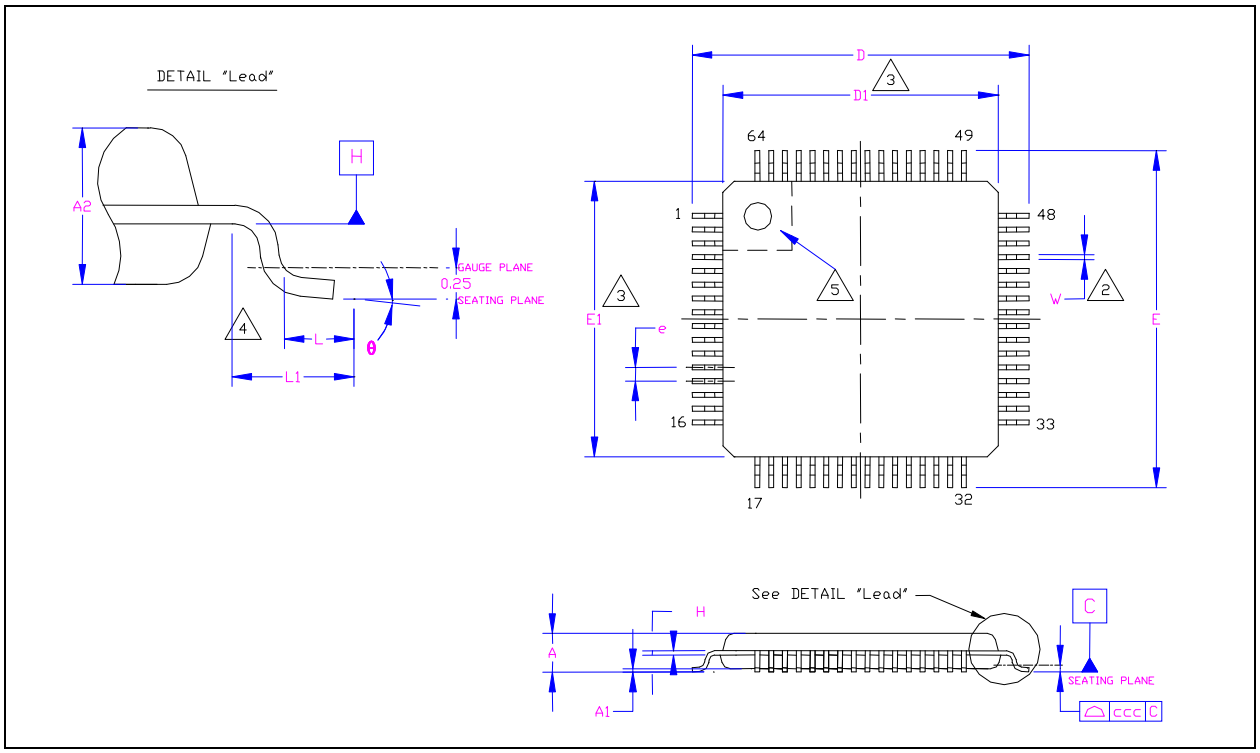
FIGURE 1: SIO1007 BLOCK DIAGRAM



PACKAGE OUTLINE

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging.

FIGURE 2: 64-PIN STQFP PACKAGE



	Min	Nominal	Max	Remarks
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	1.40	1.45	Body Thickness
D	8.80	9.00	9.20	X Span
D1	6.80	7.00	7.20	X body Size
E	8.80	9.00	9.20	Y Span
E1	6.80	7.00	7.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00 REF.	~	Lead Length
e	0.40 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
ccc	~	~	0.08	Coplanarity

Note 1: Controlling Unit: millimeter.

2: Tolerance on the true position of the leads is ± 0.035 mm maximum.

3: Package body dimensions D1 and E1 do not include the mold protrusion.

4: Maximum mold protrusion is 0.25 mm per side. D1 and E1 dimensions determined at datum plane H.

5: Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.

6: Details of pin 1 identifier are optional but must be located within the zone indicated.

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APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001815A (08-25-14)	Replaces previous SMSC version Rev. 0.11 (03-03-05)	

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PART NO.[1]	-	XXX[2]	-	[X][3]
Device		Package		Tape and Reel Option

Device:	SIO1007 [1]		
Package:	JV	=	64-pin STQFP [2]
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel [3]

Example:

SIO1007-JV = 64-pin STQFP

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html .

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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