SL23EP04

Not Recommended for New Designs

Low Jitter and Skew 10 to 220 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 220 MHz operating frequency range
- Low output clock skew: 60ps-typ
- Low output clock Jitter:
- Low part-to-part output skew: 150 ps-typ
- 3.3V to 2.5V power supply range
- Low power dissipation:
  - 12 mA-typ at 66MHz and VDD=3.3V
  - 10 mA-typ at 66MHz and VDD=2.5V
- One input drives 4 outputs
- Multiple configurations and drive options
- SpreadThru™ PLL that allows use of SSCG
- Available in 8-pin SOIC package
- Available in Commercial and Industrial grades

Applications

- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Datacom and Telecom
- High-Speed Digital Embeded Systems

Description

The SL23EP04 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to four (4) clock outputs from one (1) reference input clock, for high speed clock distribution applications.

The product has an on-chip PLL and a feedback pin (FBK) which can be used to obtain feedback from any one of the 4 output clocks. The SL23EP04 offers X/2,1X and 2X frequency options at the output with respect to input reference clock. Refer to the “Product Configuration Table” for the details of these options.

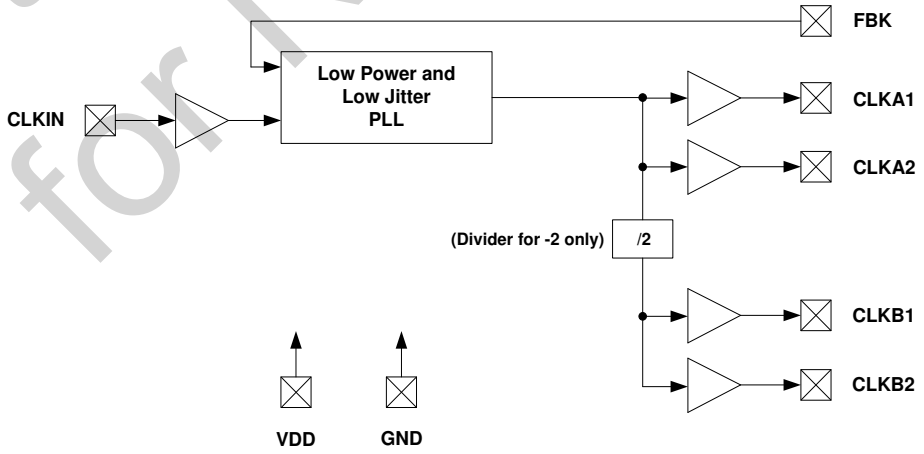
The SL23EP04-1H and -2H High Drive version operates up to 220 MHz and 200MHz at 3.3 and 2.5V power supplies respectively. The standard versions -1 and -2 operate up to 167MHz and 135MHz at 3.3V and 2.5V power supplies respectively with CL=15pF output load.

The SL23EP04 enter into Power Down (PD) mode if the input at CLKIN is DC (GND to VDD). In this state all 4 output clocks are tri-stated and the PLL is turned off, leading to 8µA-typ power supply current draw.

Benefits

- Up to four (4) distribution of input clock
- Standard and High-Drive levels to control impedance level, frequency range and EMI
- Low skew, jitter and power dissipation

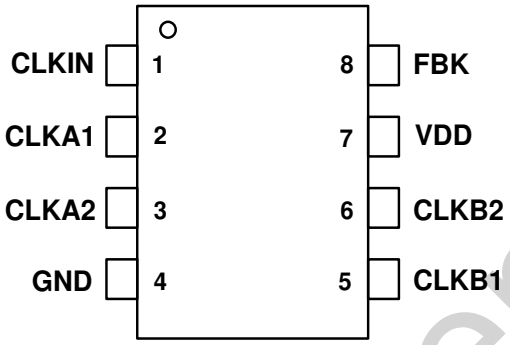
Block Diagram



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Pin Configuration



8-Pin SOIC

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Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (250kΩ).
2	CLKA1	Output	Buffered Clock Output Weak pull-down (250kΩ).
3	CLKA2	Output	Buffered Clock Output. Weak pull-down (250kΩ).
4	GND	Power	Power Ground.
5	CLKB1	Output	Buffered Clock Output. Weak pull-down (250kΩ).
6	CLKB2	Output	Buffered Clock Output. Weak pull-down (250kΩ).
7	VDD	Power	2.5V to 3.3V Power Supply.
8	FBK	Input	PLL Feedback Input. This pin must be connected to one of the clock outputs.

General Description

The SL23EP04 is a low skew, low jitter Zero Delay Buffer with very low operating current.

The product includes an on-chip high performance PLL that locks into the input reference clock and produces four (4) output clock drivers tracking the input reference clock for systems requiring clock distribution.

in addition to FBK pin used for internal PLL feedback, there are two (2) banks with two (2) outputs in each bank, bringing the number of total available output clocks to four (4).

Input and output Frequency Range

The input and output frequency is the same (1x) for SL23EP04-1 and -1H versions. For SL23EP04-2 and -2H versions, the output frequency is 1/2x, 1x or 2x of the CLKIN as given in the "Available SL23EP04 Configurations" Table 1. But, the frequency range depends on VDD, drive levels and CL (Load Capacitance) as given in the electrical specifications tables.

When the input clock frequency is DC (from GND to VDD), this input state is detected by an input level detection circuitry and all four (4) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 12 µA (8 µA –typ) supply current.

SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL23EP04 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its reference CLKIN input to the output clocks. The same spread spectrum characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency.

High and Low-Drive Product Options

All SL23EP04 products are offered with the high drive "-1H" and "-2H" as well as the standard drive "-1" and "-2" options. These drive options enable the user to control load levels, frequency range and EMI levels. Refer to the electrical tables for the details of the drive levels.

Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output skew and input-to-output delay specifications as given in the switching electrical tables. However, the delay between input and outputs can be adjusted by changing the load at FBK pin relative to the banks A and B clocks since FBK pin is the feedback to the internal PLL.

In addition, the input reference clock rise and fall time should be similar to the output rise and fall time to obtain the best skew results.

Power Supply Range (VDD)

The SL23EP04 is designed to operate from 3.3V (3.63V-max) to 2.5V (2.25V-min) VDD power supply range. An internal on-chip voltage regulator is used to provide to PLL constant power supply of 1.8V internally. This leads to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation. The SL23EP04 I/O is powered by using VDD.

Contact SLI for 1.8V power supply ZDB called SL23EPL04.

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Device	Feedback From	Bank-A Frequency	Bank-B Frequency
SL23EP04-1 and 1H	Bank-A or Bank-B	Reference	Reference
SL23EP04-2 and -2H	Bank-A	Reference	Reference / 2
SL23EP04-2 and -2H	Bank-B	2 x Reference	Reference

Table 1. Available SL23EP04 Configurations

Absolute Maximum Ratings (All Products)

Description	Condition	Min	Max	Unit
Supply voltage, VDD		-0.5	4.6	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	-	125	°C
Soldering Temperature		-	260	°C
ESD Rating (Human Body Model)	JEDECCC22-A114D	-4000	4000	V
ESD Rating (Change Device Model)	JEDECCC22-C101C	-1500	1500	V
ESD Rating (Machine Model)	JEDECCC22-A115D	-200	200	V

Operating Conditions (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Operating Temperature	TA	Ambient Temperature	0	-	70	°C
Input Capacitance	VIH	Pins 1 and 8	-	5	7	pF
Output Impedance	R_{OUT-1}	High Drive (-1H and -2H)	-	28	-	Ω
Output Impedance	R_{OUT-2}	Standard Drive (-1 and -2)	-	40	-	Ω

DC Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input LOW Voltage	VINL	Pins 1 and 8	–	–	0.8	V
Input HIGH Voltage	VINH	Pins 1 and 8	2.0	–	VDD+0.3	V
Input LOW Current	IINL	0 < VIN < 0.8V, Pins 1 and 8	–	20	50	µA
Input HIGH Current	IINH	2.4V < VIN < VDD Pins 1 and 8	–	20	50	µA
Output LOW Voltage	VOL	IOL = 8 mA (-1, -2 drives)	–	–	0.4	V
		IOL = 12 mA (-1H, -2H drives)	–	–	0.4	V

Not Recommended for New Designs

DC Electrical Characteristics (C-Grade and VDD=3.3V – Cont.)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output HIGH Voltage	VOH	IOH = –8 mA (-1, -2 drives)	2.4	–	–	V
		IOH = –12 mA (-1H, -2H drives)	2.4	–	–	V
Power Down Supply Current	IDDPD	Measured when CLKIN= GND to VDD or floating	–	8	12	µA
Power Supply Current	IDD1	All Outputs CL=0, 33.3 MHz CLKIN All versions	–	10	14	mA
Power Supply Current	IDD2	All Outputs CL=0, 66.6 MHz CLKIN All versions	–	12	17	mA
Power Supply Current	IDD3	All Outputs CL=0, 133.3 MHz CLKIN All versions	–	14	20	mA
Power Supply Current	IDD4	All Outputs CL=0, 166.6 MHz CLKIN All versions	–	16	23	mA
Pull-down Resistors	RPD	Pin-1, 2, 3, 5, and 6	150	250	350	kΩ

Switching Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pf, -1H and -2H versions	10	-	220	MHz
	FOUT2	CL=22pf, -1H and -2H versions	10	-	180	MHz
	FOUT3	CL=30pf, -1H and -2H versions	10	-	135	MHz
	FOUT4	CL=15pf, -1, and -2 versions	10	-	180	MHz
	FOUT5	CL=22pf, -1 and -2 versions	10	-	135	MHz
	FOUT6	CL=30pf, -1 and -2 versions	10	-	100	MHz
Input Duty Cycle	DC1	Measured at VDD/2, all versions	30	50	70	%
Output Duty Cycle	DC2	CL=30pF, Fout=66 MHz, all versions Measured at 1.4V	40	50	60	%
Output Duty Cycle	DC3	CL=15pF, Fout=66 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC4	CL=15pF, Fout=133 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC5	CL=15pF, Fout=166 MHz, all versions Measured at VDD/2	45	50	55	%
Output Rise/Fall Time	tr/f1	CL=30pF, -1 and -2 versions, measured from 0.8V to 2.0V	-	-	2.2	ns
Output Rise/Fall Time	tr/f2	CL=15pF, -1 and -2 versions, measured from 0.8V to 2.0V	-	-	1.5	ns

Not Recommended for New Designs

Switching Electrical Characteristics (C-Grade and VDD=3.3V – Cont.)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Output Rise/Fall Time	tr/f3	CL=30pF -1H and -2H version, measured from 0.8V to 2.0V	-	-	1.5	ns
Output Rise/Fall Time	tr/f4	CL=15pF -1H and -2H version, measured from 0.8V to 2.0V	-	-	1.2	ns
Output-to-Output Skew on Same Bank	SKW1	-1 and -2 measured at VDD/2 and outputs are equally loaded	-	70	150	ps
Output-to-Output Skew on Same Bank	SKW2	-1H and -2H measured at VDD/2 and outputs are equally loaded	-	60	125	ps
Output-to-Output Skew Between Bank A and B	SKW3	-1 and -2 measured at VDD/2 and outputs are equally loaded	-	110	250	ps
Output-to-Output Skew Between Bank A and B	SKW4	-1H and -2H measured at VDD/2 and outputs are equally loaded	-	90	200	ps
Device-to-Device Skew	SKW5	All versions, measured at VDD/2 and outputs are equally loaded	-	150	400	ps
Input-to-Output Delay	Dt	All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded	-200	+/-70	200	ps
Cycle-to-Cycle Jitter (-1 and, -1H Versions)	CCJ1	Fout=66.6 MHz and CL=15pF	-	-	100	ps
		Fout=133.3MHz and CL=15PF	-	-	100	ps
		Fout=66.6MHz and CL=30pF	-	-	100	ps
Cycle-to-Cycle Jitter (-2 and -2H Versions)	CCJ2	Fout=66.6 MHz and CL=15pF	-	-	400	ps
		Fout=166.6MHz and CL=15pF	-	-	400	ps
		Fout=66.6 MHz and CL=30pF	-	-	400	ps
PLL Lock Time	tLOCK	From 0.95VDD and valid clock presented at CLKIN	-	-	1.0	ms

Operating Conditions (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.97	3.3	3.63	V
Operating Temperature	TA	Ambient Temperature	-40	-	85	°C
Input Capacitance	VIH	Pins 1 and 8	-	5	8	pF
Output Impedance	R_{OUT-1}	High Drive (-1H and -2H)	-	28	-	Ω
Output Impedance	R_{OUT-2}	Standard Drive (-1 and -2)	-	40	-	Ω

Not Recommended for New Designs

DC Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°

Description	Symbol	Condition	Min	Typ	Max	Unit
Input LOW Voltage	VINL	Pins 1 and 8	–	–	0.8	V
Input HIGH Voltage	VINH	Pins 1 and 8	2.0	–	VDD+0.3	V
Input LOW Current	IINL	0 < VIN < 0.8V, Pins 1 and 8	–	20	50	µA
Input HIGH Current	IINH	2.4V < VIN < VDD Pins 1 and 8	–	20	50	µA
Output LOW Voltage	VOL	IOL = 8 mA (-1, -2 drives)	–	–	0.4	V
		IOL = 12 mA (-1H, -2H drives)	–	–	0.4	V
Output HIGH Voltage	VOH	IOH = –8 mA (-1, -2 drives)	2.4	–	–	V
		IOH = –12 mA (-1H, -2H drives)	2.4	–	–	V
Power Down Supply Current	IDDPD	Measured when CLKIN= GND to VDD or floating	–	12	18	µA
Power Supply Current	IDD1	All Outputs CL=0, 33.3 MHz CLKIN All versions	–	12	17	mA
Power Supply Current	IDD2	All Outputs CL=0, 66.6 MHz CLKIN All versions	–	14	20	mA
Power Supply Current	IDD3	All Outputs CL=0, 133.3 MHz CLKIN All versions	–	16	22	mA
Power Supply Current	IDD4	All Outputs CL=0, 166.6 MHz CLKIN All versions	–	18	25	mA
Pull-down Resistors	RPD	Pin-1, 2, 3, 5 and 6	125	250	375	kΩ

Switching Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pf, -1H and -2H versions	10	-	220	MHz
	FOUT2	CL=22pf, -1H and -2H versions	10	-	180	MHz
	FOUT3	CL=30pf, -1H and -2H versions	10	-	135	MHz
	FOUT4	CL=15pf, -1, and -2 versions	10	-	180	MHz
	FOUT5	CL=22pf, -1 and -2 versions	10	-	135	MHz
	FOUT6	CL=30pf, -1 and -2 versions	10	-	100	MHz
Input Duty Cycle	DC1	Measured at VDD/2	30	50	70	%
Output Duty Cycle	DC2	CL=30pF, Fout=66 MHz, all versions Measured at 1.4V	40	50	60	%

Not Recommended for New Designs

Switching Electrical Characteristics (I-Grade and VDD=3.3V – Cont.)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Output Duty Cycle	DC3	CL=15pF, Fout=66 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC4	CL=15pF, Fout=133 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC5	CL=15pF, Fout=166 MHz, all versions Measured at VDD/2	45	50	55	%
Output Rise/Fall Time	tr/f1	CL=30pF, -1 and -2 versions, measured from 0.8V to 2.0V	-	-	2.2	ns
Output Rise/Fall Time	tr/f2	CL=15pF, -1 and -2 versions, measured from 0.8V to 2.0V	-	-	1.5	ns
Output Rise/Fall Time	tr/f3	CL=30pF -1H and -2H version, measured from 0.8V to 2.0V	-	-	1.5	ns
Output Rise/Fall Time	tr/f4	CL=15pF -1H and -2H version, measured from 0.8V to 2.0V	-	-	1.2	ns
Output-to-Output Skew on Same Bank	SKW1	-1 and -2 measured at VDD/2 and outputs are equally loaded	-	70	150	ps
Output-to-Output Skew on Same Bank	SKW2	-1H and -2H measured at VDD/2 and outputs are equally loaded	-	60	125	ps
Output-to-Output Skew Between Bank A and B	SKW3	-1 and -2 measured at VDD/2 and outputs are equally loaded	-	110	250	ps
Output-to-Output Skew Between Bank A and B	SKW4	-1H and -2H measured at VDD/2 and outputs are equally loaded	-	90	200	ps
Device-to-Device Skew	SKW5	All versions, measured at VDD/2 and outputs are equally loaded	-	150	400	ps
Input-to-Output Delay	Dt	All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded	-200	+/-70	200	ps
Cycle-to-Cycle Jitter (-1 and, -1H Versions)	CCJ1	Fout=66.6 MHz and CL=15pF	-	-	100	ps
		Fout=133.3MHz and CL=15pF	-	-	100	ps
		Fout=66.6 MHz and CL=30pF	-	-	100	ps

Not Recommended for New Designs

Switching Electrical Characteristics (I-Grade and VDD=3.3V – Cont.)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Cycle-to-Cycle Jitter (-1H and -2H Versions)	CCJ2	Fout=66.6 MHz and CL=15pF	-	-	400	ps
		Fout=166.6MHz and CL=15pF	-	-	400	ps
		Fout=66.6 MHz and CL=30pF	-	-	400	ps
PLL Lock Time	tLOCK	From 0.95VDD and valid clock presented at CLKIN	-	-	1.0	ms

Operating Conditions (C-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Operating Temperature	TA	Ambient Temperature	-40	-	85	°C
Input Capacitance	VIH	Pins 1 and 8	-	5	8	pF
Output Impedance	ROUT-1	High Drive (-1H and -2H)	-	36	-	Ω
Output Impedance	ROUT-2	Standard Drive (-1 and -2)	-	42	-	Ω

DC Electrical Characteristics (C-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input LOW Voltage	VINL	Pins 1 and 8	–	–	0.7	V
Input HIGH Voltage	VINH	Pins 1 and 8	1.7	–	VDD+0.3	V
Input LOW Current	IINL	0 < VIN < 0.8V, pins 1 and 8	–	20	50	µA
Input HIGH Current	IINH	2.4V < VIN < VDD, pins 1 and 8	–	20	50	µA
Output LOW Voltage	VOL	IOL = 6 mA, -1 and -2	–	–	0.3	V
		IOL = 8 mA, -1H and -2H	–	–	0.3	V
Output HIGH Voltage	VOH	IOH = –6 mA, -1 and -2	2.0	–	–	V
		IOH = –8 mA, -1H and -2H	2.0	–	–	V
Power Down Supply Current	IDDPD	Measured when CLKIN= GND to VDD	–	10	18	µA
Power Supply Current	IDD1	All Outputs CL=0, 33.3 MHz CLKIN	–	8	11	mA
Power Supply Current	IDD2	All Outputs CL=0, 66.6 MHz CLKIN, all versions	–	10	14	mA
Power Supply Current	IDD3	All Outputs CL=0, 133.3 MHz CLKIN, all versions	–	12	17	mA
Power Supply Current	IDD4	All Outputs CL=0, 166.6 MHz CLKIN, all versions	–	14	20	mA
Pull-down Resistors	RPD	Pin-1, 2, 3, 5 and 6	150	250	350	kΩ

Not Recommended for New Designs

Switching Electrical Characteristics (C-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pf, -1H and -2H versions	10	-	170	MHz
	FOUT2	CL=22pf, -1H and -2H versions	10	-	135	MHz
	FOUT1	CL=30pf, -1H and -2H versions	10	-	100	MHz
	FOUT4	CL=15pf, -1 and -2 versions	10	-	135	MHz
	FOUT5	CL=22pf, -1 and -2 versions	10	-	100	MHz
	FOUT6	CL=30pf, -1 and -2 versions	10	-	75	MHz
Input Duty Cycle	DC1	Measured at VDD/2, all versions	40	50	60	%
Output Duty Cycle	DC2	CL=15pF, Fout=66 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC3	CL=15pF, Fout=133 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC4	CL=15pF, Fout=166 MHz, all versions Measured at VDD/2	40	50	60	%
Output Rise/Fall Time	tr/f1	CL=30pF, -1 and -2 versions Measured at 0.6 to 1.8V	-	-	3.0	ns
Output Rise/Fall Time	tr/f2	CL=15pF, -1 and -2 versions Measured at 0.6 to 1.8V	-	-	2.0	ns
Output Rise/Fall Time	tr/f3	CL=30pF, -1H and -2H versions Measured at 0.6 to 1.8V	-	-	2.0	ns
Output Rise/Fall Time	tr/f4	CL=15pF, -1H and -2H versions Measured at 0.6 to 1.8V	-	-	1.4	ns
Output-to-Output Skew on Same Bank	SKW1	-1 and -2, measured at VDD/2 and outputs are equally loaded	-	80	175	ps
Output-to-Output Skew on Same Bank	SKW2	-1H and -2H, measured at VDD/2 and outputs are equally loaded	-	70	150	ps
Output-to-Output Skew Between Bank A and B	SKW3	-1 and -2, measured at VDD/2 and outputs are equally loaded	-	125	300	ps
Output-to-Output Skew Between Bank A and B	SKW4	-1H and -2H, measured at VDD/2 and outputs are equally loaded	-	110	250	ps
Device-to-Device Skew	SKW5	All versions, measured at VDD/2 and outputs are equally loaded	-	175	450	ps
Input-to-Output Delay	Dt	All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded	-250	+/-90	250	ps
Cycle-to-Cycle Jitter (-1 and -1H Versions)	CCJ1	Fout=66.6 MHz and CL=15pF	-	-	150	ps
		Fout=133.3 MHz and CL=15pF	-	-	150	ps

Not Recommended for New Designs

Switching Electrical Characteristics (C-Grade and VDD=2.5V-Cont.)

Unless otherwise stated VDD= 2.5+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Cycle-to-Cycle Jitter (-1H and -2H Versions)	CCJ2	Fout=66.6 MHz and CL=15pF	-	-	400	ps
		Fout=166.6 MHz and CL=15pF	-	-	400	ps
PLL Lock Time	tLOCK	From 0.95VDD and valid clock presented at CLKIN	-	-	1.0	ms

Operating Conditions (I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Operating Temperature	TA	Ambient Temperature	-40	-	85	°C
Input Capacitance	VIH	Pins 1 and 8	-	5	8	pF
Output Impedance	ROUT-1	High Drive (-1H and -2H)	-	36	-	Ω
Output Impedance	ROUT-2	Standard Drive (-1 and -2)	-	42	-	Ω

DC Electrical Characteristics (I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°

Description	Symbol	Condition	Min	Typ	Max	Unit
Input LOW Voltage	VINL	Pins 1 and 8	–	–	0.7	V
Input HIGH Voltage	VINH	Pins 1 and 8	1.7	–	VDD+0.3	V
Input LOW Current	IINL	0 < VIN < 0.8V, pins 1 and 8	–	30	60	µA
Input HIGH Current	IINH	2.4V < VIN < VDD, pins 1 and 8	–	30	60	µA
Output LOW Voltage	VOL	IOL = 6 mA, -1 and -2 versions	–	–	0.3	V
		IOL = 8 mA, -1H and -2H versions	–	–	0.3	V
Output HIGH Voltage	VOH	IOH = –6 mA, -1 and -2 versions	2.0	–	–	V
		IOH = –8 mA, -1H and -2H versions	2.0	–	–	V
Power Down Supply Current	IDDPD	Measured when CLKIN= GND to VDD or floating	–	15	25	µA
Power Supply Current	IDD1	All Outputs CL=0, 33.3 MHz CLKIN All versions	–	10	14	mA
Power Supply Current	IDD2	All Outputs CL=0, 66.6 MHz CLKIN All versions	–	12	17	mA
Power Supply Current	IDD3	All Outputs CL=0, 133.3 MHz CLKIN All versions	–	14	20	mA
Power Supply Current	IDD4	All Outputs CL=0, 133.3 MHz CLKIN All versions	–	16	24	mA
Pull-down Resistors	RPUD	Pin-1, 2, 3, 5 and 6	125	250	375	kΩ

Not Recommended for New Designs

Switching Electrical Characteristics (I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pf, -1H and -2H versions	10	-	170	MHz
	FOUT2	CL=22pf, -1H and -2H versions	10	-	135	MHz
	FOU3	CL=30pF, -1H and -2H versions	10	-	100	MHz
	FOUT4	CL=15pf, -1 and -2 versions	10	-	135	MHz
	FOUT5	CL=22pf, -1 and -2 versions	10	-	100	MHz
	FOUT6	CL=30pf, -1 and -2 versions	10	-	75	MHz
Input Duty Cycle	DC1	Measured at VDD/2, all versions	40	50	60	%
Output Duty Cycle	DC2	CL=30pF, Fout=66 MHz, all versions Measured at VDD/2	40	50	60	%
Output Duty Cycle	DC3	CL=15pF, Fout=66 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC4	CL=15pF, Fout=133 MHz, all versions Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC5	CL=15pF, Fout=166 MHz, all versions Measured at VDD/2	40	50	60	%
Output Rise/Fall Time	tr/f1	CL=30pF, -1 and -2 versions Measured at 0.6 to 1.8V	-	-	3.2	ns
Output Rise/Fall Time	tr/f2	CL=15pF, -1 and -2 versions Measured at 0.6 to 1.8V	-	-	2.0	ns
Output Rise/Fall Time	tr/f3	CL=30pF, -1H and -2H versions Measured at 0.6 to 1.8V	-	-	2.0	ns
Output Rise/Fall Time	tr/f4	CL=15pF, -1H and -2H version Measured at 0.6 to 1.8V	-	-	1.5	ns
Output-to-Output Skew on Same Bank	SKW1	-1 and -2, measured at VDD/2, and outputs are equally loaded	-	100	220	ps
Output-to-Output Skew on Same Bank	SKW2	-1H and -2H, measured at VDD/2 and outputs are equally loaded	-	100	220	ps
Output-to-Output Skew Between Bank A and B	SKW3	-1 and -2, measured at VDD/2, and outputs are equally loaded	-	100	220	ps
Output-to-Output Skew Between Bank A and B	SKW4	-1H and -2H, measured at VDD/2 and outputs are equally loaded	-	180	375	ps
Device-to-Device Skew	SKW5	All versions, measured at VDD/2 and outputs are equally loaded	-	225	550	ps
Input-to-Output Delay	Dt	All versions, CLKIN to FBK rising edge, measured at VDD/2 and outputs are equally loaded	-300	+/-125	300	ps

Not Recommended for New Designs

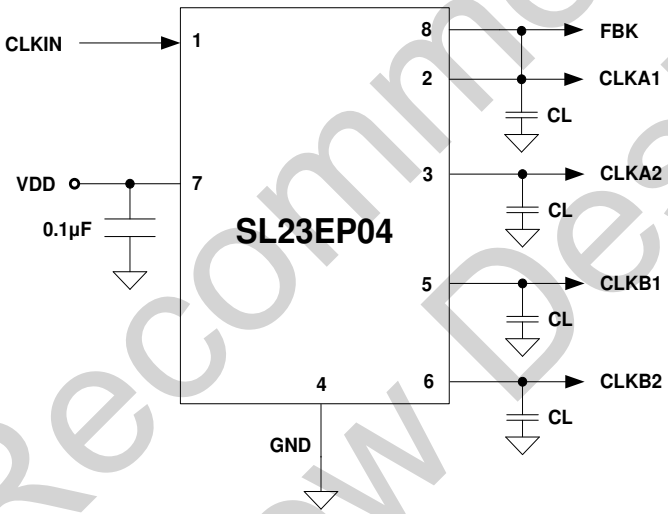
Switching Electrical Characteristics (I-Grade and VDD=2.5V – Cont.)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Cycle-to-Cycle Jitter (-1 and -2 Versions)	CCJ1	Fout=66.6 MHz and CL=15pF	-	-	150	ps
		Fout=133.3 MHz and CL=15pF	-	-	150	ps
Cycle-to-Cycle Jitter (-1H and -2H Versions)	CCJ2	Fout=66.6 MHz and CL=15pF	-	-	400	ps
		Fout=166.6 MHz and CL=15pF	-	-	400	ps
PLL Lock Time	tLOCK	From 0.95VDD and valid CLKIN	-	-	1.0	ms

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

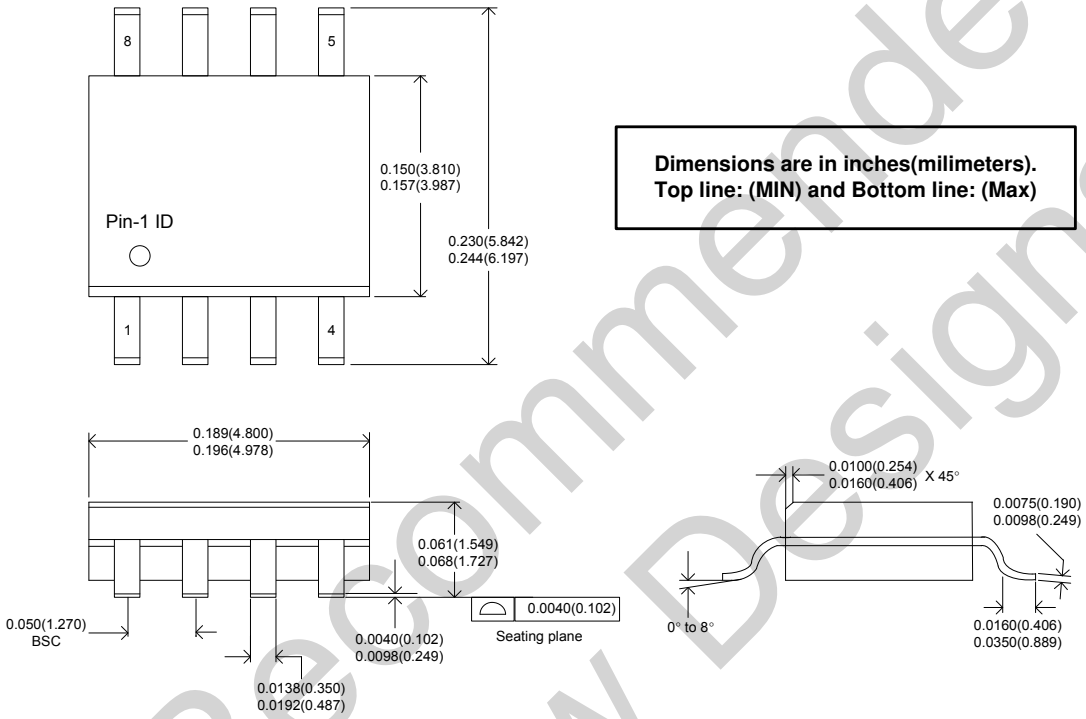
Series Termination Resistor: A series termination resistor is recommended if the distance between the output clocks and the load is over 1 ½ inch. The nominal impedance of the clock outputs is given in the Operating Condition Tables. Place the series termination resistors as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve "Zero Delay" between the CLKIN and the outputs. The FBK pin is connected to PLL internally on-chip for feedback and should be connected to one of to output clocks externally. For applications requiring zero input/output delay, the load at the all output pins including the FBK pin must be the same. If any delay adjustment is required, the capacitance at the FBK pin could be increased or decreased to increase or decrease the delay between Bank A and B clocks relative to CLKIN. For minimum pin-to-pin skew, the external load at all the Bank A and B clocks must be the same. In addition, the rise and fall time of the reference clock at CLKIN pin should be similar to rise and fall times at the CLKA and CLK B bank outputs.

Not Recommended for New Designs

Package Outline and Package Dimensions

8-Pin SOIC (150 Mil)



Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	157	-	°C/W
	θ JA	1m/s air flow	-	142	-	°C/W
	θ JA	3m/s air flow	-	131	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	42	-	°C/W

Not Recommended for New Designs

Ordering Information [3]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL23EP04SC-1	SL23EP04SC-1	Tube	8-pin SOIC	0 to 70°C
SL23EP04SC-1T	SL23EP04SC-1	Tape and Reel	8-pin SOIC	0 to 70°C
SL23EP04SI-1	SL23EP04SI-1	Tube	8-pin SOIC	-40 to 85°C
SL23EP04SI-1T	SL23EP04SI-1	Tape and Reel	8-pin SOIC	-40 to 85°C
SL23EP04SC-1H	SL23EP04SC-1H	Tube	8-pin SOIC	0 to 70°C
SL23EP04SC-1HT	SL23EP04SC-1H	Tape and Reel	8-pin SOIC	0 to 70°C
SL23EP04SI-1H	SL23EP04SI-1H	Tube	8-pin SOIC	-40 to 85°C
SL23EP04SI-1HT	SL23EP04SI-1H	Tape and Reel	8-pin SOIC	-40 to 85°C
SL23EP04SC-2	SL23EP04SC-2	Tube	8-pin SOIC	0 to 70°C
SL23EP04SC-2T	SL23EP04SC-2	Tape and Reel	8-pin SOIC	0 to 70°C
SL23EP04SI-2	SL23EP04SI-2	Tube	8-pin SOIC	-40 to 85°C
SL23EP04SI-2T	SL23EP04SI-2	Tape and Reel	8-pin SOIC	-40 to 85°C
SL23EP04SC-2H	SL23EP04SC-2H	Tube	8-pin SOIC	0 to 70°C
SL23EP04SC-2HT	SL23EP04SC-2H	Tape and Reel	8-pin SOIC	0 to 70°C
SL23EP04SI-2H	SL23EP04SI-2H	Tube	8-pin SOIC	-40 to 85°C
SL23EP04SI-2HT	SL23EP04SI-2H	Tape and Reel	8-pin SOIC	-40 to 85°C

Notes:

1. The SL23EP04 products are RoHS compliant.

Not Recommended for New Designs



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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