SL23EP04NZ

Low Jitter and Skew DC to 220 MHz Clock Buffer

Key Features

- DC to 220 MHz operating frequency range
- Low output clock skew: 60ps-typ
- Low part-to-part output skew: 80 ps-typ
- 3.3V to 2.5V operation supply voltage range
- Low power dissipation:
  - 10 mA-typ at 66MHz at VDD=3.3V
  - 9 mA-typ at 66MHz at VDD=2.5V
- One input to four output fanout buffer drivers
- Output Enable (OE) control function
- Available in 8-pin TSSOP package
- Available in Commercial and Industrial grades
- Available in Lead (Pb) free package

Applications

- General Purpose PCI/PCI-X Clock Buffer
- Printers, MFPs and Digital Copiers
- PCs and Work Stations
- Routers, Switchers and Servers
- Datacom and Telecom
- High-Speed Digital Embeded Systems

Description

The SL23EP04NZ is a low skew, jitter and power fanout buffer designed to produce up to four (4) clock outputs from one (1) reference input clock, for high speed clock distribution, including PCI/PCI-X applications.

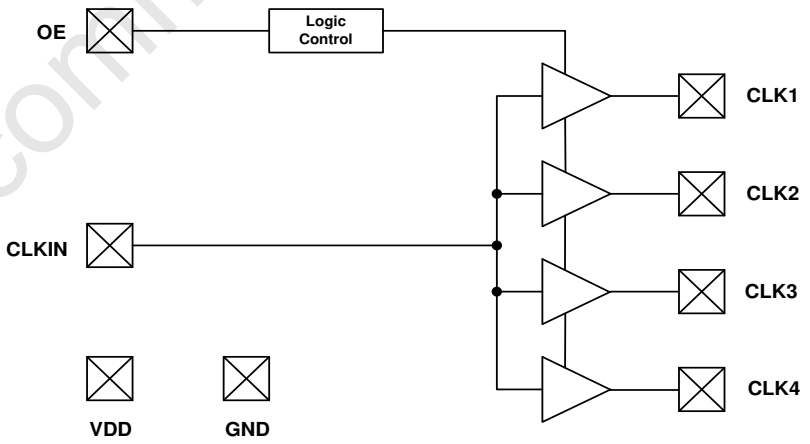
The SL23EP04NZ products operate from DC to 220MHz.

The only difference between SL23EP04-1 and SL23EP04NZ-1Z is the OE logic implementation. Refer to the Available OE Logic Configuration Table. 1

Benefits

- Up to four (4) distribution of input clock
- Low propagation delay
- Low output-to-output skew
- Low output jitter
- Low power dissipation

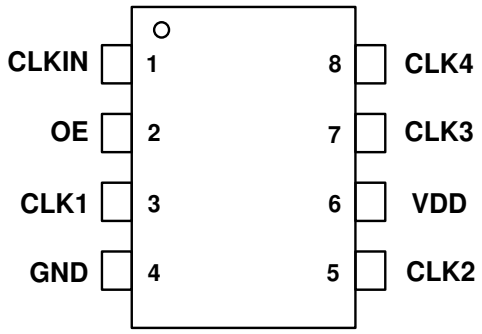
Block Diagram



Not Recommended for New Design

2400 West Cesar Chavez, Austin, TX 78701 1+(512) 416-8500 1+(512) 416-9669 www.silabs.com

Pin Configuration



8-Pin TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Clock Input
2	OE	Output	Output Enable. Refer to the Table. 1 for Logic Table
3	CLK1	Output	Buffered Clock Output 1
4	GND	Power	Power Ground.
5	CLK2	Output	Buffered Clock Output 2
6	VDD	Output	3.3V to 2.5V +/-10% Power Supply
7	CLK3	Power	Buffered Clock Output 3
8	CLK4	Input	Buffered Clock Output 4

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General Description

The SL23EP04NZ is a low skew, jitter and power fanout clock distribution buffer designed to produce up to four (4) clock outputs from one (1) reference input clock, for high speed clock distribution, including PCI/PCI-X applications.

Input and output Frequency Range

The input and output frequency is the same (1x) for SL23EP04NZ-1 and SL23EP04NZ-1Z. The products operate from DC to 220MHz clock range with up to 30pF output loads at each output.

OE (Output Enable) Function

The only difference between SL23EP04-1 and SL23EP04NZ-1Z is the OE logic implementation. When OE=0, SL23EP04NZ-1 outputs are disabled and outputs are at Logic Low. In the case of SL23EP04NZ-1Z the outputs are at High-Z. Refer to the Available OE Logic Configuration Table. 1 below.

Output Clock Skew

All outputs should drive the similar load to achieve output-to-output skew and input-to-output delay specifications as given in the switching electrical tables.

Power Supply Range (VDD)

The SL23EP04 is designed to operate from 3.3V+/-10% to 2.5V+/-10% VDD power supply range. An internal on-chip voltage regulator is used to provide to constant power supply of 1.8V in the core, leading to a consistent and stable electrical performance in terms of skew and jitter. The SL23EP04NZ I/O is powered by using VDD.

Contact SLI for 1.8V power supply Fan-Out Buffer and ZDB products.

CLKIN (Pin-1)	OE (Pin-2)	SL2304NZ-1 CLKOUT [1:4]	SL2304NZ-1Z CLKOUT [1:4]
Low	Low	Low	High-Z
High	Low	Low	High-Z
Low	High	Low	Low
High	High	High	High

Table 1. Available SL23EP04 CLKIN and OE Logic Configurations

Not Recommended for New Design

Absolute Maximum Ratings (All Products)

Description	Condition	Min	Max	Unit
Supply voltage, VDD		-0.5	4.2	V
All Inputs and Outputs		-0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	-40	85	°C
Storage Temperature	No power is applied	-65	150	°C
Junction Temperature	In operation, power is applied	–	125	°C
Soldering Temperature		–	260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-4,000	4,000	V
ESD Rating (Charge Device Model)	JEDEC22-C101C	-1,500	1,500	V
ESD Rating (Machine Model)	JEDEC22-A115D	-250	250	V

Operating Conditions (C and I-Grade)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD1	VDD+/-10%	2.97	3.3	3.63	V
Operating Temperature	TA-1	Ambient Temperature C-Grade	0	–	70	°C
	TA-2	Ambient Temperature I-Grade	-40	–	85	°C
Input Capacitance	VINC	Pins 1 and 2	–	3	5	pF
Load Capacitance	CL1	All Outputs≤220MHz, 3.3V	–	–	15	pF
	CL2	All Outputs≤134MHz, 3.3V	–	–	30	pF
Operating Frequency	FCLKIN1	Input Clock Range, CL=15pF	DC	–	220	MHz
Operating Frequency	FCLKIN2	Input Clock Range, CL=30pF	DC	–	134	MHz

Not Recommended for New Design

DC Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	VINL	CLKIN and OE	–	–	0.8	V
Input High Voltage	VINH	CLKIN and OE	2.0	–	VDD+0.3	V
Input Low Current	IINL	0 < VIN < 0.8V	–	–	10	µA
Input High Current	IINH	2.4V < VIN < VDD	–	–	15	µA
Output Low Voltage	VOL	I_{OL}=12mA	–	–	0.4	V
Output High Voltage	VOH	I_{OH}=-12mA	2.4	–	–	V
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)	–	8	12	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	–	10	15	mA
Power Supply Current	IDD3	CLKIN=166MHz CL=0 (No load at outputs)	–	14	20	mA

Switching Electrical Characteristics (C-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pF	0	-	220	MHz
	FOUT2	CL=30pF	0	-	134	MHz
Input Duty Cycle	DC1	Measured at VDD/2	20	50	80	%
Output Duty Cycle	DC2	CL=15pF, Fout=166MHz Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC3	CL=30pF, Fout=100MHz Measured at VDD/2	40	50	60	%
Output Rise/Fall Time	tr/f-1	CL=15pF, measured at 0.8V to 2.0V	–	–	1.2	ns
Output Rise/Fall Time	tr/f-2	CL=30pF, measured at 0.8V to 2.0V	–	–	1.6	ns
Output to Output Skew	SKW1	Measured at VDD/2 and Outputs are equally loaded	–	60	120	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	–	80	160	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge and Outputs are equally loaded	1.5	2.5	3.5	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=0 (No Load)	–	35	70	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=166MHz and CL=0 (No Load)	–	25	50	ps
Power-up Time	tpu	Power-up time for VDD to reach maximum specified time	0.05	–	100	ms

Not Recommended for New Design

DC Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	VINL	CLKIN and OE	–	–	0.8	V
Input High Voltage	VINH	CLKIN and OE	2.0	–	VDD+0.3	V
Input Low Current	IINL	0 < VIN < 0.8V	–	–	10	µA
Input High Current	IINH	2.4V < VIN < VDD	–	–	15	µA
Output Low Voltage	VOL	I_{OL}=12mA	–	–	0.4	V
Output High Voltage	VOH	I_{OH}=-12mA	2.4	–	–	V
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)	–	9	13	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	–	11	16	mA
Power Supply Current	IDD3	CLKIN=166MHz CL=0 (No load at outputs)	–	15	21	mA

Switching Electrical Characteristics (I-Grade and VDD=3.3V)

Unless otherwise stated VDD= 3.3V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pF	0	-	200	MHz
	FOUT2	CL=30pF	0	-	134	MHz
Input Duty Cycle	DC1	Measured at VDD/2	20	50	80	%
Output Duty Cycle	DC2	CL=15pF, Fout=166MHz Measured at VDD/2	45	50	55	%
Output Duty Cycle	DC3	CL=30pF, Fout=134MHz Measured at VDD/2	40	50	60	%
Output Rise/Fall Time	tr/f-1	CL=15pF, measured at 0.6V to 1.8V	–	–	1.4	ns
Output Rise/Fall Time	tr/f-2	CL=30pF, measured at 0.6V to 1.8V	–	–	1.8	ns
Output to Output Skew	SKW1	Measured at VDD/2 and Outputs are equally loaded	–	70	140	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	–	90	180	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge and Outputs are equally loaded	1.2	2.5	3.8	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=0 (No Load)	–	40	80	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=166MHz and CL=0 (No Load)	–	30	60	ps
Power-up Time	tpu	Power-up time for VDD to reach minimum specified time	0.05	–	100	ms

Not Recommended for New Design

Operating Conditions (C and I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	VDD+/-10%	2.25	2.5	2.75	V
Operating Temperature	TA-1	Ambient Temperature C-Grade	0	–	70	°C
	TA-2	Ambient Temperature I-Grade	-40	–	85	°C
Input Capacitance	VINC	Pins 1 and 2	–	3	5	pF
Load Capacitance	CL1	All Outputs≤180MHz	–	–	15	pF
	CL2	All Outputs≤80MHz	–	–	30	pF
Operating Frequency	CLKIN1	Input Clock Range, CL=15pF	DC	–	180	MHz
Operating Frequency	CLKIN2	Input Clock Range, CL=30pF	DC	–	80	MHz

DC Electrical Characteristics (C-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	VINL	CLKIN and OE	–	–	0.7	V
Input High Voltage	VINH	CLKIN and OE	1.7	–	VDD+0.3	V
Input Low Current	IINL	0 < VIN < 0.8V	–	–	10	µA
Input High Current	IINH	2.4V < VIN < VDD	–	–	15	µA
Output Low Voltage	VOL	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	VOH	I_{OH}=-8mA	VDD-0.6	–	–	V
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)	–	7	11	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	–	9	14	mA
Power Supply Current	IDD3	CLKIN=166MHz CL=0 (No load at outputs)	–	13	18	mA

Switching Electrical Characteristics (C-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pF	0	-	180	MHz
	FOUT2	CL=30pF	0	-	80	MHz
Input Duty Cycle	DC1	Measured at VDD/2	20	50	80	%
Output Duty Cycle	DC2	CL=15pF, Fout=166MHz Measured at VDD/2	45	50	55	%

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Output Duty Cycle	DC3	CL=30pF, Fout=80MHz Measured at VDD/2	40	50	60	%
Output Rise/Fall Time	tr/f-1	CL=15pF, measured at 0.6V to 1.7V	–	–	1.6	ns
Output Rise/Fall Time	tr/f-2	CL=30pF, measured at 0.6V to 1.7V	–	–	2.0	ns
Output to Output Skew	SKW1	Measured at VDD/2 and Outputs are equally loaded	–	70	140	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	–	90	180	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge and Outputs are equally loaded	–	xxx	xxx	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=0 (No Load)	–	50	100	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=166MHz and CL=0 (No Load)	–	40	80	ps
Power-up Time	tpu	Power-up time for VDD to reach minimum specified time	0.05	–	100	ms

DC Electrical Characteristics (I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	VINL	CLKIN and OE	–	–	0.7	V
Input High Voltage	VINH	CLKIN and OE	1.7	–	VDD+0.3	V
Input Low Current	IINL	0 < VIN < 0.8V	–	–	10	µA
Input High Current	IINH	2.4V < VIN < VDD	–	–	15	µA
Output Low Voltage	VOL	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	VOH	I_{OH}=-8mA	VDD-0.6	–	–	V
Power Supply Current	IDD1	CLKIN=33MHz CL=0 (No load at outputs)	–	8	12	mA
Power Supply Current	IDD2	CLKIN=66MHz CL=0 (No load at outputs)	–	10	15	mA
Power Supply Current	IDD3	CLKIN=166MHz CL=0 (No load at outputs)	–	12	19	mA

Switching Electrical Characteristics (I-Grade and VDD=2.5V)

Unless otherwise stated VDD= 2.5V+/- 10%, CL=15pF and Ambient Temperature range -40 to +85°C

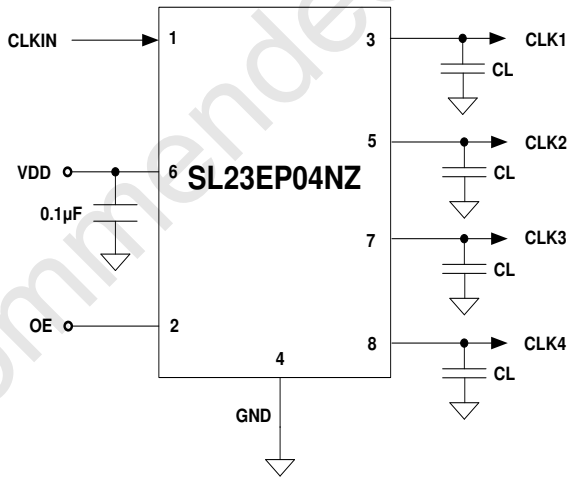
Description	Symbol	Condition	Min	Typ	Max	Unit
Output Frequency Range	FOUT1	CL=15pF	0	-	180	MHz
	FOUT2	CL=30pF	0	-	80	MHz
Input Duty Cycle	DC1	Measured at VDD/2	20	50	80	%
Output Duty Cycle	DC2	CL=15pF, Fout=166 MHz Measured at VDD/2	45	50	55	%

Not Recommended for New Design

Output Duty Cycle	DC3	CL=15pF, Fout=80 MHz Measured at VDD/2	45	50	55	%
Output Rise/Fall Time	tr/f-1	CL=15pF, measured at 0.6V to 1.7V	–	–	1.8	ns
Output Rise/Fall Time	tr/f-2	CL=30pF, measured at 0.6V to 1.7V	–	–	2.4	ns
Output to Output Skew	SKW1	Measured at VDD/2 and Outputs are equally loaded	–	100	200	ps
Part to Part Skew	SKW2	Measured at VDD/2 and Outputs are equally loaded	–	120	240	ps
Propagation Delay Time	PDT	Measured at VDD/2 from CLKIN to Output Clock rising edge and Outputs are equally loaded	–	4.2	6.8	ns
Cycle-to-Cycle Jitter	CCJ1	CLKIN=66MHz and CL=0 (No Load)	–	70	140	ps
Cycle-to-Cycle Jitter	CCJ2	CLKIN=133MHz and CL=0 (No Load)	–	60	120	ps
Power-up Time	tpu	Power-up time for VDD to reach minimum specified time	0.05	–	100	ms

External Components & Design Considerations

Typical Application Schematic



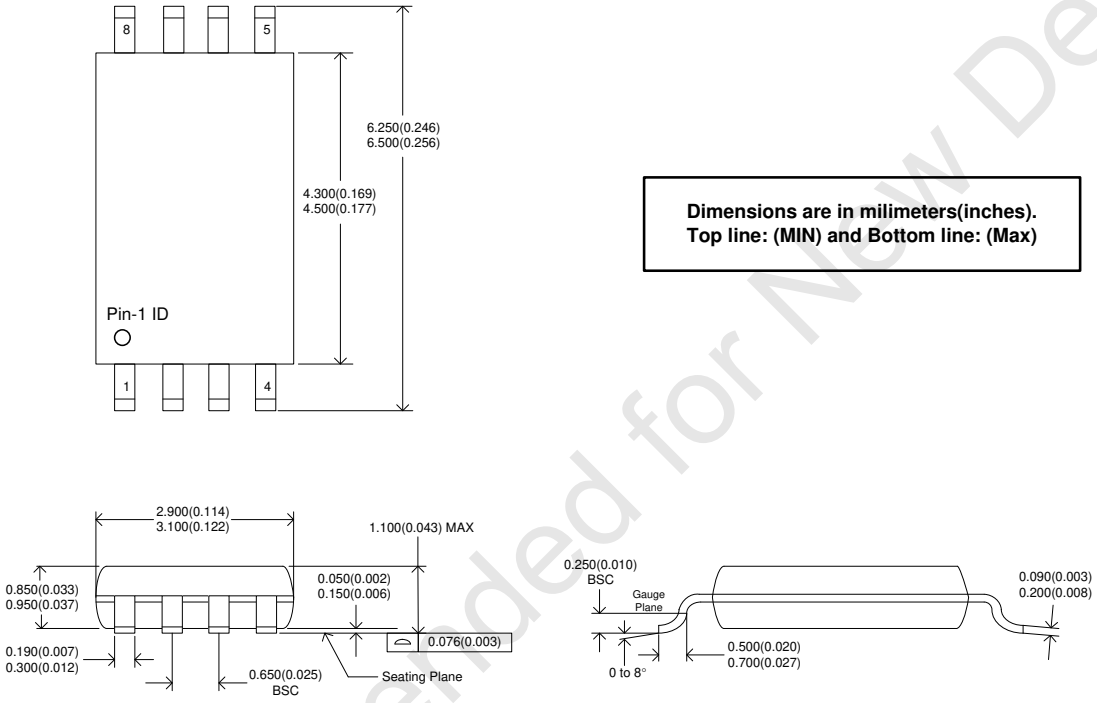
Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS pins. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Not Recommended for New Design

Package Outline and Package Dimensions

8-Pin TSSOP (4.4 mm)



Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	110	-	°C/W
	θ JA	1m/s air flow	-	100	-	°C/W
	θ JA	3m/s air flow	-	80	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	35	-	°C/W

Not Recommended for New Design

Ordering Information [1]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL23EP04NZZC-1	SL23EP04NZC-1	Tube	8-pin TSSOP	0 to 70°C
SL23EP04NZZC-1T	SL23EP04NZC-1	Tape and Reel	8-pin TSSOP	0 to 70°C
SL23EP04NZZI-1	SL23EP04NZI-1	Tube	8-pin TSSOP	-40 to 85°C
SL23EP04NZZI-1T	SL23EP04NZI-1	Tape and Reel	8-pin TSSOP	-40 to 85°C
SL23EP04NZZC-1Z	SL23EP04NZC-1Z	Tube	8-pin TSSOP	0 to 70°C
SL23EP04NZZC-1ZT	SL23EP04NZC-1Z	Tape and Reel	8-pin TSSOP	0 to 70°C
SL23EP04NZZI-1Z	SL23EP04NZI-1Z	Tube	8-pin TSSOP	-40 to 85°C
SL23EP04NZZI-1ZT	SL23EP04NZI-1Z	Tape and Reel	8-pin TSSOP	-40 to 85°C

Notes:

1. The SL23EP04NZ products are RoHS compliant.

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ClockBuilder Pro

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Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

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