OC-48/24/12/3 SONET/SDH MULTIRATE TRANSCEIVER

FEATURES

- **Fully Integrated SONET/SDH Transceiver to Support Clock/Data Recovery and Multiplexer/Demultiplexer Functions**
- **Supports OC-48, OC-24, OC-12, Gigabit Ethernet, and OC-3 Data Rate With Autorate Detection**
- **Supports Transmit Only, Receiver Only, Transceiver and Repeater Functions in a Single Chip Through Configuration Pins**
- **Supports SONET/SDH Frame Detection**
- **On-Chip PRBS Generation and Verification**
- **Supports 4-Bit LVDS (OIF99.102) Electrical Interface**
- **Parity Checking and Generation for the LVDS Interface**
- **Single 2.5-V Power Supply**
- **Interfaces to Back Plane, Copper Cables, or Optical Modules**
- **Hot Plug Protection**
- **Low Jitter PECL Compatible Differential Serial Interface With Programmable De-Emphasis for the Serial Output**
- **On-Chip Termination for LVDS and PECL Compatible Interface**
- **Receiver Differential Input Thresholds 150 mV Min**
- **Supports SONET Loop Timing**
- **Low Power CMOS**
- **ESD Protection >2 kV**
- **155-MHz or 622-MHz Reference Clock**
- **Maintains Clock Output in Absence of Data**
- **Local and Remote Loopback**
- **100-Pin PZP Package With PowerPAD™ Design With 5-mm × 5-mm (Typ) Heatsink**

DESCRIPTION

The SLK2511B is a single chip multirate transceiver IC used to derive high-speed timing signals for SONET/SDH based equipment. The chip performs clock and data recovery, serial-to-parallel/parallel-to-serial conversion and frame detection function conforming to the SONET/SDH standards.

The device can be configured to operate under OC-48, OC-24, OC-12, or OC-3 data rates through the rate selection pins or the autorate detection function. An external reference clock operating at 155.52 MHz or 622.08 MHz is required for the recovery loop, and it also provides a stable clock source in the absence of serial data transitions.

The SLK2511B accepts 4-bit LVDS parallel data/clock and generates a NRZ SONET/SDH-compliant signal at OC-3, OC-12, OC-24, or OC-48 rates. It also recovers the data and clock from the serial SONET stream and demultiplexes it into 4-bit LVDS parallel data for full duplex operation. TXDATA0 and RXDATA0 are the first bits that are transmitted and received in time, respectively. The serial interface is a low jitter, PECL compatible differential interface.

The SLK2511B provides a comprehensive suite of built-in tests for self-test purposes including local and remote loopback and PRBS (2^7-1) generation and verification.

The device comes in a 100-pin VQFP package that requires a single 2.5-V supply with 3.3-V tolerant inputs on the control pins. The SLK2511B is power efficient, dissipating less than 900 mW at 2.488 Gbps, the OC-48 data rate, and it is characterised for operation from –40°C to 85°C.

AVAILABLE PACKAGE OPTIONS(1)

T_A	PowerPAD QUAD (PZP)
–40°C to 85°C	SLK2511BPZP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com

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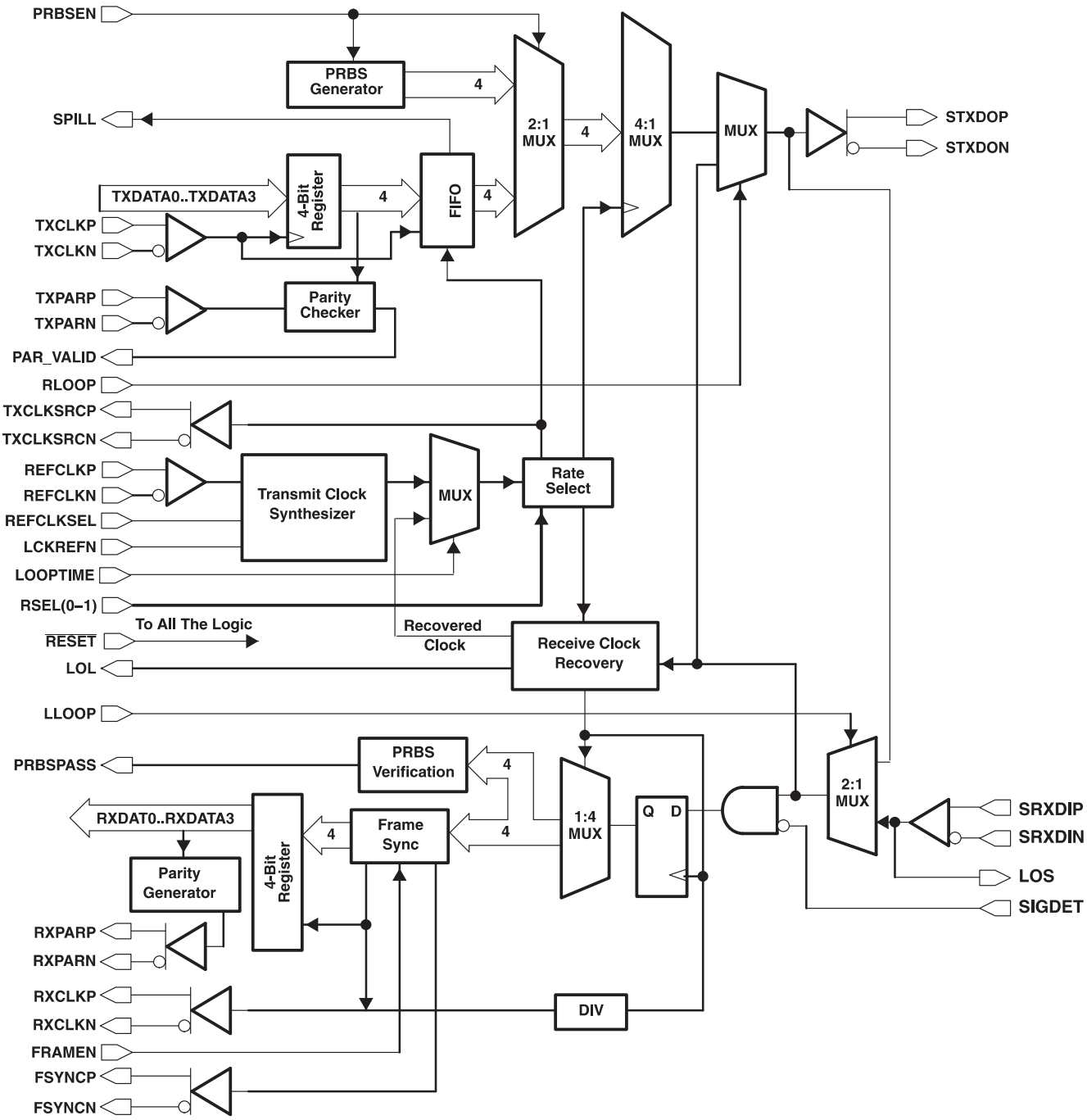
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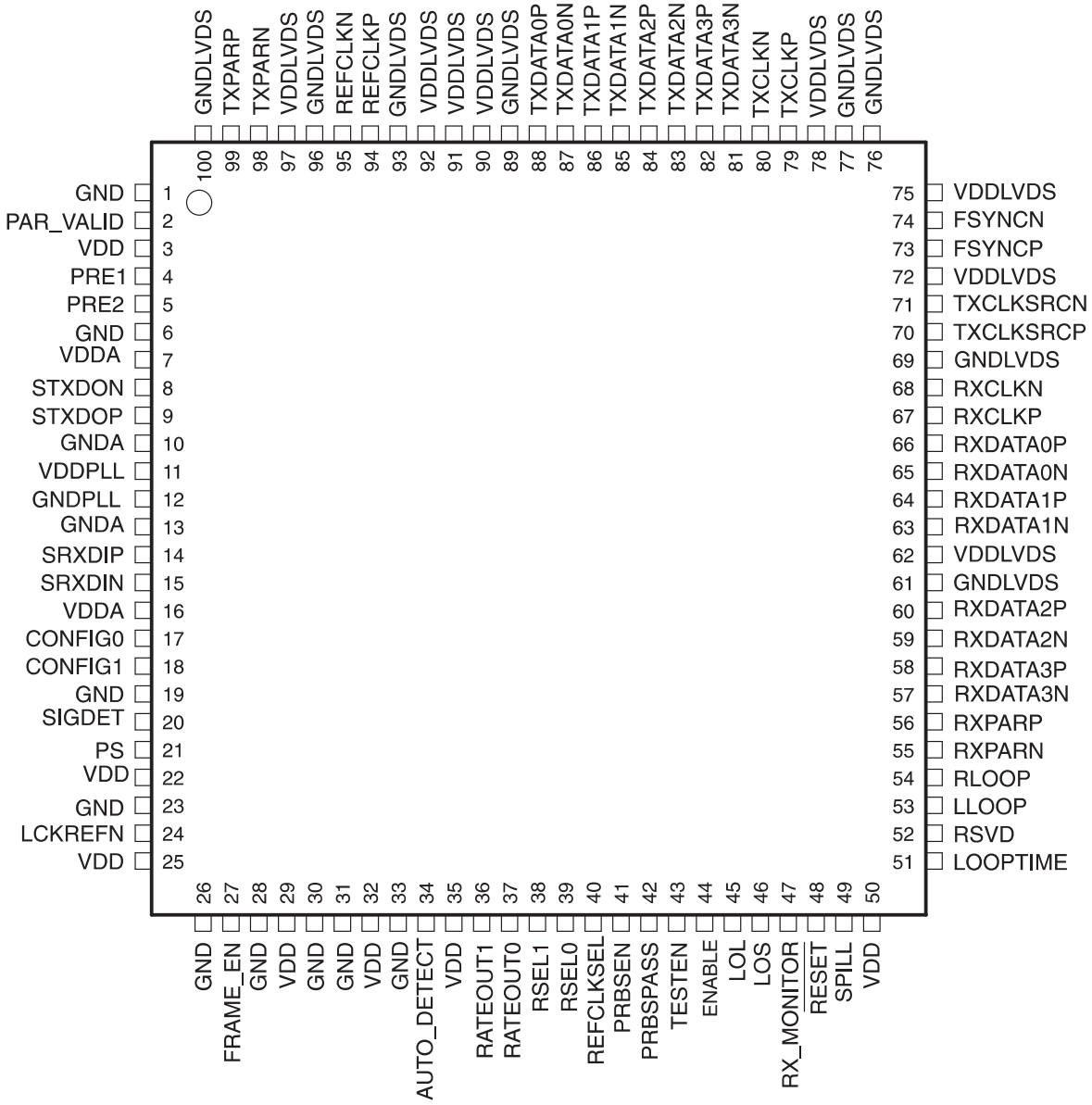
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM



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PZP PACKAGE
(TOP VIEW)



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Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
CLOCK PINS			
REFCLKP, REFCLKN	94 95	LVDS/PECL compatible input	Differential reference input clock. There is an on-chip 100-Ω termination resistor differentially placed between REFCLKP and REFCLKN. The dc bias is also provided on-chip for ac-coupled case.
RXCLKP, RXCLKN	67 68	LVDS output	Receive data clock. The data on RXDATA(0:3) is on the falling edges of RXCLKP. The interface of RXDATA(0:3) and RXCLKP is source synchronous (see Figure 7).
TXCLKP, TXCLKN	79 80	LVDS input	Transmit data clock. The data on TXDATA(0:3) is latched on the rising edge of TXCLKP.
TXCLKSRCP, TXCLKSRCN	70 71	LVDS output	Transmit clock source. A clock source generated from the SLK2511B to the downstream device (i.e., framer) that could be used by the downstream device to transmit data back to the SLK2511B. This clock is frequency-locked to the local reference clock.
SERIAL SIDE DATA PINS			
SRXDIP, SRXDIN	14 15	PECL compatible input	Receive differential pairs; high-speed serial inputs.
STXDOP, STXDON	9 8	PECL compatible input	Transmit differential pairs; high-speed serial outputs.
PARALLEL SIDE DATA PINS			
FSYNCP, FSYNCN	73 74	LVDS output	Frame sync pulse. This signal indicates the frame boundaries of the incoming data stream. If the frame-detect circuit is enabled, FSYNC pulses for four RXCLKP and RXCLKN clock cycles when it detects the framing patterns.
RXDATA[0:3] P/N	66–63, 60–57	LVDS output	Receive data pins. Parallel data on this bus is valid on the falling edge of RXCLKP (seeFigure 7). RXDATA0 is the first bit received in time.
RXPARP, RXPARN	56 55	LVDS output	Receive data parity output
TXDATA[0:3] P/N	88–81	LVDS input	Transmit data pins. Parallel data on this bus is clocked on the rising edge of TXCLKP. TXDATA0 is the first bit transmitted in time.
TXPARP, TXPARN	99 98	LVDS input	Transmit data parity input
CONTROL/STATUS PINS			
AUTO_DETECT	34	TTL input (with pulldown)	Data rate autodetect enable. Enable the auto-detection function for different data rates. When AUTO_DETECT is high, the autodetection circuit generates RATEOUT0 and RATEOUT1 to indicate the data rates for the downstream device.
CONFIG0, CONFIG1	17 18	TTL input (with pulldown)	Configuration pins. Put the device under one of the four operation modes: TX only, RX only, transceiver, or repeater mode. (See Table 4)
ENABLE	44	TTL input (with pullup)	Standby enable. When this pin is held low, the device is disabled for IDDQ testing. When high, the device operates normally.
FRAME_EN	27	TTL input (with pullup)	Frame sync enable. When this pin is asserted high, the frame synchronization circuit for byte alignment is turned on.
LCKREFN	24	TTL input (with pullup)	Lock to reference. When low, RXCLKP/N output is forced to lock to REFCLK. When high, RXCLKP/N is the divided down clock extracted from the receive serial data.
LLOOP	53	TTL input (with pulldown)	Local loopback enable. When high, the serial output is internally looped back to its serial input.
LOL	45	TTL output	Loss of lock. When the clock recovery loop has locked to the input data stream and the phase differs by less than 100 ppm from REFCLK then LOL is high. When the phase of the input data stream differs by more than 100 ppm from REFCLK, then LOL is low. If the difference is too big (> 500 ppm), the LOL output is not valid.
LOOPTIME	51	TTL input (with pulldown)	Loop timing mode. When high, the PLL for clock synthesizer is bypassed. The recovered clock timing is used to send the transmit data.
LOS	46	TTL output	Loss of signal. When no transitions appear on the input data stream for more than 2.3 µs, a loss of signal occurs and LOS goes high. The device also transmits all zeroes downstream using REFCLK as its clock source. When a valid SONET signal received the LOS signal goes low.
PRBSEN	41	TTL input (with pulldown)	PRBS testing enable. When this pin is asserted high, the device is put into the PRBS testing mode.
PRE1, PRE2	4 and 5	TTL input (with pulldown)	Programmable de-emphasis control. Combinations of these two bits can be used to optimize serial data transmission.
PS	21	TTL input (with pulldown)	Polarity select. This pin, used with the SIGDET pin, sets the polarity of SIGDET. When high, SIGDET is an active low signal. When low, SIGDET is an active high signal.
RATEOUT0, RATEOUT1	37 36	TTL output	Autorate detection outputs. When AUTO_DETECT is high, the autodetection circuit generates these two bits to indicate the data rates for the downstream device.
$\overline{\text{RESET}}$	48	TTL input	TXFIFO and LOL reset pin. Low is reset and high is normal operation.
RLOOP	54	TTL input (with pulldown)	Remote loopback enable. When high, the serial input is internally looped back to its serial output with the timing extracted from the serial data.

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Table 1. TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
RSEL0, RSEL1	39 38	TTL input (with pulldown)	Data rate configuration pins. Puts the device under one of the four data rate operations: OC-48, OC-24, OC-12, or OC-3.
RX_MONITOR	47	TTL input (with pulldown)	RX parallel data monitor in repeater mode. This pin is only used when the device is put under the repeater mode. When high, the RX demux circuit is enabled and the parallel data is presented. When low, the demux is shut down to save power.
SIGDET	20	TTL input (with pulldown)	Signal detect. This pin is generally connected to the output of an optical receiver. This signal may be active high or active low depending on the optical receiver. The SIGDET input is XORed with the PS pin to select the active state. When SIGDET is in the inactive state, data is processed normally. When activated, indicating a loss of signal event, the transmitter transmits all zeroes and force the LOS signal to go high.
TESTEN	43	TTL input (with pulldown)	Production test mode enable. This pin should be left unconnected or tied low.
PAR_VALID	2	TTL output	Parity checker output. The internal parity checker on the parallel side of the transmitter checks for even parity. If there is a parity error, the pin is pulsed low for 2 clock cycles.
PRBSPASS	42	TTL output	PRBS test result. This pin reports the status of the PRBS test results (high = pass). When PRBSEN is disabled, the PRBSPASS pin is set low. When PRBSEN is enabled and a valid PRBS is received, then the PRBSPASS pin is set high.
REFCLKSEL	40	TTL input (with pulldown)	Reference clock select. The device can accept a clock frequency of 155.52 MHz or 622.08 MHz, which is selected by this pin (0 = 622.08-MHz mode and 1 = 155.52-MHz mode).
			SPILL 49 TTL output TX FIFO collision output
VOLTAGE SUPPLY AND RESERVED PINS			
GND	1, 6, 19, 23, 26, 28, 30, 31, 33	Ground	Digital logic ground
GNDA	10, 13	Ground	Analog ground
GNDLVDS	61, 69, 76, 77, 89, 93, 96, 100	Ground	LVDS ground
GNDPLL	12	Supply	PLL ground
RSVD	52	Reserved	This pin needs to be tied to ground or left floating for normal operation.
VDD	3, 22, 25, 29, 32, 35, 50	Supply	Digital logic supply voltage (2.5 V)
VDDA	7, 16	Supply	Analog voltage supply (2.5 V)
VDDLVDS	62, 72, 75, 78, 90, 91, 92, 97	Supply	LVDS supply voltage (2.5 V)
VDDPLL	11	Supply	PLL voltage supply (2.5 V)

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DETAILED DESCRIPTION

The SLK2511B is designed to support OC-48/24/12. The operating data speed can be configured through the RSEL0 and RSEL1 pins as indicated in Table 2.

Table 2. Data Rate Select

SERIAL DATA RATE	RSEL0	RSEL1	PARALLEL LVDS DATA RATE	TXCLK/RXCLK
OC-48:2.488 Gb/s	0	0	622.08 Mbps	622.08 MHz
OC-24:1.244 Gb/s	1	0	311.04 Mbps	311.04 MHz
OC-12:622 Mb/s	0	1	155.52 Mbps	155.52 MHz
OC-3:155 Mb/s	1	1	38.88 Mbp	38.88 MHz

The user can also enable the autorate detection circuitry through the AUTO_DETECT pin. The device automatically detects the OC-N of the data line rate and generates two bits of output to indicate the data rate to other devices in the system. When using AUTO_DETECT, RSEL0 and RSEL1 need to be set to 00 or be unconnected.

Table 3. Data Rate Reporting Under Autorate Detection Mode

SERIAL DATA RATE	RATEOUT0	RATEOUT1	PARALLEL LVDS DATA RATE	TXCLK/RXCLK
OC-48:2.488 Gb/s	0	0	622.08 Mbps	622.08 MHz
OC-24:1.244 Gb/s	1	0	311.04 Mbps	311.04 MHz
OC-12:622 Mb/s	0	1	155.52 Mbps	155.52 MHz
OC-3:155 Mb/s	1	1	38.88 Mbp	38.88 MHz

The SLK2511B has four operational modes controlled by two configuration pins. These operational modes are listed in Table 4. When the device is put in a certain mode, unused circuit blocks are powered down to conserve the system power.a

While the transceiver mode, transmit only mode, and receive only mode are straightforward, the repeater mode of operation is shown in Figure 4. The receive serial data is recovered by the extracted clock and it is then sent back out on the transmit serial outputs. The data eye is open both vertically and horizontally in this process. In the repeater mode, the user can select to turn on the RX demux function through the RX_MONITOR pin and allow the parallel data to be presented. This feature enables the repeater device not only to repeat but also to *listen in*.

Table 4. Operational Modes

MODE	CONFIG0	CONFIG1	DESCRIPTION
1	0	0	Full duplex transceiver mode
2	0	1	Transmit only mode
3	1	0	Receive only mode
4	1	1	Repeater mode

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HIGH-SPEED ELECTRICAL INTERFACE

The high-speed serial I/O uses a PECL compatible interface. The line could be directly coupled or ac-coupled. See Figure 10 and Figure 11 for configuration details. As shown in the figures, an on-chip 100-Ω termination resistor is placed differentially at the receive end.

The PECL output also provide de-emphasis for compensating ac loss when driving a cable or PCB backplane over long distance. The level of the de-emphasis is programmable via PRE1 and PRE2 pins. Users can use software to control the strength of the de-emphasis to optimize the device for a specific system requirement.

Table 5. Programmable De-Emphasis

PRE1	PRE2	DE-EMPHASIS LEVEL ($V_{(ODp)}d/V_{(ODd)}$ (1) – 1)
0	0	De-emphasis disabled
1	0	10%
0	1	20%
1	1	30%

(1) $V_{(ODp)}$: Differential voltage swing when there is a transition in the data stream.
$V_{(ODd)}$: Differential voltage swing when there is no transition in the data stream.

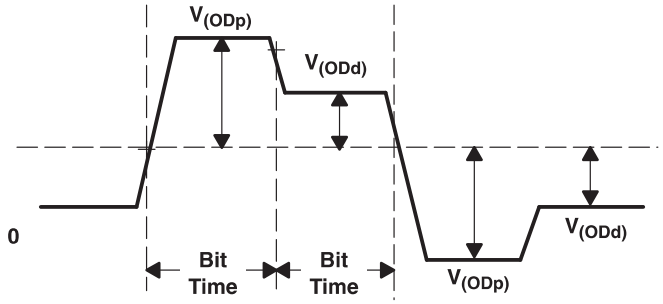


Figure 1. Output Differential Voltage Under De-Emphasis

LVDS PARALLEL DATA INTERFACE

The parallel data interface consists of a 4-bit parallel LVDS data and clock. The device conforms to OIF99.102 specification when operating at the OC-48 rate. When operating at lower serial rates the clock and data frequency are scaled down accordingly, as indicated in Table 2. The parallel data TXDATA[0:3] is latched on the rising edge of the TXCLK and then is sent to a data FIFO to resolve any phase difference between TXCLK and REFCLK. If there is a FIFO overflow condition, the SPILL pin is set high. The FIFO resets itself to realign between two clocks. The internal PLL for the clock synthesizer is locked to the REFCLK and it is used as the timing to serialize the parallel data (except for the loop timing mode where the recovered clock is used). On the receive side, RXDATA[0:3] is updated on the rising edge of RXCLK. Figure 7 and Figure 8 show the timing diagram for the parallel interface.

The SLK2511B also has a built-in parity checker and generator for error detection of the LVDS interface. On the transmit side, it accepts the parity bit, TXPARP/N, and performs the parity checking function for even parity. If an error is detected, it pulses the PAR_VALID pin low for two clock cycles. On the receive side, the parity bit RXPARP/N is generated for the downstream device for parity error checking.

Differential termination 100-Ω resistors are included on-chip between TXDATAP/N.

REFERENCE CLOCK

The device accepts either a 155.52-MHz or a 622.08-MHz clock. A clock select pin (REFCLKSEL) allows the selection of the external reference clock frequency. The REFCLK input is compatible with the LVDS level and also the 3.3-V LVPECL level using ac-coupling. A 100-Ω differential termination resistor is included on-chip, as well as a dc biasing circuit (3 kΩ to VDD and 4.5 kΩ to GND) for the ac-coupled case. A high quality REFCLK must be used on systems required to meet SONET/SDH standards. For non-SONET/SDH compliant systems, loose tolerances may be used.

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Table 6. Reference Clock Frequency

REFCLKSEL	REFERENCE CLOCK FREQUENCY
0	622.08 MHz
1	155.52 MHz

CLOCK AND DATA RECOVERY

The CDR unit of SLK2511B recovers the clock and data from the incoming data streams.

In the event of receive data loss, the PLL automatically locks to the local REFCLK to maintain frequency stability. If the frequency of the data differs by more that 100 ppm with respect to the REFCLK frequency, the LOL pin is asserted as a warning. Actual loss of lock occurs if the data frequency differs by more than 170 ppm.

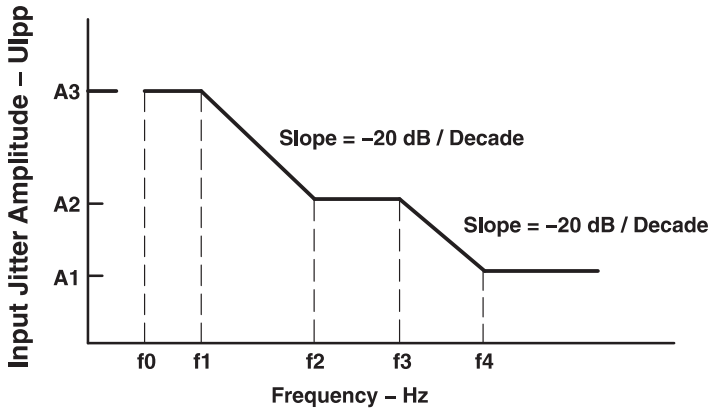
MINIMUM TRANSITION DENSITY

The loop filter transfer function is optimized to enable the CDR to track ppm difference in the clocking and tolerate the minimum transition density that can be received in a SONET data signal (±20 ppm). The transfer function yields a typical capture time of 3500 bit times for random incoming NRZ data after the device is powered up and achieves frequency locking.

The device tolerates up to 72 consecutive digits (CID) without sustaining an error.

JITTER TOLERANCE

Input jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input signal that causes the equivalent 1-dB optical/electrical power penalty. This refers to the ability of the device to withstand input jitter without causing a recovered data error. The device has a jitter tolerance that exceeds the mask shown in Figure 2 (GR-253 Figure 5-28)(1). This jitter tolerance is measured using a pseudorandom data pattern of 2^{31}–1.



OC-N/STS-N LEVEL	f0 (Hz)	F1 (Hz)	F2 (Hz)	F3 (kHz)	F4 (kHz)	A1 (UIpp)	A2 (UIpp)	A3 (UIpp)
3	10	30	300	6.5	65	0.15	1.5	15
12	10	30	300	25	250	0.15	1.5	15
24	Not Specified							
48	10	600	6000	100	1000	0.15	1.5	15

(1) The tolerance margin is 20% or more at all modulating frequencies when measured using the HP 7150A jitter analysis system on the Texas Instruments provided EVM.

Figure 2. Input Jitter Tolerance

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JITTER GENERATION

The jitter of a serial clock and serial data outputs must not exceed 0.01 UI_{rms}/0.1 UI_{p-p} when a serial data with no jitter is presented to the inputs. The measurement bandwidth for intrinsic jitter is 12 kHz to 20 MHz.

LOOP TIMING MODE

When LOOPTIME is high, the clock synthesizer used to serialize the transmit data is bypassed and the timing is provided by the recovered clock. However, REFCLK is still needed for the recovery loop operation.

LOSS OF LOCK INDICATOR

The SLK2511B has a lock detection circuit to monitor the integrity of the data input. When the clock recovery loop is locked to the input serial data stream, the LOL signal goes high. If the recovered clock frequency deviates from the reference clock frequency by more than 100 ppm, LOL goes low. If the data stream clock rate deviates by more than 170 ppm, loss of lock occurs. If the data streams clock rate deviates more than 500 ppm from the local reference clock, the LOL output status might be unstable. Upon power up, the LOL goes low until the PLL is close to phase lock with the local reference clock.

LOSS OF SIGNAL

The loss of signal (LOS) alarm is set high when no transitions appear in the input data path for more than 2.3µs. The LOS signal becomes active when the above condition occurs. If the serial inputs of the device are ac-coupled to its source, the ac-couple capacitor needs to be big enough to maintain a signal level above the threshold of the receiver for the 2.3µs no transition period. Once activated, the LOS alarm pin is latched high until the receiver detects an A1A2 pattern. The recovered clock (RXCLK) is automatically locked to the local reference when LOS occurs. The parallel data (RXDATAx) may still be processed even when LOS is activated.

SIGNAL DETECT

The SLK2511B has an input SIGDET pin to force the device into the loss of signal state. This pin is generally connected to the signal detect output of the optical receiver. Depending on the optics manufacturer, this signal can be either active high or active low. To accommodate the differences, a polarity select (PS) pin is used. For an active low, SIGDET input sets the PS pin high. For an active high, SIGDET input sets the PS pin low. When the PS signal pin and SIGDET are of opposite polarities, the loss of signal state is generated and the device transmits all zeroes downstream.

MULTIPLEXER OPERATION

The 4-bit parallel LVDS data is clocked into an input buffer by a clock derived from the synthesized clock. The data is then clocked into a 4:1 multiplexer. The D0 bit is the most significant bit and is shifted out first in the serial output stream.

DEMULTIPLEXER OPERATION

The serial 2.5 Gbps data is clocked into a 1:4 demultiplexer by the recovered clock. The D0 bit is the first bit that is received in time from the input serial stream. The 4-bit parallel data is then sent to the LVDS driver along with the divided down recovered clock.

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FRAME SYNCHRONIZATION

The SLK2511B has a SONET/SDH-compatible frame detection circuit that can be enabled or disabled by the user. Frame detection is enabled when the FRAMEN pin is high. When enabled it detects the A1, A2 framing pattern, which is used to locate and align the byte and frame boundaries of the incoming data stream. When FRAMEN is low the frame detection circuitry is disabled and the byte boundary is frozen to the location found when detection was previously enabled.

The frame detect circuit searches the incoming data for three consecutive A1 bytes followed immediately by one A2 byte. The data alignment circuit then aligns the parallel output data to the byte and frame boundaries of the incoming data stream. During the framing process the parallel data bus does not contain valid and aligned data. Upon detecting the third A1, A2 framing patterns that are separated by 125µs from each other, the FSYNC signal goes high for 4 RXCLK cycles, indicating frame synchronization has been achieved.

The probability that random data in a SONET/SDH data stream mimics the framing pattern in the data payload is extremely low. However, there is a state machine built in to prevent false reframing if a framing pattern does show up in the data payload.

TESTABILITY

The SLK2511B has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable pin allows for all circuitry to be disabled so that an Iddq test can be performed. The PRBS function allows for a BIST (built-in self-test).

IDDQ FUNCTION

When held low, the ENABLE pin disables all quiescent power in both the analog and digital circuitry. This allows for IDDQ testing on all power supplies and can also be used to conserve power when the link is inactive.

LOCAL LOOPBACK

The LLOOP signal pin controls the local loopback. When LLOOP is high, the loopback mode is activated and the parallel transmit data is selected and presented on the parallel receive data output pins. The parallel transmit data is also multiplexed and presented on the high-speed serial transmit pins. Local loopback can only be enabled when the device is under the transceiver mode.

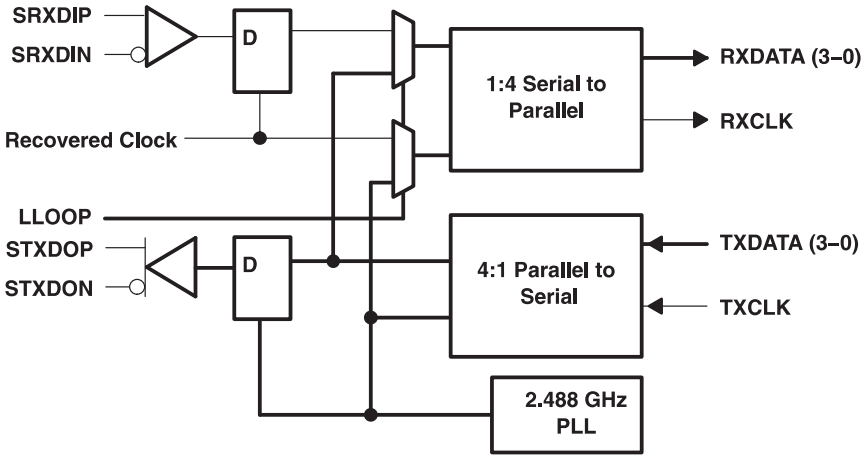


Figure 3. Local Loopback Data Path

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REMOTE LOOPBACK

The RLOOP signal pin controls the remote loopback. When RLOOP is high, the serial receive data is selected and presented on the serial transmit data output pins. The serial received data is also demultiplexed and presented on the parallel receive data pins. The remote loop can be enabled only when the device is under transceiver mode. When the device is put under the repeater mode with RX_MONITOR high, it performs the same function as the remote loopback.

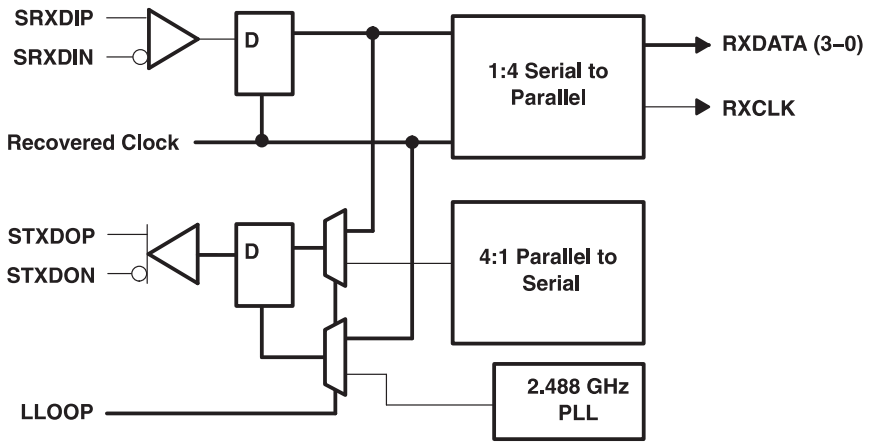


Figure 4. Remote Loopback Data Path/Repeater Mode Operation

PRBS

The SLK2511B has two built-in pseudorandom bit stream (PRBS) functions. The PRBS generator is used to transmit a PRBS signal. The PRBS verifier is used to check and verify a received PRBS signal.

When the PRBSEN pin is high, the PRBS generator and verifier are both enabled. A PRBS is generated and fed into the parallel transmitter input bus. Data from the normal input source is ignored in PRBS mode. The PBRS pattern is then fed through the transmitter circuitry as if it was normal data and sent out by the transmitter. The output can be sent to a bit error rate tester (BERT) or to the receiver of another SLK2511B. If an error occurs in the PRBS pattern, the PRBSPASS pin is set low for 2 RXCLKP/N cycles.

POWER-ON RESET

Upon application of minimum valid power, the SLK2511B generates a power-on reset. During the power-on reset the PRXDATA[0:3] signal pins goes to 3-state. RXCLKP and RXCLKN are held low. The length of the power-on reset cycle is dependent upon the REFCLKP and REFCLKN frequency but is less than 1ms in duration.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{DD}	Supply voltage		–0.3 to 3	V
	Voltage range	TTL input terminals	–0.3 to 4	V
		LVDS terminals	–0.3 to 3	V
		Any other terminal except aboven	–0.3 to V_{DD} + 0.3	V
P_D	Package power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature		–65 to 150	°C
	Electrostatic discharge		HBM: 2 kv	
T_A	Characterized free-air operating temperature range		–40 to 85	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
PZP(2)	3.4 W	33.78 mW/°C	1.3 W
PZP(3)	2.27 W	22.78 mW/°C	0.911 W

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).
(2) 2 oz trace and copper pad with solder.
(3) 2 oz trace and copper pad without solder.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		2.375	2.5	2.625	V
P_D	Power dissipation	Frequency = 2.488 Gb/sec, PRBS pattern		900	1100	mW
	Shutdown current	Enable = 0, VDDA, VDD pins, VDD = max		20		µA
T_A	Operating free-air temperature		–40		85	°C

START-UP SEQUENCE

To ensure proper start up, follow one of the following steps when powering up the SLK2511B.

1. Keep ENABLE (pin 44) low until power supplies and reference clock have become stable.
2. Drive ENABLE (pin 44) low for at least 30 ns after power supplies and reference clock have become stable.

   The following step is recommended with either of the above two sequences.
3. Drive $\overline{\text{RESET}}$ low for at least 10 ns after link has become stable to center the TXFIFO.

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ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TTL						
V_{IH}	High-level input voltage		2		3.6	V
V_{IL}	Low-level input voltage				0.80	V
I_{IH}	Input high current	V_{DD} = MAX, V_{IN} = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = MAX, V_{IN} =0.4 V	–40			µA
V_{OH}	High-level output voltage	I_{OH} = –1 mA	2.10	2.3		V
V_{OL}	Low-level output voltage	I_{OH} = 1 mA		0.25	0.5	V
C_I	Input capacitance				4	pF
LVDS INPUT SIGNALS						
V_I	Input voltage		825		1575	mV
$V_{ID(th)}$	Input differential threshold voltage See Figure 5	Assumes 60% / 40% duty cycle	250			mV
		Assumes 55% / 45% duty cycle	200			
t_r/t_f	Input transition time	20% to 80%			375	ps
C_I	Input capacitance				3	pF
R_I	Input differential impedance	On-chip termination	80	100	120	Ω
t_{su}	Input setup time requirement	See Figure 8	300			ps
t_h	Input hold time requirement	See Figure 8	300			ps
$T_{(duty)}$	Input clock duty cycle		40%		60%	
LVDS OUTPUT SIGNALS						
V_{OD}	Output differential voltage	R_L = 100 ±1%	300		800	mV
V_{OS}	Output common mode voltage		1070		1375	
V_{OD}	Change VOD between 1 and 0				25	
V_{OS}	Change VOS between 1 and 0				25	
$I_{(SP)}$, $I_{(SN)}$, $I_{(SPN)}$	Output short circuit current	Outputs shorted to ground or shorted together			24	mA
I_{off}	Power-off current	V_{DD} = 0 V			10	µA
$t_{(cq_min)}$	Clock-output time	See Figure 7			100	ps
$t_{(cq_max)}$					100	
t_r/t_f	Output transition time	20% to 80%	100		300	ps
	Output clock duty cycle		45%		55%	
	Data output to FRAME_SYNC delay		4		7	Bit times

(OC-48 = 622.08 MHz, Clock Rates With t_r/t_f ≤ 500 ps)

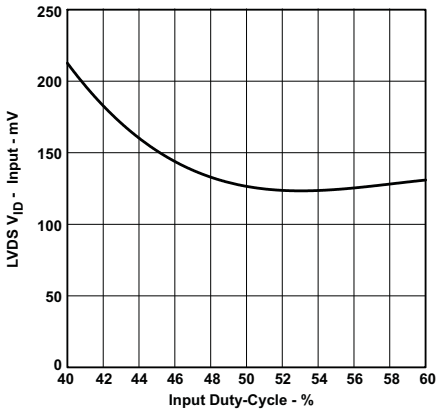


Figure 5. LVDS Differential Input Voltage vs Input Duty Cycle

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TIMING REQUIREMENTS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK (REFCLK)						
	Frequency tolerance(1)		–20		20	ppm
	Duty cycle		40%	50%	60%	
	Jitter	12 kHz to 20 MHz			3	ps rms
PLL PERFORMANCE SPECIFICATIONS						
	PLL startup lock time	V_{DD}, V_{DDC} = 2.3 V, after REFCLK is stable			1	ms
	Acquisition lock time	Valid SONET signal or PRBS OC-48		2031		Bit Times
SERIAL TRANSMITTER/RECEIVER CHARACTERISTICS						
	$V_{(ODD)}$ = |STXDOP-STXDON|, transmit differential output voltage under de-emphasis	PRE1 = 0, PRE2 = 0, Rt = 50, See Table 5 and Figure 1	650	850	1000	mV
		PRE1 = 1, PRE2 = 0	550	750	900	
		PRE1 = 0, PRE2 = 1	540	700	860	
		PRE1 = 1, PRE2 = 1	500	650	800	
$V_{(CMT)}$	Transmit common mode voltage range	Rt = 50Ω	1100	1250	1400	mV
	Receiver Input voltage requirement, V_{ID}=|SRXDIP–SRXDIN|		150			mV
$V_{(CMR)}$	Receiver common mode voltage range		1100	1250	2250	mV
I_I	Receiver input leakage		-550		550	µA
R_I	Receiver differential impedance		80	100	120	Ω
C_I	Receiver input capacitance				1	pF
$t_{d(TX_Latency)}$					50	Bit Times
$t_{d(RX_Latency)}$					50	

(1) The ±20 ppm tolerance is required to meet SONET/SDH requirements. For non-SONET/SDH compliant systems, looser tolerances may apply.

SERIAL DIFFERENTIAL SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_t	Differential signal rise time (20% to 80%)	R_L = 50Ω	80	100	140	ps
t_j	Output jitter	Jitter-free data, 12 kHz to 20 MHz, RLOOP = 1		0.05	0.1	$UI_{(pp)}$
	Jitter tolerance	RLOOP = 1, See Figure 2, Figure 12				
		RLOOP = 1, OC-12, f = 250 kHz to 5 MHz	0.4			$UI_{(pp)}$
	Jitter transfer	RLOOP = 1, See Figure 2				

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TYPICAL CHARACTERISTICS

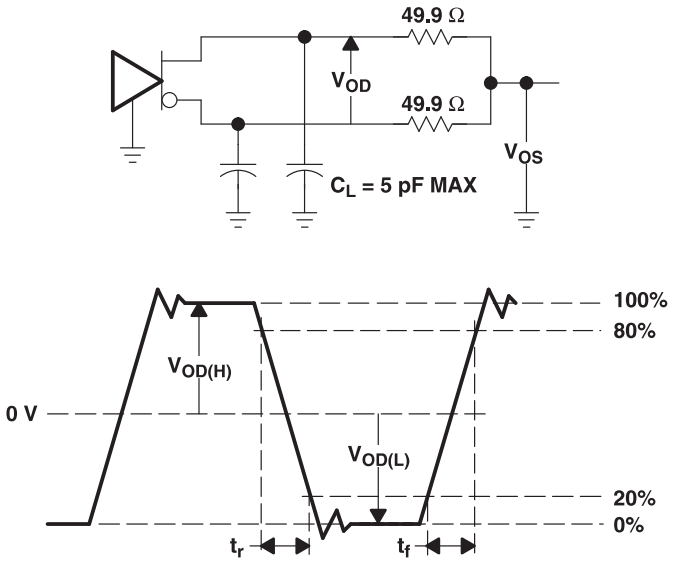


Figure 6. Test Load and Voltage Definitions for LVDS Outputs

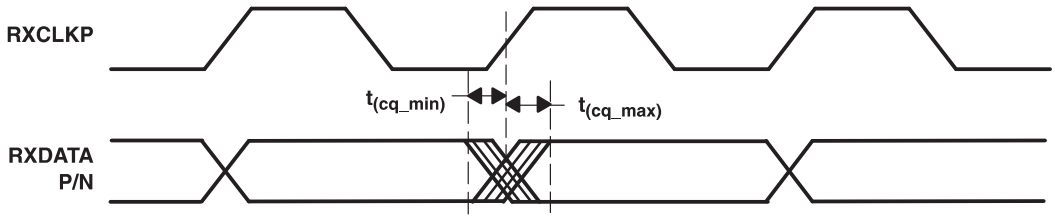


Figure 7. LVDS Output Waveform

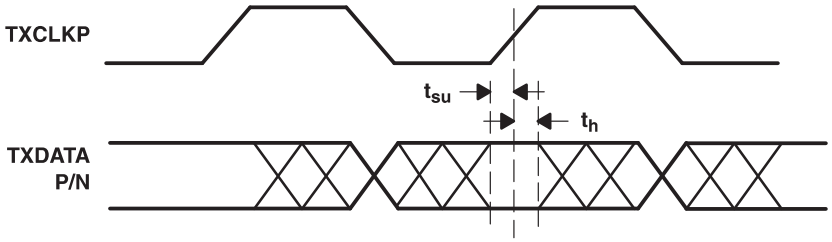


Figure 8. LVDS Input Waveform

APPLICATION INFORMATION

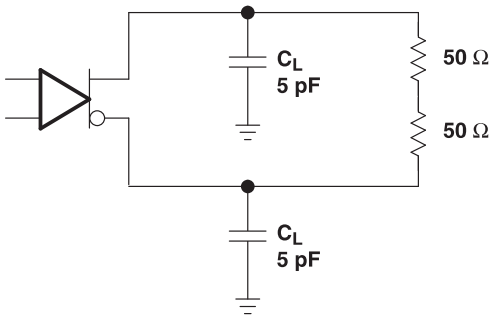


Figure 9. Transmitter Test Setup

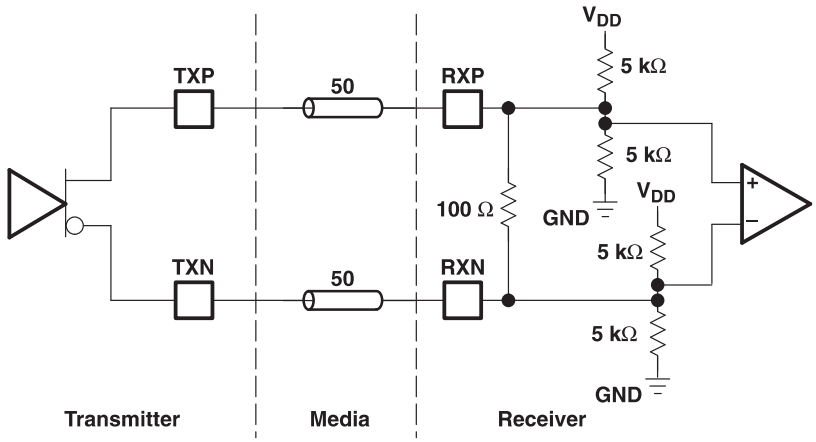


Figure 10. High-Speed I/O Directly Coupled Mode

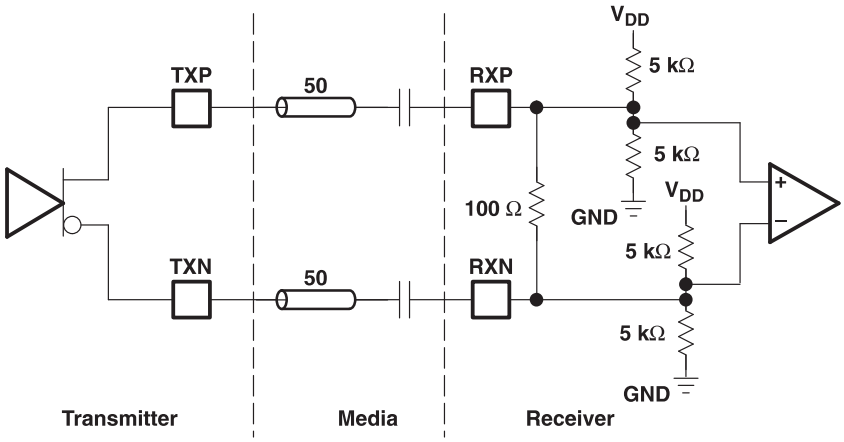


Figure 11. High-Speed I/O AC Coupled Mode

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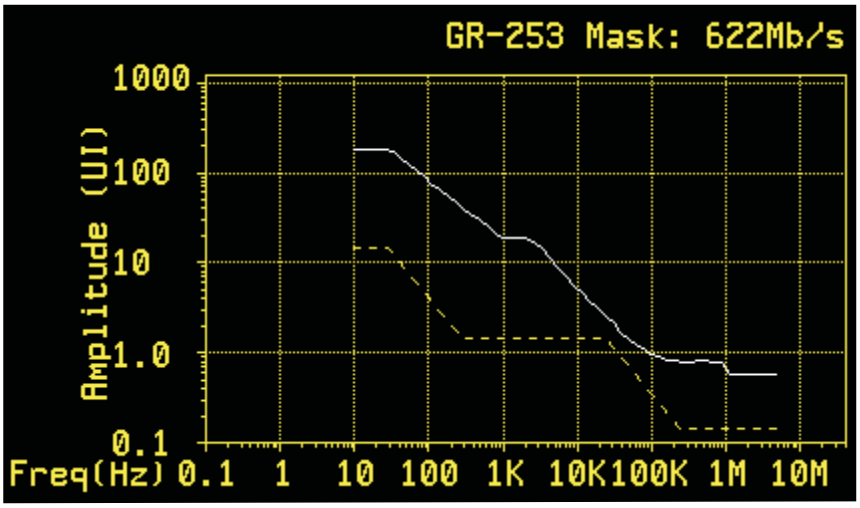


Figure 12. Jitter Tolerance Performance: 622 Mbps

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DESIGNING WITH THE PowerPAD PACKAGE

The SLK2511B is housed in high-performance, thermally enhanced, 100-pin PZP PowerPAD packages. Use of a PowerPAD package does not require any special considerations except to note that the PowerPAD, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Correct device operation requires that the PowerPAD be soldered to the thermal land. Do not run any etches or signal vias under the device, but have only a grounded thermal land, as explained below. Although the actual size of the exposed die pad may vary, the minimum size required for the keepout area for the 100-pin PZP PowerPAD package is 12 mm $\times$ 12 mm.

A thermal land, which is an area of solder-tinned-copper, is required underneath the PowerPAD package. The thermal land varies in size depending on the PowerPAD package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias, depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the TI application note *PowerPAD™ Thermally Enhanced Package* Application Report, TI literature number SLMA002, available via the TI Web pages beginning at URL http://www.ti.com.

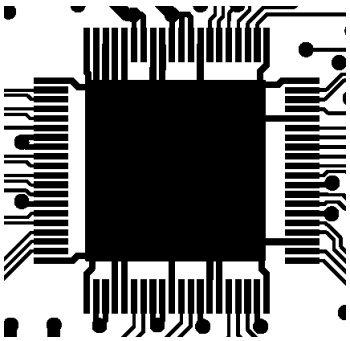


Figure 13. Example of a Thermal Land

For the SLK2511B, this thermal land should be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size should be as large as possible without shorting device signal terminals. The thermal land may be soldered to the exposed PowerPAD using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low-impedance ground plane of the device. More information may be obtained from the TI application note *PHY Layout*, TI literature number SLLA020.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SLK2511BPZP	LIFEBUY	HTQFP	PZP	100		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

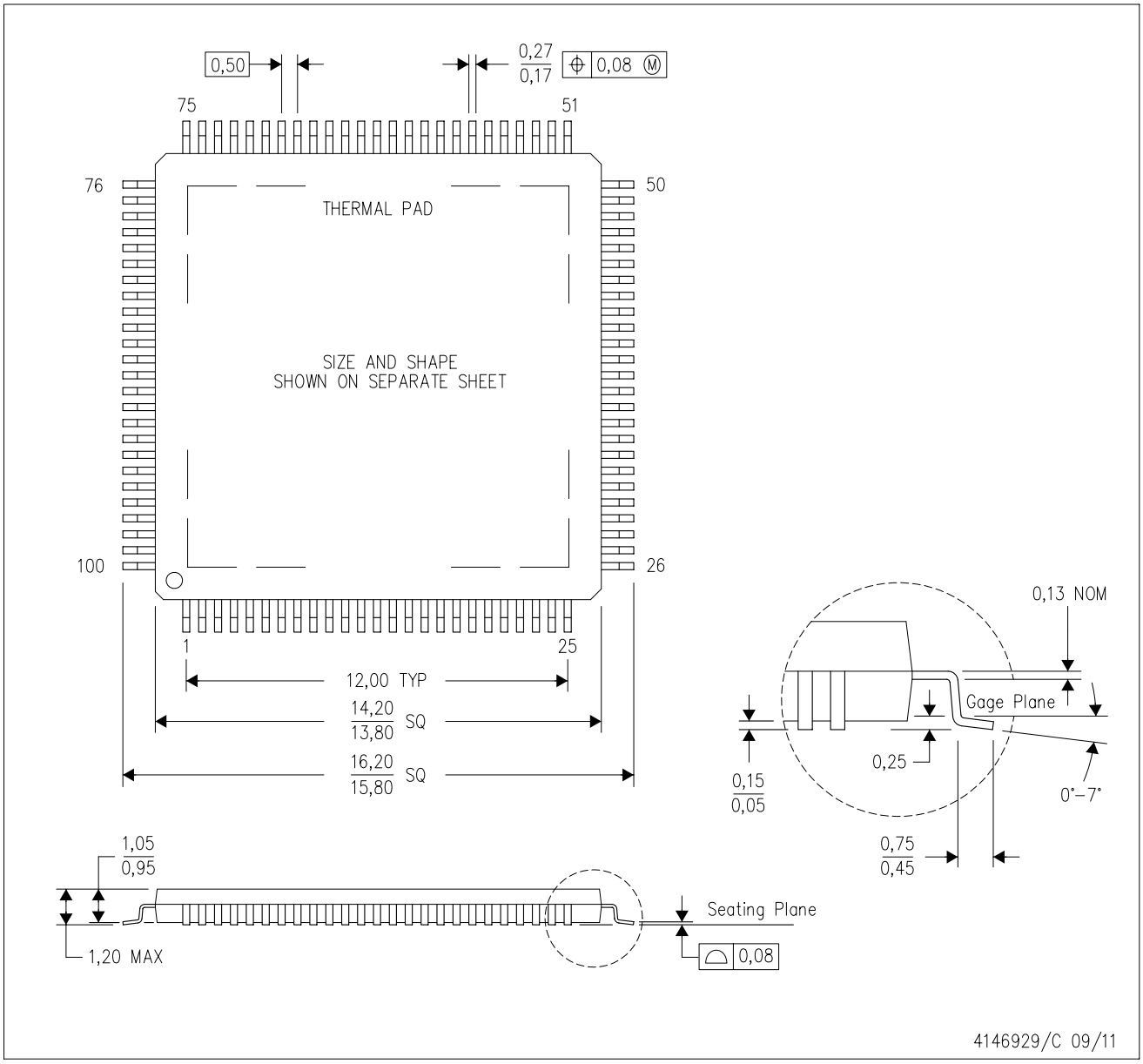
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

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