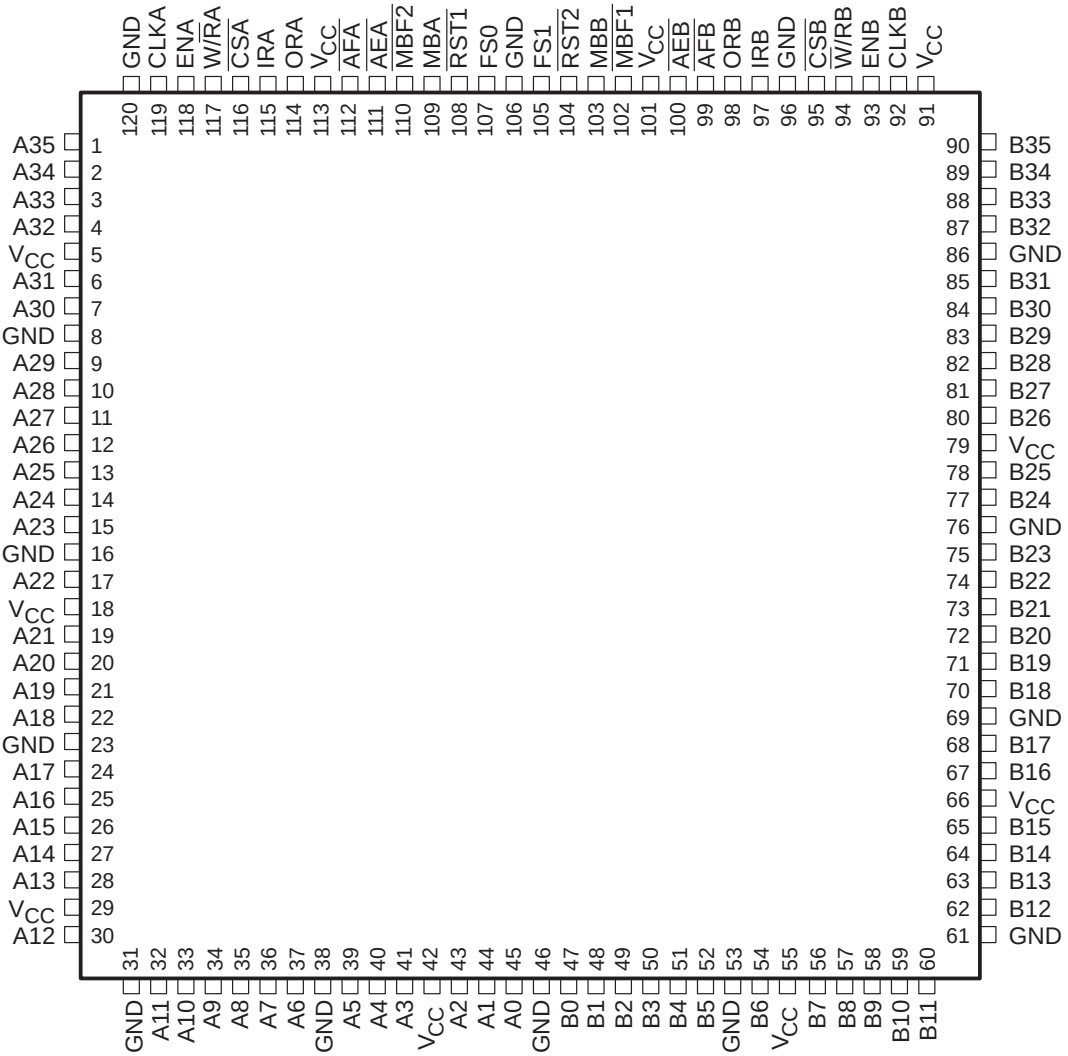
- **Free-Running CLKA and CLKB Can Be Asynchronous or Coincident**
- **Two Independent Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox-Bypass Register for Each FIFO**
- **Programmable Almost-Full and Almost-Empty Flags**
- **Microprocessor Interface Control Logic**
- **IRA, ORA, $\overline{\text{AEA}}$, and $\overline{\text{AFA}}$ Flags Synchronized by CLKA**
- **IRB, ORB, $\overline{\text{AEB}}$, and $\overline{\text{AFB}}$ Flags Synchronized by CLKB**
- **Low-Power 0.8 μm Advanced CMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 11 ns**
- **Pin-to-Pin Compatible With the SN74ACT3632 and SN74ACT3642**
- **Package Options Include 120-Pin Thin Quad Flat (PCB) and 132-Pin Plastic Quad Flat (PQ) Packages**

PCB PACKAGE
(TOP VIEW)

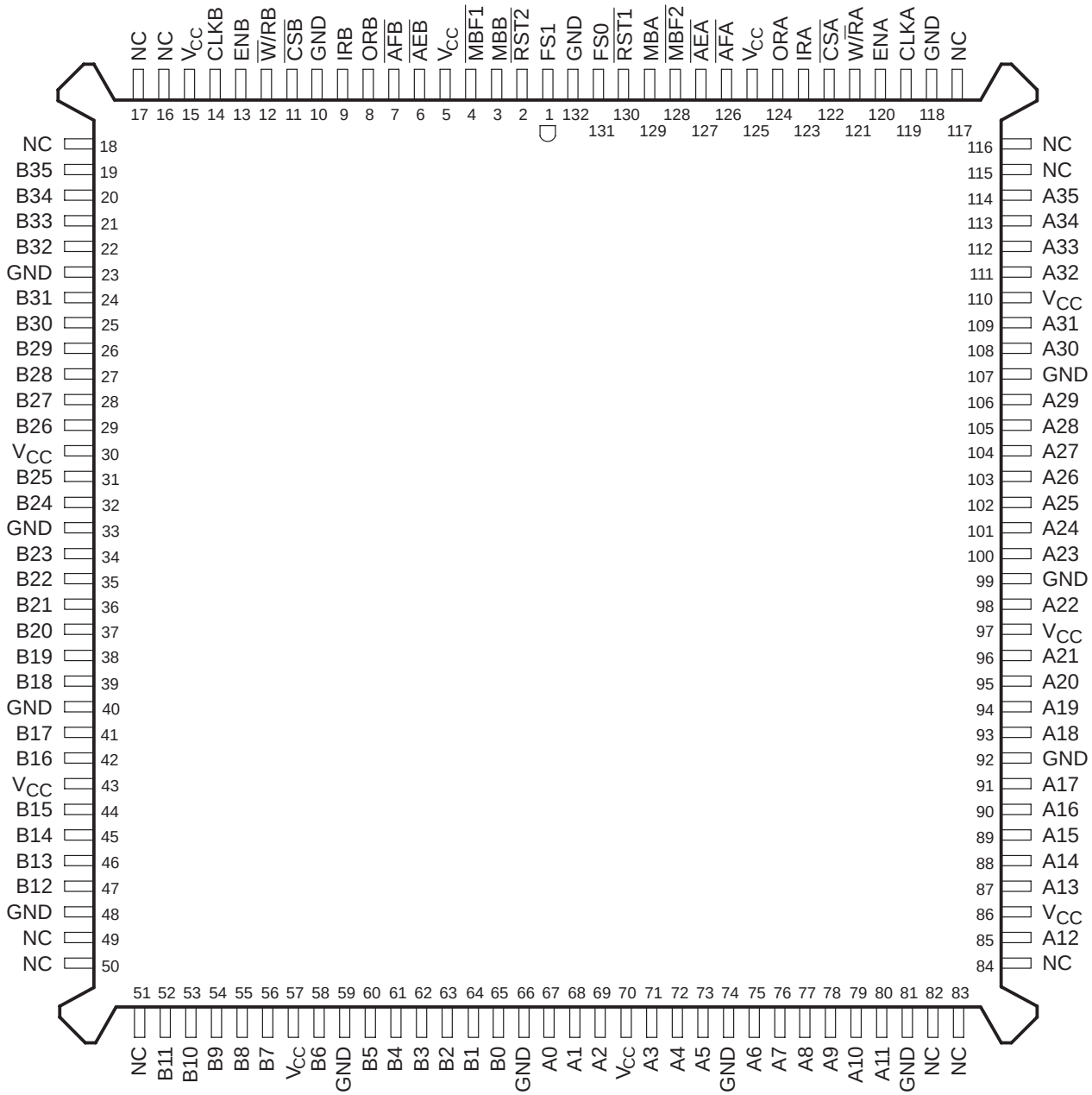


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PQ PACKAGE†
(TOP VIEW)



NC – No internal connection
† Uses Yamaichi socket IC51-1324-828

description

The SN74ACT3622 is a high-speed, low-power CMOS clocked bidirectional FIFO memory. It supports clock frequencies up to 67 MHz with read access times of 11 ns. Two independent 256 × 36 dual-port SRAM FIFOs on the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags almost full ($\overline{AF}$) and almost empty ($\overline{AE}$) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices can be used in parallel to create wider datapaths.

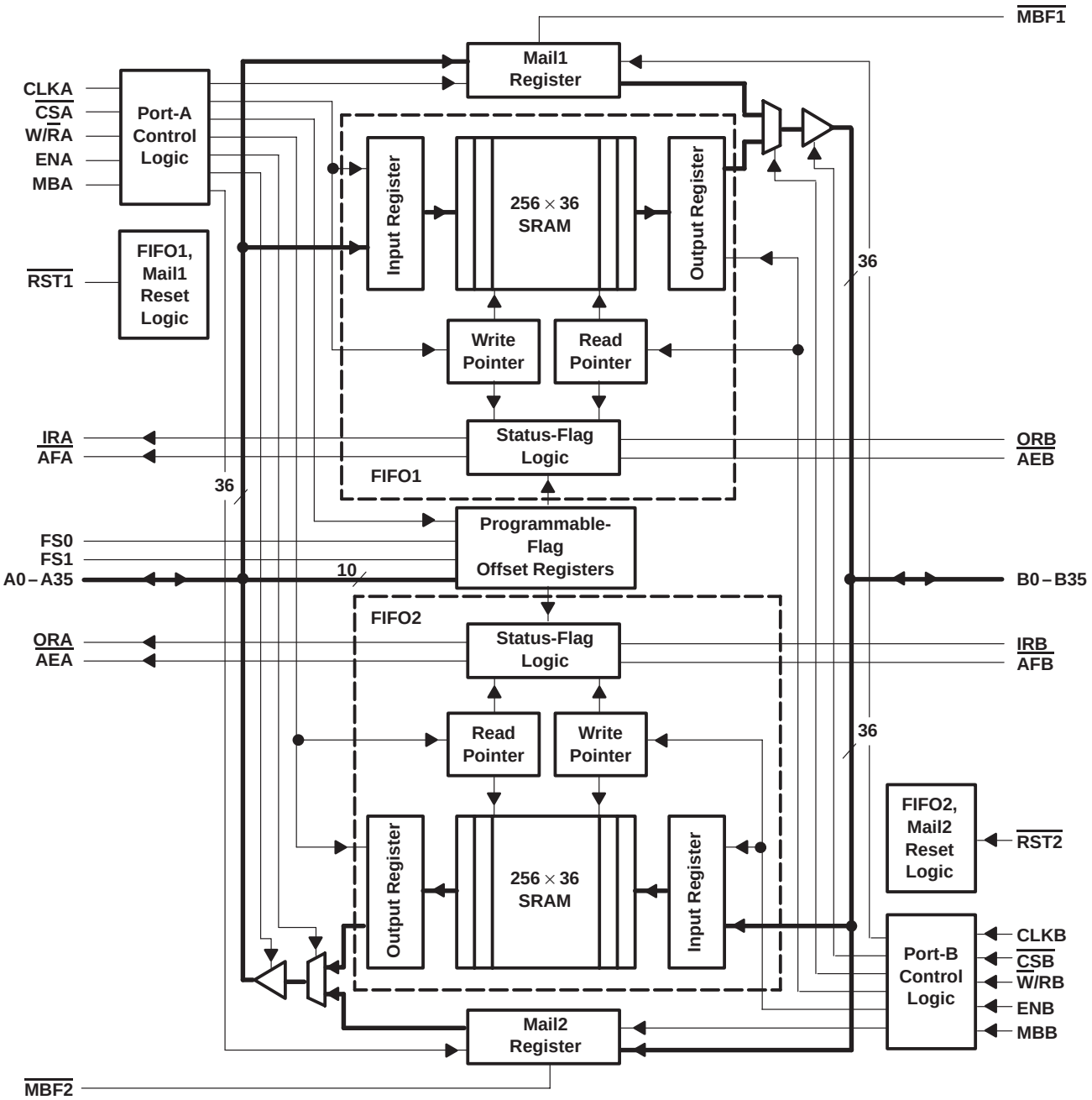
The SN74ACT3622 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The input-ready (IRA, IRB) flag and almost-full ($\overline{AFA}$, $\overline{AFB}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output-ready (ORA, ORB) flag and almost-empty ($\overline{AEA}$, $\overline{AEB}$) flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the $\overline{AF}$ and $\overline{AE}$ flags of the FIFO can be programmed from port A.

The SN74ACT3622 is characterized for operation from 0°C to 70°C.

For more information on this device family, see the application report *FIFO Mailbox-Bypass Registers: Using Bypass Registers to Initialize DMA Control* (literature number SCAA007) and *Metastability Performance of Clocked FIFOs* (literature number SCZA004).

functional block diagram



Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A35	I/O	Port-A data. The 36-bit bidirectional data port for side A.
$\overline{AEA}$	O (port A)	Port-A almost-empty flag. Programmable flag synchronized to CLKA. $\overline{AEA}$ is low when the number of words in FIFO2 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{AEB}$	O (port B)	Port-B almost-empty flag. Programmable flag synchronized to CLKB. $\overline{AEB}$ is low when the number of words in FIFO1 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{AFA}$	O (port A)	Port-A almost-full flag. Programmable flag synchronized to CLKA. $\overline{AFA}$ is low when the number of empty locations in FIFO1 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{AFB}$	O (port B)	Port-B almost-full flag. Programmable flag synchronized to CLKB. $\overline{AFB}$ is low when the number of empty locations in FIFO2 is less than or equal to the value in the almost-full B offset register, Y2.
B0–B35	I/O	Port-B data. The 36-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the low-to-high transition of CLKA.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port-A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port-B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
ENA	I	Port-A enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port-B enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO $\overline{AF}$ and $\overline{AE}$ flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost-full and almost-empty offsets for both FIFOs.
IRA	O (port A)	Input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O (port B)	Input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port-A mailbox select. A high level on MBA chooses a mailbox register for a port-A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output and a low level selects FIFO2 output-register data for output.
MBB	I	Port-B mailbox select. A high level on MBB chooses a mailbox register for a port-B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output and a low level selects FIFO1 output-register data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by a low-to-high transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is low. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port-B read is selected and MBB is high. $\overline{MBF1}$ is set high when FIFO1 is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by a low-to-high transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is low. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port-A read is selected and MBA is high. $\overline{MBF2}$ is also set high when FIFO2 is reset.
ORA	O (port A)	Output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

Terminal Functions (continued)

TERMINAL NAME	I/O	DESCRIPTION
ORB	O (port B)	Output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{\text{RST1}}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST1}}$ is low. The low-to-high transition of $\overline{\text{RST1}}$ latches the status of FS0 and FS1 for $\overline{\text{AFA}}$ and $\overline{\text{AEB}}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{\text{RST2}}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RST2}}$ is low. The low-to-high transition of $\overline{\text{RST2}}$ latches the status of FS0 and FS1 for $\overline{\text{AFB}}$ and $\overline{\text{AEA}}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{\text{RA}}$	I	Port-A write/read select. A high on W/$\overline{\text{RA}}$ selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is high.
$\overline{\text{W}}$/RB	I	Port-B write/read select. A low on $\overline{\text{W}}$/RB selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{\text{W}}$/RB is low.

detailed description

reset

The FIFO memories of the SN74ACT3622 are reset separately by taking their reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) inputs low for at least four port-A clock (CLKA) and four port-B clock (CLKB) low-to-high transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready (IRA, IRB) flag low, the output-ready (ORA, ORB) flag low, the almost-empty ($\overline{\text{AEA}}$, $\overline{\text{AEB}}$) flag low, and the almost-full ($\overline{\text{AFA}}$, $\overline{\text{AFB}}$) flag high. Resetting a FIFO also forces the mailbox ($\overline{\text{MBF1}}$, $\overline{\text{MBF2}}$) flag of the parallel mailbox register high. After a FIFO is reset, its IR flag is set high after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A low-to-high transition on a FIFO reset ($\overline{\text{RST1}}$, $\overline{\text{RST2}}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see *almost-empty flag and almost-full flag offset programming*).

almost-empty flag and almost-full flag offset programming

Four registers in the SN74ACT3622 are used to hold the offset values for the $\overline{\text{AE}}$ and $\overline{\text{AF}}$ flags. The port-B almost-empty ($\overline{\text{AEB}}$) flag offset register is labeled X1 and the port-A almost-empty ($\overline{\text{AEA}}$) flag offset register is labeled X2. The port-A almost-full ($\overline{\text{AFA}}$) flag offset register is labeled Y1 and the port-B almost-full ($\overline{\text{AFB}}$) flag offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1).

almost-empty flag and almost-full flag offset programming (continued)

Table 1. Flag Programming

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS†	X2 AND Y2 REGISTERS‡
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

† X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
‡ X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

To load the FIFO $\overline{AE}$ flag and $\overline{AF}$ flag offset registers with one of the three preset values listed in Table 1, at least one of the flag-select inputs must be high during the low-to-high transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be high when FIFO1 reset ($\overline{RST1}$) returns high. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{RST2}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. Each offset register uses port-A inputs (A7–A0). The highest numbered input is used as the most-significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 252. After all the offset registers are programmed from port A, the port-B input-ready (IRB) flag is set high and both FIFOs begin normal operation.

FIFO write/read operation

The state of the port-A data (A0–A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0–A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. The A0–A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are low.

Data is loaded into FIFO1 from the A0–A35 inputs on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, ENA is high, MBA is low, and IRA is high. Data is read from FIFO2 to the A0–A35 outputs by a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, ENA is high, MBA is low, and ORA is high (see Table 2). FIFO reads and writes on port A are independent of any concurrent port-B operation.

Table 2. Port-A Enable Function Table

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0–A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ high)

FIFO write/read operation (continued)

The port-B control signals are identical to those of port A, with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{R}$A). The state of the port-B data (B0–B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select ($\overline{W}$/RB). The B0–B35 outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. The B0–B35 outputs are active when $\overline{CSB}$ is low and $\overline{W}$/RB is high.

Data is loaded into FIFO2 from the B0–B35 inputs on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, MBB is low, and IRB is high. Data is read from FIFO1 to the B0–B35 outputs by a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, ENB is high, MBB is low, and ORB is high (see Table 3). FIFO reads and writes on port B are independent of any concurrent port-A operation.

Table 3. Port-B Enable Function Table

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B0–B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ high)

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is low during a clock cycle, the port-chip select and write/read select may change states during the setup- and hold-time window of the cycle.

When a FIFO OR flag is low, the next data word is sent to the FIFO output register automatically by the low-to-high transition of the port clock that sets the OR flag high. When the OR flag is high, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

synchronized FIFO flags

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. ORA, $\overline{AEA}$, IRA, and $\overline{AFA}$ are synchronized to CLKA. ORB, $\overline{AEB}$, IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

synchronized FIFO flags (continued)

Table 4. FIFO1 Flag Operation

NUMBER OF WORDS IN FIFO1†‡	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	ORB	$\overline{\text{AEB}}$	$\overline{\text{AFA}}$	IRA
0	L	L	H	H
1 to X1	H	L	H	H
(X1 + 1) to [256 – (Y1 + 1)]	H	H	H	H
(256 – Y1) to 255	H	H	L	H
256	H	H	L	L

† X1 is the almost-empty offset for FIFO1 used by $\overline{\text{AEB}}$. Y1 is the almost-full offset for FIFO1 used by $\overline{\text{AFA}}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.
‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

Table 5. FIFO2 Flag Operation

NUMBER OF WORDS IN FIFO2†‡	SYNCHRONIZED TO CLKA		SYNCHRONIZED TO CLKB	
	ORA	$\overline{\text{AEA}}$	$\overline{\text{AFB}}$	IRB
0	L	L	H	H
1 to X2	H	L	H	H
(X2 + 1) to [256 – (Y2 + 1)]	H	H	H	H
(256 – Y2) to 255	H	H	L	H
256	H	H	L	L

† X2 is the almost-empty offset for FIFO2 used by $\overline{\text{AEA}}$. Y2 is the almost-full offset for FIFO2 used by $\overline{\text{AFB}}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.
‡ When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

output-ready flags (ORA, ORB)

The OR flag of a FIFO is synchronized to the port clock that reads data from its array. When the OR flag is high, new data is present in the FIFO output register. When the OR flag is low, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the OR flag synchronizing clock; therefore, an OR flag is low if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The OR flag of the FIFO remains low until the third low-to-high transition of the synchronizing clock occurs, simultaneously forcing the OR flag high and shifting the word to the FIFO output register.

A low-to-high transition on an OR flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{sk1}, or greater, after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

input-ready flags (IRA, IRB)

The IR flag of a FIFO is synchronized to the port clock that writes data to its array. When the IR flag is high, a memory location is free in the SRAM to receive new data. No memory locations are free when the IR flag is low and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the IR flag synchronizing clock; therefore, an IR flag is low if less than two cycles of the IR flag synchronizing clock have elapsed since the next memory write location has been read. The second low-to-high transition on the IR flag synchronizing clock after the read sets the IR flag high.

A low-to-high transition on an IR flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{sk1}, or greater, after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

almost-empty flags ($\overline{AEA}$, $\overline{AEB}$)

The $\overline{AE}$ flag of a FIFO is synchronized to the port clock that reads data from its array. The $\overline{AE}$ state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An $\overline{AE}$ flag is low when its FIFO contains X or fewer words and is high when its FIFO contains (X + 1) or more words. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the $\overline{AE}$ flag synchronizing clock are required after a FIFO write for its $\overline{AE}$ flag to reflect the new level of fill; therefore, the $\overline{AE}$ flag of a FIFO containing (X + 1) or more words remains low if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X + 1) level. An $\overline{AE}$ flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO write that fills memory to the (X + 1) level. A low-to-high transition of an $\overline{AE}$ flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the write that fills the FIFO to (X + 1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 11 and 12).

almost-full flags ($\overline{AFA}$, $\overline{AFB}$)

The $\overline{AF}$ flag of a FIFO is synchronized to the port clock that writes data to its array. The $\overline{AF}$ state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming*). An $\overline{AF}$ flag is low when the number of words in its FIFO is greater than or equal to (256 – Y). An $\overline{AF}$ flag is high when the number of words in its FIFO is less than or equal to [256 – (Y + 1)]. A data word present in the FIFO output register has been read from memory.

Two low-to-high transitions of the $\overline{AF}$ flag synchronizing clock are required after a FIFO read for its $\overline{AF}$ flag to reflect the new level of fill; therefore, the $\overline{AF}$ flag of a FIFO containing [256 – (Y + 1)] or fewer words remains low if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256 – (Y + 1)]. An $\overline{AF}$ flag is set high by the second low-to-high transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256 – (Y + 1)]. A low-to-high transition of an $\overline{AF}$ flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{sk2}, or greater, after the read that reduces the number of words in memory to [256 – (Y + 1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figures 13 and 14).

mailbox registers

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A low-to-high transition on CLKA writes A0–A35 data to the mail1 register when a port-A write is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and with MBA high. A low-to-high transition on CLKB writes B0–B35 data to the mail2 register when a port-B write is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB and with MBB high. Writing data to a mail register sets its corresponding flag ($\overline{\text{MBF1}}$ or $\overline{\text{MBF2}}$) low. Attempted writes to a mail register are ignored while the mail flag is low.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port-mailbox-select input is low and from the mail register when the port-mailbox-select input is high. The mail1 register flag ($\overline{\text{MBF1}}$) is set high by a low-to-high transition on CLKB when a port-B read is selected by $\overline{\text{CSB}}$, $\overline{\text{W}}$/RB, and ENB and with MBB high. The mail2 register flag ($\overline{\text{MBF2}}$) is set high by a low-to-high transition on CLKA when a port-A read is selected by $\overline{\text{CSA}}$, W/$\overline{\text{RA}}$, and ENA and with MBA high. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

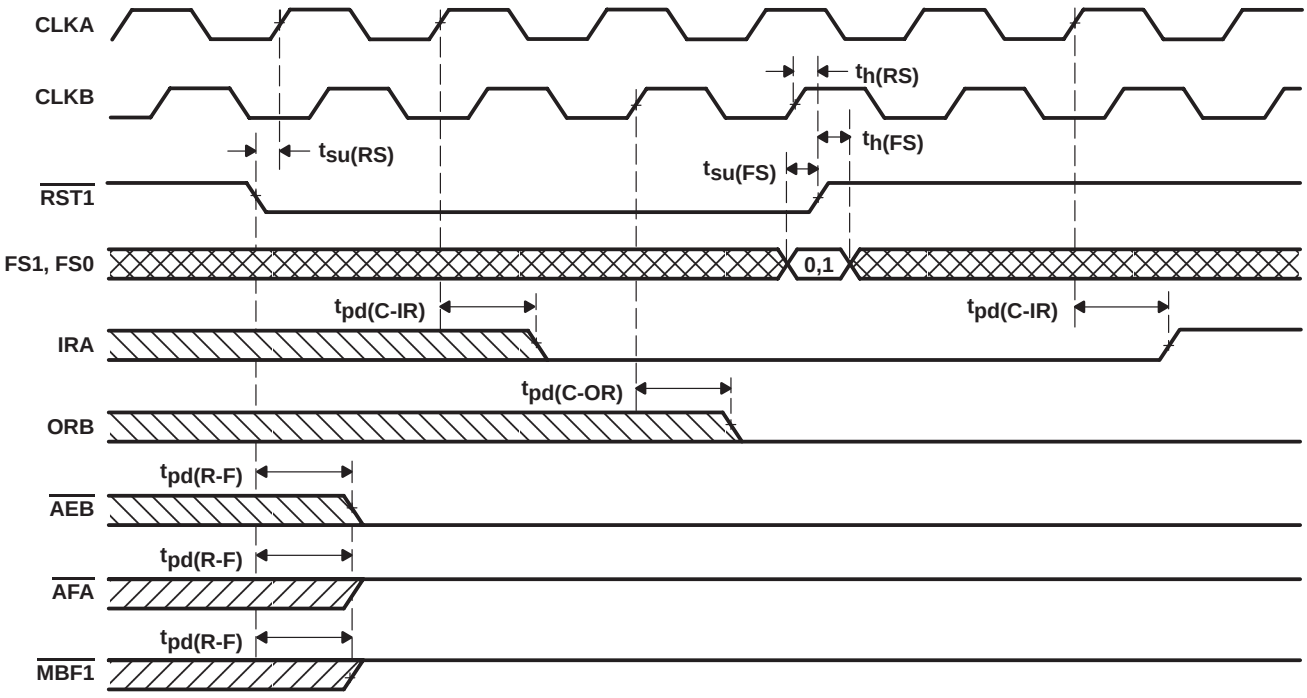
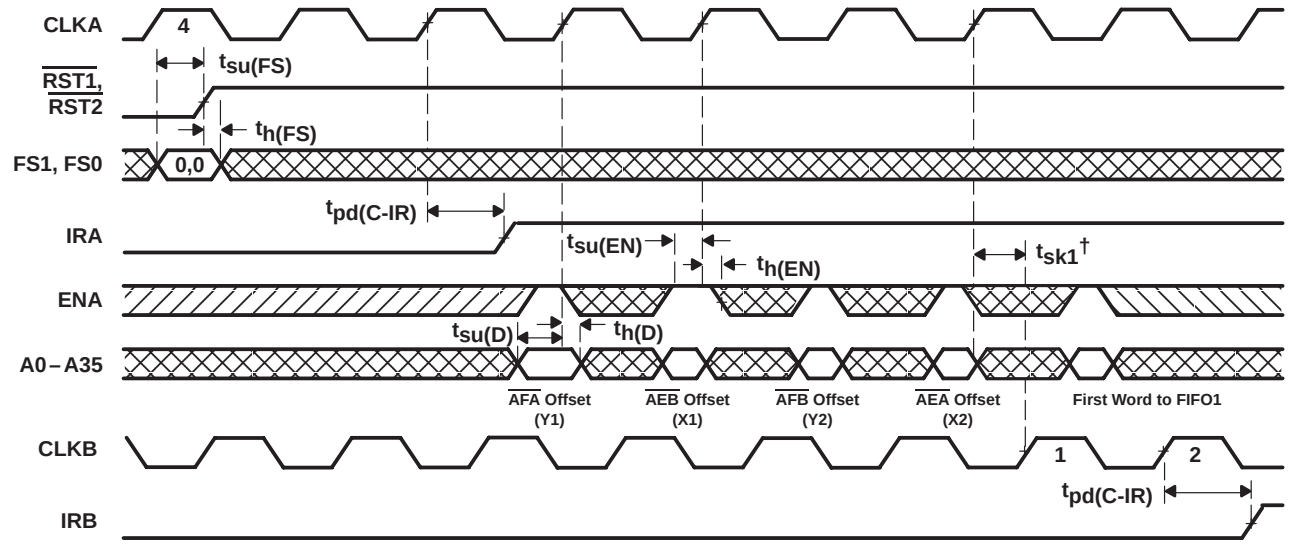


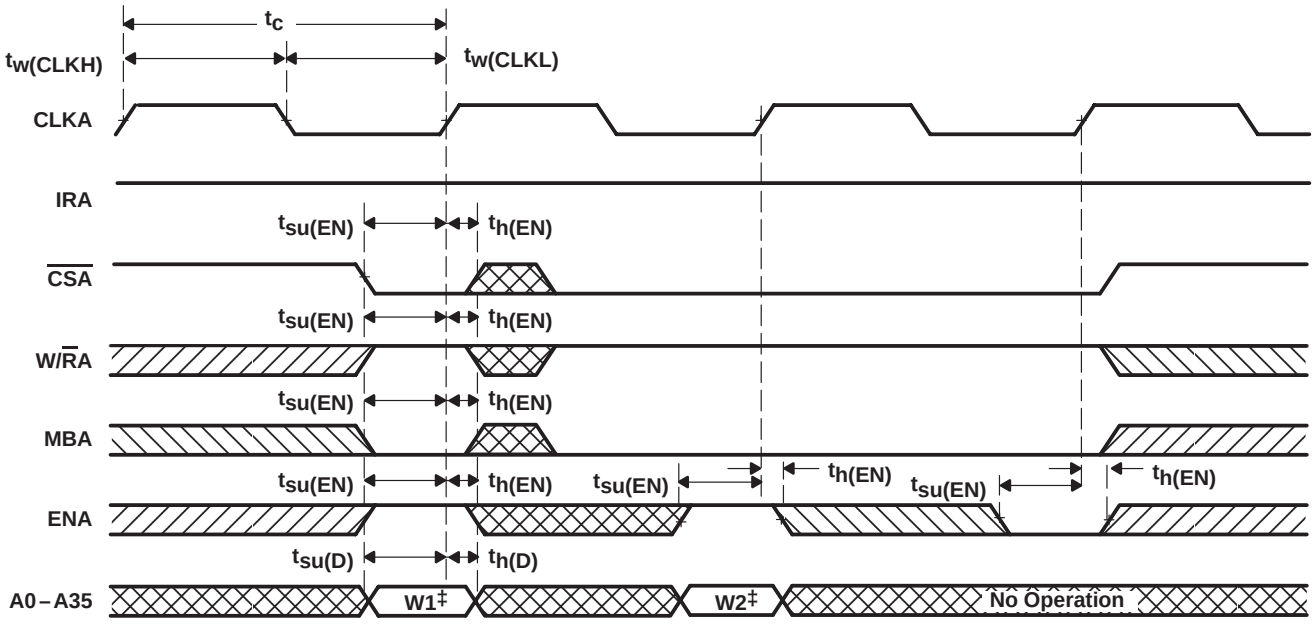
Figure 1. FIFO1 Reset Loading X1 and Y1 With a Preset Value of Eight†

† FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



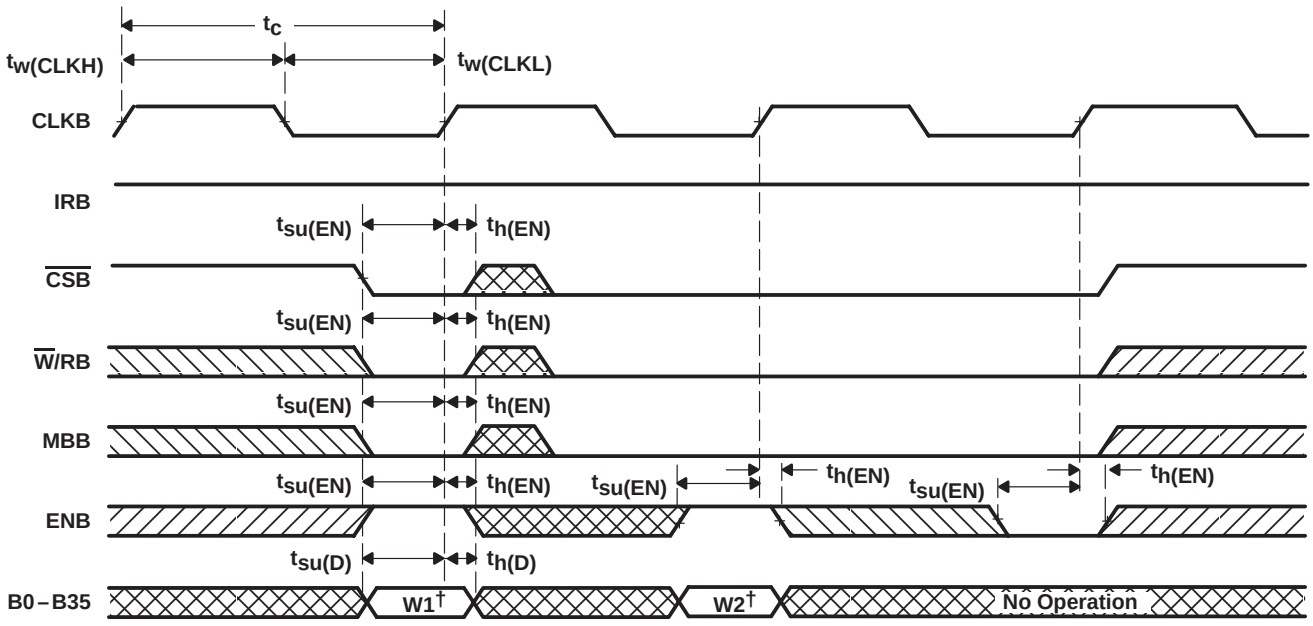
† t_{sk1} is the minimum time between the rising CLKA edge and a rising CLKB edge for IRB to transition high in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than t_{sk1}, IRB may transition high one cycle later than shown.
NOTE A: $\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the $\overline{AF}$ Flag and $\overline{AE}$ Flag Offset Values After Reset



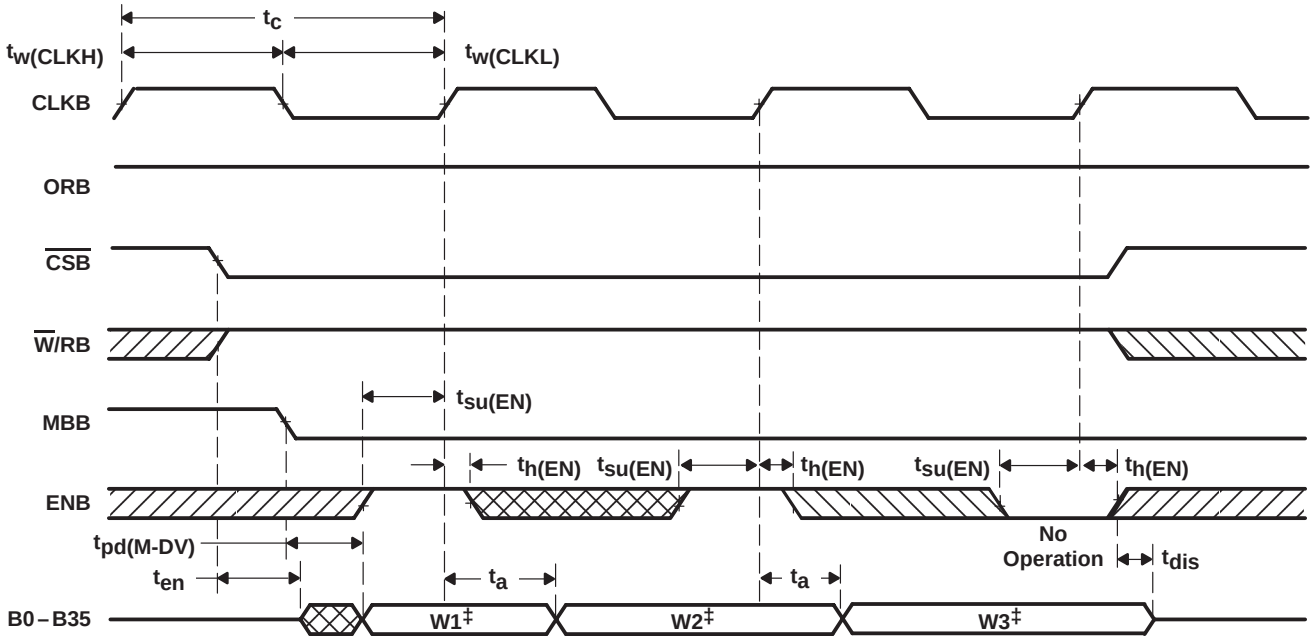
‡ Written to FIFO1

Figure 3. Port-A Write-Cycle Timing for FIFO1



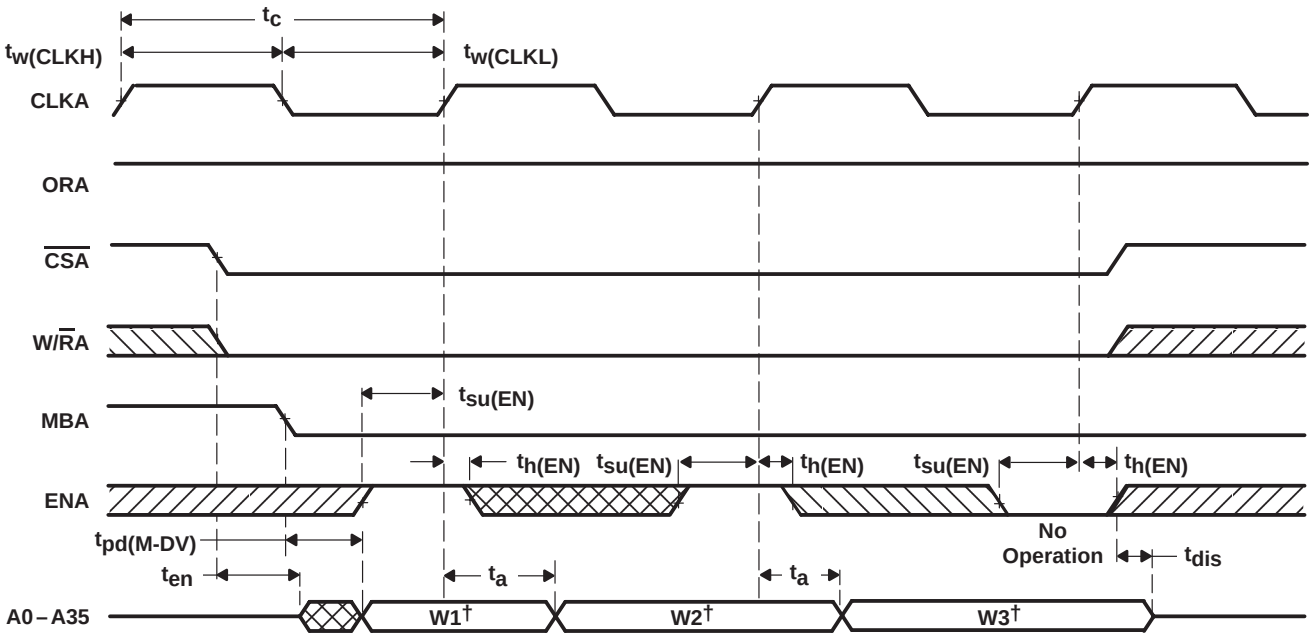
† Written to FIFO2

Figure 4. Port-B Write-Cycle Timing for FIFO2



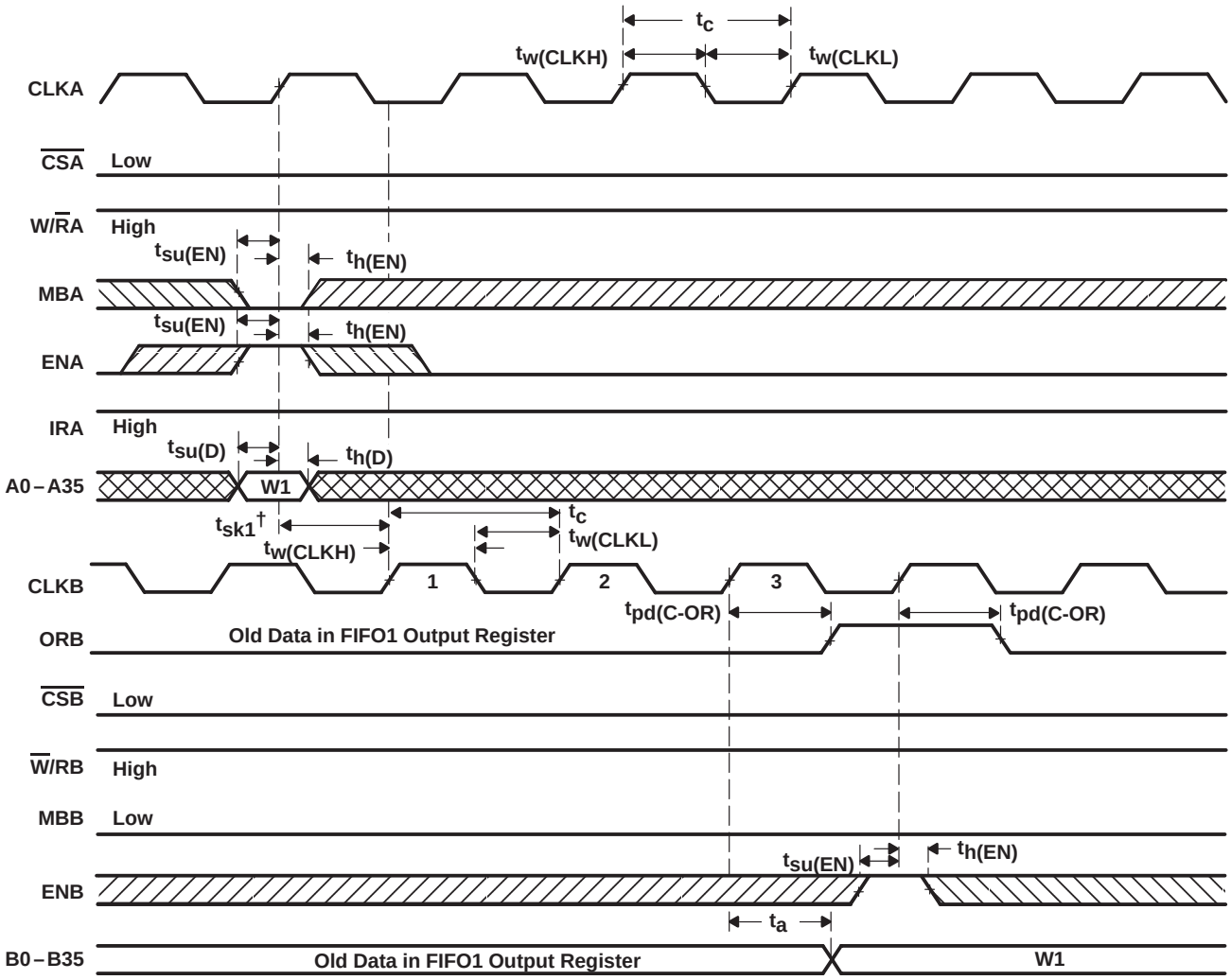
‡ Read from FIFO1

Figure 5. Port-B Read-Cycle Timing for FIFO1



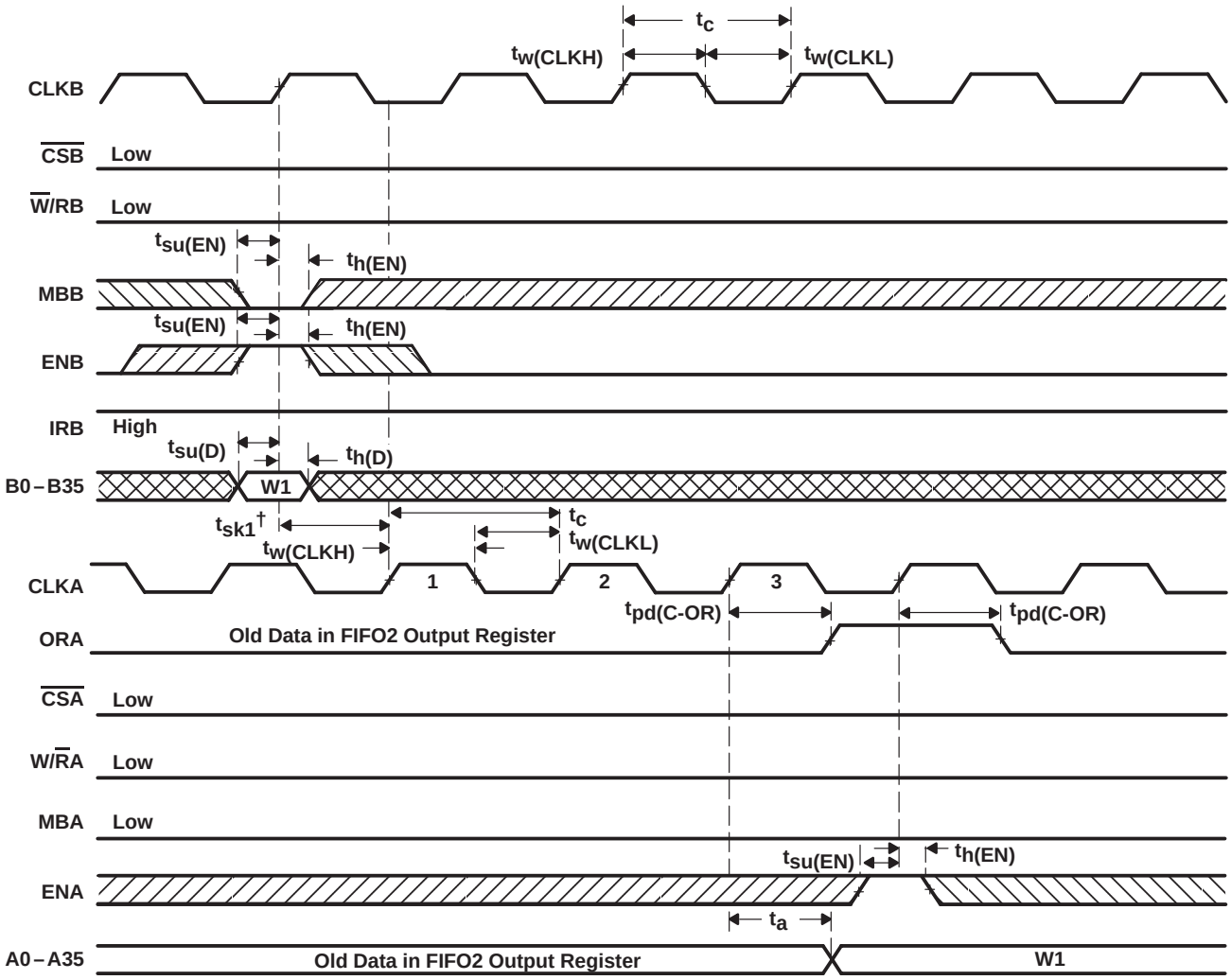
† Read from FIFO2

Figure 6. Port-A Read-Cycle Timing for FIFO2



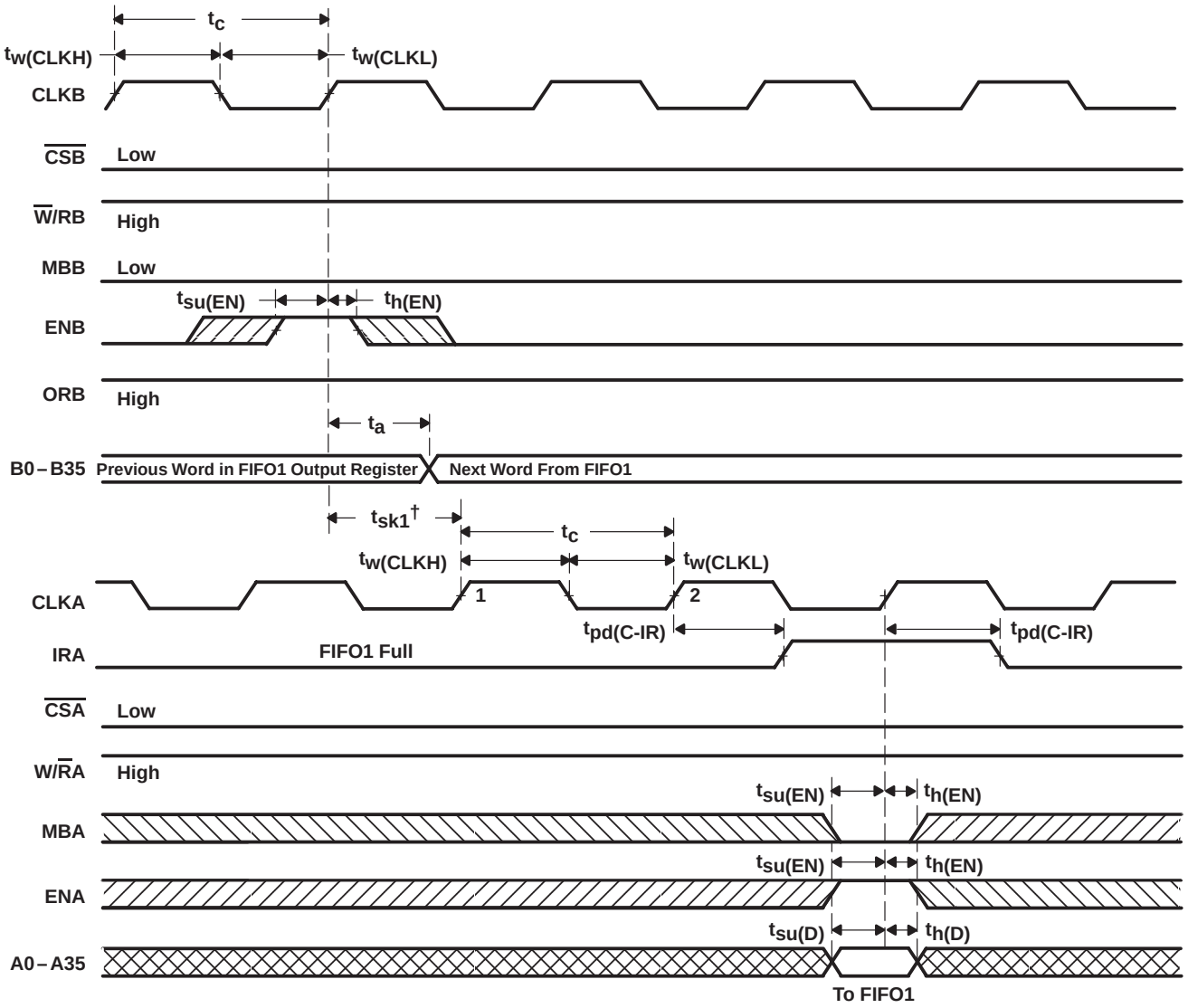
† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition high and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, the transition of ORB high and load of the first word to the output register may occur one CLKB cycle later than shown.

Figure 7. ORB-Flag Timing and First Data-Word Fall Through When FIFO1 Is Empty



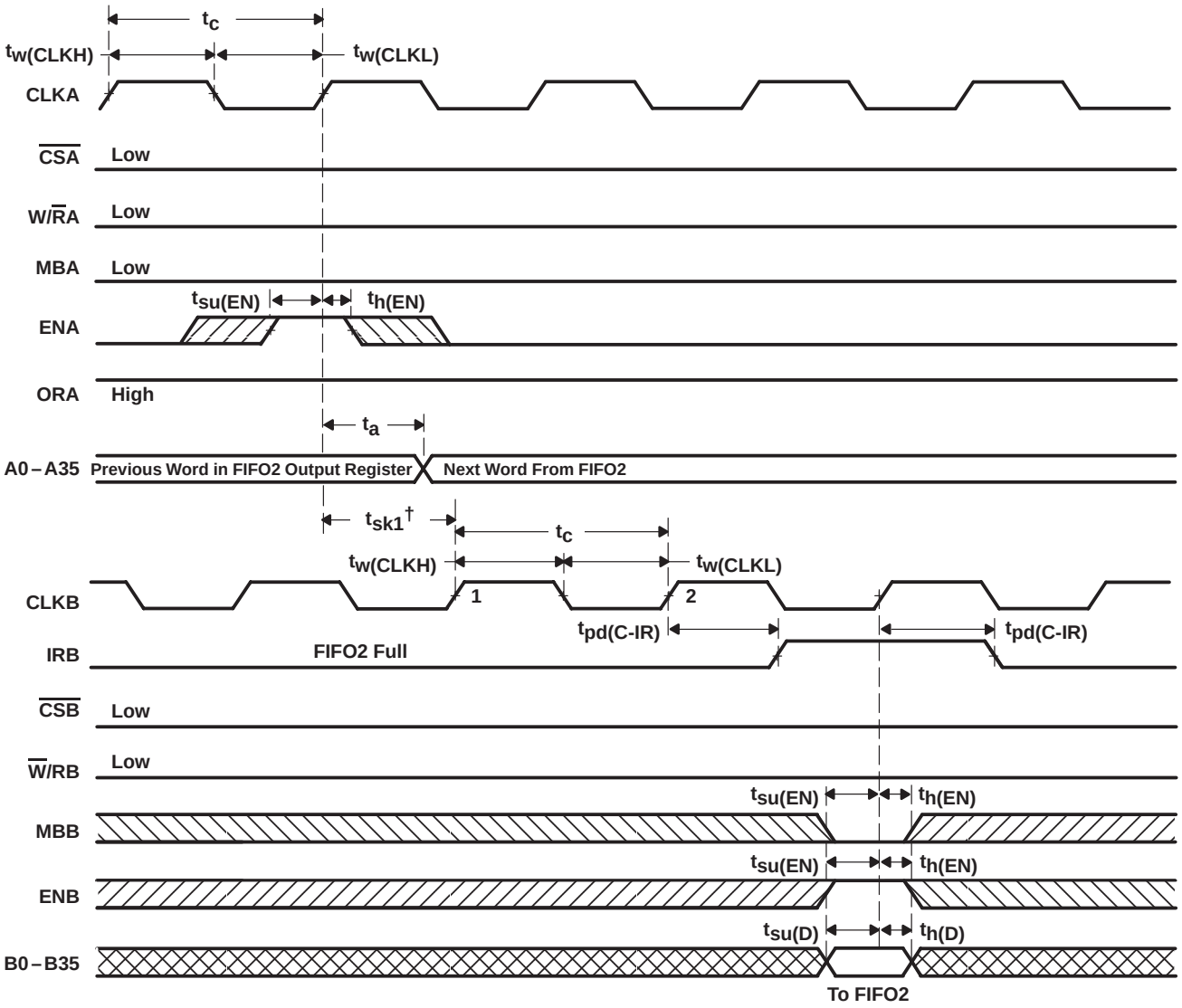
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition high and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, the transition of ORA high and load of the first word to the output register may occur one CLKA cycle later than shown.

Figure 8. ORA-Flag Timing and First Data-Word Fall Through When FIFO2 Is Empty



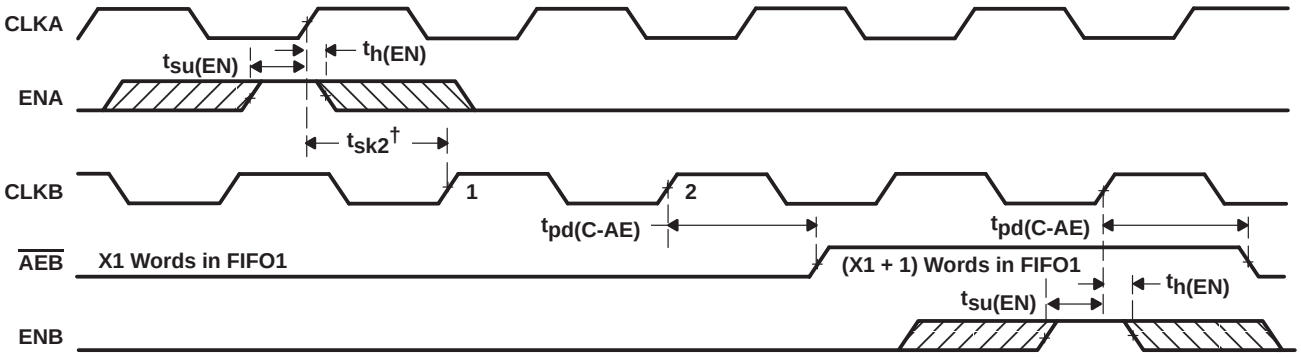
† t_{sk1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk1}, IRA may transition high one CLKA cycle later than shown.

Figure 9. IRA-Flag Timing and First Available Write When FIFO1 Is Full



† t_{sk1} is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk1}, IRB may transition high one CLKB cycle later than shown.

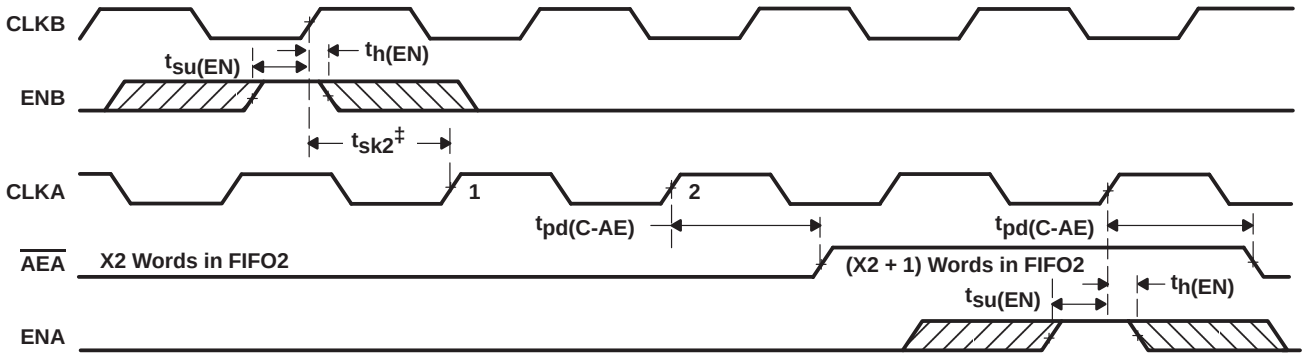
Figure 10. IRB-Flag Timing and First Available Write When FIFO2 Is Full



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition high in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AEB}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, W/$\overline{RB}$ = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

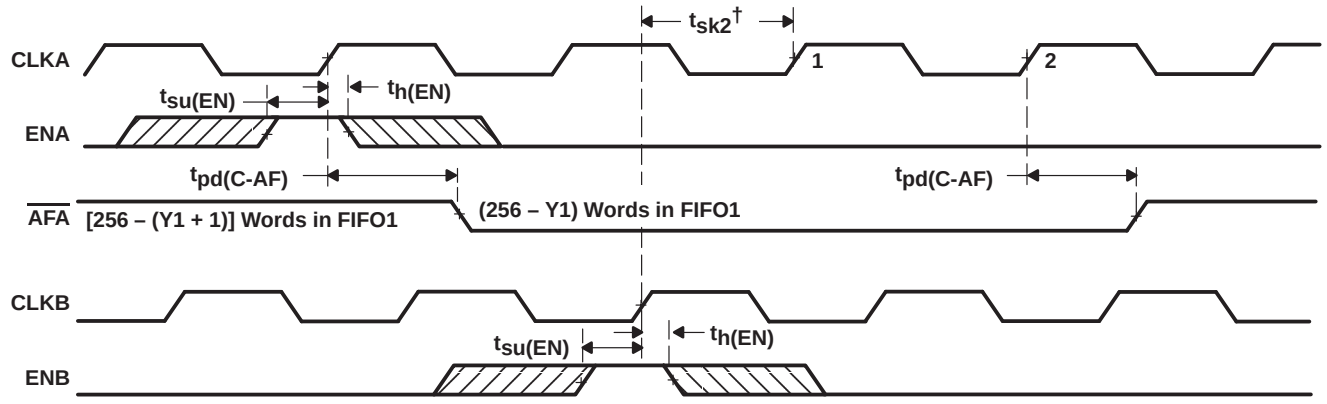
Figure 11. Timing for $\overline{AEB}$ When FIFO1 Is Almost Empty



‡ t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition high in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AEA}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

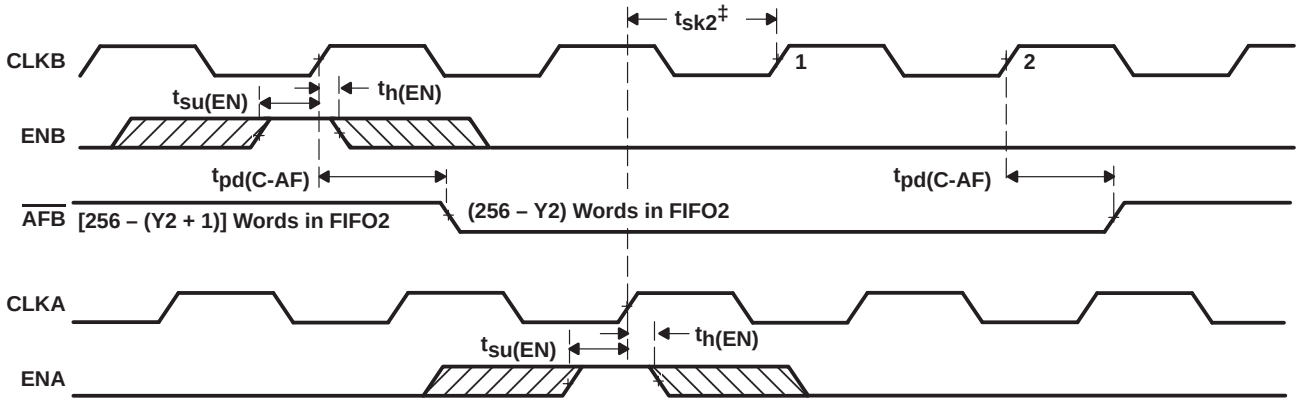
Figure 12. Timing for $\overline{AEA}$ When FIFO2 Is Almost Empty



† t_{sk2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition high in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{sk2}, $\overline{AFA}$ may transition high one CLKB cycle later than shown.

NOTE A: FIFO1 write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO1 read ($\overline{CSB}$ = L, $\overline{W}$/RB = H, MBB = L). Data in the FIFO1 output register has been read from the FIFO.

Figure 13. Timing for $\overline{AFA}$ When FIFO1 Is Almost Full



‡ t_{sk2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition high in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{sk2}, $\overline{AFB}$ may transition high one CLKA cycle later than shown.

NOTE A: FIFO2 write ($\overline{CSB}$ = L, $\overline{W}$/RB= L, MBB = L), FIFO2 read ($\overline{CSA}$ = L, W/$\overline{RA}$ = L, MBA = L). Data in the FIFO2 output register has been read from the FIFO.

Figure 14. Timing for $\overline{AFB}$ When FIFO2 Is Almost Full

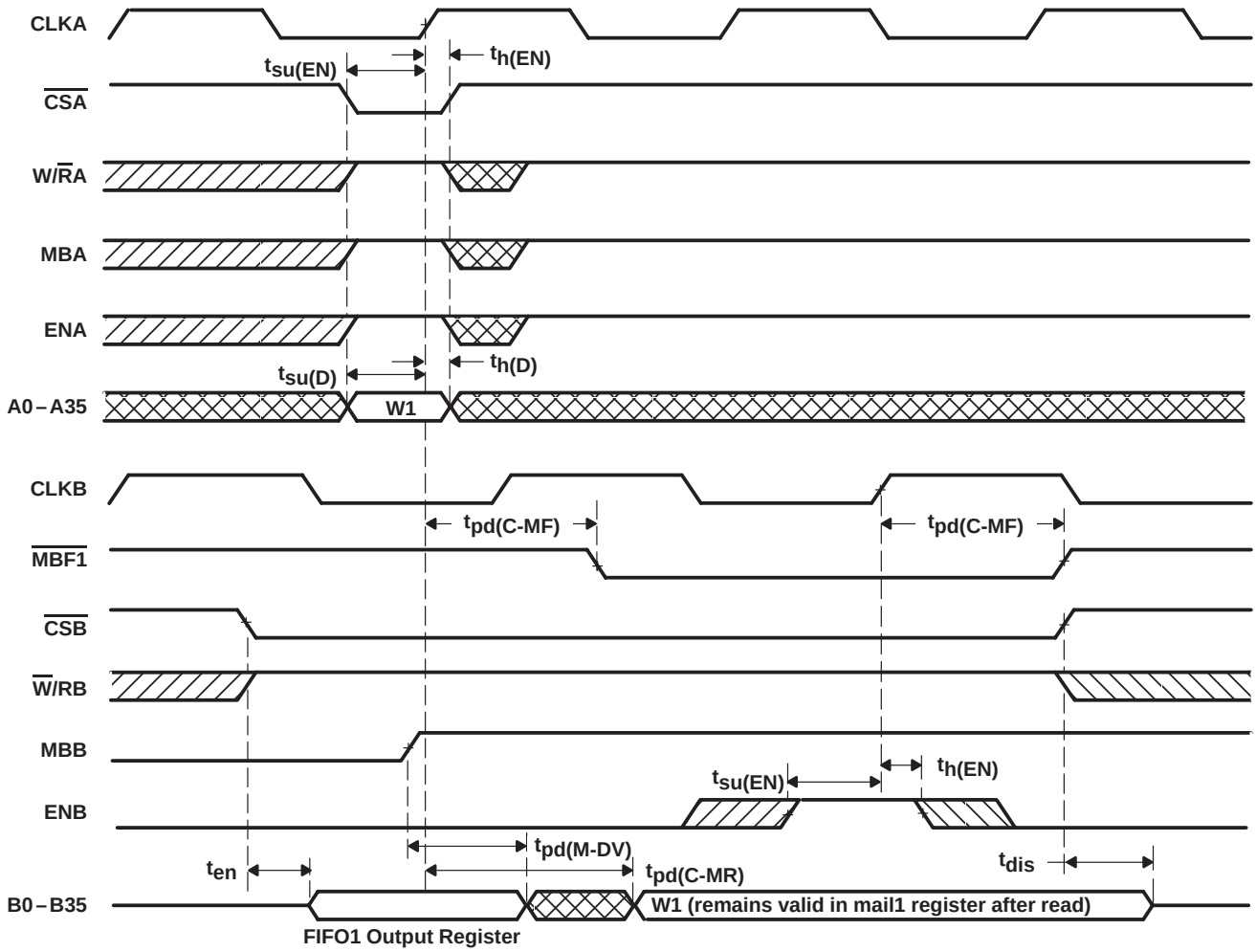


Figure 15. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

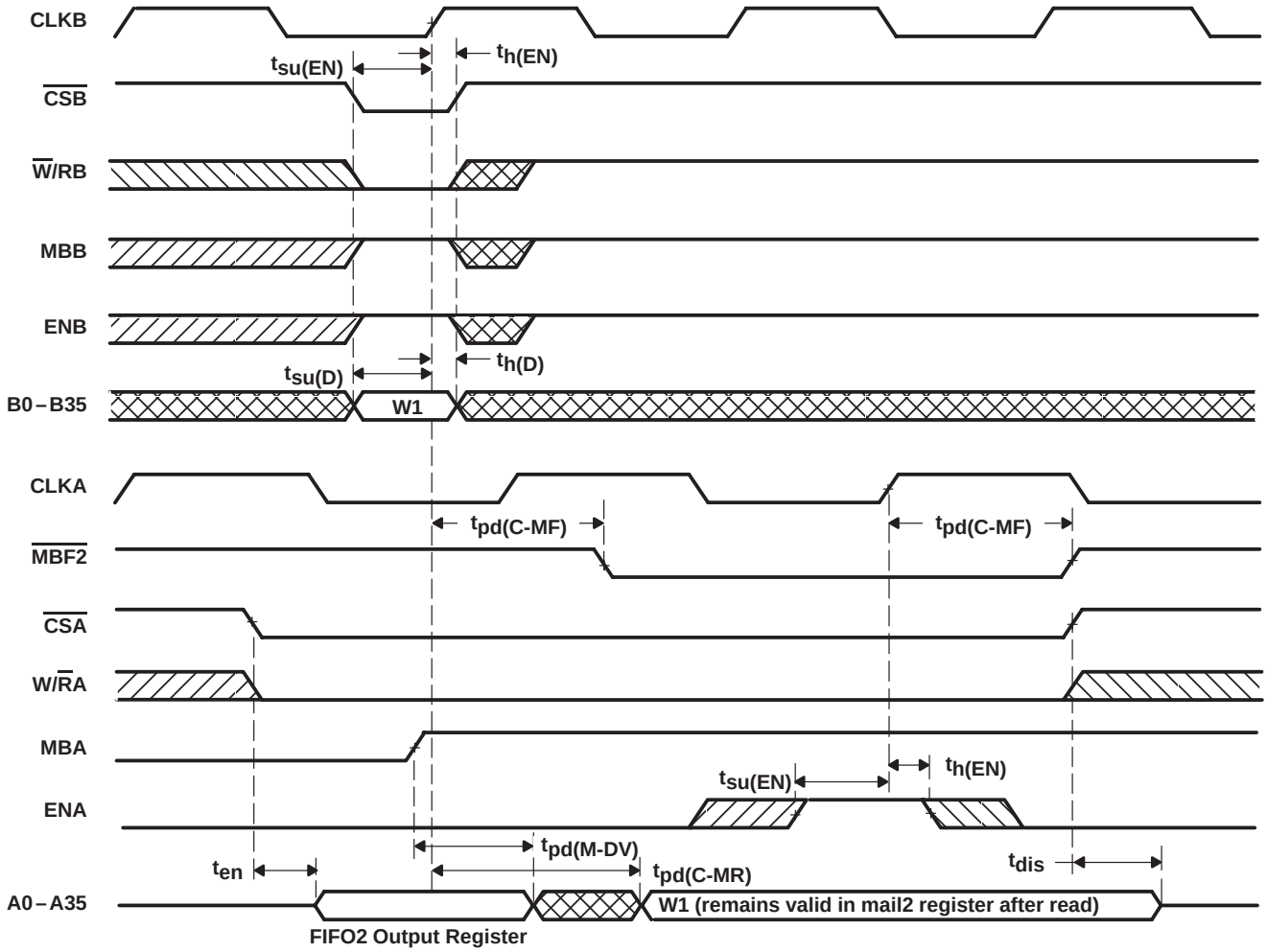


Figure 16. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±400 mA
Package thermal impedance, θ_{JA} (see Note 2): PCB package . . . . . 28°C/W
PQ package . . . . . 46°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V, I_{OH} = –4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or 0					±5	μA
I_{OZ}	V_{CC} = 5.5 V, V_O = V_{CC} or 0					±5	μA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} – 0.2 V or 0					400	μA
ΔI_{CC}‡	V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	$\overline{CSA}$ = V_{IH}	A0–A35		0		mA
		$\overline{CSB}$ = V_{IH}	B0–B35		0		
		$\overline{CSA}$ = V_{IL}	A0–A35			1	
		$\overline{CSB}$ = V_{IL}	B0–B35			1	
		All other inputs				1	
C_i	V_I = 0, f = 1 MHz				4		pF
C_o	V_O = 0, f = 1 MHz				8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This is the supply current when each input is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 through 17)

		’ACT3622-15		’ACT3622-20		’ACT3622-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKA or CLKB		66.7		50		33.4	MHz
t_c	Clock cycle time, CLKA or CLKB	15		20		30		ns
$t_{w(CLKH)}$	Pulse duration, CLKA and CLKB high	6		8		10		ns
$t_{w(CLKL)}$	Pulse duration, CLKA and CLKB low	6		8		10		ns
$t_{su(D)}$	Setup time, A0–A35 before CLKA↑ and B0–B35 before CLKB↑	4		5		6		ns
$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB before CLKB↑	4.5		5		6		ns
$t_{su(RS)}$	Setup time, $\overline{RST1}$ or $\overline{RST2}$ low before CLKA↑ or CLKB↑§	5		6		7		ns
$t_{su(FS)}$	Setup time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ high	7.5		8.5		9.5		ns
$t_{h(D)}$	Hold time, A0–A35 after CLKA↑ and B0–B35 after CLKB↑	0		0		0		ns
$t_{h(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, and MBB after CLKB↑	0		0		0		ns
$t_{h(RS)}$	Hold time, $\overline{RST1}$ or $\overline{RST2}$ low after CLKA↑ or CLKB↑§	4		4		5		ns
$t_{h(FS)}$	Hold time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ high	1		2		2		ns
t_{sk1}¶	Skew time between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	7.5		9		11		ns
t_{sk2}¶	Skew time between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12		16		20		ns

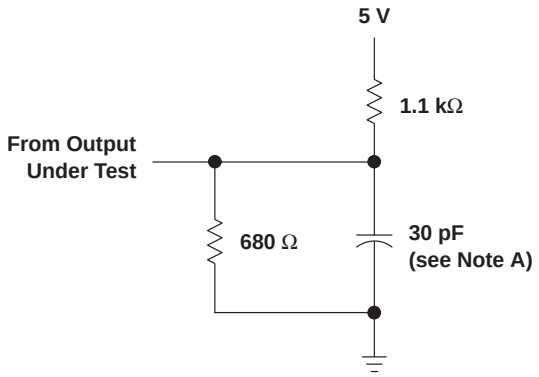
§ Requirement to count the clock edge as one of at least four needed to reset a FIFO
¶ Skew time is not a timing constraint for proper device operation and is included only to illustrate the timing relationship between CLKA cycle and CLKB cycle.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (see Figures 1 through 17)

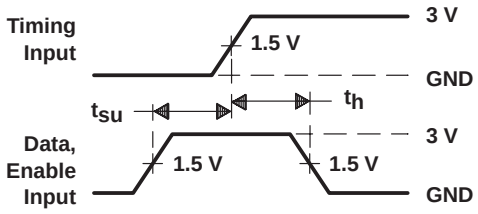
PARAMETER		'ACT3622-15		'ACT3622-20		'ACT3622-30		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKA or CLKB	66.7		50		33.4		MHz
t_a	Access time, CLKA↑ to A0–A35 and CLKB↑ to B0–B35	3	11	3	13	3	15	ns
$t_{pd(C-IR)}$	Propagation delay time, CLKA↑ to IRA and CLKB↑ to IRB	2	8	2	10	2	12	ns
$t_{pd(C-OR)}$	Propagation delay time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	1	10	1	12	ns
$t_{pd(C-AE)}$	Propagation delay time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	1	10	1	12	ns
$t_{pd(C-AF)}$	Propagation delay time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	1	8	1	10	1	12	ns
$t_{pd(C-MF)}$	Propagation delay time, CLKA↑ to $\overline{MBF1}$ low or $\overline{MBF2}$ high and CLKB↑ to $\overline{MBF2}$ low or $\overline{MBF1}$ high	0	8	0	10	0	12	ns
$t_{pd(C-MR)}$	Propagation delay time, CLKA↑ to B0–B35† and CLKB↑ to A0–A35‡	3	13.5	3	15	3	17	ns
$t_{pd(M-DV)}$	Propagation delay time, MBA to A0–A35 valid and MBB to B0–B35 valid	3	11	3	13	3	15	ns
$t_{pd(R-F)}$	Propagation delay time, $\overline{RST1}$ low to $\overline{AEB}$ low, $\overline{AFA}$ high, and $\overline{MBF1}$ high, and $\overline{RST2}$ low to $\overline{AEA}$ low, $\overline{AFB}$ high, and $\overline{MBF2}$ high	1	15	1	20	1	30	ns
t_{en}	Enable time, $\overline{CSA}$ and W/$\overline{RA}$ low to A0–A35 active and $\overline{CSB}$ low and $\overline{W}$/RB high to B0–B35 active	2	12	2	13	2	14	ns
t_{dis}	Disable time, $\overline{CSA}$ or W/$\overline{RA}$ high to A0–A35 at high impedance and $\overline{CSB}$ high or $\overline{W}$/RB low to B0–B35 at high impedance	1	11	1	12	1	14	ns

† Writing data to the mail1 register when the B0–B35 outputs are active and MBB is high
‡ Writing data to the mail2 register when the A0–A35 outputs are active and MBA is high

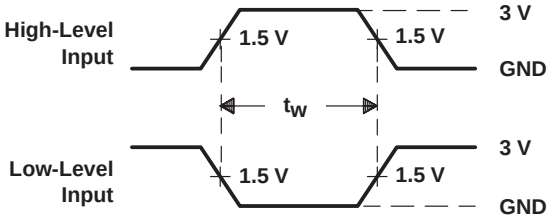
PARAMETER MEASUREMENT INFORMATION



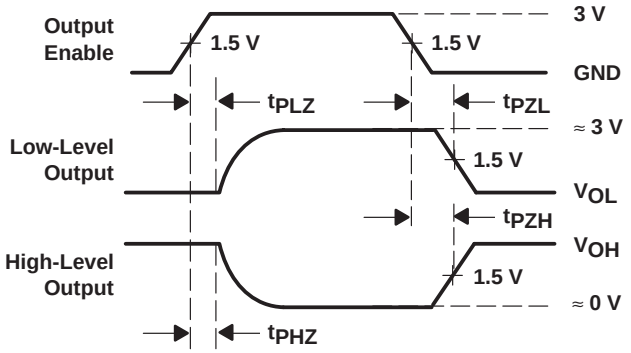
LOAD CIRCUIT



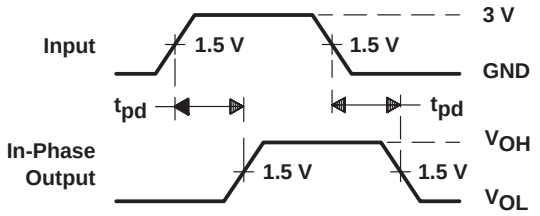
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. Includes probe and jig capacitance
B. t_{PZL} and t_{PZH} are the same as t_{en}.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Figure 17. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

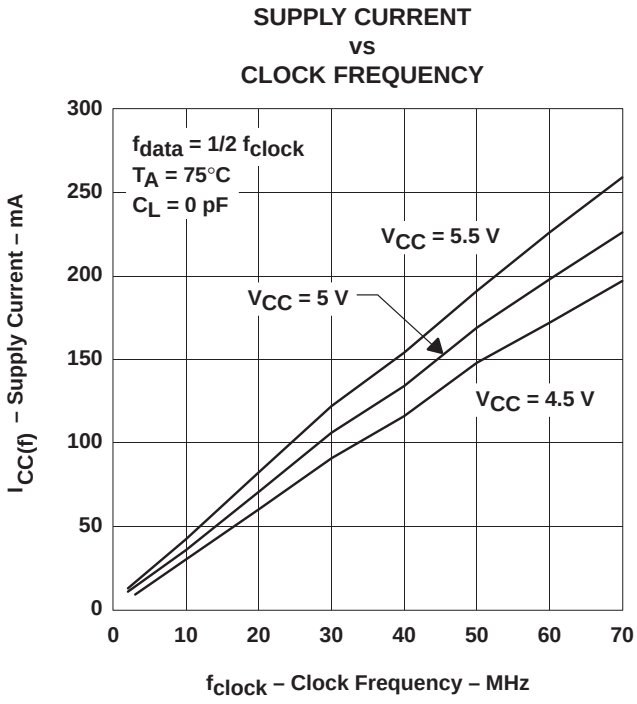


Figure 18

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