ST1284

Parallel port single termination network with ±15 kV ESD protection

Features

- One device for parallel port termination
- Compliant with IEEE1284 standard
- EMI / RFI noise filtering
- Highly integrated solution in 28 pins QSOP package
- One single device provides the proper termination for 8 datalines, 1 strobe line, 4 control lines and 4 statuts lines
- In system ESD protection of ±15 kV (air discharge) as per IEC 61000-4-2 level 4
- ECOPACK®2 compliant component

Complies with the following standards:

- IEC 61000-4-2 level 4
  - ±15 kV (air discharge)
  - ± 8 kV (contact discharge)

MIL STD 883G - Method 3015-7 Class 3

- Human body model

Applications

ECP/EPP parallel port termination on:

- Desktops
- Notebooks
- Workstations
- Servers
- PC peripherals
- Set top box



QSOP28

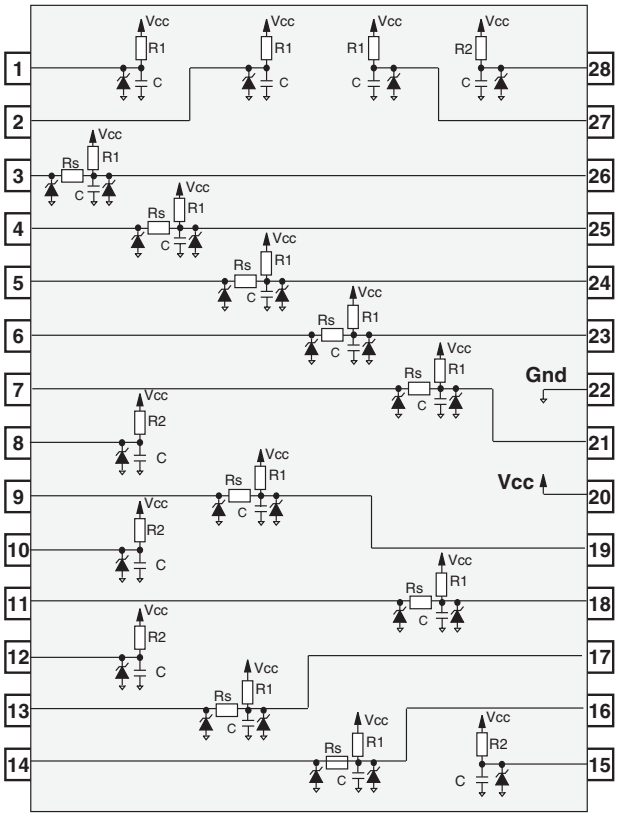
Description

The ST1284-01A8 is a highly integrated termination for enhanced high speed parallel ports. The integrated termination complies to the IEEE1284 Standard recommendations and government EMC compatibility requirements. It is built around two basic cells. The first one (cell 1) provides line termination, EMI filtering and ESD protection for the Strobe and Datalines while the second one (cell 2) provides EMI filtering and ESD protection for the Control and Status lines.

In addition, ST1284-01A8 provides extra protection against ESD. When tested according to IEC 61000-4-2, they withstand ±8 kV contact discharges and ±15 kV air-discharges, thereby providing to the system the necessary robustness to meet up to level 4 of IEC 61000-4-2, without the need for additional ESD protection components. Cells 1 and 2 are described in more detail in *Figure 2* and *Figure 3.*

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Figure 1. Schematic diagram



	R1	R2	Rs	C
Code 01	4.7 kΩ	4.7 kΩ	33 Ω	180 pF
Tolerance	± 10%	± 10%	± 10 %	± 20%

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, air discharge	±16	kV
	ESD discharge IEC 61000-4-2, contact discharge	±9	
	IESD discharge - MIL STD 883E - Method 3015-7	± 25	
V_{CC}	Supply voltage	5.5	V
P_r	Power rating per resistor	100	mW
P_P	Package Power rating	1	Ω
T_{op}	Operating temperature range	0 to + 70	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C
T_j	Maximum operating junction temperature	125	°C

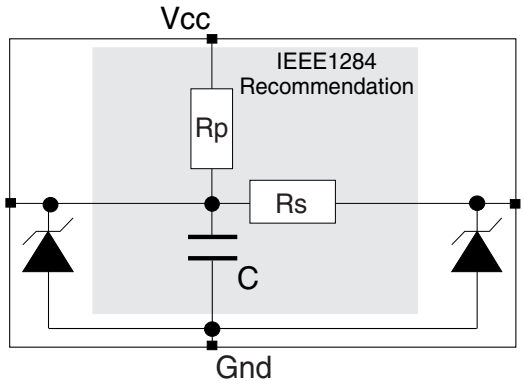
Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_R	Leakage current	V_{CC} = 5.0 V			10	µA
V_{BR}	Breakdown voltage	I_R = 1 mA	6			V
V_F	Forward voltage drop	I_F = 50 mA		0.9		V

Basic cell configurations

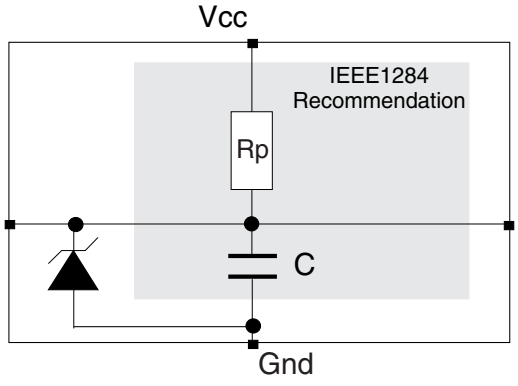
The ST1284-01A8 is built around the two basic cells described below which integrate the recommended IEEE1284 network and the ESD protection compatible with IEC 61000-4-2 level 4.

Figure 2. Cell 1 for line termination, EMI filtering and ESD protection for the datalines and strobe signals



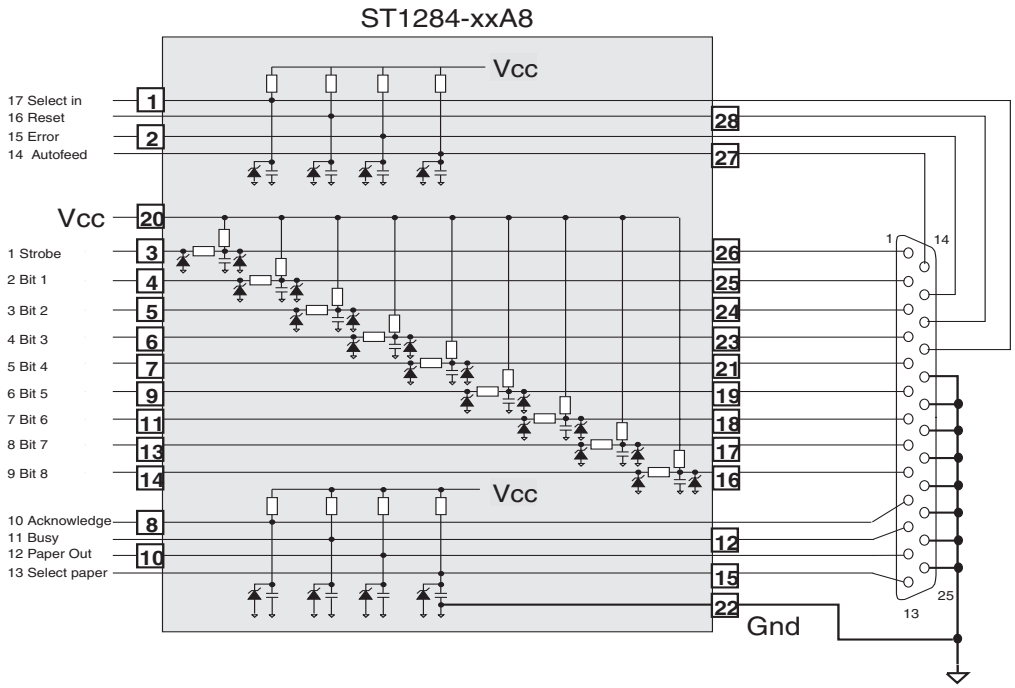
There are 9 of these cells in the ST1284-xxA8

Figure 3. Cell 2 for EMI filtering and ESD protection of the control and status signals



There are 8 of these cells in the ST1284-xxA8

Figure 4. Functional diagram



2 Application information

The functional diagram here above presents a IEEE1284-A connector pinout and show how to connect the ST1284-01A8 in order to correctly terminate and filter the 17 signal lines. The IEEE1284-A connector is the PC standard for the host connection.

Control and status lines (from 10 to 17) only require a pull-up resistor (R_p) and a filter capacitor (C).

The data lines (from 2 to 9) and the STROBE (pin 1) also require a termination series resistor (R_s) in addition to the pull-up resistor and a filter capacitor. The V_{CC} is connected to pin 20 and the ground to pin 22.

The ST1284-01A8 can be used with all 3 types of connectors defined in the IEEE1284 standard:

- IEEE1284-A is a 25 dB connector which is the PC standard for the host connection.
- IEEE1284-B is a 36 pin, 0.085 inch centerline connector used on the peripheral device.
- IEEE1284-C is a new 36 pin, 0.050 inch centerline connector which can be used for both host and peripherals.

3 Technical information

3.1 Frequency behavior of data and strobe signals

Figure 5. Measurement conditions

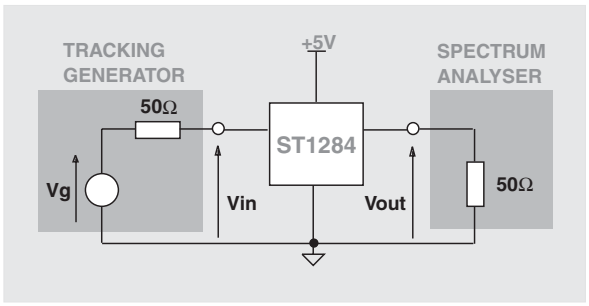
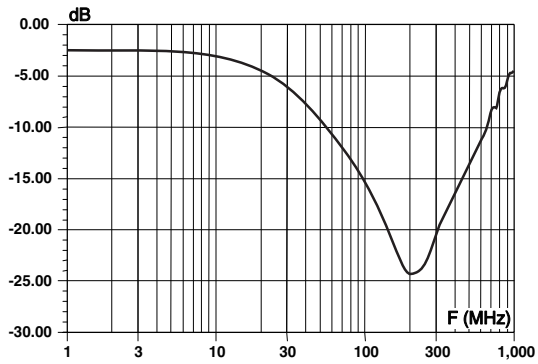


Figure 6. Typical frequency response curve for data and STROBE signal



3.2 ESD protection

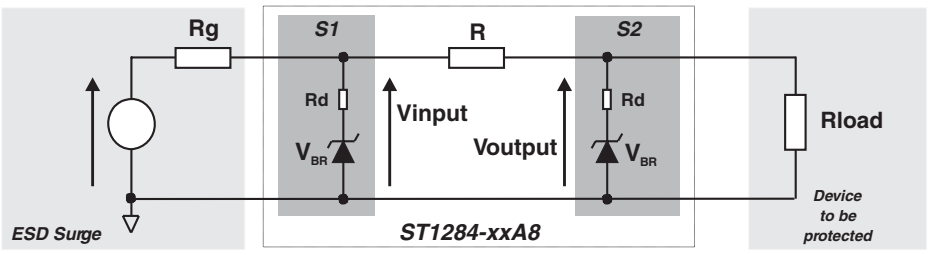
In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remain operational without user intervention.

The ST1284-01A8 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$V_{ouput} = V_{BR} + R_d .I_{PP}$

This protection function is splitted in 2 stages. As shown in *Figure 7*, the ESD strikes are clamped by the first stage S_1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the voltage very low at the output.

Figure 7. ST1284 ESD clamping behavior



To have a good approximation of the remaining voltages at both V_{in} and V_{out} stages, we give the typical dynamical resistance value R_d.

By taking into account these following hypothesis:
$R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, it gives these formulas:

$$Vinput = \frac{R_g \cdot V_{BR} + R_d \cdot V_{PP}}{R_g}$$

$$Voutput = \frac{R_t \cdot V_{BR} + R_d \cdot Vinput}{R_t}$$

The results of the calculation done for V_{PP} = 8 kV, R_g = 330 Ω (IEC 61000-4-2 standard), V_{BR} = 7 V (typ.) and R_d = 1 Ω (typ.) give:

- V_{input} = 31.2 V
- V_{output} = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the input side. This parasitic effect is not present at the output side due the low current involved after the resistance R.

The measurements done here after show very clearly (*Figure 9*) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on V_{out} stage
- V_{output} clamping voltage very close to V_{BR} (positive strike) and $-V_F$ (negative strike)

Figure 8. Measurement conditions

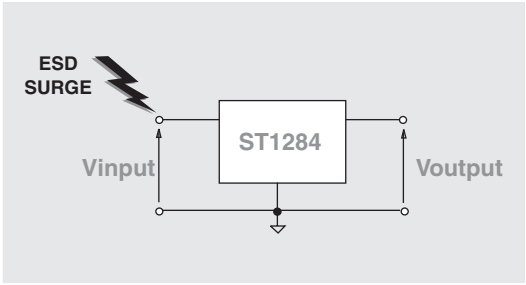
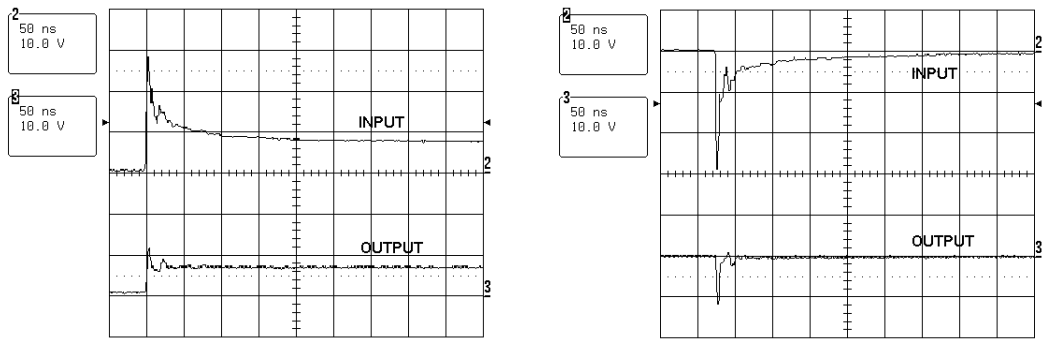


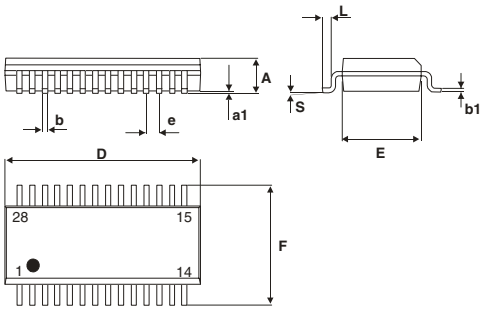
Figure 9. Remaining voltage at the input and output of the device during a ±16 kV ESD surge (IEC 61000-4-2)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. QSOP28 dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.55	1.75	0.061	0.069
a1	0.10	0.25	0.004	0.010
b	0.20	0.30	0.008	0.012
b1	0.18	0.25	0.007	0.010
D	9.80	9.98	0.386	0.393
E	5.79	6.20	0.228	0.244
e	0.64 typ.		0.025 typ.	
F	3.80	3.98	0.15	0.157
L	0.40	0.90	0.016	0.035
S	8° max		8° max	

Figure 10. Footprint (dimensions in mm)

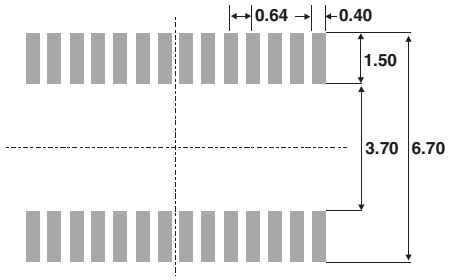


Table 4. Mechanical specifications

Lead plating	Tin-lead
Lead plating thickness	7 µm min. 25 µm max.
Lead material	Copper Alloy
Lead coplanarity	0.102 mm (0.004”)
Body material	Molded epoxy
Resine	Meets UL94V-0 standard

5 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ST1284-01A8	ST1284-01	QSOP28	0.147 g	48	Tube
ST1284-01A8RL	ST1284-01			2500	Tape and Reel

6 Revision history

Table 6. Document revision history

Date	Revision	Changes
Oct-2003	2B	Last release.
12-Mar-2010	3	Updated table in *Figure 1* and *Figure 10.*

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