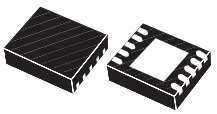
# STBB1xx

## 1 A, high efficiency single inductor dual mode buck-boost DC-DC converter

**Preliminary data**

## Features

- Buck-boost DC-DC converter
- Operating input voltage range from 2.0 V to 5.5 V
- 2% DC feedback voltage tolerance
- Synchronous rectification
- Shutdown function
- 1.5 MHz switching frequency
- Power save mode at light load
- Typical efficiency: > 94 %
- 1 A output current capability
- Shutdown current < 1 µA
- Available in DFN10 3 x 3 mm



**DFN10 (3 x 3 mm)**

## Application

- Single cell LI-ION and 3 cells alkaline, NI-MH powered devices
- Memory SD/MMC cards supply
- Palmtop computers
- Cell phones
- Digital cameras

## Description

The STBB1 is a fixed frequency, high efficiency, Buck-boost DC-DC converter able to provide output voltages ranging from 1.2 V to 5.5 V and input voltage from 2.0 V to 5.5 V. The device can operate with input voltages higher, equal or lower than the output voltage making the product suitable for single lithium-Ion, multicell alkaline or NiMH applications where the output voltage is within the battery voltage range.

The integrated low-$R_{DSon}$ N-channel and P-channel MOSFET switches contribute to achieve high efficiency.

The MODE pin allows selecting between auto mode and forced PWM mode thus taking benefit either of lower power consumption or best dynamic performance. The device includes also soft-start control, thermal shutdown and current limit. The STBB1 is packaged in DFN10 3x3 mm.

**Table 1. Device summary**

| Order codes | Marking | Output voltage |
|---|---|---|
| STBB1-18PUR | BB1 18 | 1.8 V |
| STBB1-25PUR | BB1 25 | 2.5 V |
| STBB1-28PUR | BB1 28 | 2.8 V |
| STBB1-33PUR | BB1 33 | 3.3 V |
| STBB1PUR | BB1 | ADJ |



This is preliminary information on a new product in development or undergoing evaluation. Details are subject to change without notice.

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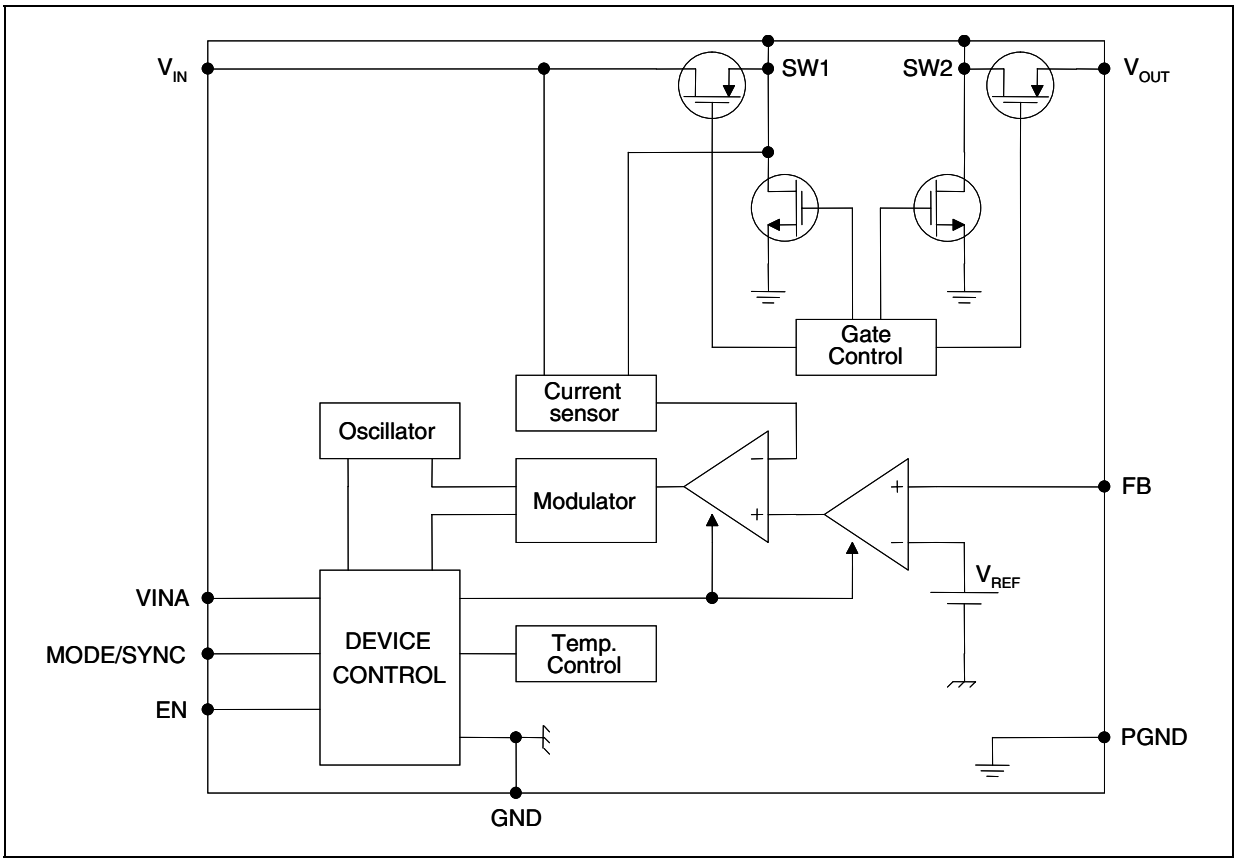
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# 1 Diagram

**Figure 1. Block diagram**



# 2 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VINA, VIN | Input voltage | - 0.3 to 7 | V |
| VOUT | Output voltage | - 0.3 to 7 | V |
| SW1, SW2 | DC voltage | - 0.3 to 7 | V |
| FB | DC voltage | - 0.3 to 1.5 | V |
| MOD/SYNC, EN | DC voltage | - 0.3 to 7 | V |
| $T_J$ | Maximum junction temperature | 150 | °C |
| $T_{STG}$ | Storage temperature range | - 65 to + 150 | °C |
| $T_{JOP}$ | Operating junction temperature range | - 40 to + 85 | °C |
| ESD | Human body model | 2 | kV |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance junction-case | 2.96 | °C/W |
| $R_{thJA}$ | Thermal resistance junction-ambient | 30.9 | °C/W |

# 3 Pin configuration

**Figure 2. Pin connections (top view)**

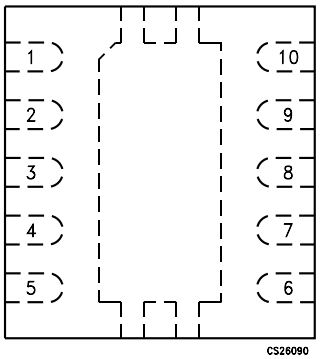



**Table 4. Pin description**

| Pin n° | Symbol | Name and function |
|---|---|---|
| 1 | VOUT | Output voltage |
| 2 | SW2 | Switch pin - Internal switches are connected to this pin. Connect inductor between SW1 to SW2 |
| 3 | PGND | Power ground |
| 4 | SW1 | Switch pin - Internal switches are connected to this pin. Connect inductor between SW1 and SW2 |
| 5 | VIN | Power input voltage. Connect a ceramic bypass capacitor (10 µF minimum) between this pin and PGND |
| 6 | EN | Enable pin. Connect this pin to GND or a voltage lower than 0.4 V to shut down the IC. A voltage higher than 1.2 V is required to enable the IC. |
| 7 | MODE (SYNC) | Operation mode selection.<br>If MODE pin is low, the STBB1 automatically switches between pulse skipping and fixed frequency PWM according to the load level.<br>If MODE pin is pulled high, the STBB1 works always in PWM mode.<br>When a square waveform is applied, this pin provides the clock signal for oscillator synchronization |
| 8 | VINA | Supply voltage for control stage |
| 9 | GND | Signal ground |
| 10 | FB | Feedback voltage |
| | Exposed pad | Power ground |

# 4 Typical application

**Figure 3. Application circuit adjustable version**

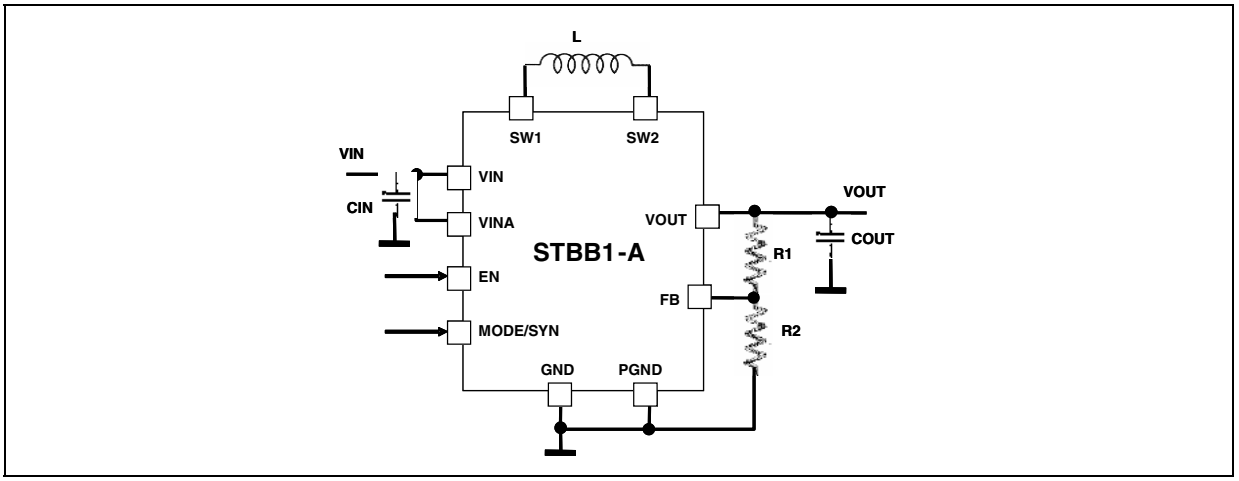



**Figure 4. Application circuit fixed output voltage**

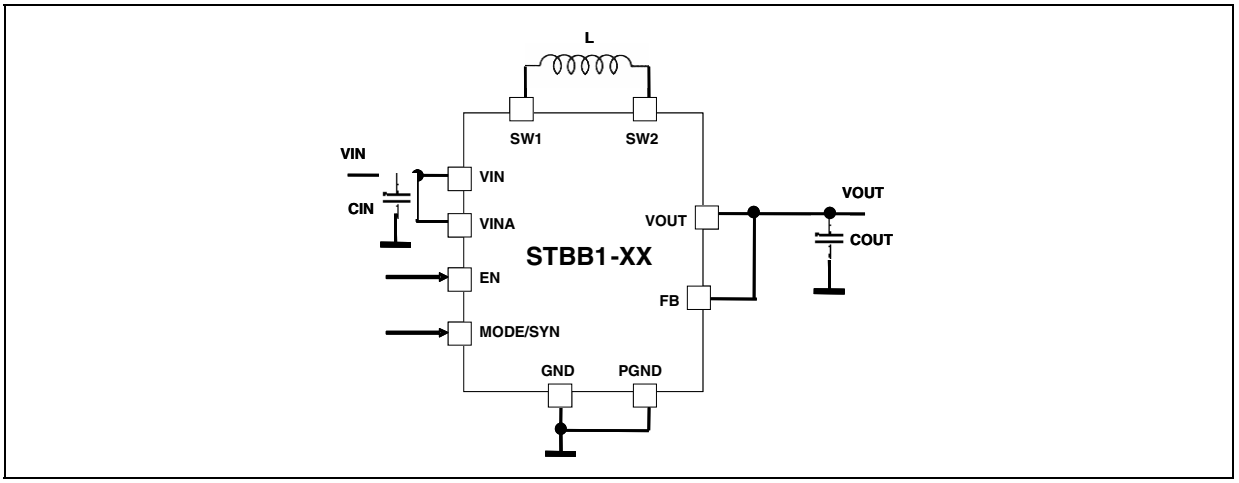



**Table 5. List of external components (1)**

| Component | Manufacturer | Part number | Value | Size |
|---|---|---|---|---|
| CIN | Murata | GRM188R60J106ME47D | 10 µF | 0603 |
| COUT | Murata | GRM188R60J106ME47D | 10 µF | 0603 |
| L | TDK | VLCF4020T-2R2N1R7 | 2.2 µH | 4 x 4 x 2 mm |
| R1 | | 560 kΩ ($V_O$ = 3.3 V) | (2) | 0402 |
| R2 | | 100 kΩ | | 0402 |

1. Above listed components refer to typical application. Operation of the STBB1 is not limited to the choice of these external components.
2. R1 and R2 are calculated according to the following formula.

R1 = R2 x (VOUT/VFB - 1).

Suggested value for R2 is 100 kΩ. In order to reduce the quiescent current a maximum value of 500 kΩ is possible.

# 5 Electrical characteristics

($V_{IN}$ = $V_{INA}$ = $V_{EN}$ = 3.6 V, $C_{IN}$ = 10 µF, $C_{OUT}$ = 10 µF, L = 2.2 µH, $T_J$ = - 40 to 85°C (unless otherwise specified; typical values are referred to $T_A$ = 25°C)

**Table 6. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | | 2.0 | | 5.5 | V |
| $V_{UVLO}$ | Under voltage lockout threshold | VINA rising | | 1.70 | 1.80 | V |
| | | VINA falling | 1.50 | 1.60 | | |
| $V_{FB}$ | Feedback voltage | | 485 | 500 | 515 | mV |
| | | $T_J$ = 25°C | 490 | 500 | 510 | mV |
| $V_{OUT}$ | Output voltage range | | 1.2 | | 5.5 | V |
| $Z_{FB}$ | FB input impedance | | | 10 | | MΩ |
| $I_Q$ | No switching quiescent current (VIN+VINA) (see *Figure 3*, *4*) | FB = 0.7 V, $V_{MODE}$ = 0 V | | 160 | 250 | µA |
| | | FB = 0.7 V, $V_{MODE}$ = $V_{IN}$ | | 600 | 750 | |
| $I_Q$ | Operating quiescent current (VIN+VINA) | $I_{OUT}$ = 0 A, $V_{OUT}$ = 3.3 V, $V_{MODE}$ = 0 V | | 200 | | µA |
| | | $I_{OUT}$ = 0 A, $V_{OUT}$ = 3.3 V, $V_{MODE}$ = $V_{IN}$ | | 3.4 | 5.0 | mA |
| $I_{QSHDN}$ | Shutdown quiescent current | $V_{EN}$ = 0 V, $V_{IN}$ = 3.6 V | | 0.1 | 1 | µA |
| Freq | Oscillator frequency | | 1300 | 1500 | 1750 | kHz |
| | Frequency range for synchronization | | 1300 | | 2000 | |
| $V_{EN}$ | Enable input logic low | $V_{IN}$ = 2.2V to 5.5V | | | 0.4 | V |
| | Enable input logic high | $V_{IN}$ = 2.2V to 5.5V | 1.2 | | | |
| $I_{EN}$ | Enable pin current | $V_{EN}$ = 5.5V | | 0.01 | 1 | µA |
| $V_{MODE/SYNC}$ | MODE/SYNC input logic low | $V_{IN}$ = 2.2V to 5.5V | | | 0.4 | V |
| | MODE/SYNC input logic high | $V_{IN}$ = 2.2V to 5.5V | 1.2 | | | |
| $I_{MODE/SYNC}$ | MODE/SYNC pin current | $V_{MODE/SYNC}$ = 5.5V | | 0.01 | 1 | µA |
| %$V_{OUT}$ | Line regulation | 2.2V<$V_{IN}$<5.5V; $I_{OUT}$=1mA | | 0.5 | | % |
| %$V_{OUT}$ | Load regulation | 10mA<$I_{OUT}$<1000mA | | 1 | | % |
| $I_{SWL}$ | Switch current limitation | $V_{IN}$ = 3.3 V | 1.6 | 2.3 | 2.4 | A |
| $I_{LKN}$ | NMOS leakage current | $V_{IN}$ = 5.5 V | | 0.01 | 1 | µA |
| $I_{LKP}$ | PMOS leakage current | | | 0.01 | 1 | µA |
| RDSon-N | NMOS switch on resistance | | | 0.13 | 0.35 | Ω |
| RDSon-P | PMOS switch on resistance | | | 0.13 | 0.35 | Ω |
| ν | Efficiency, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.3 V | $I_{OUT}$=10mA; $V_{MODE}$=0 | | 89 | | % |
| | | $I_{OUT}$=10mA; $V_{MODE}$=$V_{IN}$ | | 67 | | |
| | | $I_{OUT}$=100mA; $V_{MODE}$=$V_{IN}$ | | 94 | | |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{SHDN}$ | Thermal shut down | | | 140 | | °C |
| $T_{HYS}$ | Thermal shut down hysteresis | | | 20 | | °C |

# 6 Detailed description

## 6.1 General description

The STBB1 is a high efficiency dual mode buck-boost switch mode converter. Thanks to the internal 4 switches, 2 P-channel and 2 N-channel, and its particular control technique it is able to deliver e well regulated output voltage with a variable input voltage which can be higher, equal or lower than the desired output voltage. This solves most of the power supply problems that circuit designers face when dealing with battery powered equipment.

The controller uses an average current mode technique in order to obtain good stability in all possible conditions of input voltage, output voltage and output current. In addition the peak inductor current is monitored in order to avoid saturation of the coil.

The STBB1 can work in two different modes: PWM mode or power save mode. In the first case the device operates with a fixed oscillator frequency in all line/load conditions. This is the suitable condition to obtain the maximum dynamic performances. In the second case the device operates in burst mode allowing a drastic reduction of power consumption.

Top-class line and load transients are achieved thanks to feed-forward technique and due to the innovative control method specifically designed to optimize the performances in the buck-boost region where input voltage is very close to the output voltage.

The STBB1 is self protected by short circuit, over-temperature and adjustable version. Under voltage lockout and soft start guarantee proper operation during start-up.

Input voltage and ground connections are split in power and signal pins. This allows reducing internal disturbances when the 4 internal switches are working. The switches bridge is connected between VIN and PGND pins while all logic blocks are connected between VINA and GND.

## 6.2 Dual mode operation

The STBB1 works in PWM or in power save (PS) mode according to the different operating conditions.

If the Mode pin is pulled high the device works always in PWM mode even at light or no load. In this condition STBB1 provides the best dynamic performances.

If MODE pin is logic low, the STBB1 operation changes according to the average input current handled by the device.

At low average current the STBB1 enters in PS mode allowing very low power consumption and thus obtaining very good efficiency event at light load. When the average current increases, the device automatically switches to PWM mode in order to deliver the power needed by the load.

In PS mode the STBB1 implements a burst mode operation. If the output voltage increases above its nominal value the device stops switching. As soon the $V_{OUT}$ falls below the nominal value the device starts switching again with a programmed average current higher than the one needed by the load. *Figure 8* in Section 7 shows PS mode operation areas vs output current in typical application conditions.

## 6.3 External synchronization

The STBB1 implements external synchronization pin. If and external clock signal is applied to the MODE (SYN) pin with a frequency between 1.35 MHz and 2.0 MHz and with proper low/high levels, the device automatically goes in PWM mode and the external clock is used as switching oscillator.

## 6.4 Enable pin

The device operates when EN pin is set high. If EN pin is set low the device stops switching, all the internal blocks are turned off. In this condition the current drawn from VIN/VINA is below 1 µA in the whole temperature range. In addition the internal switches are in off state so the load is electrically disconnected from the input, this avoids unwanted current leakage from the input to the load.

## 6.5 Protections

The STBB1 implements different type of protections.

### 6.5.1 Soft start and short circuit

After the EN pin is pulled high, or after a suitable voltage is applied to VIN, VINA and EN the device initiates the start-up phase. The average current limit is set to 400 mA at the beginning and it is gradually increased tracking the output voltage increase. As soon the output voltage reaches 1.0 V the average current limit is set to its nominal value.

This method allows having a current limit proportional to the output voltage, if there is a short in the $V_{OUT}$ pin, the output current will not exceed 400 mA.

This process is not handled by any timer so the device is also able to start-up in case of large capacitive loads.

### 6.5.2 Under voltage lockout

The under voltage lockout function avoids improper operation of STBB1 when the input voltage is not high enough. When the input voltage is below the VUVLO threshold the device is in shutdown mode. The hysteresis of 100 mV avoids unstable operation when the input voltage is close to the UVLO threshold.

### 6.5.3 Over-temperature protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 140 °C typically the device stops operating. As soon the temperature falls below 120 °C typically normal operation is restored.

# 7 Typical performance characteristics

(L = 2.2 µH, $V_O$ = 3.3 V, all the measurements done with circuit shown in *Figure 3* and external components listed in *Table 5*)

**Figure 5. Efficiency vs $I_{OUT}$ in auto mode**

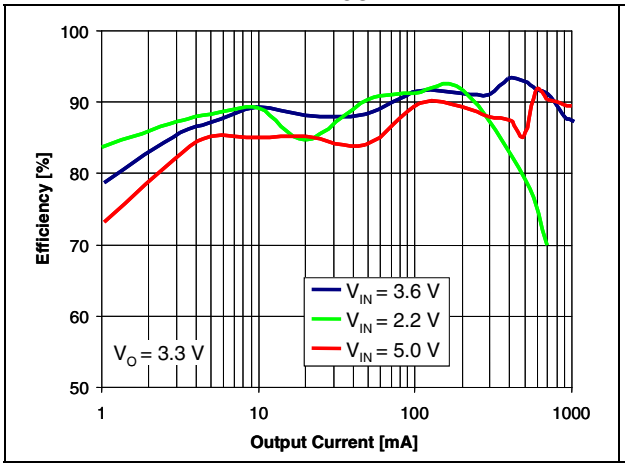



**Figure 6. Efficiency vs $I_{OUT}$ in PWM mode**

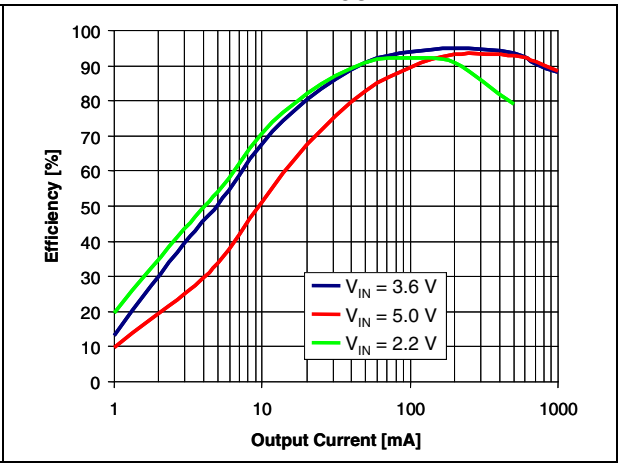



**Figure 7. Efficiency vs $V_{IN}$, $I_{OUT}$ = 550 mA**

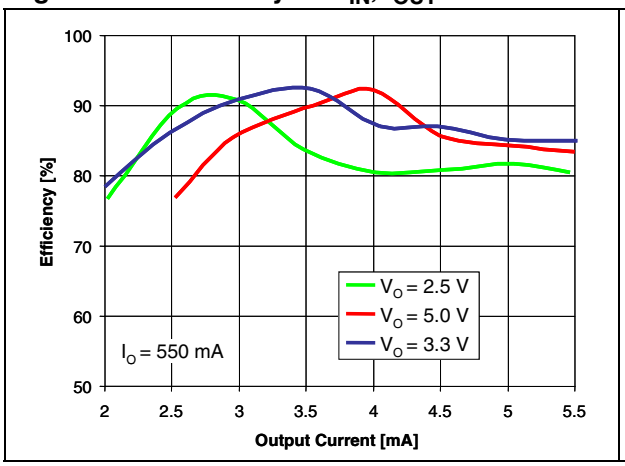



**Figure 8. PS to PWM transition**

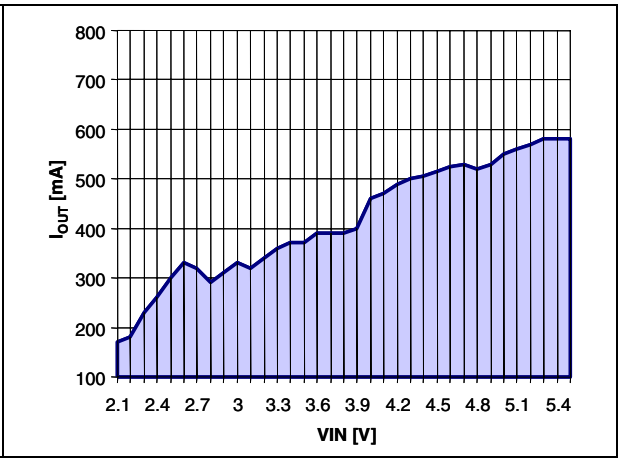



**Figure 9. Max $I_{OUT}$ vs $V_{IN}$**

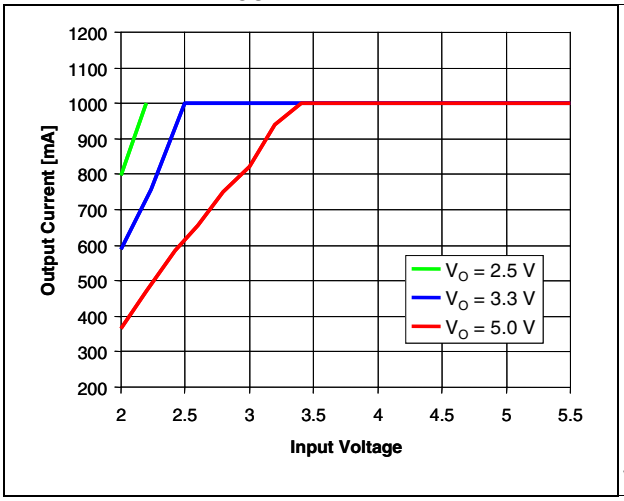
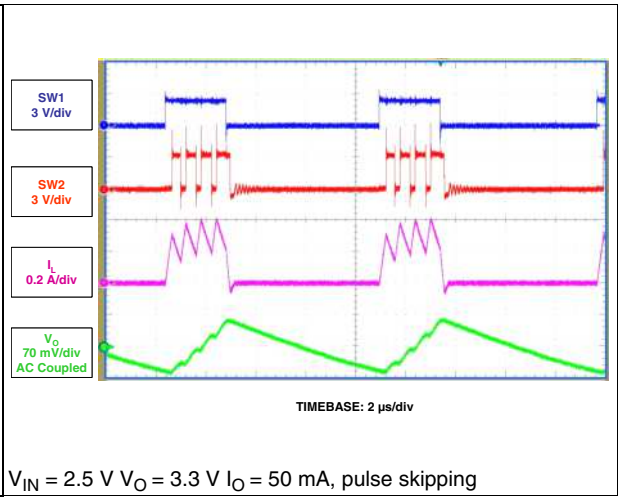
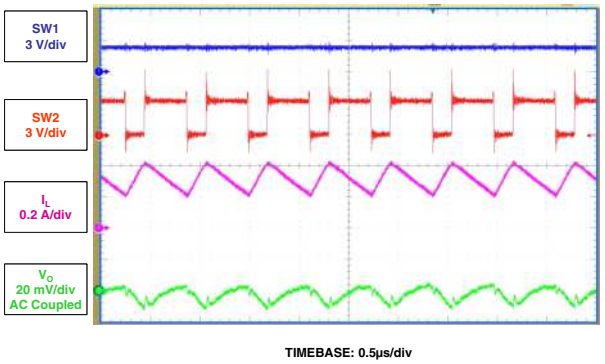



**Figure 10. Boost region operation**



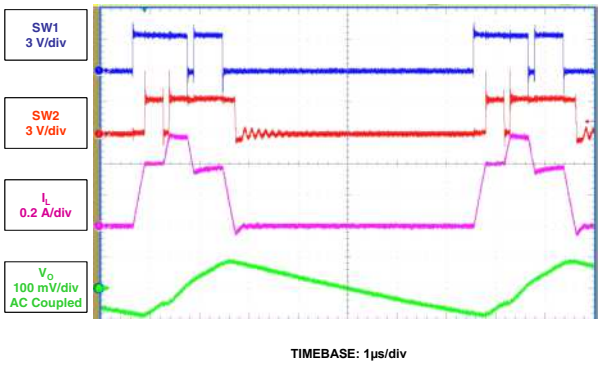

$V_{IN}$ = 2.5 V $V_O$ = 3.3 V $I_O$ = 50 mA, pulse skipping

**Figure 11. Boost region operation**



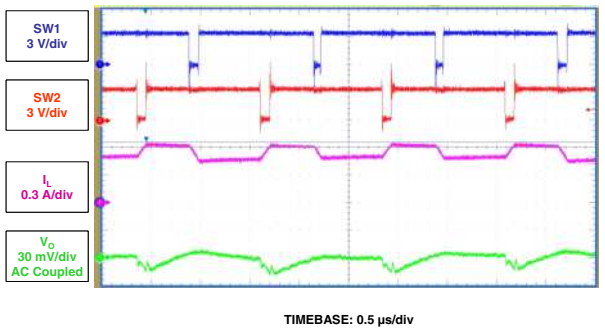

$V_{IN}$ = 2.5 V $V_O$ = 3.3 V $I_O$ = 200 mA, PWM mode

**Figure 12. Buck-boost region operation**



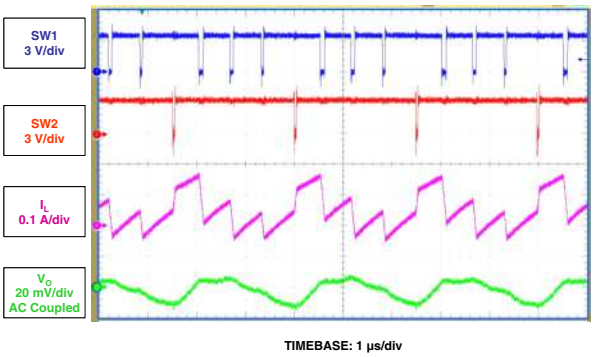

$V_{IN}$ = 3.6 V $V_O$ = 3.3 V $I_O$ = 100 mA, pulse skipping mode

**Figure 13. Buck-boost region operation**



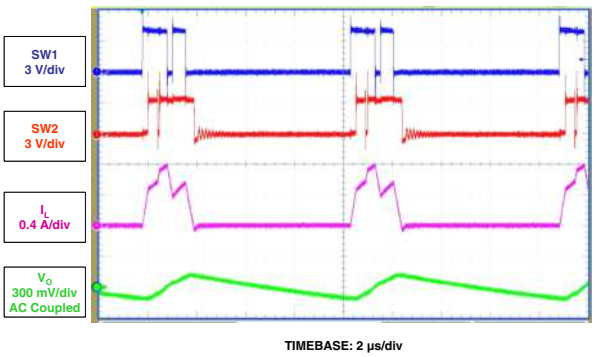

$V_{IN}$ = 3.6 V $V_O$ = 3.3 V $I_O$ = 500 mA, PWM mode

**Figure 14. Buck-boost region operation**



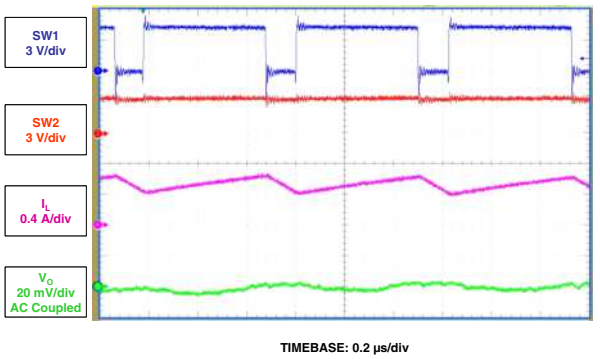

$V_{IN}$ = 3.6 V $V_O$ = 3.3 V $I_O$ = 50 mA, PWM mode

**Figure 15. Buck region operation**




$V_{IN}$ = 4.2 V $V_O$ = 3.3 V $I_O$ = 100 mA, pulse skipping mode

**Figure 16. Buck region operation**




$V_{IN}$ = 4.2 V $V_O$ = 3.3 V $I_O$ = 500 mA, PWM mode

# 8 Application information

## 8.1 Programming the output voltage

The STBB1 is available in several two types of version: fixed output voltage (STBB1-xx) and adjustable output voltage (STBB1-A).

In the first case the device integrates the resistor divider needed to set the right output voltage. This allows saving 2 external components. The FB pin must be connected directly to $V_{OUT}$.

For the adjustable version, the resistor divider must be connected between $V_{OUT}$ and GND and the middle point of the divider must be connected to FB as shown in *Figure 4*.

**Equation 1**

$$R1 = R2 \times \left( \frac{V_{OUT}}{V_{FB}} - 1 \right)$$

A suggested value for R2 is 100 kΩ, anyhow, in order to reduce the power consumption a maximum value of 500 kΩ can be used.

## 8.2 Inductor selection

The inductor is the key passive component for switching converters. In case of buck-boost device, the inductor selection must take into consideration the boundary conditions in which the converter works as buck at the maximum input voltage and as a boost at the minimum input voltage.

Two critical inductance values are then obtained according to the following formulas:

**Equation 2**

$$L_{MIN-BUCK} = \frac{VOUT \times (VIN_{MAX} - VOUT)}{VIN_{MAX} \times fs \times \Delta I_L}$$

**Equation 3**

$$L_{MIN-BOOST} = \frac{VIN_{MIN} \times (VOUT - VIN_{MIN})}{VOUT \times fs \times \Delta I_L}$$

Where:

Fs: minimum switching frequency;

ΔIL = is the peak-to-peak inductor ripple current. As a rule of thumb, the peak-to-peak ripple can be set at 10 % - 20 % of the output current.

The minimum inductor value for the application is the higher between *Equation 2* and *Equation 3*. In addition, to the inductance value also the maximum current the inductor can handle must be calculated in order to avoid saturation.

**Equation 4**

$$I_{PEAK-BUCK} = I_{OUT} \times \frac{VOUT \times (VIN_{MAX} - VOUT)}{2 \times VIN_{MAX} \times fs \times L}$$

**Equation 5**

$$I_{PEAK-BOOST} = \frac{VOUT \times I_{OUT}}{\eta \times VIN_{MIN}} \times \frac{VIN_{MIN} \times (VOUT - VIN_{MIN})}{2 \times VOUT \times fs \times L}$$

The maximum of the two values above must be considered when selecting the inductor.

## 8.3 Input and output capacitor selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to get stable operation. Minimum values of 10 µF for both capacitors are needed to achieve a good behavior of the device.

The input capacitor must be placed as close as possible to the device.

# 9 Recommended PCB layout

**Figure 17. Component placement**

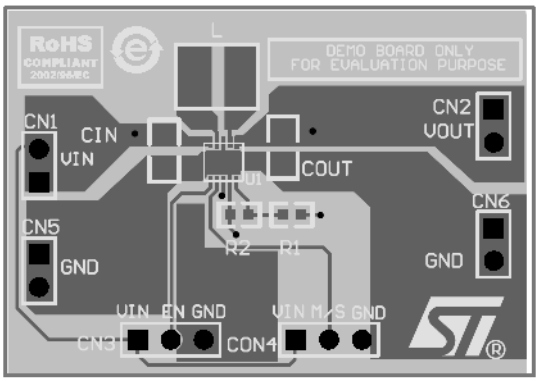



**Figure 18. Top layer routing**

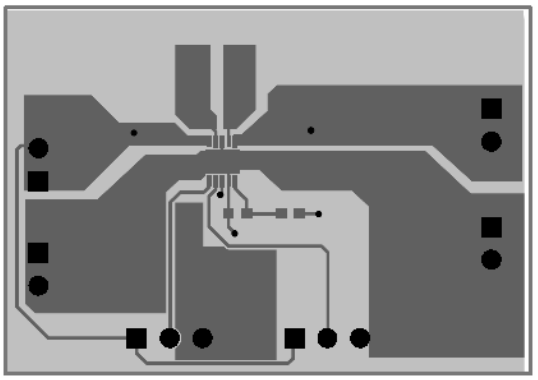
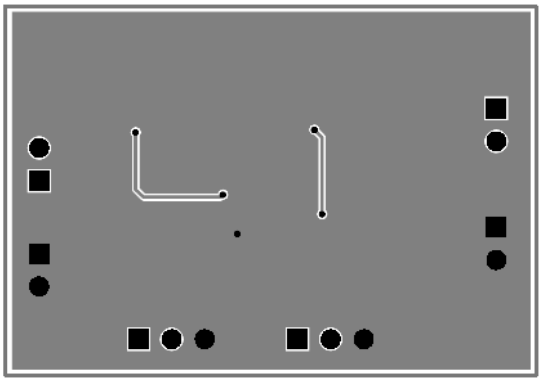


**Figure 19. Bottom layer routing**

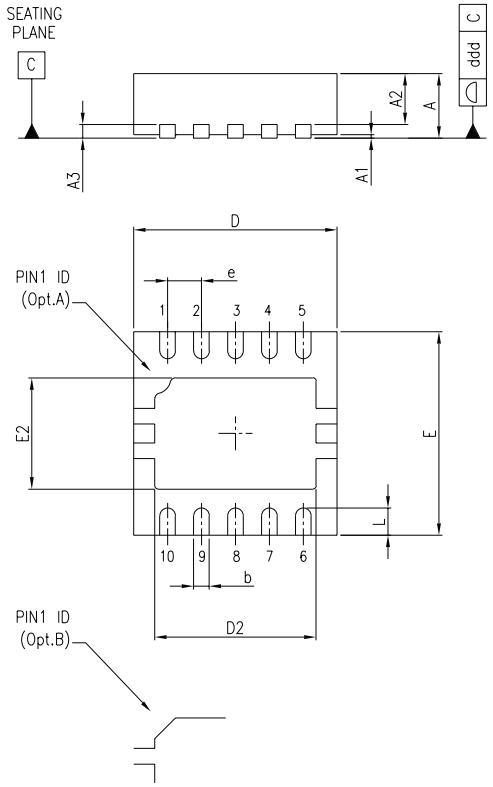


# 10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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## DFN10 (3x3 mm) mechanical data

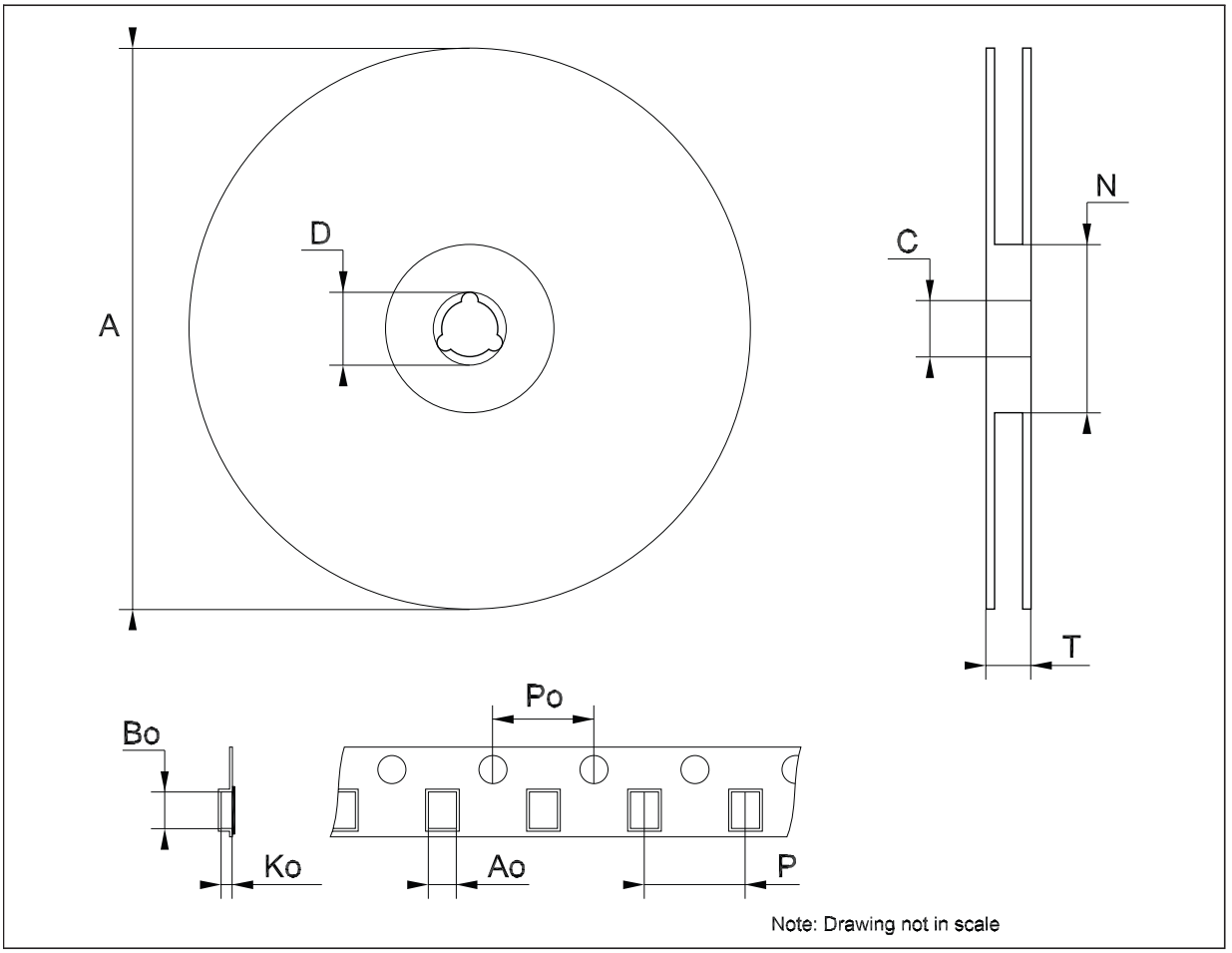
| Dim. | mm. | | | mils. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1.00 | 31.5 | 35.4 | 39.4 |
| A1 | | 0.02 | 0.05 | | 0.8 | 2.0 |
| A2 | 0.55 | 0.65 | 0.80 | 21.7 | 25.6 | 31.5 |
| A3 | | 0.20 | | | 7.9 | |
| b | 0.18 | 0.25 | 0.30 | 7.1 | 9.8 | 11.8 |
| D | 2.85 | 3.00 | 3.15 | 112.2 | 118.1 | 124.0 |
| D2 | 2.20 | | | 86.6 | | |
| E | 2.85 | 3.00 | 3.15 | 112.2 | 118.1 | 124.0 |
| E2 | 1.40 | | 1.75 | 55.1 | | 68.9 |
| e | | 0.50 | | | 19.7 | |
| L | 0.30 | 0.40 | 0.50 | 11.8 | 15.7 | 19.7 |
| ddd | | | 0.08 | | | 3.1 |




7426335F

## Tape & reel QFNxx/DFNxx (3x3) mechanical data

| Dim. | mm. | | | inch. | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 180 | | | 7.087 |
| C | 12.8 | | 13.2 | 0.504 | | 0.519 |
| D | 20.2 | | | 0.795 | | |
| N | 60 | | | 2.362 | | |
| T | | | 14.4 | | | 0.567 |
| Ao | | 3.3 | | | 0.130 | |
| Bo | | 3.3 | | | 0.130 | |
| Ko | | 1.1 | | | 0.043 | |
| Po | | 4 | | | 0.157 | |
| P | | 8 | | | 0.315 | |




Note: Drawing not in scale

# 11 Revision history

**Table 7. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 09-Feb-2009 | 1 | First release. |

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