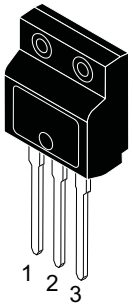
STFI13N80K5

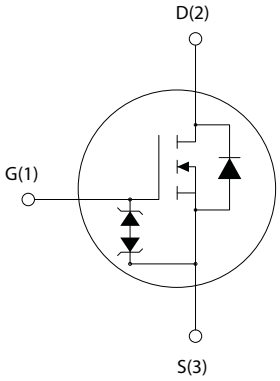
N-channel 800 V, 0.37 Ω typ.,12 A MDmesh™ K5 Power MOSFET in an I²PAKFP package

Datasheet - production data



I²PAKFP

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$	I_D	P_{TOT}
STFI13N80K5	800 V	0.45 Ω	12 A	35 W

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STFI13N80K5	13N80K5	I²PAKFP (TO-281)	Tube

This is information on a product in full production. www.st.com

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2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 9

4 Package mechanical data 10

5 Revision history 12

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	12(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	7.6(1)	A
I_{DM} (2)	Drain current (pulsed)	48(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	148	mJ
V_{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500	V
dv/dt (3)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Limited by package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq$ 12 A, di/dt $\leq$ 100 A/µs, $V_{Peak} \leq V_{(BR)DSS}$
4. $V_{DS} \leq$ 640 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.57	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.5	

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 800 V			1	µA
		V_{GS} = 0, V_{DS} = 800 V, Tc=125 °C			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 6 A		0.37	0.45	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	870	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 640 V	-	110	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	43	-	pF
R_G	Intrinsic gate resistance	f = 1MHz, I_D=0	-	5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 12 A V_{GS} =10 V *(see Figure 16)*	-	29	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 6A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 18)*	-	16	-	ns
t_r	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_f	Fall time		-	16	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		14	A
I_{SDM}	Source-drain current (pulsed)		-		56	A
V_{SD} (1)	Forward on voltage	V_{GS}=0, I_{SD}= 12 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 12 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 17)*	-	406		ns
Q_{rr}	Reverse recovery charge		-	5.7		µC
I_{RRM}	Reverse recovery current		-	28		A
t_{rr}	Reverse recovery time	I_{SD}= 12 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C *(see Figure 17)*	-	600		ns
Q_{rr}	Reverse recovery charge		-	7.9		µC
I_{RRM}	Reverse recovery current		-	26		A

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA, I_D= 0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

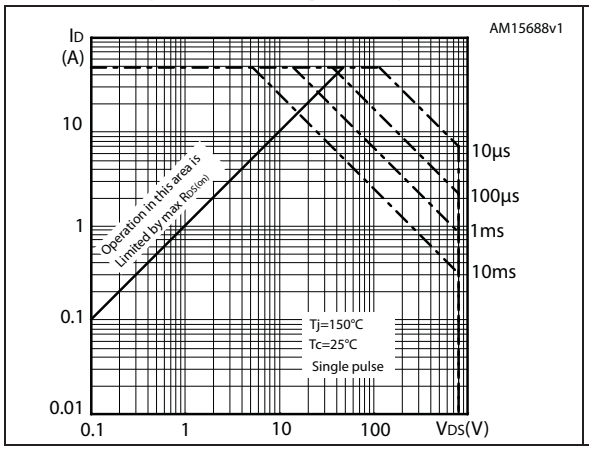


Figure 3. Thermal impedance

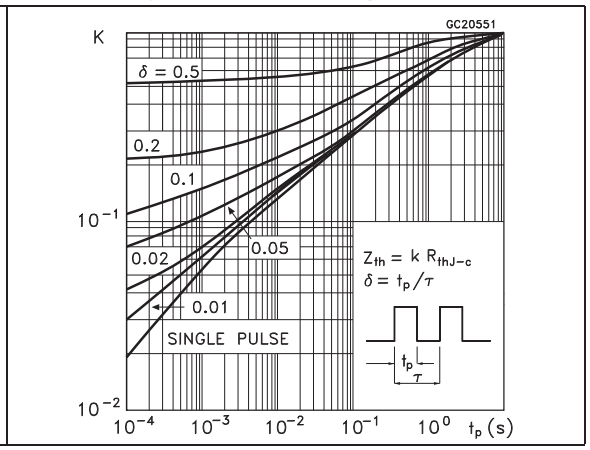


Figure 4. Output characteristics

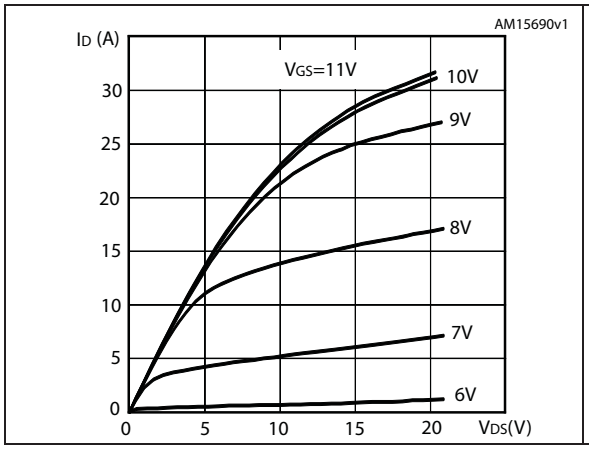


Figure 5. Transfer characteristics

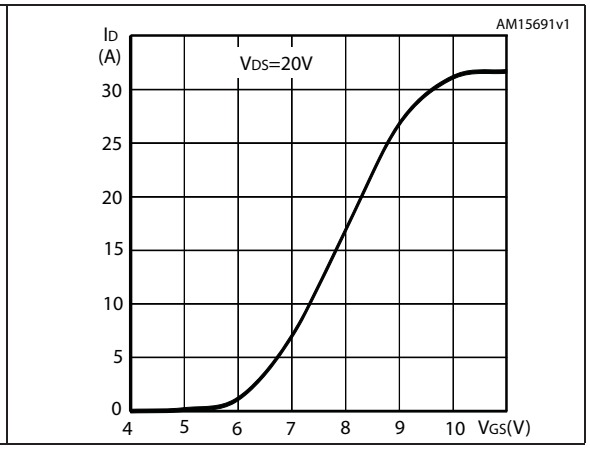


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

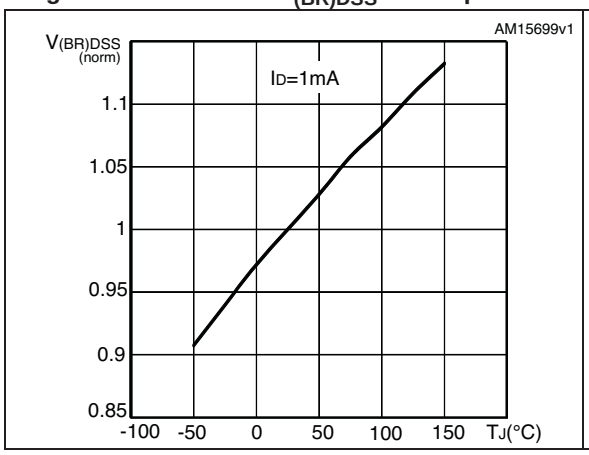


Figure 7. Static drain-source on-resistance

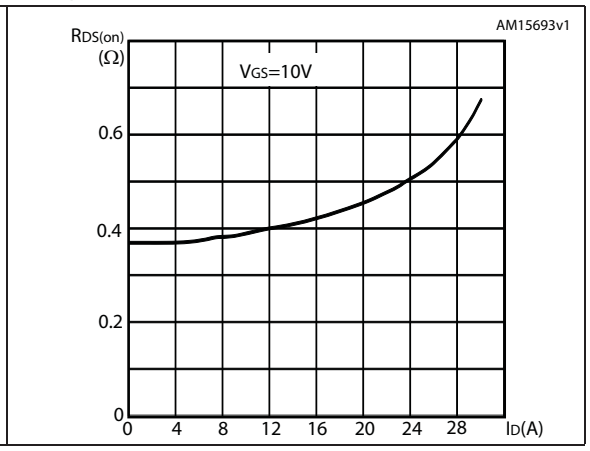


Figure 8. Gate charge vs gate-source voltage

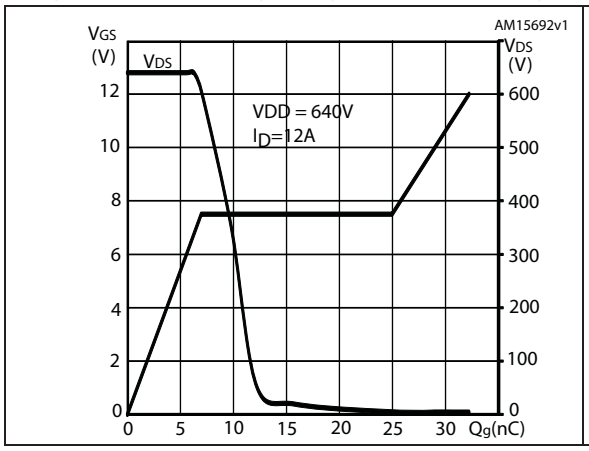


Figure 9. Capacitance variations

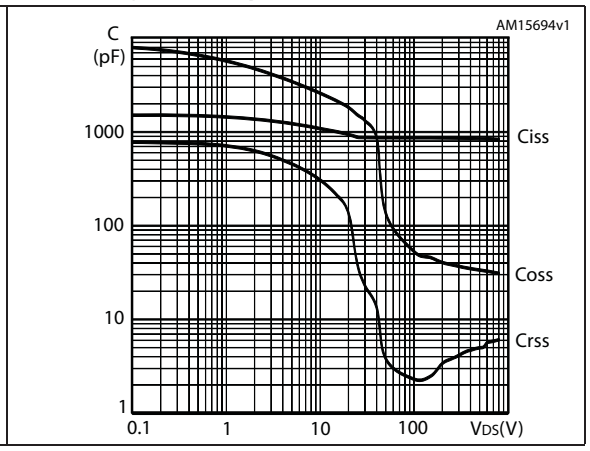


Figure 10. Normalized gate threshold voltage vs temperature

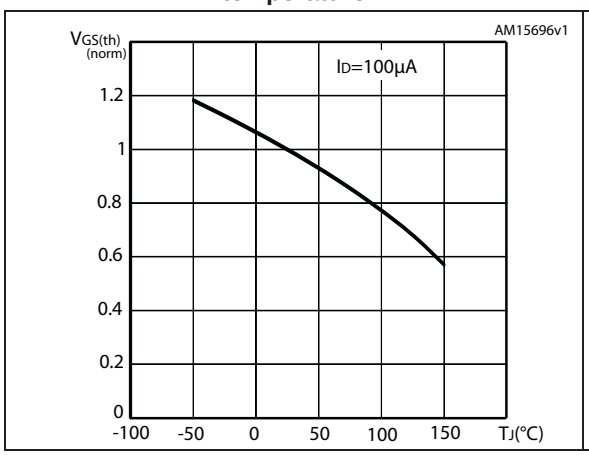


Figure 11. Normalized on-resistance vs temperature

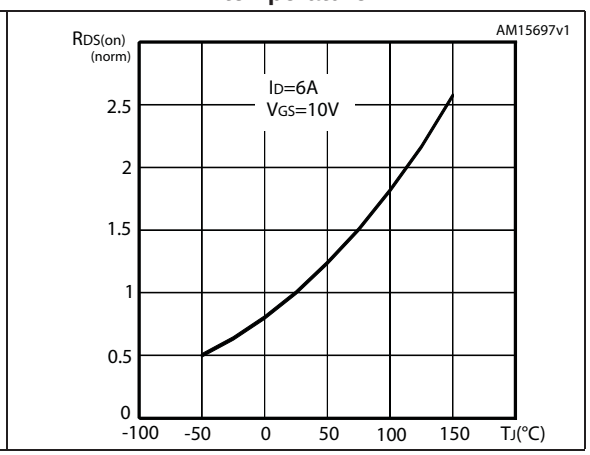


Figure 12. Source-drain diode forward characteristics

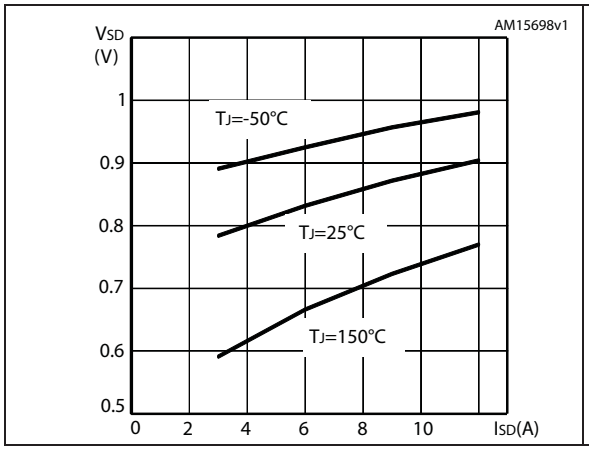


Figure 13. Output capacitance stored energy

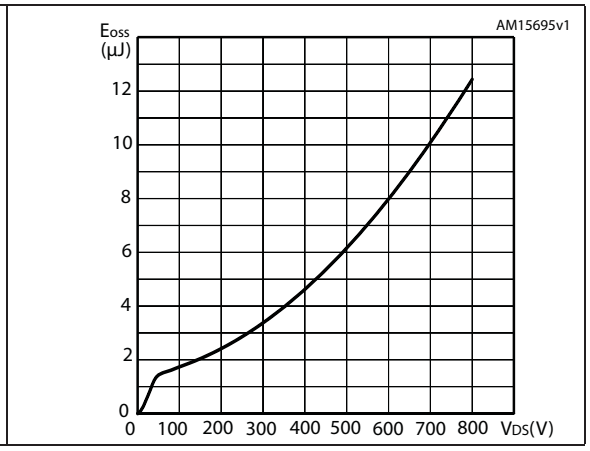
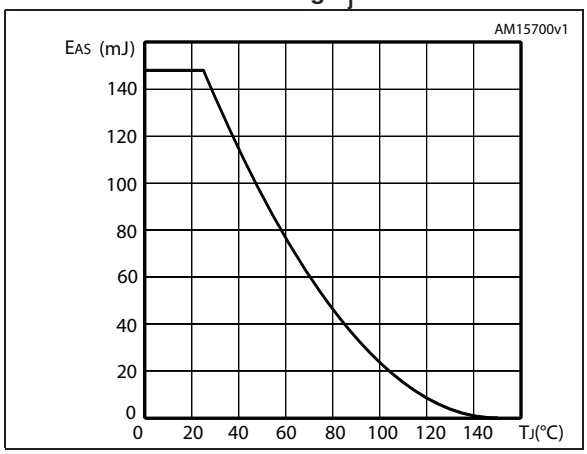


Figure 14. Maximum avalanche energy vs. starting T_j



3 Test circuits

Figure 15. Switching times test circuit for resistive load

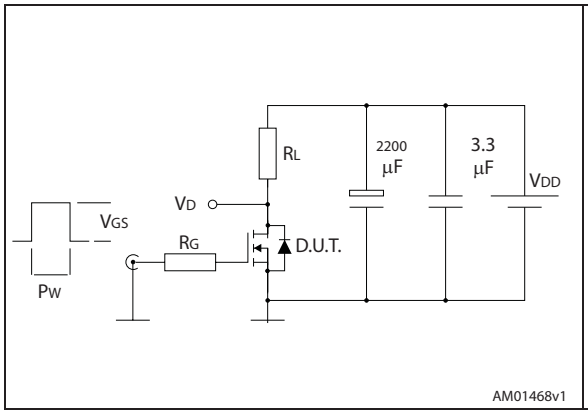


Figure 16. Gate charge test circuit

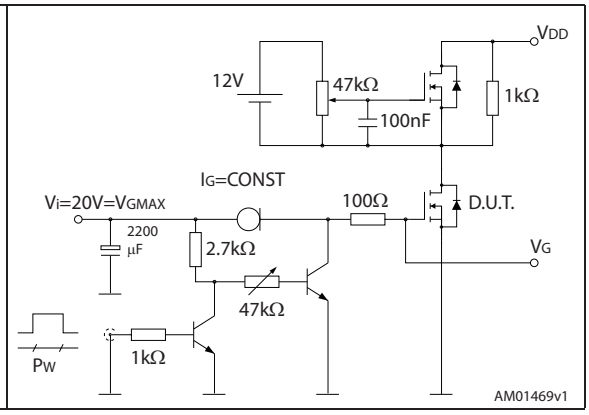


Figure 17. Test circuit for inductive load switching and diode recovery times

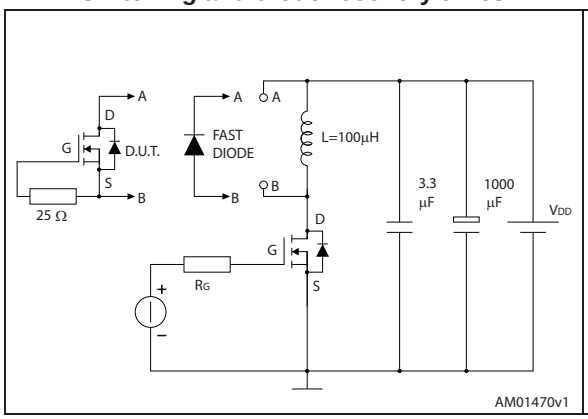


Figure 18. Unclamped inductive load test circuit

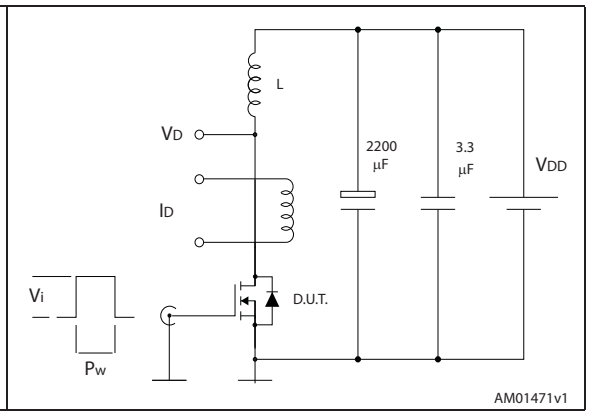


Figure 19. Unclamped inductive waveform

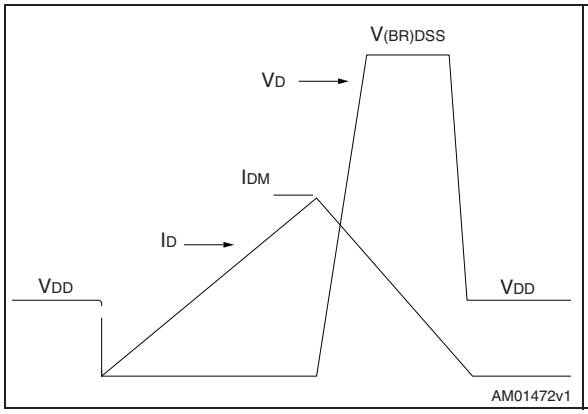
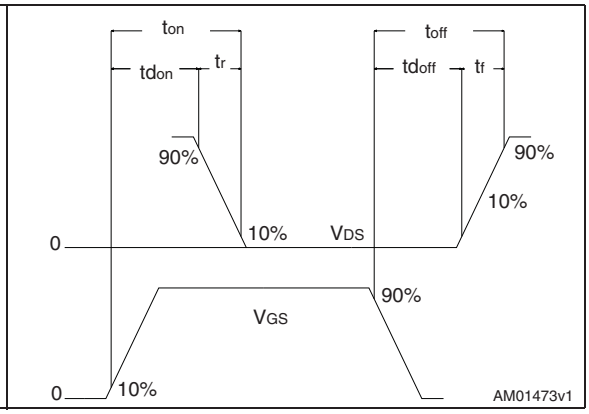


Figure 20. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 21. I²PAKFP (TO-281) drawing

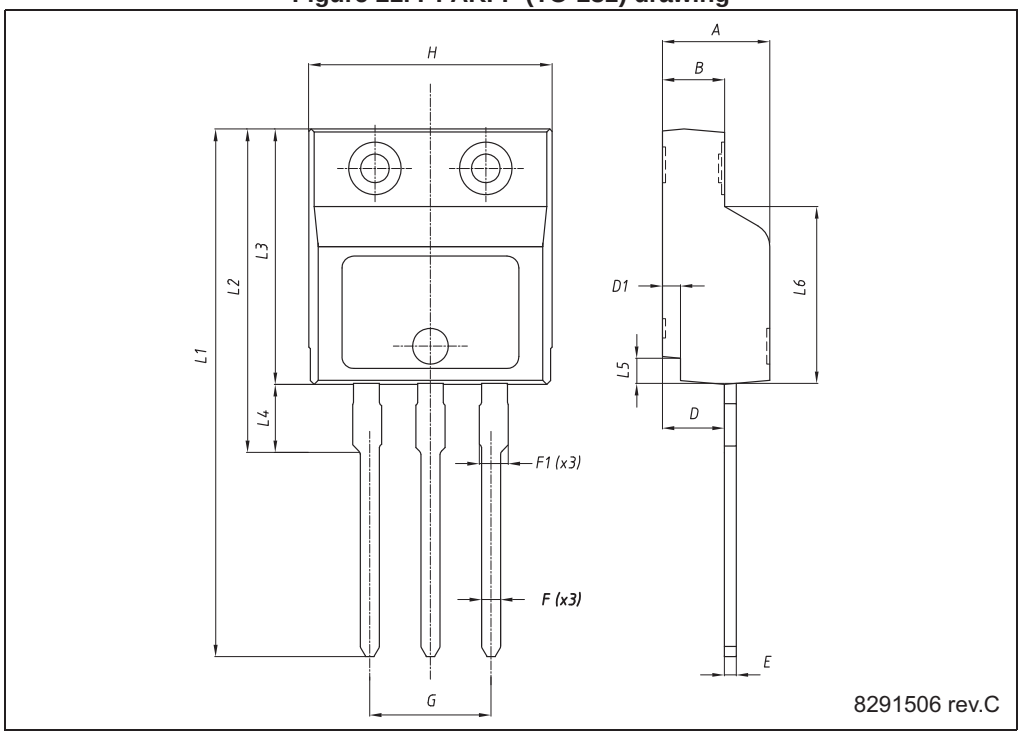


Table 9. I^2PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
25-Nov-2014	1	Initial release.
04-Dec-2014	2	Updated *4: Package mechanical data* and *Figure 1.: Internal schematic diagram* Minor text changes.

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