STK5MFU3C1A-E

2-in-1 PFC and Inverter Intelligent Power Module (IPM), 600 V, 30 A

The STK5MFU3C1A-E is a fully-integrated PFC and inverter power stage consisting of a high-voltage driver, six motor drive IGBT's, one PFC IGBT, one PFC rectifier and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors.
The IGBT's are configured in a 3-phase bridge with common emitter connections for the lower legs.
An internal comparator and reference connected to the over-current protection circuit allows the designer to set individual over-current protection levels for the PFC and the inverter stages. Additionally, the power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions.

Features

- Simple thermal design with PFC and inverter stage in one package.
- PFC operating frequency up to 40 kHz
- Cross-conduction protection
- Adjustable over-current protection level
- Integrated bootstrap diodes and resistors

Certification

- UL1557 (File Number : E339285)

Typical Applications

- Heat Pumps
- Home Appliances
- Industrial Fans
- Industrial Pumps

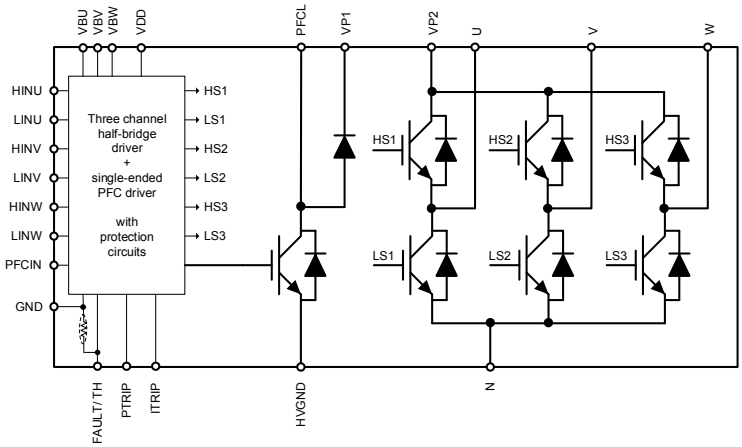


Figure 1. Functional Diagram

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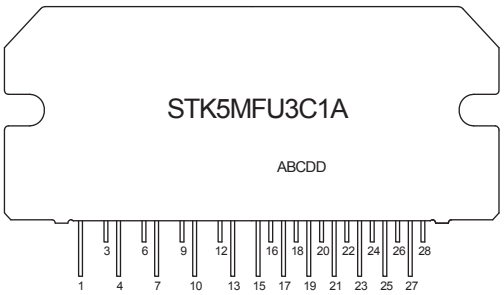
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PACKAGE PICTURE



SIP28 78x31.1

MARKING DIAGRAM



STK5MFU3C1A = Specific Device Code
A = Year
B = Month
C = Production Site
DD = Factory Lot Code
Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK5MFU3C1A-E	SIP28 78x31.1 (Pb-Free)	280 / Box

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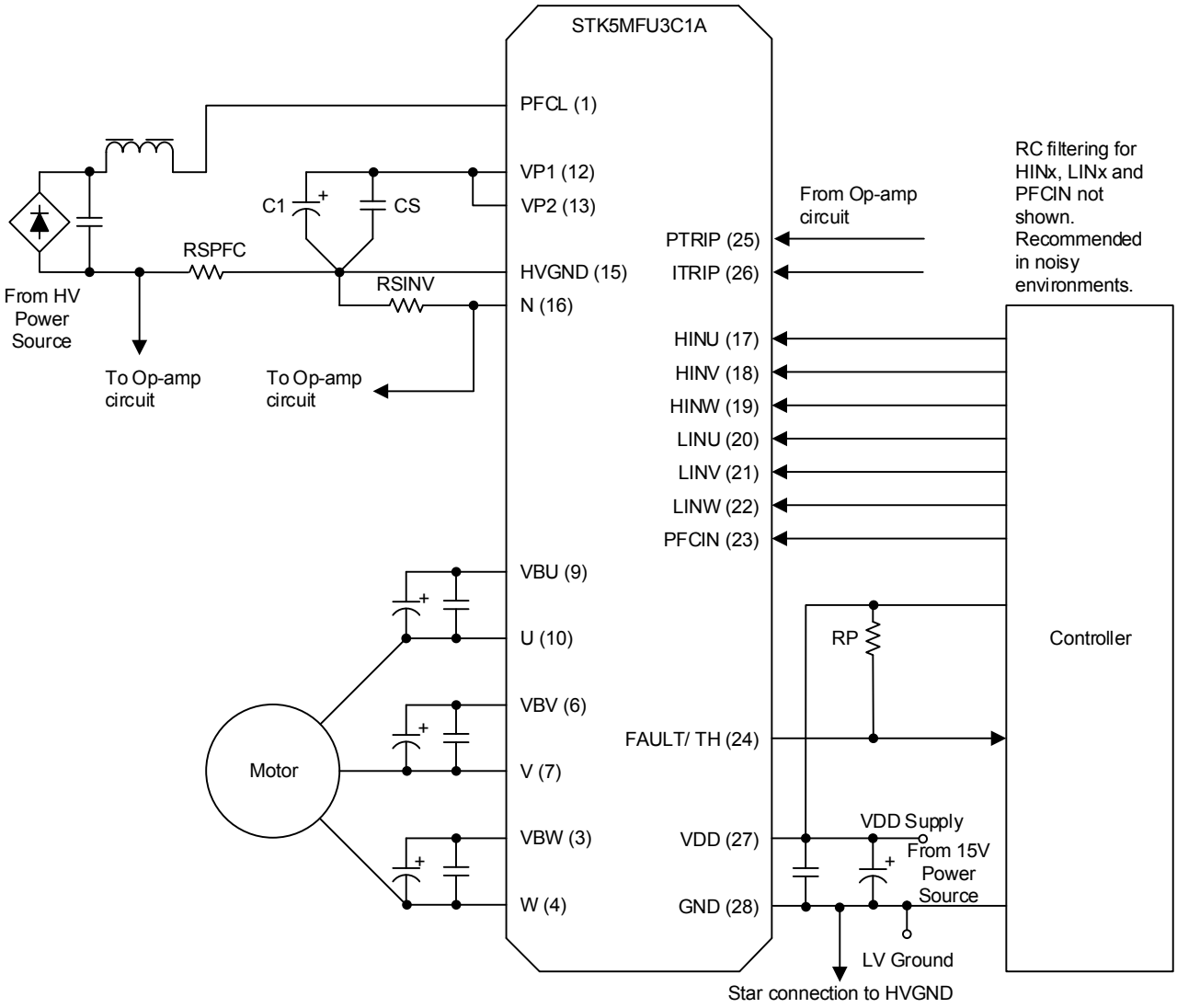


Figure 2. Application Schematic

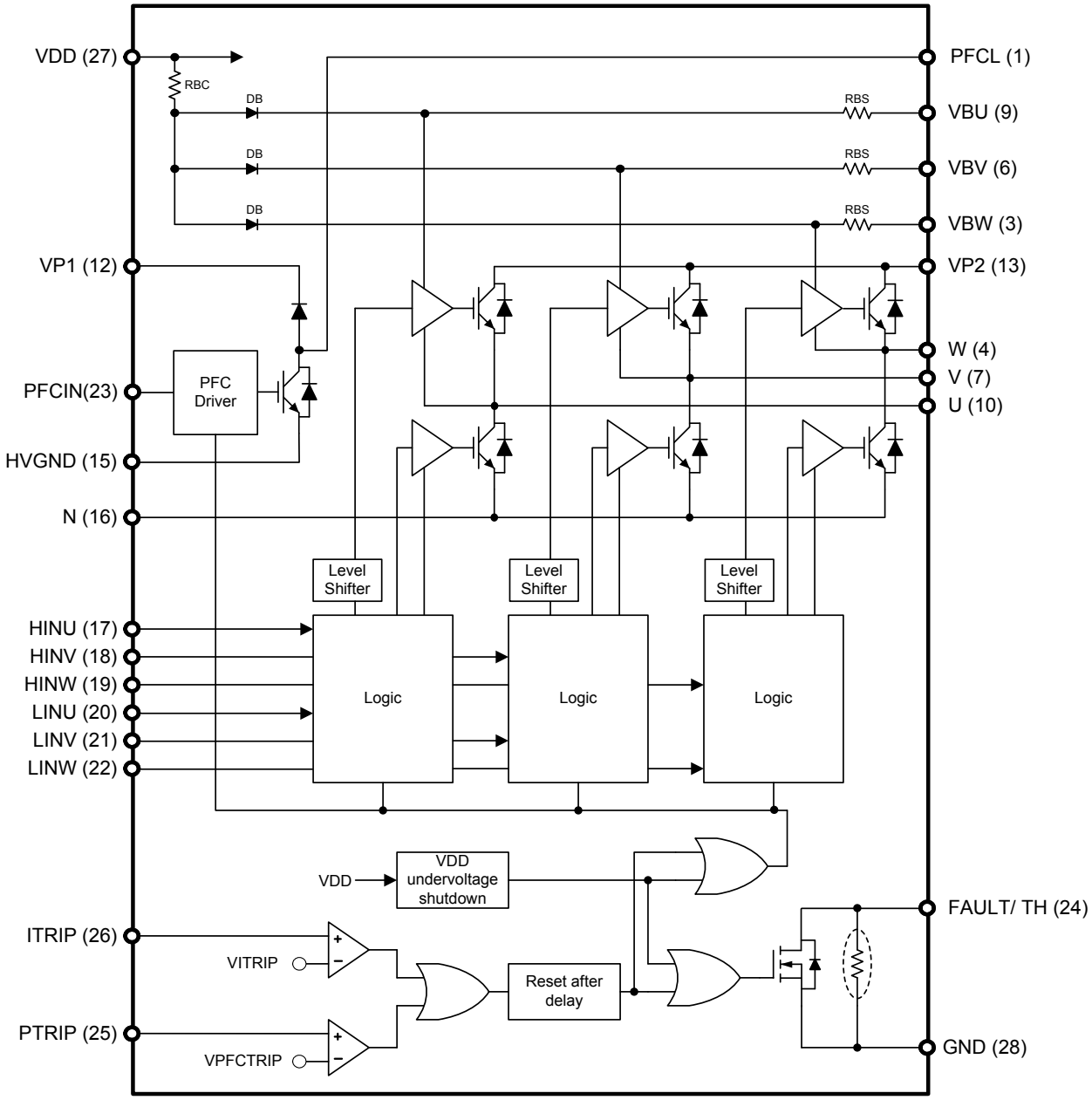


Figure 3. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	PFCL	PFC Inductor Connection to IGBT and Rectifier node
3	VBW	High Side Floating Supply voltage for W phase
4	W	V phase output. Internally connected to W phase high side driver ground
6	VBV	High Side Floating Supply voltage for V phase
7	V	V phase output. Internally connected to V phase high side driver ground
9	VBU	High Side Floating Supply voltage for U phase
10	U	U phase output. Internally connected to U phase high side driver ground
12	VP1	Positive PFC Output Voltage
13	VP2	Positive Inverter Output Voltage
15	HVGND	Negative PFC Output Voltage
16	N	Low Side Emitter Connection
17	HINU	Logic Input High Side Gate Driver - Phase U
18	HINV	Logic Input High Side Gate Driver - Phase V
19	HINW	Logic Input High Side Gate Driver - Phase W
20	LINU	Logic Input Low Side Gate Driver - Phase U
21	LINV	Logic Input Low Side Gate Driver - Phase V
22	LINW	Logic Input Low Side Gate Driver – Phase W
23	PFCIN	Logic Input PFC Gate Driver
24	FAULT / TH	FAULT output and thermistor output
25	PTRIP	Current protection pin for PFC
26	ITRIP	Current protection pin for inverter
27	VDD	+15 V Main Supply
28	GND	Negative Main Supply

Note : Pins 2, 5, 8, 11 and 14 are not present

ABSOLUTE MAXIMUM RATINGS at Tc = 25°C (Notes 1, 2)

Rating		Symbol	Conditions	Value	Unit
PFC Section					
PFC IGBT	Collector-emitter voltage	V_{CE}	PFCL to HVGND	600	V
	Repetitive peak collector current	ICP	Duty cycle 10%, pulse width 1ms	150	A
	Collector current	IC		53	A
			Tc = 100°C	26	A
	Maximum power dissipation	PC		96	W
PFC Diode	Diode reverse voltage	VRM	VP1 to PFCL	600	V
	Repetitive peak forward current	IFP1	Duty cycle 10%, pulse width 1ms	90	A
	Diode forward current	IF1		30	A
			Tc = 100°C	18	A
	Maximum power dissipation	PD1		65	W
Anti-parallel Diode	Repetitive peak forward current	IFP2	Duty cycle 10%, pulse width 1ms	11	A
	Diode forward current	IF2		3	A
	Maximum power dissipation	PD2		5	W
Maximum AC input voltage		VAC	Single-phase Full-rectified	264	V
Maximum output voltage		Vo	In the Application Circuit (VAC = 200 V)	450	V
Input AC current (steady state)		Iin		33	Arms
Inverter Section					
Supply voltage		V_{CC}	VP2 to N surge < 500 V (Note 3)	450	V
Collector-emitter voltage		V_{CE} max	VP2 to U, V, W or U, V, W to N	600	V
Output current		Io	VP2, U, V, W, N terminal current	±30	A
			VP2, U, V, W, N terminal current at Tc = 100°C	±15	A
Output peak current		Iop	VP, U, V, W, N terminal current, pulse width 1 ms	±60	A
Maximum power dissipation		Pd	IGBT per 1 channel	65	W
Gate driver section					
Gate driver supply voltage		V_{BS}	VBU to U, VBV to V, VBW to W, VDD to GND (Note 4)	−0.3 to +20.0	V
Input signal voltage		VIN	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN	−0.3 to V_{DD}	V
FAULT terminal voltage		VFAULT	FAULT terminal	−0.3 to V_{DD}	V
ITRIP terminal voltage		VITRIP	ITRIP terminal	−0.3 to +10.0	V
PFCTRIP terminal voltage		VPTRIP	PTRIP terminal	−1.5 to 2.0	V
Intelligent Power Module					
Junction temperature		Tj	IGBT, FRD, Gate driver IC	150	°C
Storage temperature		Tstg		−40 to +125	°C
Operating case temperature		Tc	IPM case temperature	−20 to +100	°C
Tightening torque		MT	Case mounting screws	1.17	Nm
Isolation voltage		Vis	50 Hz sine wave AC 1 minute (Note 5)	2000	Vrms

1. Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This surge voltage developed by the switching operation due to the wiring inductance between VP2 and N terminal.
4. V_{BS} = VBU to U, VBV to V, VBW to W
5. Test conditions : AC 2500 V, 1 second

RECOMMENDED OPERATING RANGES (Note 6)

Rating	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{CC}	VP1 to HVGND, VP2 to N	0	280	400	V
Gate driver supply voltage	VBS	VBU to U, VBV to V, VBW to W	12.5	15	17.5	V
	V_{DD}	V_{DD} to GND	13.5	15	16.5	V
ON-state input voltage	VIN(ON)	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN	2.5	-	5.0	V
OFF-state input voltage	VIN(OFF)		0	-	0.3	V
PWM frequency(PFC)	fPWMp		1	-	40	kHz
PWM frequency(Inverter)	fPWMi		1	-	20	kHz
Dead time	DT	Turn-off to Turn-on (external)	1.5	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque		'M4' type screw	0.79	-	1.17	Nm

6. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 7)

at Tc = 25°C, V_{BIAS} (V_{BS}, V_{DD}) = 15 V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
PFC Section						
Collector-emitter cut-off current	V_{CE} = 600 V	I_{CE}	-	-	0.2	mA
Reverse leakage current (PFC Diode)	VR = 600 V	IR	-	-	0.1	mA
Collector-emitter saturation voltage	IC = 40 A, Tj = 25°C	V_{CE}(sat)	-	1.6	2.2	V
	IC = 20 A, Tj = 100°C		-	1.3	-	V
Diode forward voltage (PFC Diode)	IF = 40 A, Tj = 25°C	VF1	-	2.4	3.4	V
	IF = 20 A, Tj = 100°C		-	1.5	-	
Diode forward voltage (Anti-parallel Diode)	IF = 5 A, Tj = 25°C	VF2	-	1.5	2.4	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	1.3	°C/W
	PFC Diode	θj-c(D)	-	-	1.9	°C/W
Switching characteristics						
Switching time	IC = 40 A, VP = 300 V, Tj = 25°C	tON	0.2	0.4	0.6	μs
		tOFF	0.2	0.5	0.7	μs
Diode reverse recovery time		trr	-	30	-	ns
Inverter section						
Collector-emitter leakage current	V_{CE} = 600 V	I_{CE}	-	-	0.1	mA
Bootstrap diode reverse current	VR(DB) = 600 V	IR(BD)	-	-	0.1	mA
Collector to emitter saturation voltage	IC = 30 A, Tj = 25°C	V_{CE}(SAT)	-	1.8	2.5	V
	IC = 15 A, Tj = 100°C		-	1.5	-	V
Diode forward voltage	IF = 30 A, Tj = 25°C	VF	-	2.0	2.7	V
	IF = 15 A, Tj = 100°C		-	1.6	-	V
Junction to case thermal resistance	IGBT	θj-c(T)	-	-	1.9	°C/W
	FRD	θj-c(D)	-	-	2.9	°C/W
Switching time	IC = 30 A, V_{CC} = 300 V, Tj = 25°C	t_{ON}	0.3	0.6	1.0	μs
		t_{OFF}	0.5	1.1	1.5	μs
Reverse bias safe operating area	IC = 60 A, V_{CE} = 450 V	RBSOA	Full Square			
Short circuit safe operating area	V_{CE} = 400 V, Tj = 100°C	SCSOA	4	-	-	μs
Allowable offset voltage slew rate	U, V, W to N	dv/dt	−50	-	50	V/ns

7. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (Note 8)
at Tc = 25°C

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Driver Section						
Gate driver consumption current	V_{BS} = 15 V (Note 4), per driver	ID	-	0.08	0.4	mA
	V_{DD} = 15V, total	ID	-	0.85	2.4	mA
High level Input voltage	HINU, HINV, HINW, LINU, LINV, LINW, PFCIN to GND	VIN H	2.5	-	-	V
Low level Input voltage		VIN L	-	-	0.8	V
Logic 1 input current	VIN = +3.3 V	I_{IN+}	-	100	143	μA
Logic 0 input current	VIN = 0 V	I_{IN-}	-	-	2	μA
Bootstrap diode forward voltage	IF = 0.1 A	VF(DB)	-	0.8	-	V
Bootstrap circuit resistance	Resistor value for common boot charge line	RBC	-	22	-	Ω
	Resister values for separate boot charge lines	RBS	-	33	-	Ω
FAULT terminal sink current	FAULT : ON / VFAULT = 0.1 V	IoSD	-	2	-	mA
FAULT clearance delay time		FLTCLR	1.0	1.85	2.7	ms
ITRIP threshold voltage	ITRIP to GND	VITRIP	0.44	0.49	0.54	V
PTRIP threshold voltage	PTRIP to GND	VPTRIP	−0.37	−0.31	−0.25	V
V_{DD} and V_{BS} supply undervoltage positive going input threshold		V_{CCUV+} V_{BSUV+}	10.5	11.1	11.7	V
V_{DD} and V_{BS} supply undervoltage negative going input threshold		V_{CCUV-} V_{BSUV-}	10.3	10.9	11.5	V
V_{DD} and V_{BS} supply undervoltage lockout hysteresis		V_{CCUVH} V_{BSUVH}	0.14	0.2	-	V

8. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS PFC SECTION

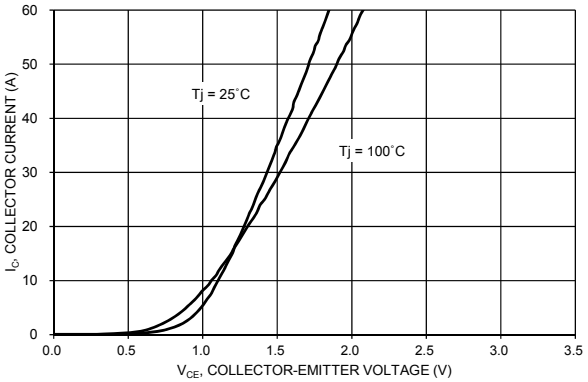


Figure 4. V_{CE} versus I_C for different temperatures (V_{DD} = 15 V)

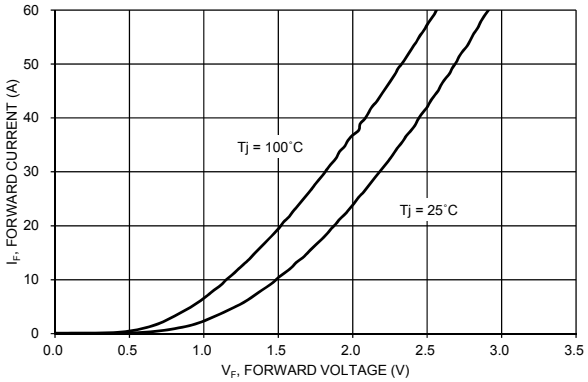


Figure 5. V_F versus I_F for different temperatures

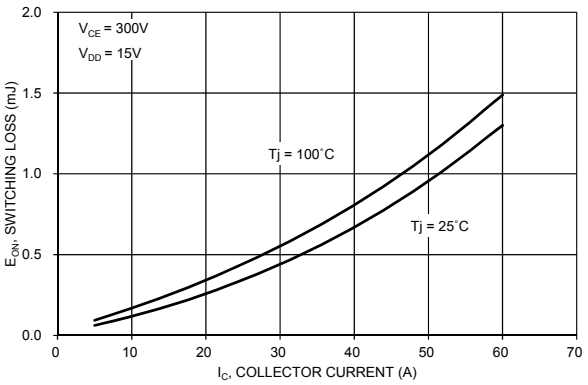


Figure 6. E_{ON} versus I_C for different temperatures

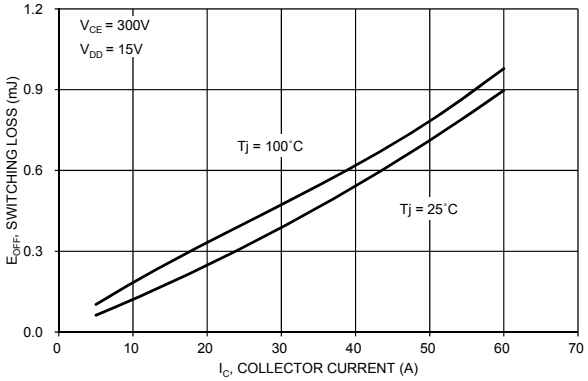


Figure 7. E_{OFF} versus I_C for different temperatures

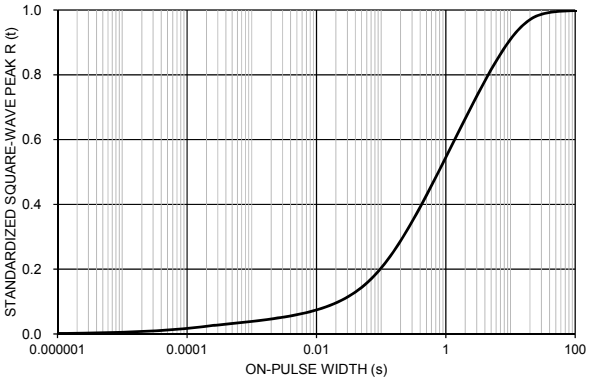


Figure 8. Thermal Impedance Plot

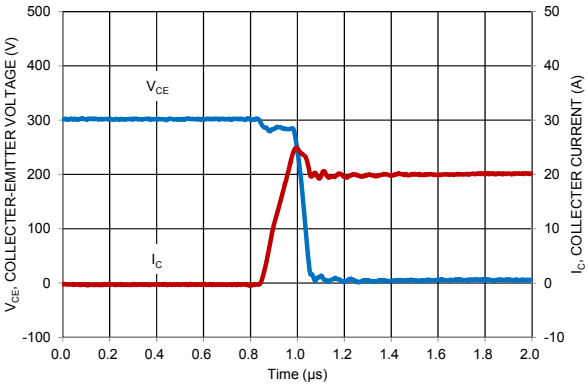


Figure 9. Turn-on waveform Tj = 100°C, V_{CC}= 300 V

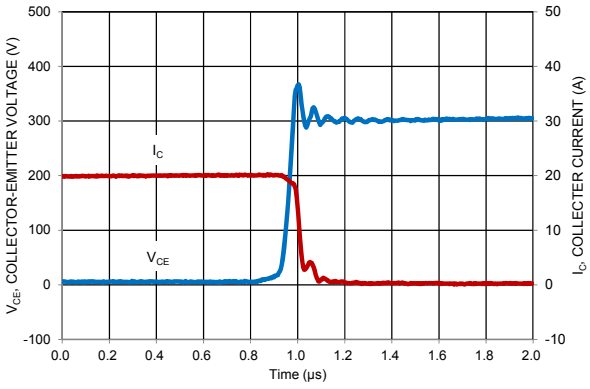


Figure 10. Turn-off waveform Tj = 100°C, V_{CC} = 300 V

TYPICAL CHARACTERISTICS INV SECTION

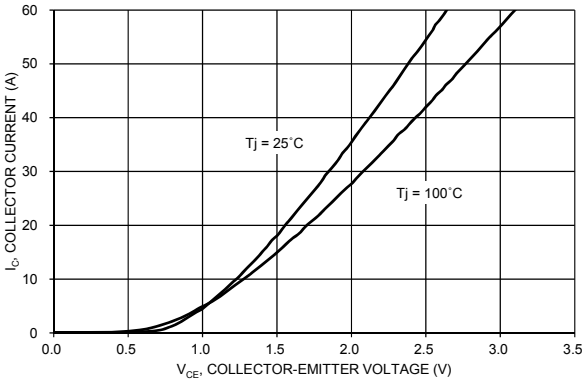


Figure 11. V_{CE} versus I_C for different temperatures (V_{DD} = 15 V)

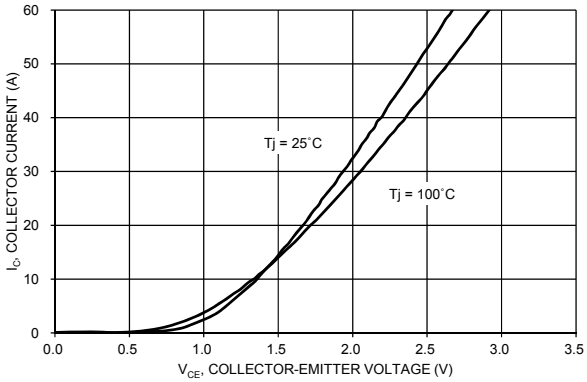


Figure 12. V_F versus I_F for different temperatures

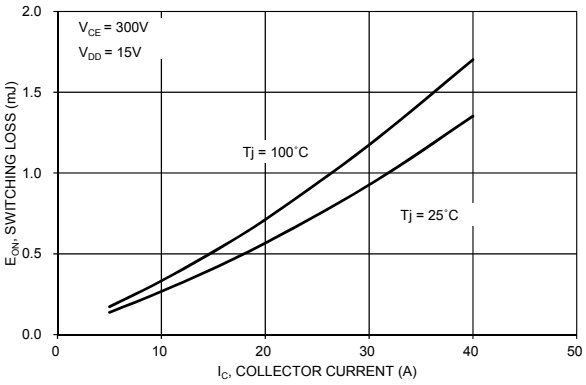


Figure 13. E_{ON} versus I_C for different temperatures

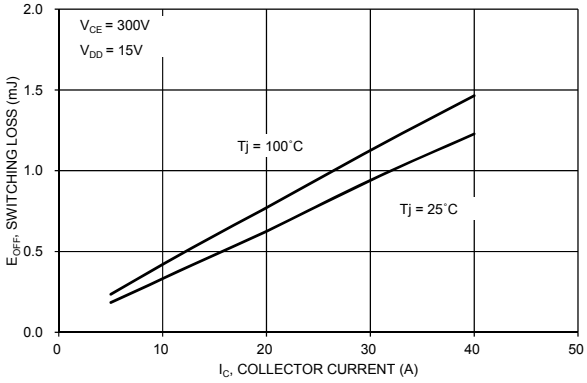


Figure 14. E_{OFF} versus I_C for different temperatures

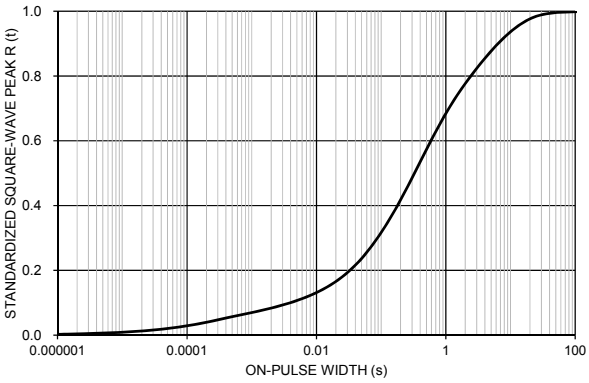


Figure 15. Thermal Impedance Plot

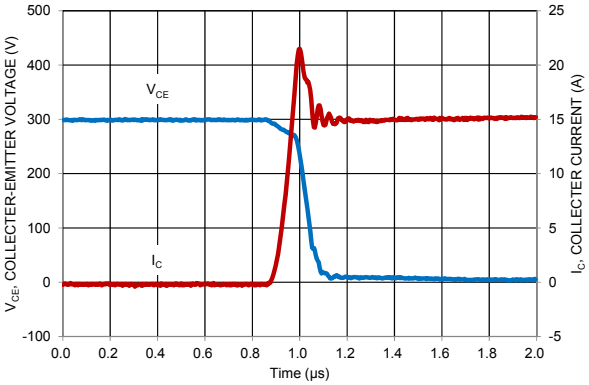


Figure 17. Turn-on waveform Tj = 100°C, V_{CC} = 300 V

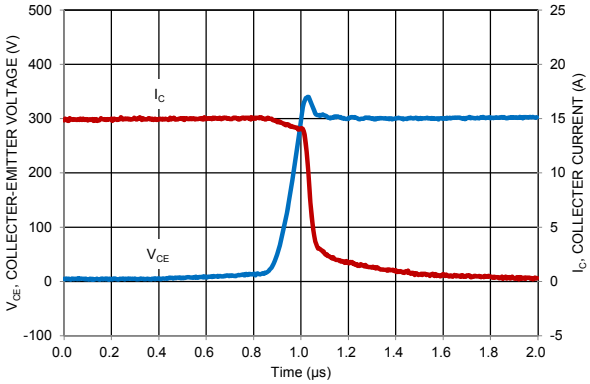


Figure 18. Turn-off waveform Tj = 100°C, V_{CC} = 300 V

APPLICATIONS INFORMATION

Input / Output Timing Chart

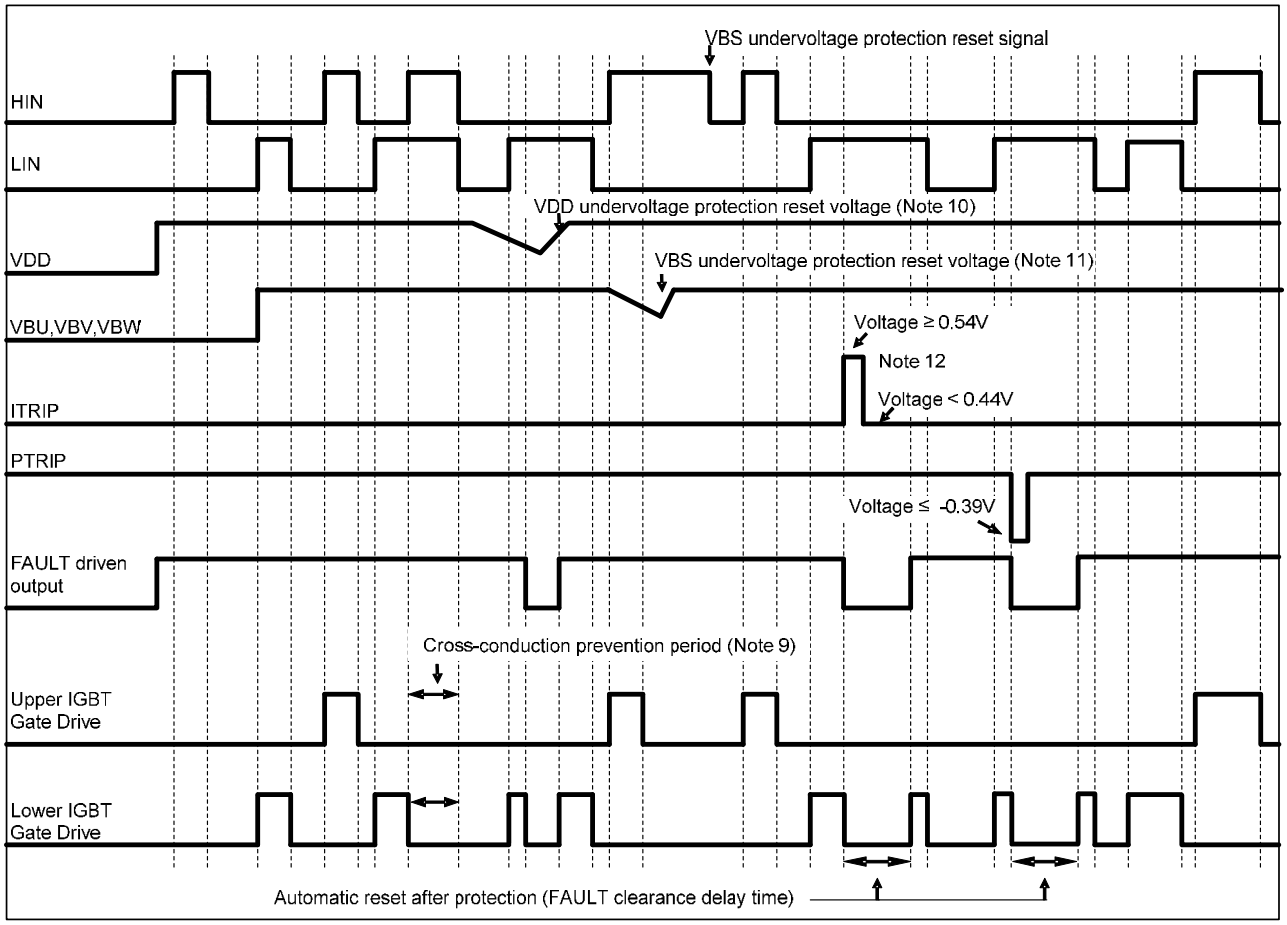


Figure 18. Input / Output Timing Chart

Notes

9. This section of the timing diagram shows the effect of cross-conduction prevention.
10. This section of the timing diagram shows that when the voltage on V_{DD} decreases sufficiently all gate output signals will go low, switching off all six IGBTs. When the voltage on V_{DD} rises sufficiently, normal operation will resume.
11. This section shows that when the bootstrap voltage on VBU (VBV, VBW) drops, the corresponding high side output U (V, W) is switched off. When the voltage on VBU (VBV, VBW) rises sufficiently, normal operation will resume.
12. This section shows that when the voltage on ITRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed. Similarly, when the voltage on PTRIP exceeds the threshold, all IGBT's are turned off. Normal operation resumes later after the over-current condition is removed

Input / Output Logic Table

INPUT				**OUTPUT**			
HIN	**LIN**	**ITRIP**	**PTRIP**	**High side IGBT**	**Low side IGBT**	**U,V,W**	**FAULT**
H	L	L	L	ON	OFF	VP	OFF
L	H	L	L	OFF	ON	N	OFF
L	L	L	L	OFF	OFF	High Impedance	OFF
H	H	L	L	OFF	OFF	High Impedance	OFF
X	X	H	X	OFF	OFF	High Impedance	ON
X	X	X	H	OFF	OFF	High Impedance	ON

Thermistor characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tth = 25°C	99	100	101	kΩ
	R_{100}	Tth = 100°C	5.18	5.38	5.60	kΩ
B-Constant (25 to 50°C)	B		4208	4250	4293	K
Temperature Range			−40		+125	°C

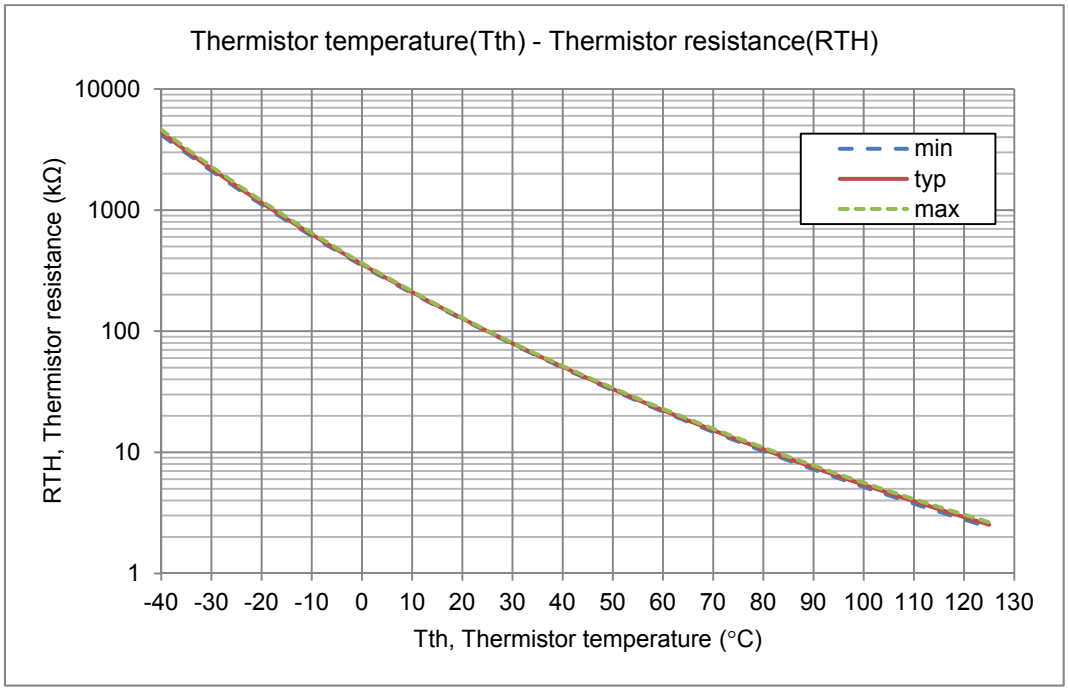


Figure 19. Thermistor Resistance versus Thermistor Temperature

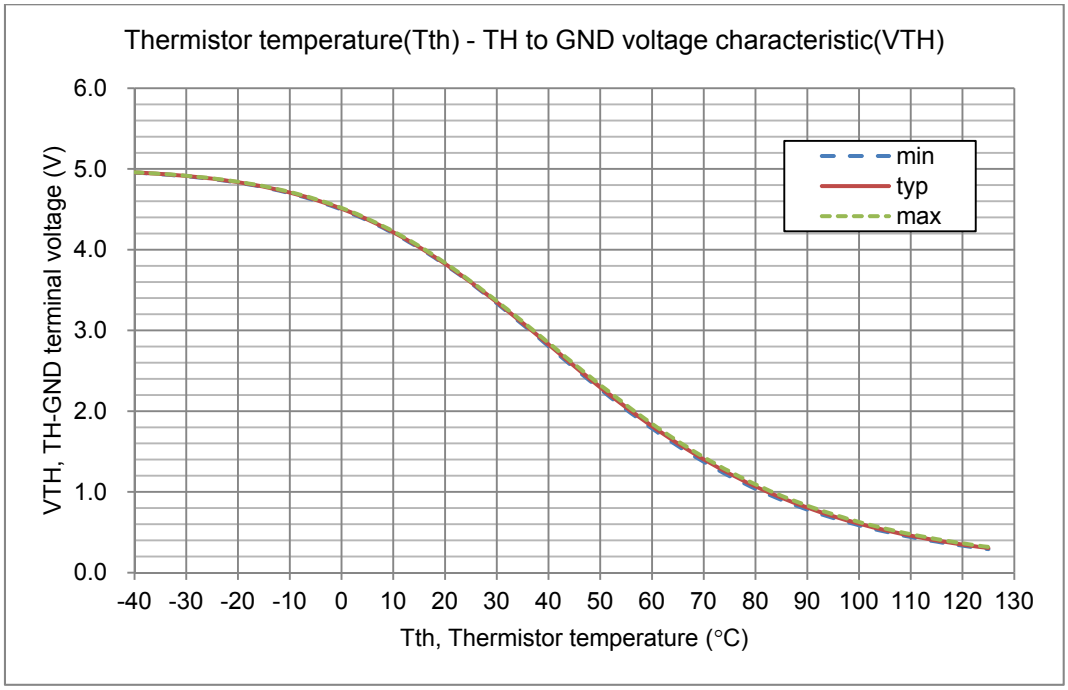


Figure 20. Thermistor Voltage versus Thermistor Temperature
Conditions: RTH = 39 kΩ, pull-up voltage 5.0 V (see Figure 2)

Signal inputs
Each signal input has a pull-down resistor. An additional pull-down resistor of between 2.2 kΩ and 3.3 kΩ is recommended on each input to improve noise immunity.

FAULT/ TH pin
The FAULT pin is connected to an open-drain FAULT output requiring a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The FAULT output is triggered if there is a V_{DD} undervoltage or an overcurrent condition on either the PFC or inverter stages.

The FAULT/ TH pin is also connected to a grounded thermistor. Thermal characteristics are shown in this datasheet for a pull up value of 39 kΩ.

Undervoltage protection
If V_{DD} goes below the V_{DD} supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until V_{DD} rises above the V_{DD} supply undervoltage lockout rising threshold. The hysteresis is approximately 200 mV.

Overcurrent protection
An over-current condition is detected if the voltage on the ITRIP/PTRIP pin is larger than the reference voltage. There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 0.6 μs, the FAULT output is switched on.

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (IO).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and V_{DD} supplies
Both the high voltage and V_{DD} supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100 nF and 10 μF.

Minimum input pulse width
When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of bootstrap capacitor value
The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor :

- VBS: Bootstrap power supply.
  15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.
  266 nC
- UVLO: Falling threshold for UVLO.
  Specified as 12 V.
- IDMAX: High side drive power dissipation.
  Specified as 0.4 mA
- TONMAX: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + IDMAX * TONMAX) / (VBS – UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply. If the capacitors selected are 47 μF or more, a series resistor of 20 Ω should be added in series with the three capacitors to limit the current. The resistors should be inserted between VBU and U, VBV and V and VBW and W.

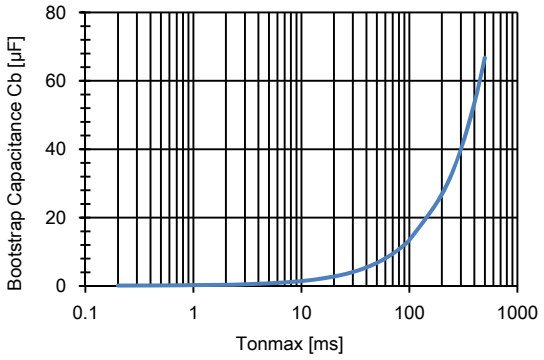
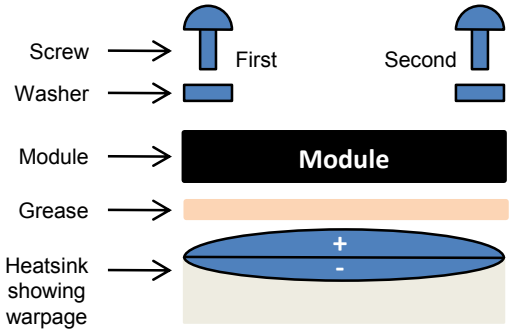


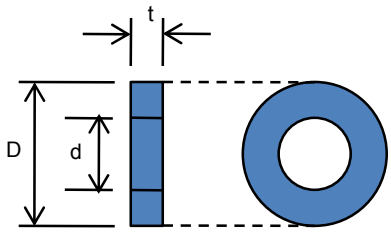
Figure 21. Bootstrap capacitance versus Tonmax

Mounting Instructions

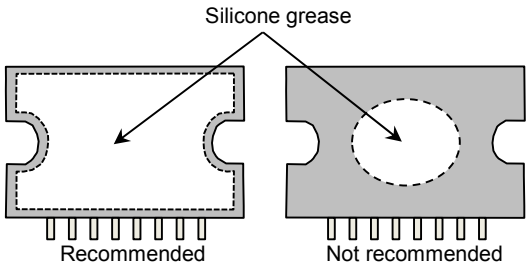
Item	Recommended Condition
Pitch	70.0 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	diameter : M4 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D : 9 mm, d : 4.3 mm and t : 0.8 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : −50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 20 to 30 % of final tightening on first screw Temporary tightening : 20 to 30 % of final tightening on second screw Final tightening : 0.79 to 1.17 Nm on first screw Final tightening : 0.79 to 1.17 Nm on second screw
Grease	Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.



Mounting components



Washer details



Thermal grease must be spread evenly (left is correct)

Figure 22. Module Mounting details: components; washer drawing; need for even spreading of thermal grease

TEST CIRCUITS

■ I_{CE}, IR(DB)

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	13	13	13	10	7	4	1
B	10	7	4	16	16	16	15

U+,V+,W+ : High side phase
U-,V-,W- : Low side phase

	U(DB)	V(DB)	W(DB)	PFC Diode
A	9	6	3	12
B	28	28	28	1

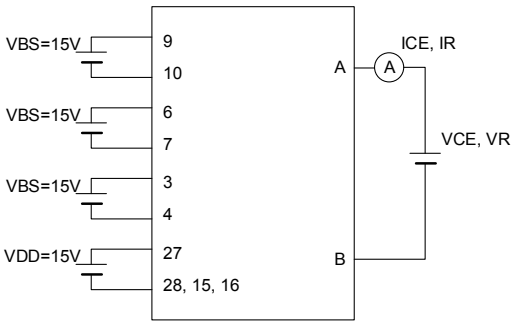


Figure 23. Test Circuit for I_{CE}

■ V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	13	13	13	10	7	4	1
B	10	7	4	16	16	16	15
C	17	18	19	20	21	22	23

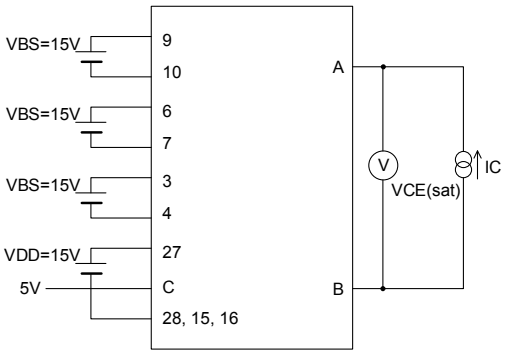


Figure 24. Test circuit for $V_{CE(SAT)}$

■ V_F (Test by pulse)

	U+	V+	W+	U-	V-	W-
A	13	13	13	10	7	4
B	10	7	4	16	16	16

	U(DB)	V(DB)	W(DB)	PFC Diode	Anti-parallel Diode
A	9	6	3	12	1
B	28	28	28	1	15

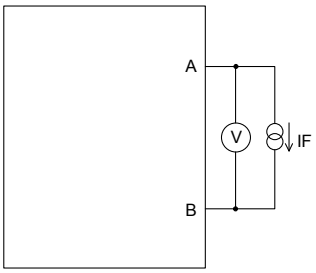


Figure 25. Test circuit for V_F

■ ID

	VBS U+	VBS V+	VBS W+	V_{DD}
A	9	6	3	27
B	10	7	4	28

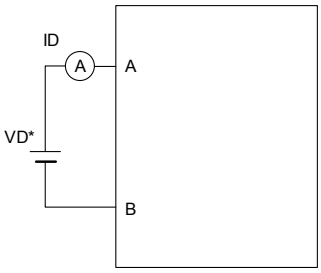
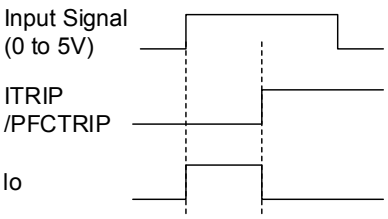


Figure 26. Test circuit for I_D

■ VITRIP, VPTRIP

	VITRIP(U-)	VPTRIP
A	10	1
B	16	15
C	20	23
D	26	25



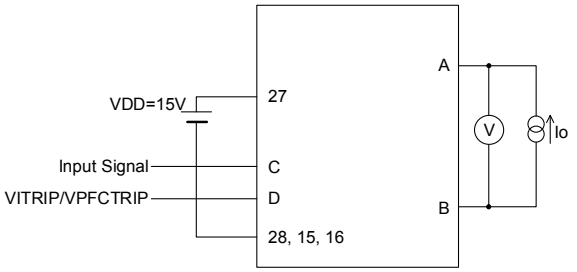
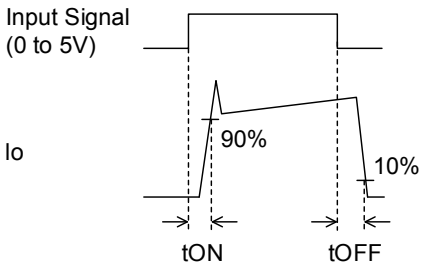


Figure 27. Test circuit for ITRIP.PTRIP

■ Switching time (The circuit is a representative example of the lower side U phase.)

	U+	V+	W+	U-	V-	W-	PFC IGBT
A	13	13	13	13	13	13	12
B	16	16	16	16	16	16	15
C	10	7	4	13	13	13	12
D	16	16	16	10	7	4	1
E	17	18	19	20	21	22	23



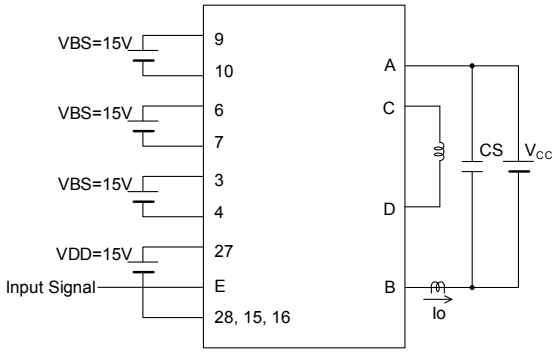
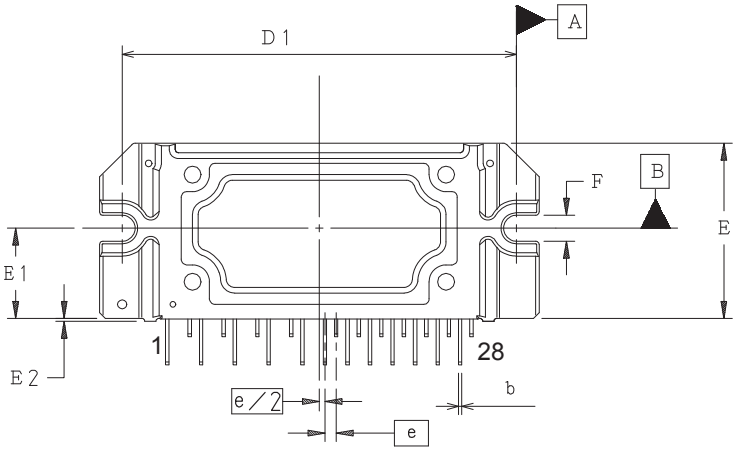


Figure 28. Test circuit for switching time

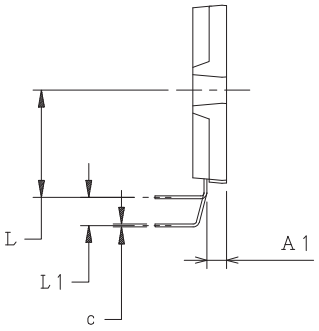
Package Dimensions

unit : mm

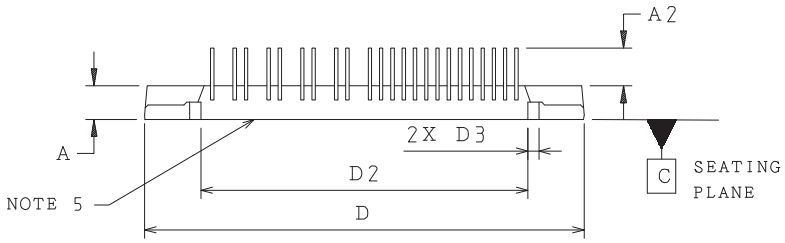
SIP28 78x31.1
CASE 127DG
ISSUE A



TOP VIEW



END VIEW



SIDE VIEW

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	5.50	6.00	6.50
A1	3.00	3.50	4.00
A2		6.70 REF	
b	0.50	0.60	0.80
c	0.40	0.50	0.70
D	77.50	78.00	78.50
D1	69.50	70.00	70.50
D2	57.50	58.00	58.50
D3	1.50	2.00	2.50
E	30.60	31.10	31.60
E1	15.50	16.00	16.50
E2	0.00	0.50	1.00
e		2.00 BSC	
F	4.10	4.60	5.10
L	18.50	19.00	19.50
L1	4.50	5.00	5.50

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND c APPLY TO THE PLATED LEAD AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. PACKAGE IS MISSING PINS: 2, 5, 8, 11, AND 14.
5. BASE MUST BE FLAT WITHIN 0.15 (CONVEX).

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