STL75N3LLZH5

N-channel 30 V, 0.0055 Ω, 19 A PowerFLAT™ (5x6) STripFET™ V Power MOSFET

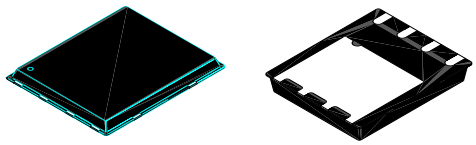
Preliminary data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STL75N3LLZH5	30 V	<0.0061 Ω	19 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses
- Built in G-S Zener diodes



PowerFLAT™ (5x6)

Application

- Switching applications

Description

The STL75N3LLZH5 is an N-channel STripFET™V Power MOSFET which has been designed to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).

Figure 1. Internal schematic diagram

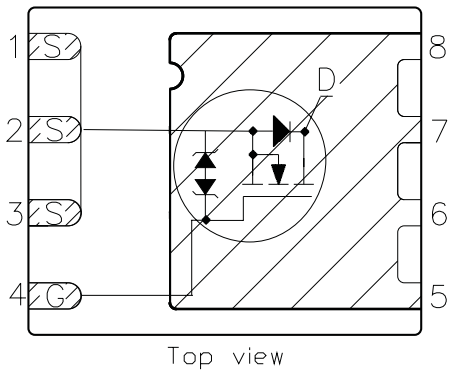


Table 1. Device summary

Order code	Marking	Package	Packaging
STL75N3LLZH5	75N3LLZH5	PowerFLAT™ (5x6)	Tape and reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	± 18	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	75	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	47	A
I_D (2)	Drain current (continuous) at T_C = 25 °C	19	A
I_D (2)	Drain current (continuous) at T_C=100°C	11.8	A
I_{DM} (3)	Drain current (pulsed)	76	A
P_{TOT} (1)	Total dissipation at T_C = 25°C	60	W
P_{TOT} (2)	Total dissipation at T_C = 25°C	4	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj\text{-}c}$.
2. The value is rated according $R_{thj\text{-}pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (Drain) (steady state)	2.08	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} = max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 18 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 9.5 A V_{GS}= 4.5 V, I_D= 9.5 A		0.0055 0.0066	0.0061 0.0078	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1510 287 40	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 19 A V_{GS} =4.5 V *Figure 3*	-	11.8 4 6	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 9.5 A, R_G=4.7 Ω, V_{GS}=10 V *Figure 2*	-	9.2 11 55 20	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}(1)	Source-drain current (pulsed)		-		76	A
V_{SD}(2)	Forward on voltage	I_{SD} = 19 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 19 A, di/dt = 100 A/µs, V_{DD}=25 V, Tj=150 °C	-	24 17 1.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration= 300 µs, duty cycle 1.5%.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

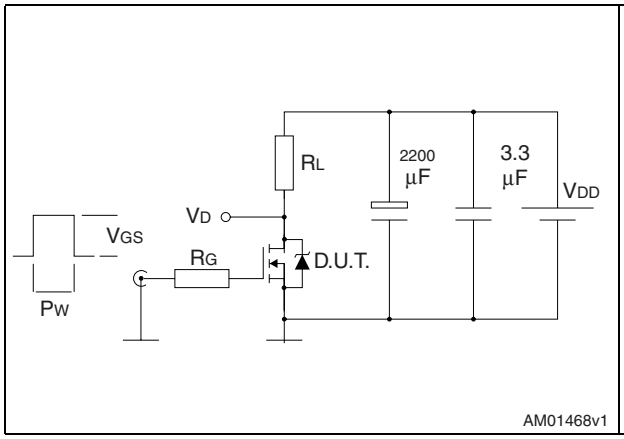


Figure 3. Gate charge test circuit

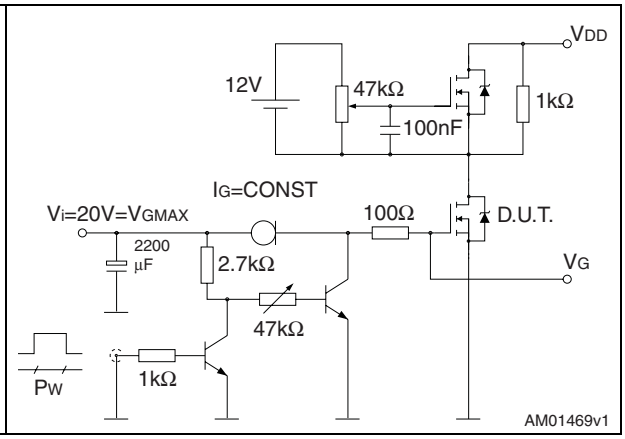


Figure 4. Test circuit for inductive load switching and diode recovery times

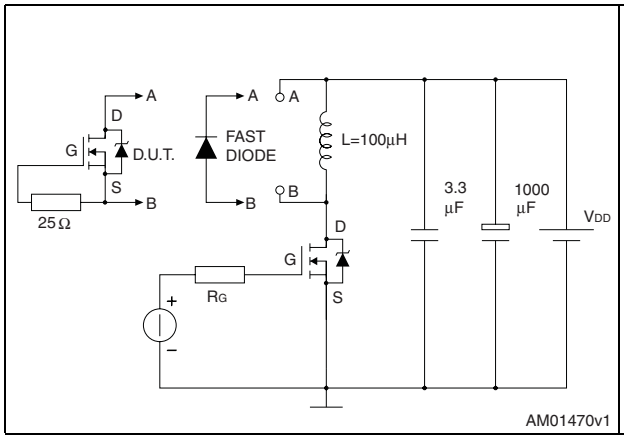


Figure 5. Unclamped inductive load test circuit

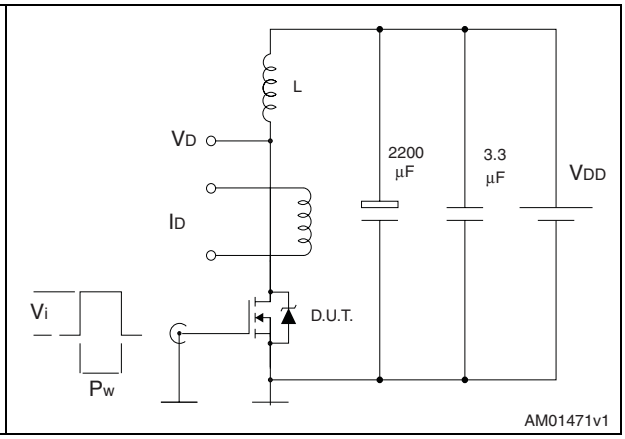


Figure 6. Unclamped inductive waveform

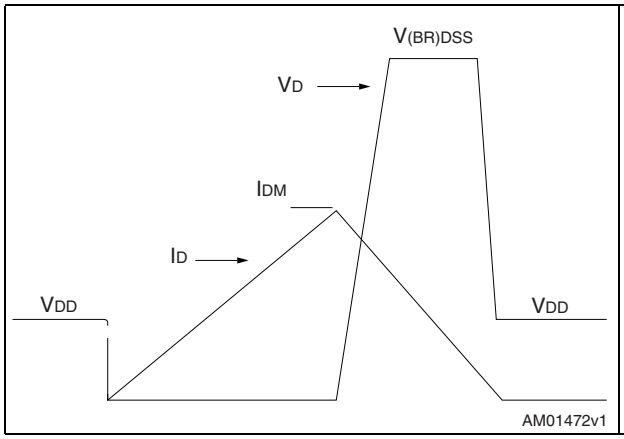
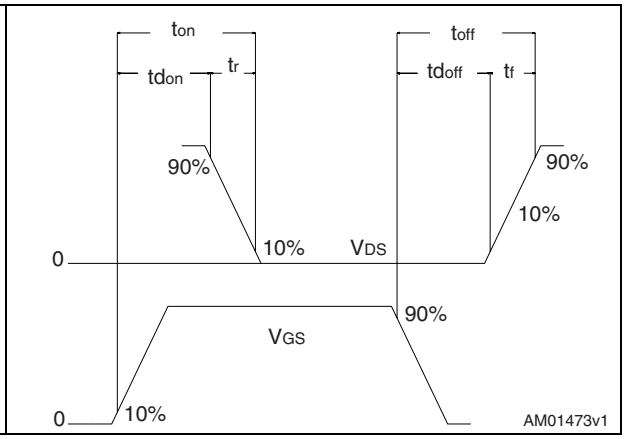


Figure 7. Switching time waveform



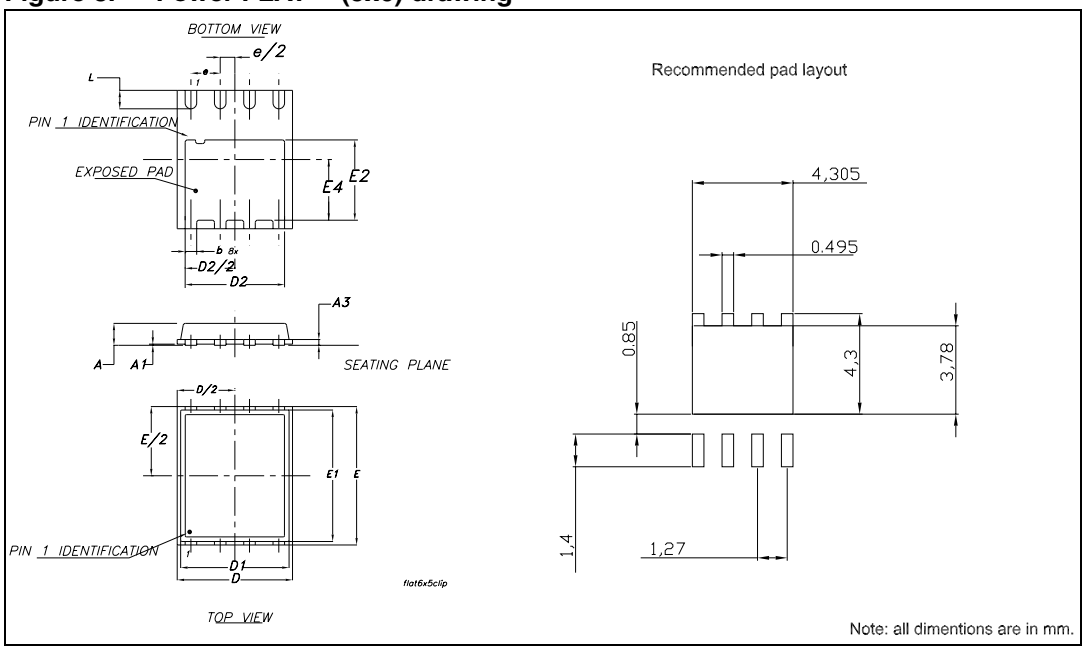
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. Power FLAT™ (5x6) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.83	0.93	0.031	0.32	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035

Figure 8. Power FLAT™ (5x6) drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
22-Jun-2010	1	First release.
08-Jul-2010	2	Modified V_{GS} in *Table 2: Absolute maximum ratings* and *Table 4: On/off states*.

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