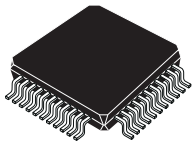
# STLC3055

## WLL & ISDN-TA SUBSCRIBER LINE INTERFACE CIRCUIT

- MONOCHIP SLIC OPTIMISED FOR WLL & ISDN-TA APPLICATIONS
- IMPLEMENT ALL KEY FEATURES OF THE BORSHT FUNCTION
- SINGLE SUPPLY (5.5 TO 15.8V)
- BUILT IN DC/DC CONVERTER CONTROLLER.
- SOFT BATTERY REVERSAL WITH PROGRAMMABLE TRANSITION TIME.
- ON-HOOK TRANSMISSION.
- PROGRAMMABLE OFF-HOOK DETECTOR THRESHOLD
- METERING PULSE GENERATION AND FILTER
- INTEGRATED RINGING
- INTEGRATED RING TRIP
- PARALLEL CONTROL INTERFACE (3.3V LOGIC LEVEL)
- PROGRAMMABLE CONSTANT CURRENT FEED
- SURFACE MOUNT PACKAGE
- INTEGRATED THERMAL PROTECTION
- -40 TO +85°C OPERATING RANGE



**TQFP44**

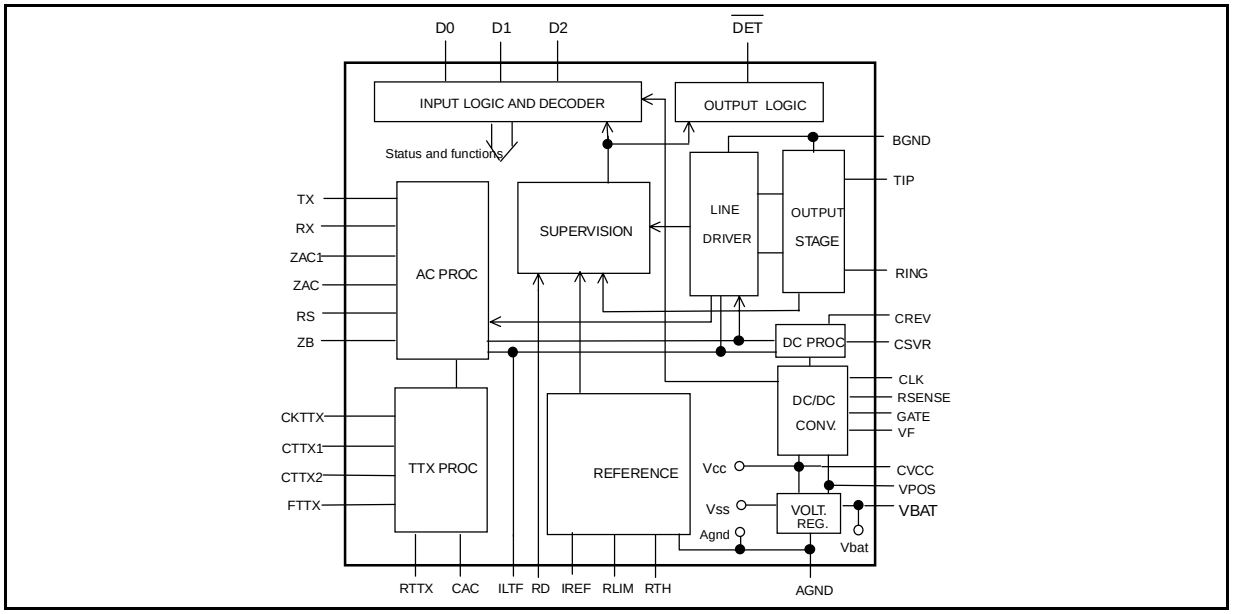
**ORDERING NUMBERS:** STLC3055Q
STLC3055QTR

### DESCRIPTION

The STLC3055 is a SLIC device specifically designed for WLL (Wireless Local Loop) and ISDN-Terminal Adaptors. One of the distinctive characteristic of this device is the ability to operate with a single supply voltage (from +5.5V to +15.8V) and self generate the negative battery by means of an on chip DC/DC converter controller that drives an external MOS switch.

The battery level is properly adjusted depending on the operating mode. A useful characteristic for

### BLOCK DIAGRAM



**DESCRIPTION** (continued)

these applications is the integrated ringing generator.

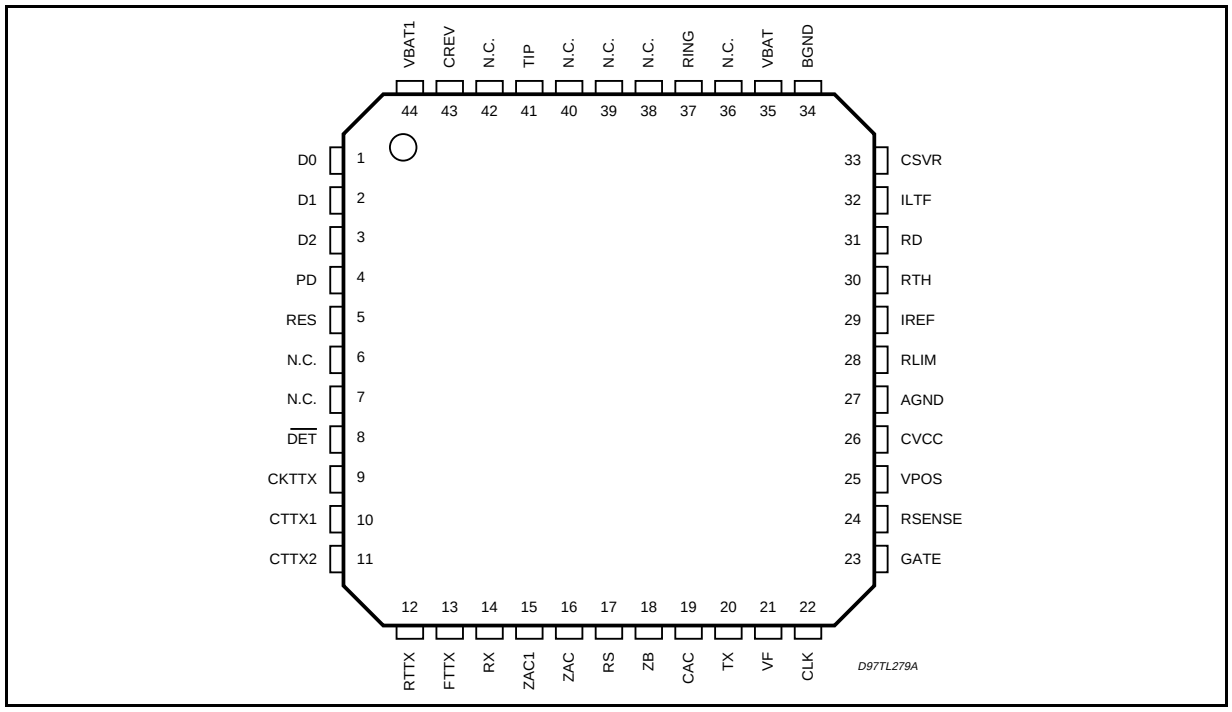
The control interface is a parallel type with open drain output and 3.3V logic levels.

The metering pulses are generated on chip starting from two logic signals (0, 3.3V) one define the metering pulse frequency and the other the metering pulse duration. An on chip circuit then provides the proper shaping and filtering. Metering pulse amplitude and shaping (rising and decay time) can be programmed by external components. A dedicated cancellation circuit avoid possible CODEC input saturation due to Metering pulse echo.

Constant current feed can be set from 20mA to 40mA. Off-hook detection threshold is programmable from 5mA to 9mA.

The device, developed in BCD100II technology (100V process), operates in the extended temperature range and integrates a thermal protection that sets the device in power down when Tj exceeds 140°C.

**PIN CONNECTION**




**ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{pos}$ | Positive Supply Voltage | -0.4 to +17 | V |
| A/BGND | AGND to BGND | -1 to +1 | V |
| $V_{dig}$ | Pin D0, D1, D2, $\overline{DET}$, CKTTX | -0.4 to 5.5 | V |
| $T_j$ | Max. junction Temperature | 150 | °C |
| $V_{btot}$ (1) | Vbtot=\|Vpos\|+\|Vbat\|. (Total voltage applied to the device supply pins). | 100 | V |

(1) Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2. RF1 and RF2 shall be selected in order to fulfil the a.m limits (see External Components Table page 10)

## OPERATING RANGE

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{pos}$ | Positive Supply Voltage | 5.5 to +15.8 | V |
| A/BGND | AGND to BGND | -100 to +100 | V |
| $V_{dig}$ | Pin D0, D1, D2, $\overline{DET}$, CKTTX, PD | -0.25 to 5.25 | V |
| $T_{op}$ | Ambient Operating Temperature Range | -40 to +85 | °C |
| $V_{bat}$ (1) | Self Generated Battery Voltage | -74 max. | V |

(1) Vbat is self generated by the on chip DC/DC converter and can be programmed via RF1 and RF2.
RF1 and RF2 shall be selected in order to fulfil the a.m limits (see External Components Table page 10)

## THERMAL DATA

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal Resistance Junction to Ambient | Typ. | 60 | °C/W |

## PIN DESCRIPTION

| N. | Name | Function |
|---|---|---|
| 25 | VPOS | Positive supply input ranging from 5.5V to 15.8V. |
| 34 | BGND | Battery Ground, must be shorted with AGND. |
| 27 | AGND | Analog Ground, must be shorted with BGND. |
| 16 | ZAC | AC impedance synthesis. |
| 15 | ZAC1 | RX buffer output, the AC impedance is connected from this node to ZAC. |
| 17 | RS | Protection resistors image (the image resistor is connected from this node to ZAC). |
| 18 | ZB | Balance Network for 2 to 4 wire conversion (the balance impedance ZB is connected from this node to AGND. ZA impedance is connected from this node to ZAC1). |
| 20 | TX | 4 wire output port (TX output). The signal is referred to AGND. If connected to single supply CODEC input it must be DC decoupled with proper capacitor. |
| 14 | RX | 4 wire input port (RX input); 300KΩ input impedance. This signal is referred to AGND. If connected to single supply CODEC output it must be DC decoupled with proper capacitor. |
| 19 | CAC | AC feedback input, AC/DC split capacitor (CAC). |
| 32 | ILTF | Transversal line current image output. |
| 41 | TIP | 2 wire port; TIP wire (Ia is the current sourced from this pin). |
| 37 | RING | 2 wire port; RING wire (Ib is the current sunk into this pin). |
| 28 | RLIM | Constant current feed programming pin (via RLIM). RLIM should be connected close to this pin and PCB layout should avoid noise injection on this pin. |
| 30 | RTH | Off-hook threshold programming pin (via RTH). RTH should be connected close to this pin and PCB layout should avoid noise injection on this pin. |
| 29 | IREF | Internal bias current setting pin. RREF should be connected close to this pin and PCB layout should avoid noise injection on this pin. |
| 43 | CREV | Reverse polarity transition time control. One proper capacitor connected between this pin and AGND is setting the reverse polarity transition time. This is the same transition time used to shape the "trapezoidal ringing" during ringing injection. |
| 31 | RD | DC feedback and ring trip input. RD should be connected close to this pin and PCB layout should avoid noise injection on this pin. |

**PIN DESCRIPTION** (continued)

| N. | Name | Function |
|---|---|---|
| 4 | PD | Power Down input. Normally connected to CVCC (or to logic level high). Can be used to set TIP and Ring terminals in open circuit setting PD=0 and D0=D1=0. |
| 26 | CVCC | Internal positive voltage supply filter. |
| 35 | VBAT | Regulated battery voltage self generated by the device via DC/DC converter. Must be shorted to VBAT1. |
| 23 | GATE | Driver for external Power MOS transistor. |
| 21 | VF | Feedback input for DC/DC converter controller. |
| 22 | CLK | Power Switch Controller Clock (typ. 125KHz). From version marked STLC3055 A5, this pin can also be connected to CVCC or AGND. When the CLK pin is connected to CVCC an internal auto-oscillation is internally generated and it is used instead of the external clock. When the CLK pin is connected to AGND, the GATE output is disabled. |
| 24 | RSENSE | Voltage input for current sensing. RSENSE should be connected close to this pin and VPOS pin. The PCB layout should minimize the extra resistance introduced by the copper tracks. |
| 1 | D0 | Control Interface: input bit 0. |
| 2 | D1 | Control Interface: input bit 1. |
| 3 | D2 | Control interface: input bit 2. |
| 8 | $\overline{DET}$ | Logic interface output of the supervision detector (active low). |
| 33 | CSVR | Battery supply filter capacitor. |
| 12 | RTTX | Metering pulse cancellation buffer output. TTX filter network should be connected to this point. If not used should be left open. |
| 13 | FTTX | Metering pulse buffer input this signal is sent to the line and used to perform TTX filtering. |
| 10 | CTTX1 | Metering burst shaping external capacitor. |
| 11 | CTTX2 | Metering burst shaping external capacitor. |
| 9 | CKTTX | Metering pulse clock input (12 KHz or 16KHz square wave). |
| 44 | VBAT1 | Frame connection. Must be shorted to VBAT. |
| 5 | RES | Reserved, must be connected to AGND. |
| 6, 7,36, 38,39, 40,42 | NC | Not connected. |

## FUNCTIONAL DESCRIPTION

The STLC3055 is a device specifically developed for WLL and ISDN-TA applications.

It is based on a SLIC core, on purpose optimised for these applications, with the addition of a DC/DC converter controller to fulfil the WLL and ISDN-TA design requirements.

The SLIC performs the standard feeding, signalling and transmission functions.

It can be set in three different operating modes via the D0, D1, D2 pins of the control logic interface (0 to 3.3V logic levels). The loop status is carried out on the $\overline{DET}$ pin (active low).

The $\overline{DET}$ pin is an open drain output to allow easy interfacing with both 3.3V and 5V logic levels.

The four possible SLIC's operating modes are:

- Power Down
- High Impedance Feeding (HI-Z)
- Active
- Ringing

Table 1 shows how to set the different SLIC operating modes.

**Table 1. SLIC operating modes.**

| PD | D0 | D1 | D2 | Operating Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | X | Power Down |
| 1 | 0 | 0 | X | H.I. Feeding (HI-Z) |
| 1 | 0 | 1 | 0 | Active Normal Polarity |
| 1 | 0 | 1 | 1 | Active Reverse Polarity |
| 1 | 1 | 1 | 0 | Active TTX injection (N.P.) |
| 1 | 1 | 1 | 1 | Active TTX injection (R.P.) |
| 1 | 1 | 0 | 0/1 | Ring (D2 bit toggles @ fring) |

The DC/DC converter controller is driving an external power MOS transistor (P-Channel) in order to generate the negative battery voltage needed for device operation.

The DC/DC converter controller is synchronised with an external CLK (125KHZ typ.).

From version marked STLC3055 A5, it can be synchronised to an internal clock generated when the pin CLK is connected to CVCC. One sensing resistor in series to Vpos supply allows to fix the maximum allowed input peak current. This feature is implemented in order to avoid overload on Vpos supply in case of line transient (ex. ring trip detection).

The typical value is obtained for a sensing resistor equal to 110mΩ that will guarantee an average current consumption from Vpos < 700mA.

When in on-hook the self generated battery voltage is set to a predefined value.

This value can be adjusted via one external resistor (RF1) and it is typical -50V. When RING mode is selected this value is increased to -70V typ.

Once the line goes in off-hook condition, the DC/DC converter automatically adjust the generated battery voltage in order to feed the line with a fixed DC current (programmable via RLIM) optimising in this way the power dissipation.

## OPERATING MODES

### Power Down

DC CHARACTERISTIC & SUPERVISION

When this mode is selected the SLIC is switched off and the TIP and RING pins are in high impedance. Also the line detectors are disabled therefore the off-hook condition cannot be detected.

This mode can be selected in emergency condition when it is necessary to cut any current delivered to the line.

This mode is also forced by STLC3055 in case of thermal overload (Tj > 140°C).

In this case the device goes back to the previous status as soon as the junction temperature decrease under the hysteresis threshold.

AC CHARACTERISTICS

The 2W port is set in high impedance, the TX output buffer is a low impedance output, no AC transmission is possible.

### High Impedance Feeding (HI-Z)

DC CHARACTERISTIC & SUPERVISION

This operating mode is normally selected when the telephone is in on-hook in order to monitor the line status keeping the power consumption at the minimum.

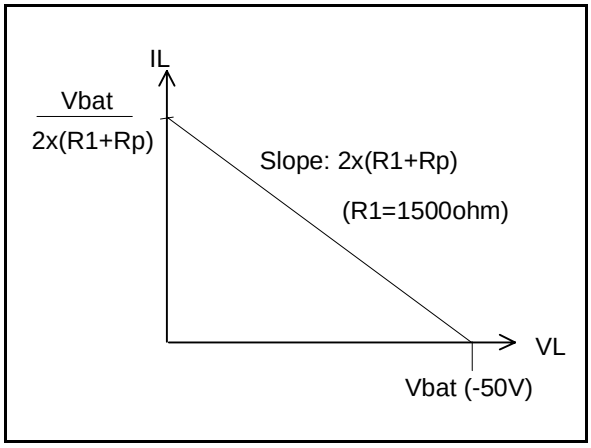
The output voltage in on-hook condition is equal to the self generated battery voltage (-50V typ).

When off-hook occurs the $\overline{DET}$ becomes active (low logic level).

The off-hook threshold in HI-Z mode is the same value as programmed in ACTIVE mode.

The DC characteristic in HI-Z mode is just equal to the self generated battery with 2x(1500W+Rp) in series (see fig.1), where Rp is the external protection resistance.

**Figure 1. DC Characteristic in HI-Z Mode.**




AC CHARACTERISTICS

The AC impedance shown at the 2W port (TIP/RING) is the same as the DC one. The TIP/RING AC impedance will be 2x(1500Ω + Rp) or high impedance.

### Active

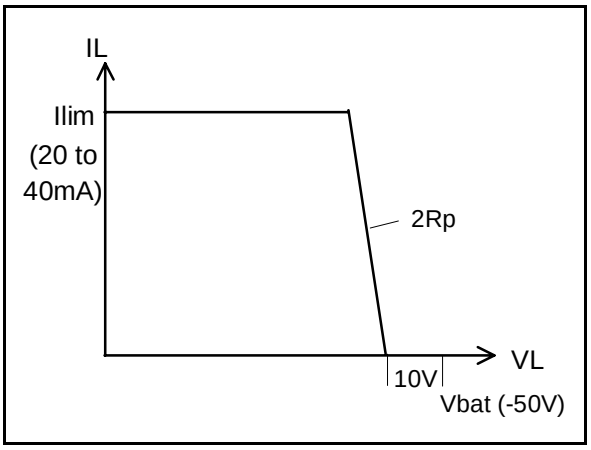
DC CHARACTERISTICS & SUPERVISION

When this mode is selected the STLC3055 provides both DC feeding and AC transmission.

The STLC3055 feeds the line with a constant current fixed by RLIM (20mA to 40mA range). The on-hook voltage is typically 40V allowing on-hook transmission; the self generated Vbat is -50V typ.

If the loop resistance is very high and the line current cannot reach the programmed constant current feed value, the STLC3055 behaves like a 40V voltage source with a series impedance equal to the protection resistors 2xRp (typ. 2x41Ω) plus the internal resistance. Fig. 2 shows the typical DC characteristic in ACTIVE mode.

**Figure 2. DC characteristic in ACTIVE mode**




The line status (on/off hook) is monitored by the SLIC's supervision circuit. The off-hook threshold can be programmed via the external resistor $R_{TH}$ in the range from 5mA to 9mA.

Independently on the programmed constant current value, the TIP and RING buffers have a current source capability limited to 70mA typ.

Moreover the power available at Vbat is controlled by the DC/DC converter that limits the peak current drawn from the Vpos supply. The maximum allowed current peak is set by the $R_{SENSE}$ resistor and it is typically 900mApk.

AC CHARACTERISTICS

The SLIC provides the standard SLIC transmission functions:

- **Input impedance synthesis:** can be real or complex and is set by a scaled (x50) external ZAC impedance.
- **Transmit and receive:** The AC signal present on the 2W port (TIP/RING) is transferred to the TX output with a -6dB gain and from the RX input to the 2W port with a 0dB gain.
- **2 to 4 wire conversion:** The balance impedance can be real or complex, the proper cancellation is obtained by means of two external impedance ZA and ZB.

Once in Active mode (D1=1) the SLIC can operate in different states setting properly D0 and D2 control bits (see also Table 2).

**Table 2. SLIC states in ACTIVE mode**

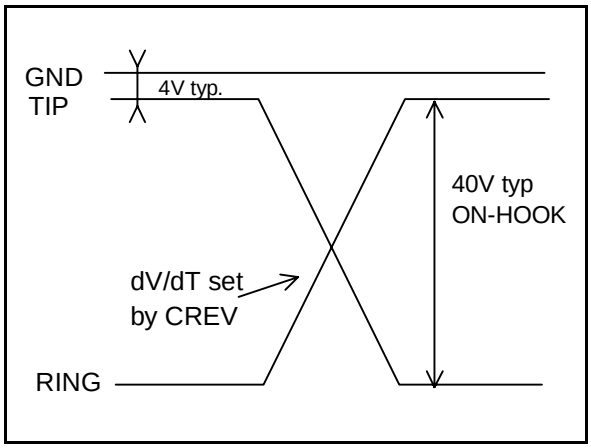
| D0 | D1 | D2 | Operating Mode |
|---|---|---|---|
| 0 | 1 | 0 | Active Normal Polarity |
| 0 | 1 | 1 | Active Reverse Polarity |
| 1 | 1 | 0 | Active TTX injection (N.P.) |
| 1 | 1 | 1 | Active TTX injection (R.P.) |

POLARITY REVERSAL

The D2 bit controls the line polarity, the transition between the two polarities is performed in a "soft" way. This means that the TIP and RING wire exchange their polarities following a ramp transition (see fig.3). The transition time is controlled by an external capacitor CREV. This capacitor is also setting the shape of the ringing trapezoidal waveform.

When the control pins set battery reversal the line polarity is reversed with a proper transition time set via an external capacitor (CREV).

**Figure 3. TIP/RING typical transition from Direct to Reverse Polarity**




METERING PULSE INJECTION (TTX)

The metering pulses circuit consist of a burst shaping generator that gives a square wave shaped and a low pass filter to reduce the harmonic distortion of the output signal.

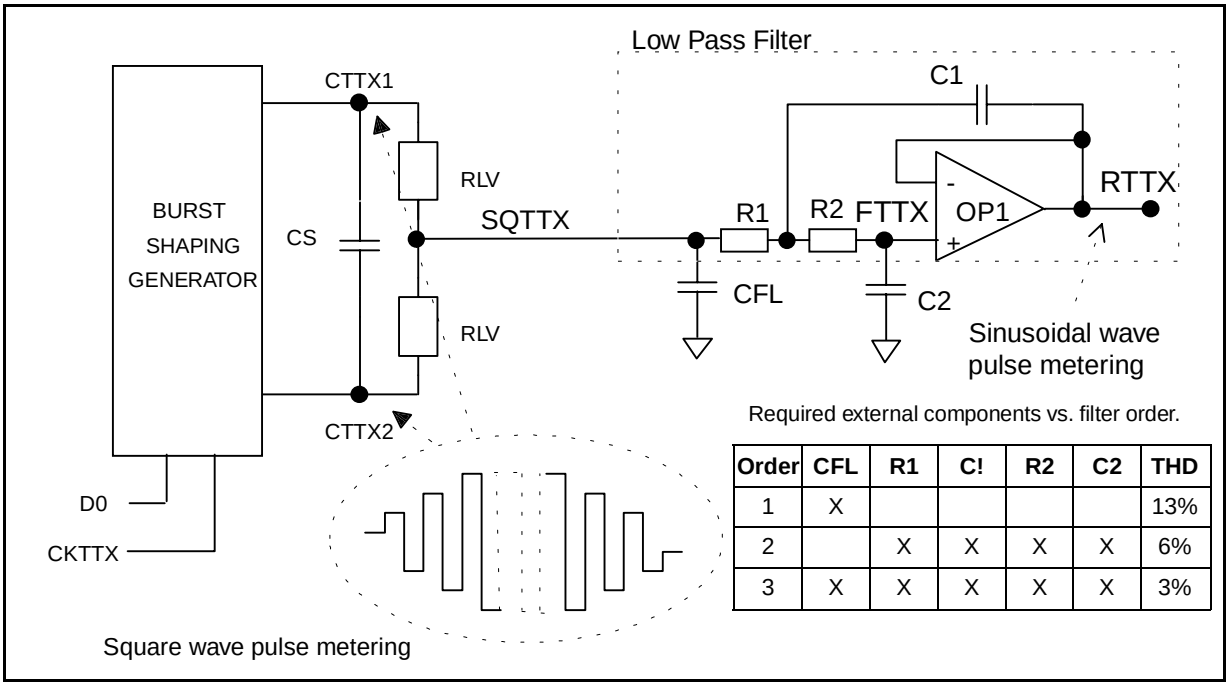
The metering pulse is obtained starting from two logic signals:

- CKTTX: is a square wave at the TTX frequency (12 or 16KHz) and should be permanently applied to the CKTTX pin or at least for all the duration of the TTX pulse (including rising and decay phases).
- D0: enable the TTX generation circuit and define the TTX pulse duration.

This two signals are then processed by a dedicated circuitry integrated on chip that generate the metering pulse as an amplitude modulated shaped squarewave (SQTTX) (see fig.4).

Both the amplitude and the envelope of the squarewave (SQTTX) can be programmed by means of external components. In particular the amplitude is set by the two resistors RLV and the

**Figure 4. Metering pulse generation circuit.**




Required external components vs. filter order.

| Order | CFL | R1 | C! | R2 | C2 | THD |
|---|---|---|---|---|---|---|
| 1 | X | | | | | 13% |
| 2 | | X | X | X | X | 6% |
| 3 | X | X | X | X | X | 3% |

shaping by the capacitor CS.

The waveform so generated is then filtered and injected on the line.

The low pass filter can be obtained using the integrated buffer OP1 connected between pin FTTX (OP1 non inverting input) and RTTX (OP1 output) (see fig.4) and implementing a "Sallen and Key" configuration.

Depending on the external components count it is possible to build an optimised application depending on the distortion level required. In particular harmonic distortion levels equal to 13%, 6% and 3% can be obtained respectively with first, second and third order filters (see fig.4).

The circuit showed in the "Application diagram" is related to the simple first order filter.

Once the shaped and filtered signal is obtained at RTTX buffer output it is injected on the TIP/RING pins with a +6dB gain.

It should be noted that this is the nominal condition obtained in presence of ideal TTX echo cancellation (obtained via proper setting of RTTX and CTTX). In addition the effective level obtained on the line will depend on the line impedance, the protection resistor value and the series switch (SW1 or SW2) on resistance.

In the typical application (TTX line impedance =200Ω , RP = 41Ω, SW1,2 on resistance = 9Ω and ideal TTX echo cancellation) the metering pulse level on the line will be 1.33 times the level applied to the RTTX pin.

As already mentioned the metering pulse echo cancellation is obtained by means of two external components (RTTX and CTTX) that should match the line impedance at the TTX frequency. This simple network has a double effect:

- Synthesise a low output impedance at the TIP/RING pins at the TTX frequency.
- Cut the eventual TTX echo that will be transferred from the line to the TX output.

### Ringing

When this mode is selected STLC3055 self generate an higher negative battery (-70V typ.) in order to allow a balanced ringing signal of typically 65Vpeak.

In this condition both the DC and AC feedback loop are disabled and the SLIC line drivers operate as voltage buffers.

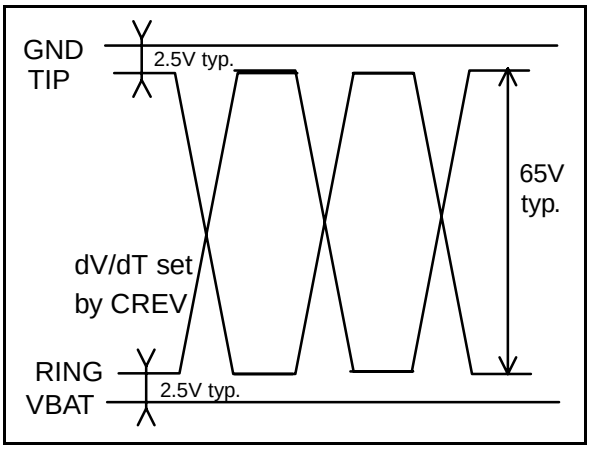
The ring waveform is obtained toggling the D2 control bit at the desired ring frequency. This bit in fact controls the line polarity (0=direct; 1=reverse). As in the ACTIVE mode the line voltage transition is performed with a ramp transition, obtaining in this way a trapezoidal balanced ring waveform (see fig.5).

The shaping is defined by the CREV external capacitor.

Selecting the proper capacitor value it is possible to get different crest factor values.

The following table shows the crest factor values

**Figure 5. TIP/RING typical ringing waveform**




obtained with a 20Hz and 25Hz ring frequency and with 1REN. This value are valid either with European or USA specification:

| CREV | CREST FACTOR @20Hz | CREST FACTOR @25Hz |
|---|---|---|
| 22nF | 1.2 | 1.26 |
| 27nF | 1.25 | 1.32 |
| 33nF | 1.33 | Not significant (*) |

(*) Distorsion already less than 10%.

The ring trip detection is performed sensing the variation of the AC line impedance from on hook (relatively high) to off-hook (low). This particular ring trip method allows to operate without DC offset superimposed on the ring signal and therefore obtaining the maximum possible ring level on the load starting from a given negative battery.

It should be noted that such a method is optimised for operation on short loop applications and may not operate properly in presence of long loop applications (> 500Ω ).

Once ring trip is detected, the $\overline{DET}$ output is activated (logic level low), at this point the card controller or a simple logic circuit should stop the D2 toggling in order to effectively disconnect the ring signal and then set the STLC3055 in the proper operating mode (normally ACTIVE).

RING LEVEL IN PRESENCE OF MORE TELEPHONE IN PARALLEL

As already mentioned above the maximum current that can be drawn from the Vpos supply is controlled and limited via the external RSENSE.

This will limit also the power available at the self generated negative battery.

If for any reason the ringer load will be too high the self generated battery will drop in order to keep the power consumption to the fixed limit and therefore also the ring voltage level will be reduced.

In the typical application with $R_{SENSE}$ = 110mΩ the peak current from Vpos is limited to about 900mA, which correspond to an average current of 700mA max. In this condition the STLC3055 can drive up to 3REN with a ring frequency fr=25Hz (1REN = 1800Ω + 1.0µF, European standard).

In order to drive up to 5REN (1REN= 6930Ω + 8µF, US standard) it is necessary to modify the external components as follows:

CREV = 15nF

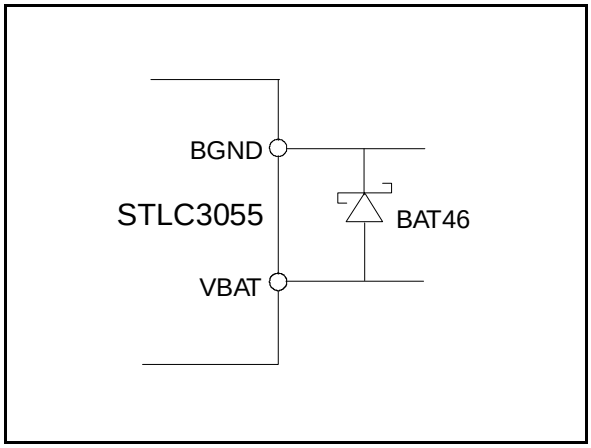
RD = 2.2KΩ

**Power On Requirements**

In order to avoid damage to the device when Vpos is first applied it is recommended to keep all the logic inputs to a low logic level (0V) until Vpos is >5.5V.

In case this power up sequence cannot be guaranteed it's recommended to connect a shottky diode (BAT46 or equivalent) between VBAT and BGND see figure below.

**Figure 6. Shottky diode connection**



### Layout Recommendation

A properly designed PCB layout is a basic issue to guarantee a correct behaviour and good noise performances.

Particular care must be taken on the ground connection and in this case the star configuration allows surely to avoid possible problems (see Application Diagram Fig. 7).

The ground of the power supply (VPOS) has to be connected to the center of the star, let's call this point PGND. This point should show a resistance as low as possible, that means it should be a ground plane.

Noise sources can be identified in not enough good grounds, not enough low impedance supplies and parasitic coupling between PCB tracks and high impedance pins of the device.

In particular to avoid noise problems the layout should prevent any coupling between the DC/DC converter components and analog pins that are referred to AGND (ex: RD, IREF, RTH, RLIM, VF). As a first reccomendation the components CV, L, D1, CVPOS, RSENSE should be kept as close as possible to each other and isolated from the other components.

Additional improvements can be obtained:

- decoupling the center of the star from the analog ground of STLC3055 using small chokes.
- adding a capacitor in the range of 100nF between VPOS and AGND in order to filter the switch frequency on VPOS.

### External Components List

In order to properly define the external components value the following system parameters have to be defined:

- The AC input impedance shown by the SLIC at the line terminals "Zs" to which the return loss measurement is referred. It can be real (typ. 600Ω) or complex.
- The AC balance impedance, it is the equivalent impedance of the line "Zl" used for evaluation of the trans-hybrid loss performances (2/4 wire conversion). It is usually a complex impedance.
- The value of the two protection resistors Rp in series with the line termination.
- The line impedance at the TTX frequency "Zlttx".
- The metering pulse level amplitude measured at line termination "$V_{LOTTX}$". In case of low order filtering, $V_{LOTTX}$ represents the amplitude (Vrms) of the fundamental frequency component. (typ 12 or 16KHz).
- Pulse metering envelope rise and decay time constant "$\tau$".
- The slope of the ringing waveform "$\Delta V_{TR}/\Delta_T$ ".
- The value of the constant current limit current "Ilim".
- The value of the off-hook current threshold "$I_{TH}$".
- The value of the ring trip rectified average threshold current "$I_{RTH}$".
- The value of the required self generated negative battery "$V_{BATR}$" in ring mode (max value is 70V). This value can be obtained from the desired ring peak level + 5V.
- The value of the maximum current peak sunk from Vpos "IPK".

## EXTERNAL COMPONENTS

| Name | Function | Formula | Typ. Value |
|---|---|---|---|
| RREF | Bias setting current | RREF = 1.3/Ibias<br>Ibias = 50µA | 26kΩ 1% |
| CSVR | Negative Battery Filter | CSVR = 1/(2π · fp · 1.8MΩ)<br>fp = 50Hz | 1.5nF 10%<br>100VL |
| RD | Ring Trip threshold setting resistor | RD = 100/$I_{RTH}$<br>2KΩ < RD < 5KΩ | 4.12kΩ 1%<br>@ IRTH = 24mA |
| CAC | AC/DC split capacitance | | 22µF 20% 15VL<br>@ RD = 4.12kΩ |
| RP | Line protection resistor | Rp > 30Ω | 41Ω 1% |
| RS | Protection and series switches resistance image | RS = 100 · (Rp + 9Ω) | 5kΩ @ Rp = 41Ω |
| ZAC | Two wire AC impedance | ZAC = 50 · (Zs - 2Rp - 18Ω) | 25kΩ 1%<br>@ Zs = 600Ω |
| ZA (1) | SLIC impedance balancing network | ZA = 50 · Zs | 30kΩ 1%<br>@ Zs = 600Ω |
| ZB (1) | Line impedance balancing network | ZB = 50 · Zl | 30kΩ 1%<br>@ Zl = 600Ω |
| CCOMP | AC feedback loop compensation | CCOMP = 1/(2π·fo·100·(RP+9Ω))<br>fo = 250kHz | 120pF 10% 10VL<br>@ Rp = 41Ω |
| CH | Trans-Hybrid Loss frequency compensation | CH = CCOMP | 120pF 10% 10VL |
| RLIM | Current limiting programming | RLIM = 1300/Ilim<br>32.5kΩ < RLIM < 65kΩ | 52.3kΩ 1%<br>@ Ilim = 25mA |
| RTH | Off-hook threshold programming (ACTIVE mode) | RTH = 260/$I_{TH}$<br>27kΩ < RTH < 52kΩ | 28.7kΩ 1%<br>@$I_{TH}$ = 9mA |
| CREV | Reverse polarity transition time programming | CREV = (1/3750) · $\Delta T/\Delta V_{TR}$) | 22nF 10% 10V<br>@ 12V/ms |
| RTTX (3) | Pulse metering cancellation resistor | RTTX = 50Re[(Zlttx+2Rp+18Ω)] | 15kΩ<br>@Zlttx = 200Ω real |
| CTTX (3) | Pulse metering cancellation capacitor | CTTX = 1/{50·2π·fttx[-Im(Zlttx)]} | 100nF 10% 10V (2)<br>@ Zlttx = 200Ω real |
| RLV | Pulse metering level resistor | RLV = 63.3·$10^3$·α·$V_{LOTTX}$<br>α = (\|Zlttx + 2Rp + 18Ω\|/\|Zlttx\|) | 27kΩ 1%<br>@ $V_{LOTTX}$ = 275mVrms |
| CS | Pulse metering shaping capacitor | CS = τ/(2·RLV) | 100nF 10% 10V<br>@ τ = 6ms, RLV = 27.1kΩ |
| CFL | Pulse metering filter capacitor | CFL = 2/(2π·fttx·RLV) | 1nF 10% 10V<br>@fttx = 12kHz<br>RLV = 27kΩ |
| RDD | Pull up resistors | | 100kΩ |
| CVCC | Internally supply filter capacitor | | 100nF 20% 10V |
| CVpos | Positive supply filter capacitor with low impedance for switch mode power supply | | 100µF(4) |
| CV | Battery supply filter capacitor with low impedance for switch mode power supply | | 100µF 20% 100V (5) |
| CVB | High frequency noise filter | | 470nF 20% 100VL |

**EXTERNAL COMPONENTS** (continued)

| Name | Function | Formula | Typ. Value |
|---|---|---|---|
| CRD (6) | High frequency noise filter | | 100nF 10% 15VL |
| Q1 | DC/DC converter switch P ch. MOS transistor | RDS(ON)≤1.2Ω,VDS = -100V Total gate charge=20nC max. with VGS=4.5V and VDS=1V ID>500mA | Possible choiches: IRF9510 or IRF9520 or IRF9120 or equivalent |
| D1 | DC/DC converter series diode | Vr > 100V, $t_{RR} \leq 50ns$ | SMBYW01-200 or equivalent |
| RSENSE | DC/DC converter peak current limiting | RSENSE = 100mV/$I_{PK}$ | 110mΩ @$I_{PK}$ = 900mA |
| L (8) | DC/DC converter inductor | DC Resistance ≤ 0.1Ω (9) | L=125µH RFP1304PV (Manuf.: All Inductive) or SUMIDA CDRH125 or equivalent |
| CF1 | DC/DC converter feedback loop stability | | 220pF to 470pF (10) |
| RF1 | Negative battery programming level | 250KΩ<RF1<300KΩ (7) | 300kW 1% @ $V_{BATR}$ = -70V |
| RF2 | Negative battery programming level | | 9.1kΩ 1% |

(1) In case Zs=Zl, ZA and ZB can be replaced by two resistors of same value: RA=RB=|Zs|.
(2) In this case CTTX is just operating as a DC decoupling capacitor (fp=100Hz).
(3) Defining ZTTX as the impedance of RTTX in series with CTTX, RTTX and CTTX can also be calculated from the following formula: ZTTX=50*(Zlttx+2Rp+18Ω).
(4) CVpos should be defined depending on the power supply current capability and maximum allowable ripple.
(5) For low ripple application use 2x47µF in parallel.
(6) Can be saved if proper PCB layout avoid noise coupling on RD pin (high impedance input).
(7) RF1 sets the self generated battery voltage in RING and ACTIVE(Il=0) mode as follows:

| | 267kΩ | 280kΩ | 294kW | 300kΩ |
|---|---|---|---|---|
| $V_{BAT(ACTIVE)}$ | -46V | -48V | -49V | -50V |
| $V_{BATR(RING)}$ | -62V | -65V | -68V | -70V |

VBATR should be defined considering the ring peak level required (Vringpeak=VBATR-6V typ.).
The above relation is valid provided that the Vpos power supply current capability and the RSENSE programming allow to source all the current requested by the particular ringer load configuration.
(8) Core: MICROMETALS T50-26C IRON POWDER, AL-VALUE 61nH/N2
Current rating: 2A (50/60Hz)
Operating Temperature -25° to +60° Centigrades
Inductance: 14µH +/-15% at 1KHz, 1mA
DC resistance of winding: MAX.100 mOhm
Code: RFY1303
Wire: UEW2, 0,60 mm
Turns: 50
Inductance (f=1KHz): >125µH
(9) For high efficiency in HI-Z mode coil resistance @125kHz must be <3ohm
(10) Function of this capacitor is to introduce a zero at the resonance frequency for loop stability. In case some parasitic resistance are already present in the loop (Coil, CVBAT, PCB layout), the presence of this capacitor can degrade the device noise performances; in this case CF1 should be removed being the loop stability already guaranteed by the parasitic resistance.

**Figure 6. Application Diagram.**

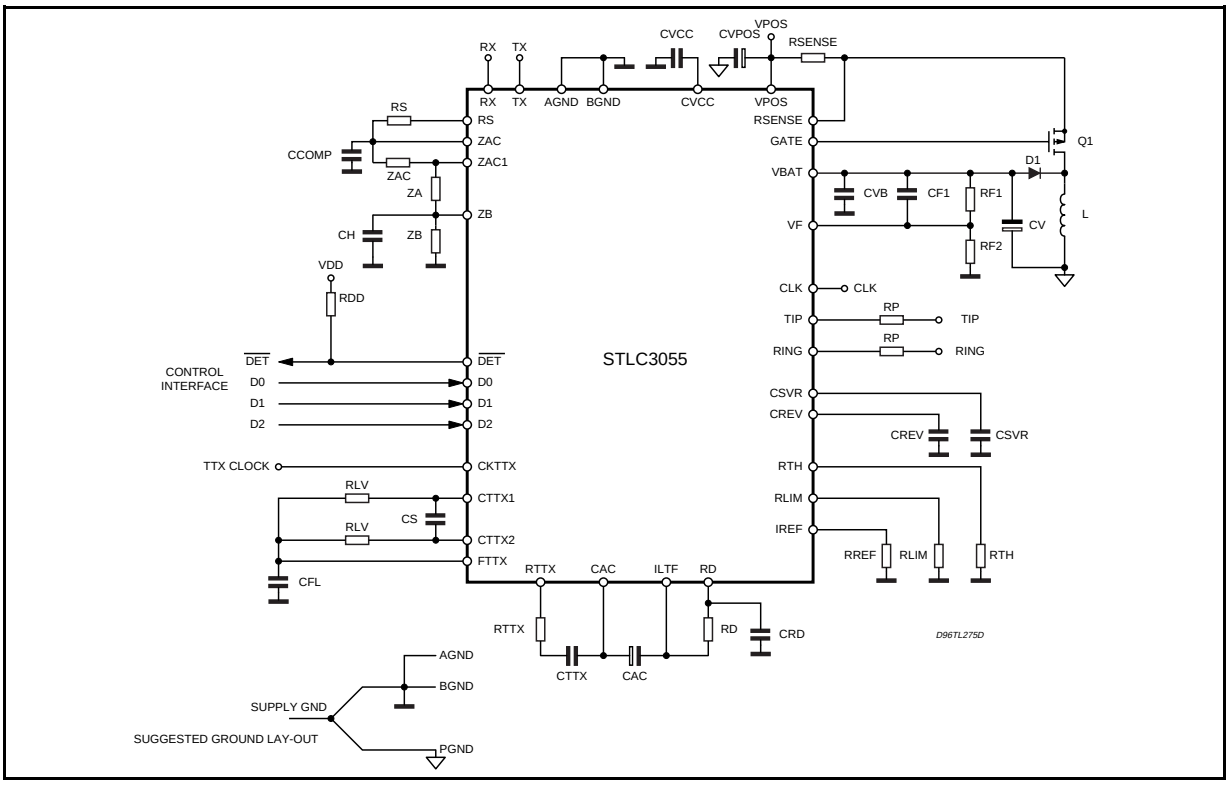
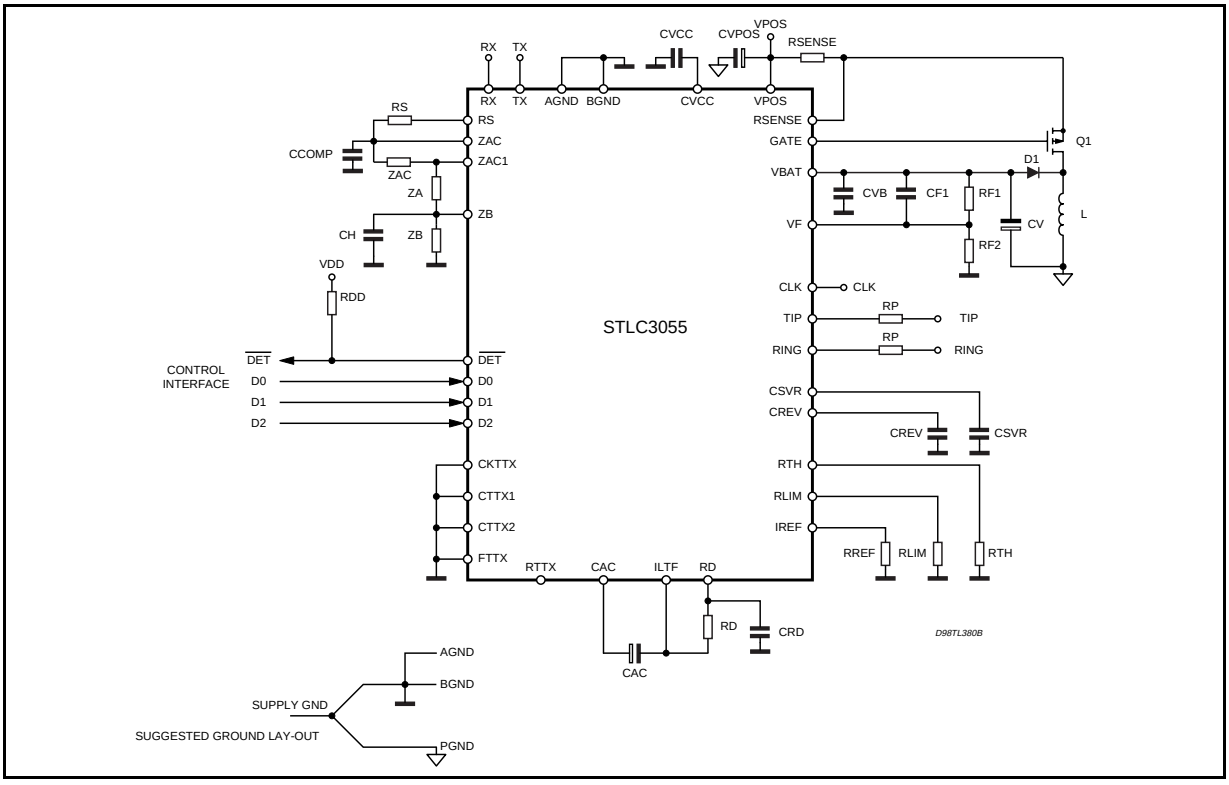



**Figure 7. Application Diagram without Metering Pulse Generation.**



## ELECTRICAL CHARACTERISTICS

Test conditions: $V_{pos}$ = 6.0V, AGND = BGND, Normal Polarity, $T_{amb}$ = 25°C.

External components as listed in the "Typical Values" column of EXTERNAL COMPONENTS Table.

Note: Testing of all parameter is performed at 25°C. Characterisation as well as design rules used allow correlation of tested performances at other temperatures. All parameters listed here are met in the operating range: -40 to +85°C.

| **DC CHARACTERISTICS** | | | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Condition** | **Min.** | **Typ.** | **Max.** | **Unit** |
| $V_{lohi}$ | Line voltage | Il = 0, HI-Z<br>(High impedance feeding)<br>$T_{amb}$ = 0 to 85°C | 44 | 50 | | V |
| $V_{lohi}$ | Line voltage | Il = 0, HI-Z<br>(High impedance feeding)<br>$T_{amb}$ = -40 to 85°C | 42 | 48 | | V |
| $V_{loa}$ | Line voltage | Il = 0, ACTIVE<br>$T_{amb}$ = 0 to 85°C | 33 | 40 | | V |
| $V_{loa}$ | Line voltage | Il = 0, ACTIVE<br>$T_{amb}$ = -40 to 85°C | 31 | 37 | | V |
| Ilim | Lim. current programming range | ACTIVE mode | 20 | | 40 | mA |
| Ilima | Lim. current accuracy | ACTIVE mode.<br>Rel. to programmed value<br>20mA to 40mA | -10 | | 10 | mA |
| Rfeed HI | Feeding resistance | HI-Z (High Impedance feeding) | 2.4 | | 3.6 | kΩ |
| Zrx | RX port input impedance | | 280 | | | kΩ |
| **AC CHARACTERISTICS** | | | | | | |
| L/T | Long. to transv.<br>(see Appendix for test circuit) | Rp = 41Ω, 1% tol.,<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>f = 300 to 3400Hz | 48 | 50 | | dB |
| T/L | Transv. to long.<br>(see Appendix for test circuit) | Rp = 41Ω, 1% tol.,<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>f = 300 to 3400Hz | 40 | 45 | | dB |
| T/L | Transv. to long.<br>(see Appendix for test circuit) | Rp = 41Ω, 1% tol.,<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>f = 1kHz | 48 | 53 | | dB |
| 2WRL | 2W return loss | 300 to 3400Hz,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | 22 | 26 | | dB |
| THL | Trans-hybrid loss | 300 to 3400Hz,<br>20Log\|VRX/VTX\|,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | 30 | | | dB |
| Ovl | 2W overload level | at line terminals on ref. imped.<br>ACTIVE N. P., $R_L$ = 600Ω (*) | 10 | | | dBm |
| TXoff | TX output offset | ACTIVE N. P., $R_L$ = 600Ω (*) | -150 | | 150 | mV |
| G24 | Transmit gain abs. | 0dBm @ 1020Hz,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | -6.4 | | -5.6 | dB |
| G42 | Receive gain abs. | 0dBm @ 1020Hz,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | -0.4 | | 0.4 | dB |
| G24f | TX gain variation vs. freq. | rel. 1020Hz; 0dBm,<br>300 to 3400Hz,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | -0.12 | | 0.12 | dB |

## ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| G42f | RX gain variation vs. freq. | rel. 1020Hz; 0dBm,<br>300 to 3400Hz,<br>ACTIVE N. P., $R_L$ = 600Ω (*) | -0.12 | | 0.12 | dB |
| V2Wp | Idle channel noise at line | psophometric filtered<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>$T_{amb}$ = 0 to +85°C | | -73 | -68 | dBmp |
| V2Wp | Idle channel noise at line | psophometric filtered<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>$T_{amb}$ = -40 to +85°C | | -68 | | dBmp |
| V4Wp | Idle channel noise at line | psophometric filtered<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>$T_{amb}$ = 0 to +85°C | | -75 | -70 | dBmp |
| V4Wp | Idle channel noise at line | psophometric filtered<br>ACTIVE N. P., $R_L$ = 600Ω (*)<br>$T_{amb}$ = -40 to +85°C | | -75 | | dBmp |
| Thd | Total Harmonic Distortion | ACTIVE N. P., $R_L$ = 600Ω (*) | | | -46 | dB |
| VTTX | Metering pulse level on line | ACTIVE - TTX<br>Zl = 200Ω fttx = 12kHz | 200 | 250 | | mVrms |
| CLKfreq | CLK operating range | | -10% | 125 | 10% | kHz |

(*) $R_L$: Line Resistance

| | | | | | | |
|---|---|---|---|---|---|---|
| **RING** | | | | | | |
| Vring | Line voltage | RING D2 toggling @ fr = 25Hz<br>Load = 3REN;<br>Crest Factor = 1.25<br>1REN = 1800Ω + 1.0µF<br>$T_{amb}$ = 0 to +85°C | 45 | 49 | | Vrms |
| Vring | Line voltage | RING D2 toggling @ fr = 25Hz<br>Load = 3REN;<br>Crest Factor = 1.25<br>1REN = 1800Ω + 1.0µF<br>$T_{amb}$ = -40 to +85°C | 44 | 48 | | Vrms |
| **DETECTORS** | | | | | | |
| IOFFTHA | Off/hook current threshold | ACT. mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | 10.5 | | | mA |
| ROFTHA | Off/hook loop resistance threshold | ACT. mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | | | 3.4 | kΩ |
| IONTHA | On/hook current threshold | ACT. mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | | | 6 | mA |
| RONTHA | On/hook loop resistance threshold | ACT. mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | 8 | | | kΩ |
| IOFFTHI | Off/hook current threshold | Hi Z mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | 10.5 | | | mA |
| ROFFTHI | Off/hook loop resistance threshold | Hi Z mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | | | 800 | Ω |
| IONTHI | On/hook current threshold | Hi Z mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | | | 6 | mA |
| RONTHI | On/hook loop resistance threshold | Hi Z mode, RTH = 28.7kΩ 1%<br>(Prog. ITH = 9mA) | 8 | | | kΩ |

**ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Irt | Ring Trip detector threshold range | RING | 20 | | 50 | mA |
| Irta | Ring Trip detector threshold accuracy | RING | -15 | | 15 | % |
| Trtd | Ring trip detection time | RING | | TBD | | ms |
| Td | Dialling distortion | ACTIVE | -1 | | 1 | ms |
| Rlrt (1) | Loop resistance | | | | 500 | Ω |
| ThAl | Tj for th. alarm activation | | | 160 | | °C |

(1) Rlrt = Maximum loop resistance (incl. telephone) for correct ring trip detection.

| | | | | | | |
|---|---|---|---|---|---|---|
| **DIGITAL INTERFACE**<br>INPUTS: D0, D1, D2, PD, CLK<br>OUTPUTS: DET | | | | | | |
| Vih | In put high voltage | | 2 | | | V |
| Vil | Input low voltage | | | | 0.8 | V |
| Iih | Input high current | | -10 | | 10 | µA |
| Iil | Input low current | | -10 | | 10 | µA |
| Vol | Output low voltage | Iol = 1mA | | | 0.45 | V |
| **PSRR AND POWER CONSUMPTION** | | | | | | |
| PSERRC | Power supply rejection Vpos to 2W port | Vripple = 100mVrms<br>50 to 4000Hz | 26 | 36 | | dB |
| Ivpos | Vpos supply current @ ii = 0 | HI-Z On-Hook<br>ACTIVE On-Hook,<br>RING (line open) | | 52<br>93<br>120 | 60<br>115<br>140 | mA<br>mA<br>mA |
| Ipk | Peak current limiting accuracy | RING Off-Hook<br>RSENSE = 110mΩ | -20% | 950 | +20% | mApk |

# APPENDIX A

## STLC3055 Test Circuits

Referring to the application diagram shown in fig. 7 of the STLC3055 datasheet and using as external components the Typ. Values specified in the "External Components" Table (page 13) find below the proper configuration for each measurement.

All measurements requiring DC current termination should be performed using "Wandel & Goltermann DC Loop Holding Circuit GH-1" or equivalent.

**Figure A1. 2W Return Loss**
***2WRL = 20Log(|Zref + Zs|/|Zref-Zs|) = 20Log(E/2Vs)***

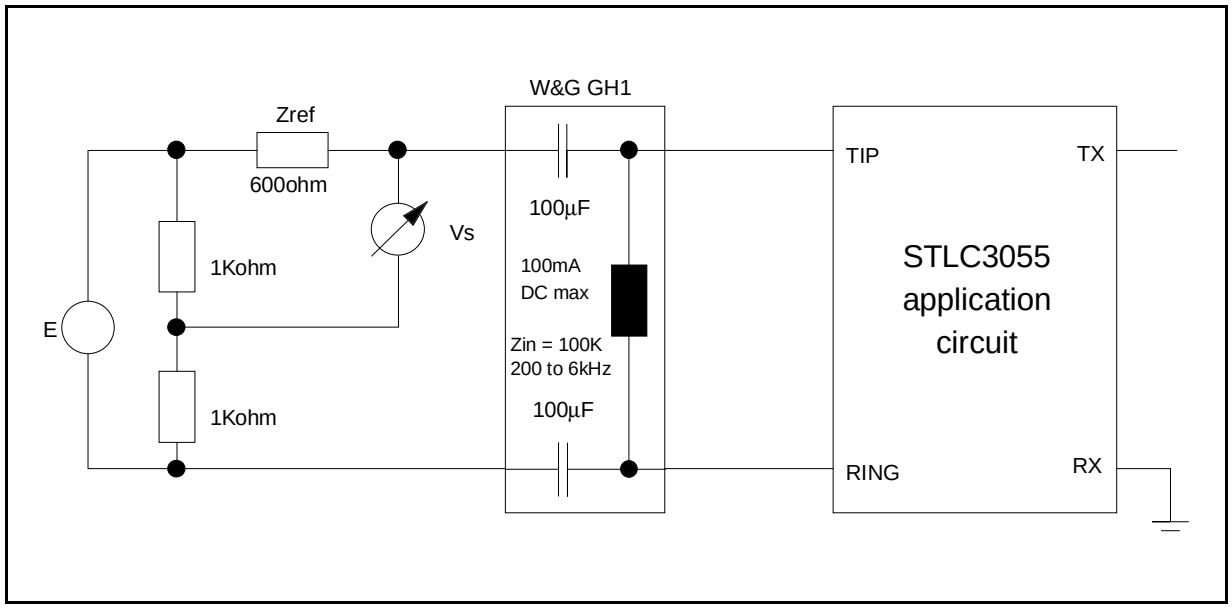



**Figure A2. THL Trans Hybrid Loss**
***THL = 20Log|Vrx/Vtx|***

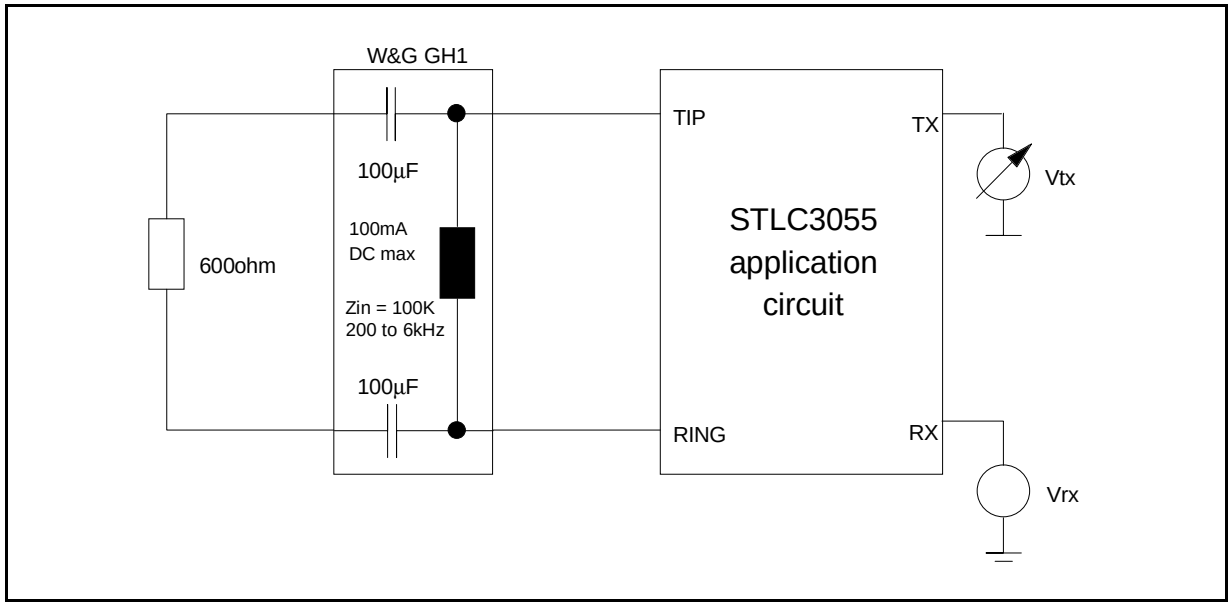


**Figure A3. G24 Transmit Gain**
***G24 = 20Log\|2Vtx/E\|***

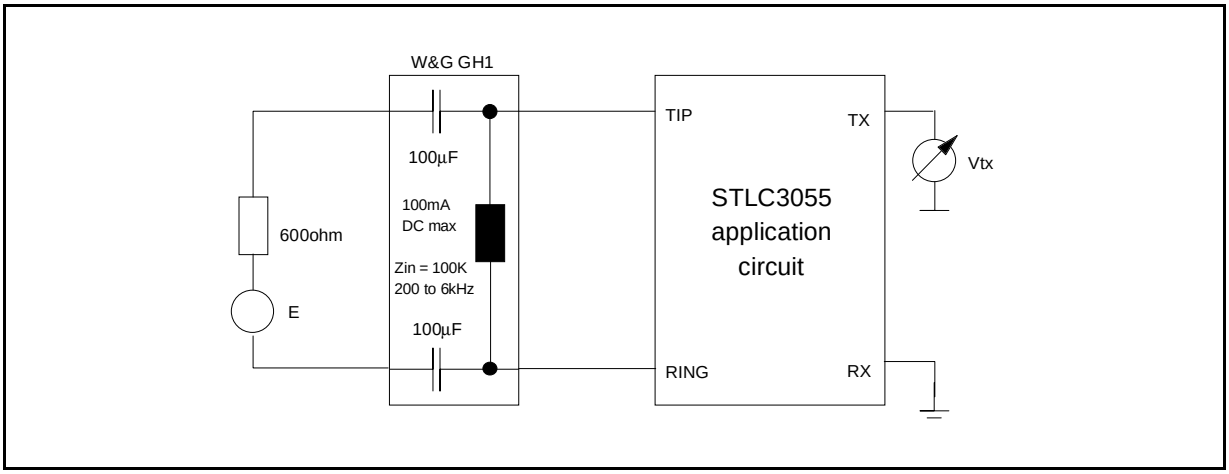



**Figure A4. G42 Receive Gain**
***G42 = 20Log\|Vl/Vrx\|***

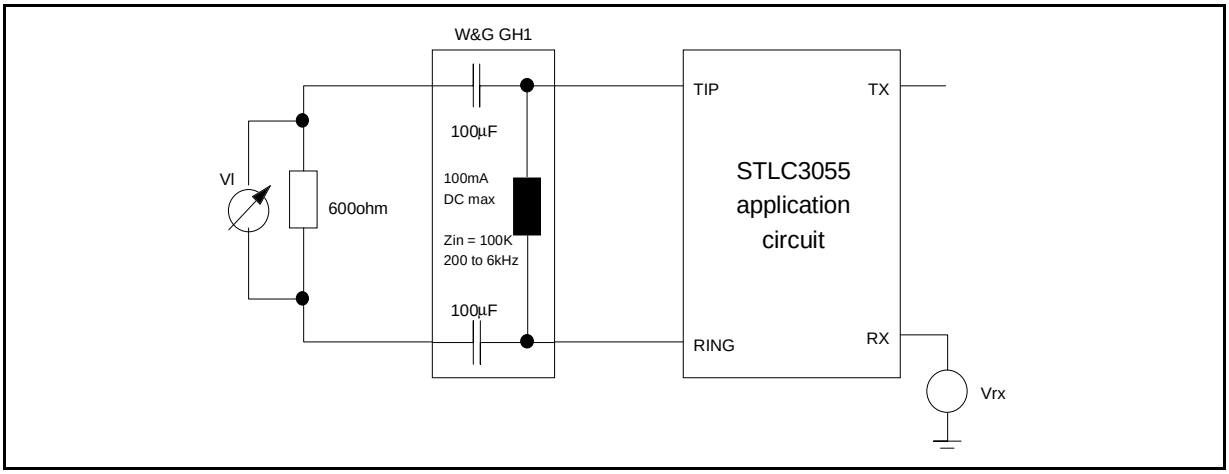



**Figure A5. PSRRC Power supply rejection Vpos to 2W port**
***PSSRC = 20Log\|Vn/Vl\|***

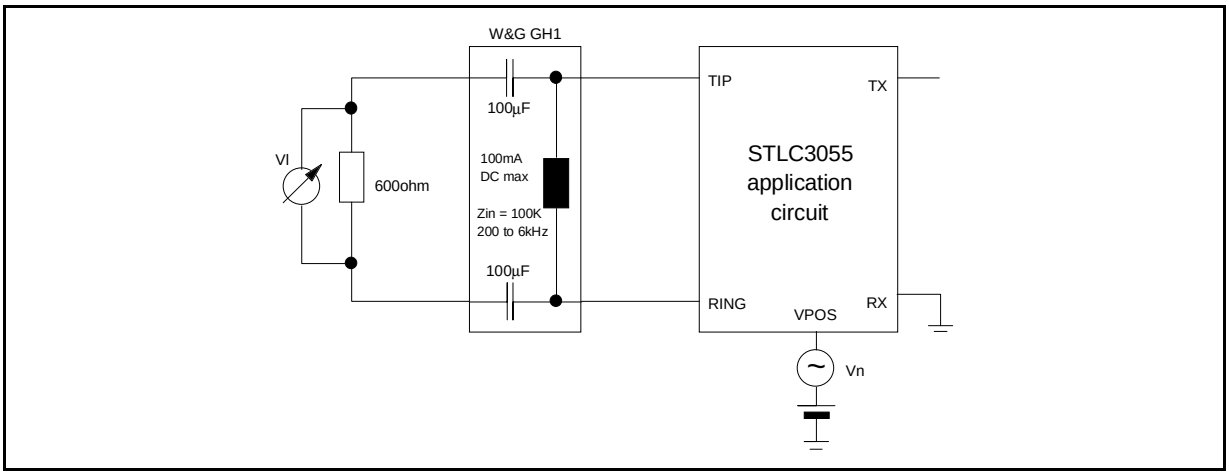


**Figure A6. L/T Longitudinal to Transversal Conversion**
***L/T = 20Log\|Vcm/Vl\|***

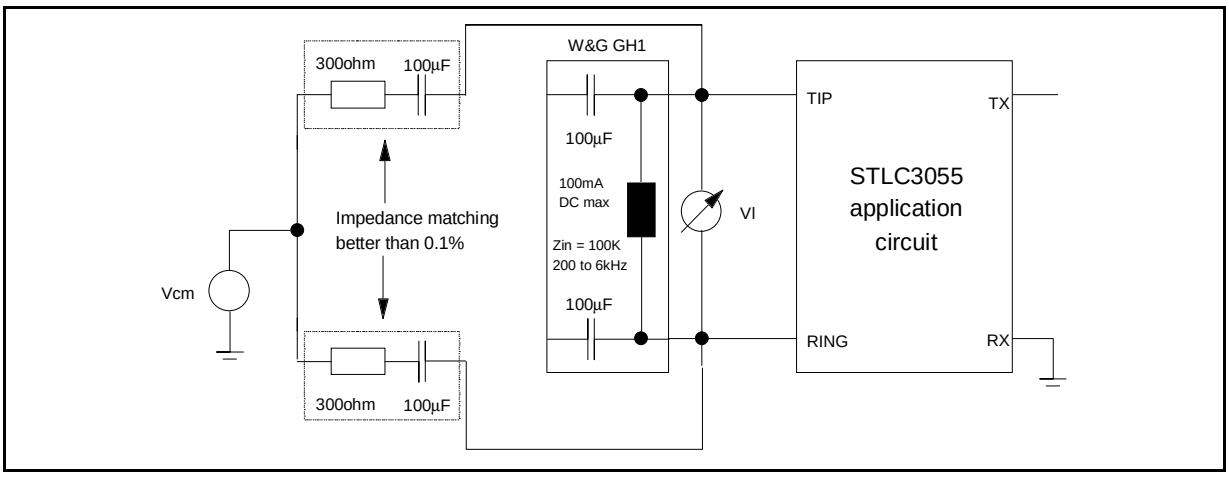



**Figure A7. T/L Transversal to Longitudinal Conversion**
***T/L = 20Log\|Vrx/Vcm\|***

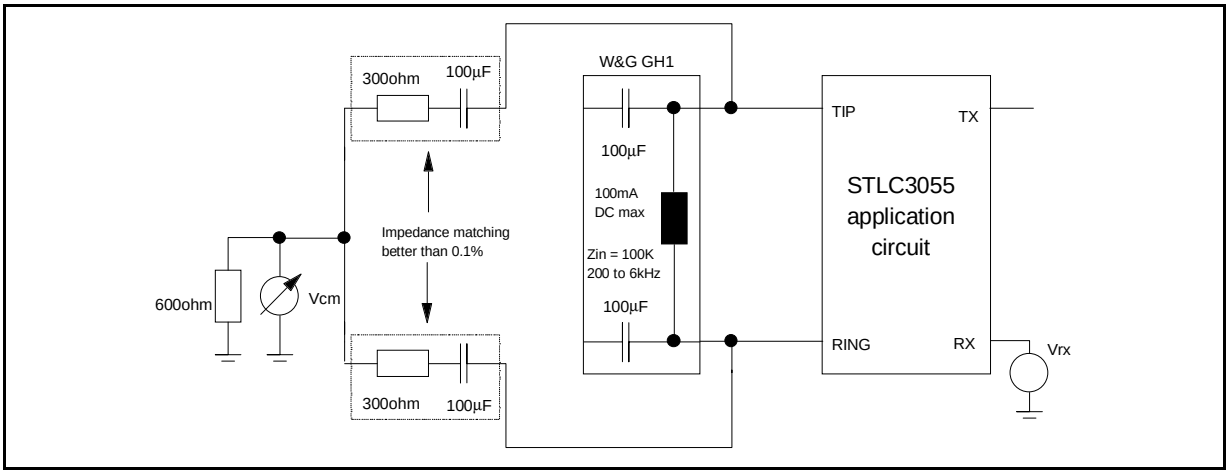



**Figure A8. VTTX Metering Pulse level on line**

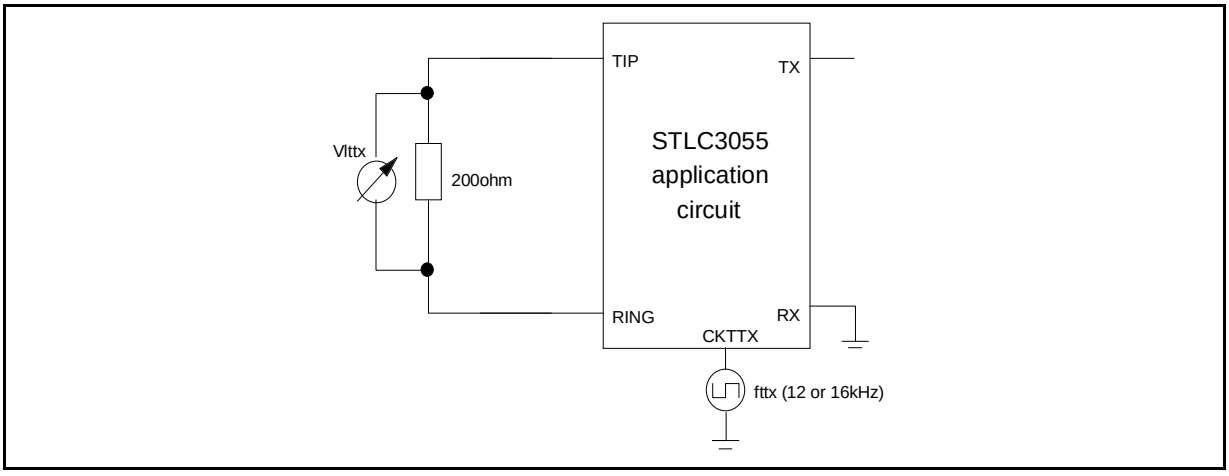
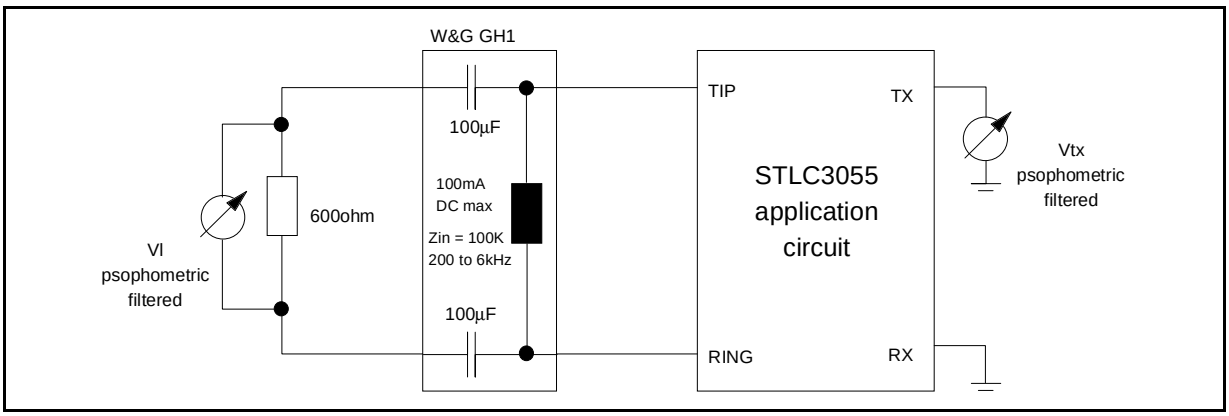


**Figure A9. V2Wp and W4Wp: Idle channel psophometric noise at line and TX.**
***V2Wp = 20Log|Vl/0.774l|; V4Wp = 20Log|Vtx/0.774l|***




# APPENDIX B

## STLC3055 Overvoltage Protection

**Figure B1. Simplified configuration for indoor overvoltage protection**

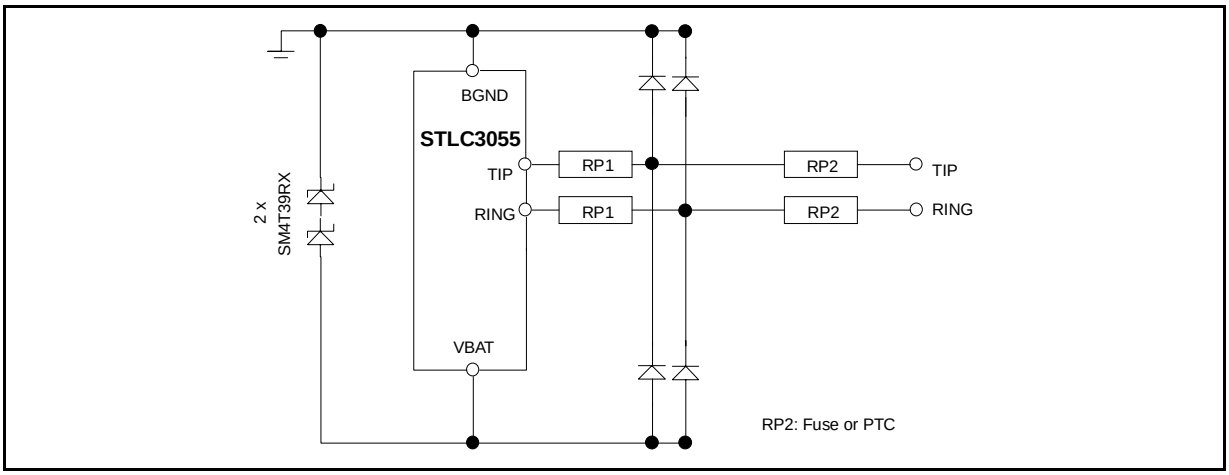
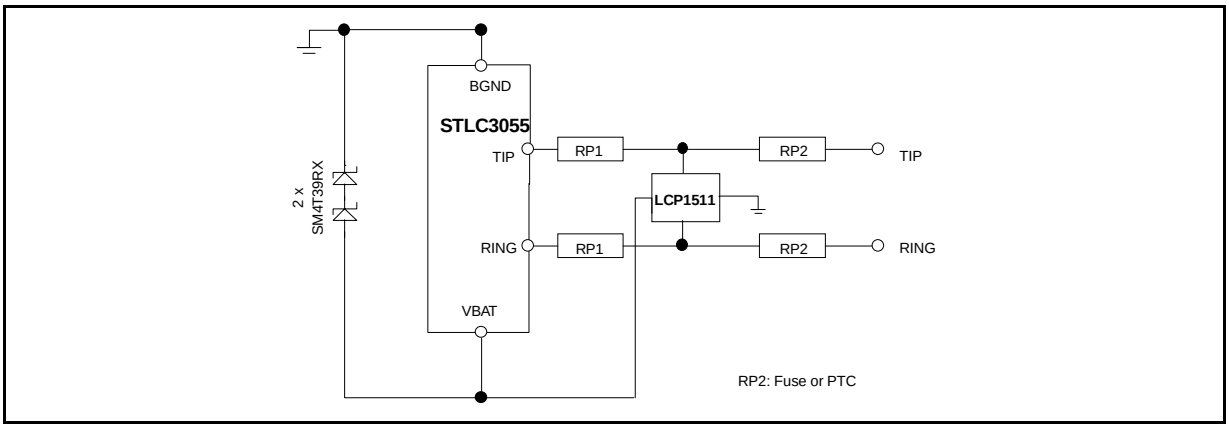


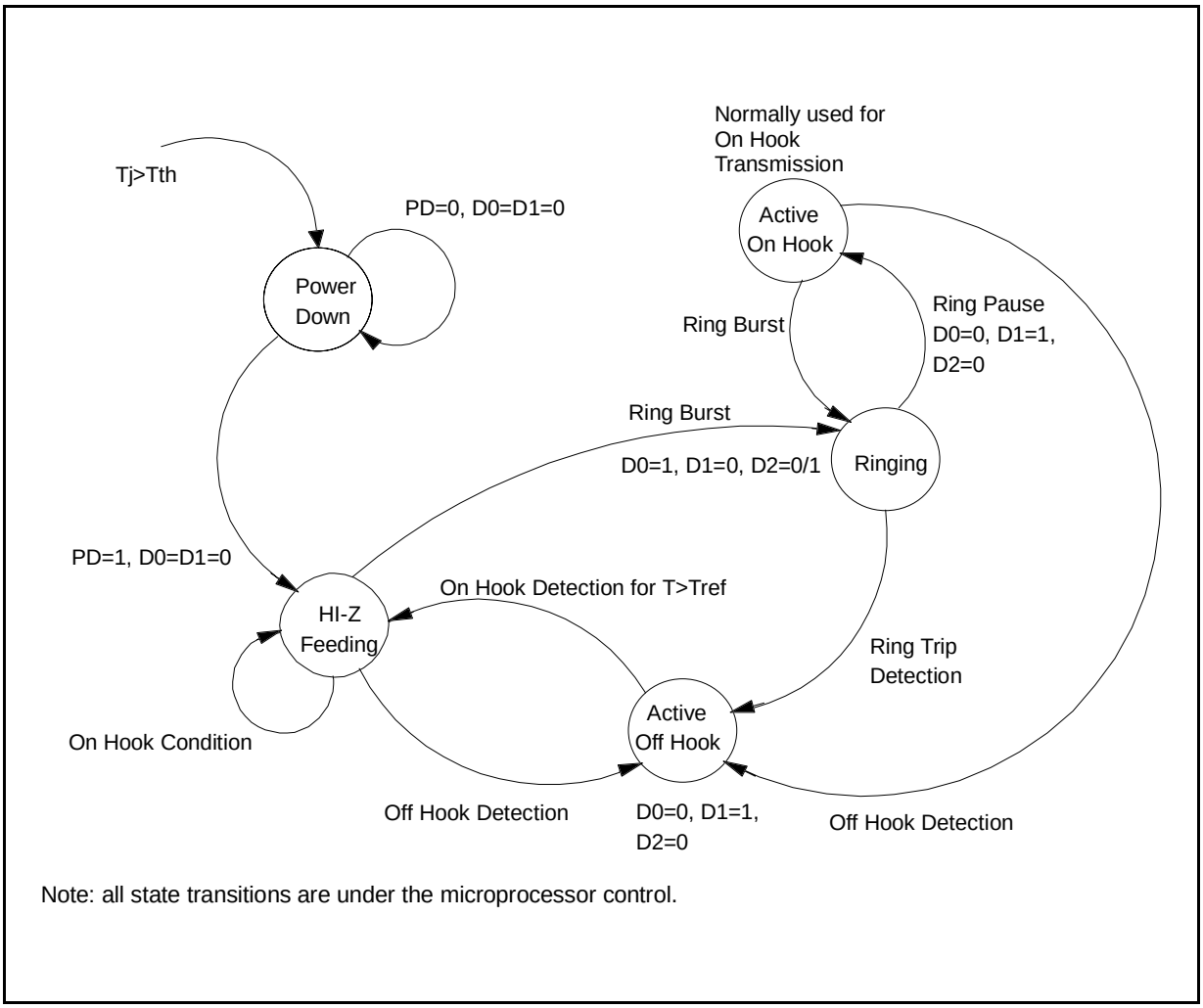

**Figure B2. Standard overvoltage protection configuration for K20 compliance**



## APPENDIX C

## TYPICAL STATE DIAGRAM FOR STLC3055 OPERATION

**Figure C1.**



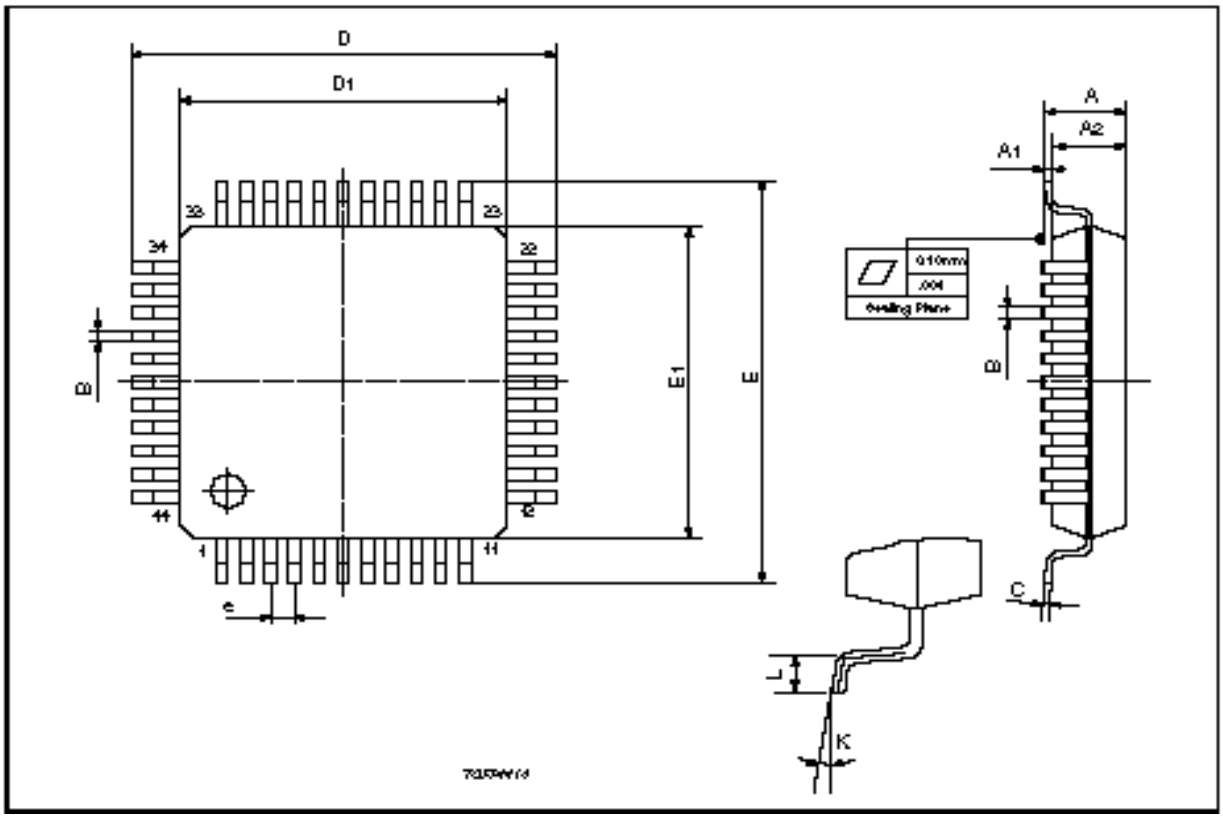

Note: all state transitions are under the microprocessor control.

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| B | 0.30 | 0.37 | 0.45 | 0.012 | 0.014 | 0.018 |
| C | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 12.00 | | | 0.472 | |
| D1 | | 10.00 | | | 0.394 | |
| D3 | | 8.00 | | | 0.315 | |
| e | | 0.80 | | | 0.031 | |
| E | | 12.00 | | | 0.472 | |
| E1 | | 10.00 | | | 0.394 | |
| E3 | | 8.00 | | | 0.315 | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |
| K | 0° (min.), 3.5° (typ.), 7° (max.) | | | | | |

## OUTLINE AND MECHANICAL DATA



## TQFP44 (10 x 10)



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