STP10NK50Z

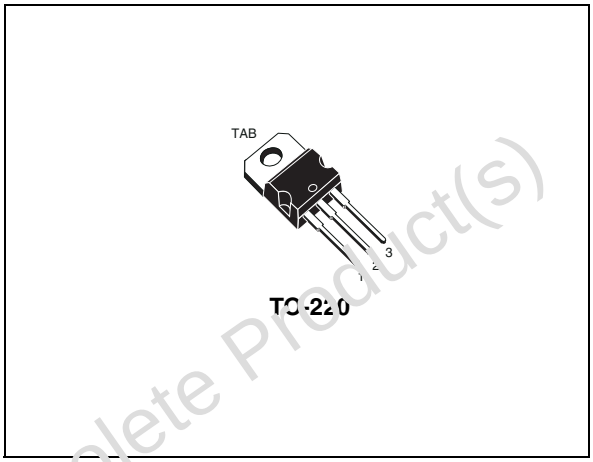
N-channel 500 V, 0.55 Ω, 9 A Zener-protected SuperMESH™ Power MOSFETs in TO-220 package

Datasheet — obsolete product

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STP10NK50Z	500 V	< 0.7 Ω	9 A	125 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Applications

- Switching application

Description

These devices are N-channel Zener-protected Power MOSFETs developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Figure 1. Internal schematic diagram

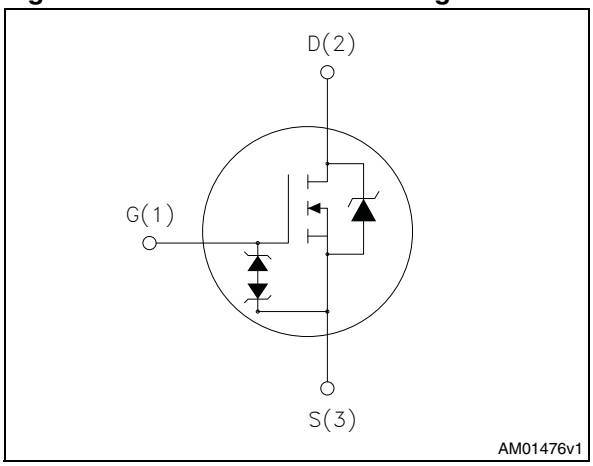


Table 1. Device summary

Order code	Marking	Package	Packaging
STP10NK50Z	P10NK50Z	TO-220	Tube

Obsolete Product(s) - Obsolete Product(s)

This is information on a discontinued product.

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	9	A
I_D	Drain current (continuous) at T_C=100 °C	5.7	A
I_{DM}(1)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	W
	Derating factor	1	W/°C
Vesd(G-S)	G-S ESD (HBM C=100 pF, R=1.5 kΩ)	4000	V
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤9 A, di/dt ≤200 A/µs,V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	9	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, I_D=I_{AR}, V_{DD}=50 V)	230	mJ

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 500 V V_{DS} = 500 V, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 4.5 A		0.55	0.7	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1219 159 40	-	pF pF pF
$C_{oss\ eq}$ (1).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0 to 640 V	-	806	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=400 V, I_D = 9 A V_{GS} =10 V See *Figure 15*	-	39.2 7.42 20.7	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Obsolete Product(s) - Obsolete Product(s)

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=250 V, I_D=4.5A, R_G=4.7Ω, V_{GS}=10V See *Figure 16*	-	19 17	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay Time Fall time		-	43 15	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM}(1)	Source-drain current (pulsed)		-		36	A
V_{SD}(2)	Forward on voltage	I_{SD}=9 A, V_{GS}=0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=9 A, di/dt = 100 A/µs, V_{DD}=35 V	-	268 1.83 13.7		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=9 A, di/dt = 100 A/µs, V_{DD}=35 V, Tj=150 °C	-	343 2.6 15.15		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Table 9. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=±1 mA (open drain)	30	-		V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

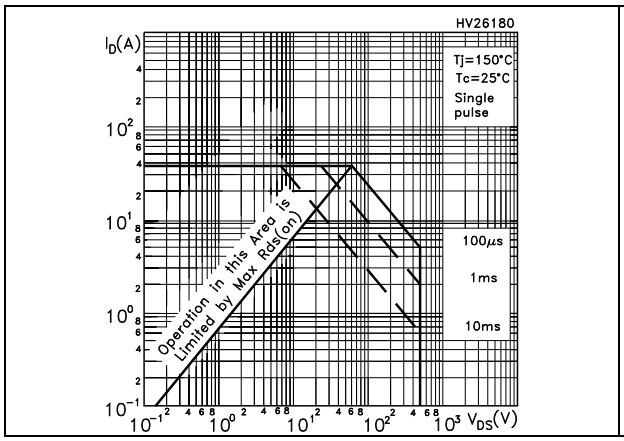


Figure 3. Thermal impedance

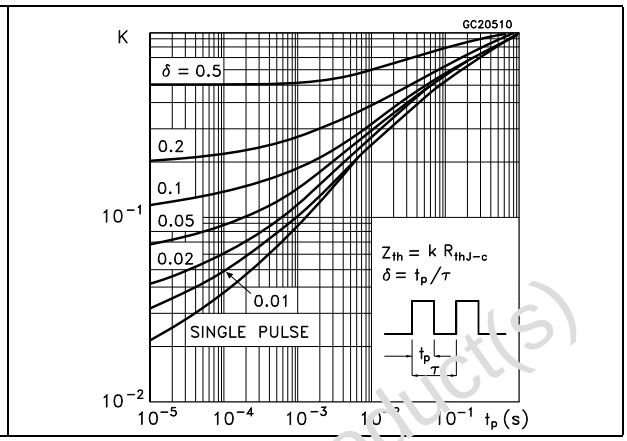


Figure 4. Output characterisics

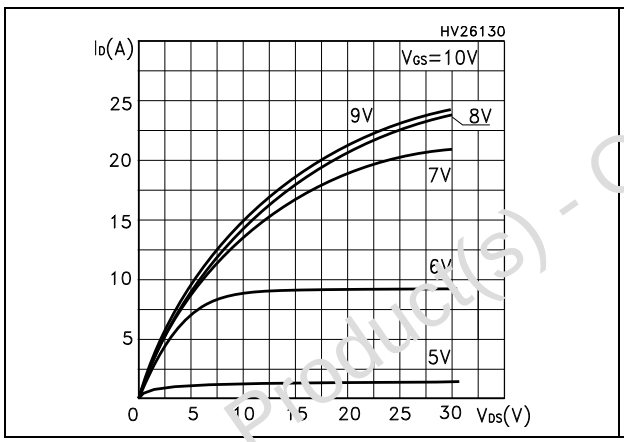


Figure 5. Transfer characteristics

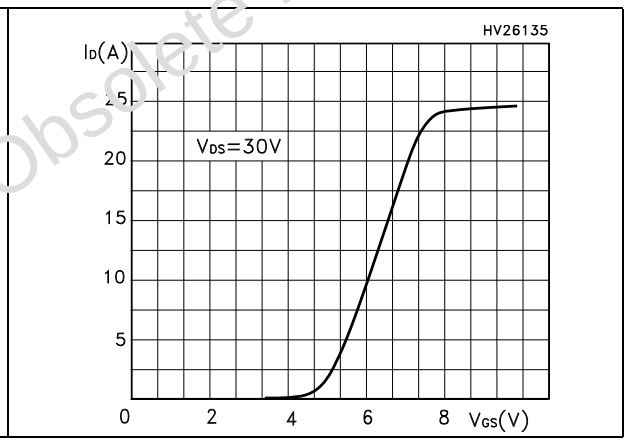


Figure 6. Normalized BV_{DSS} vs temperature

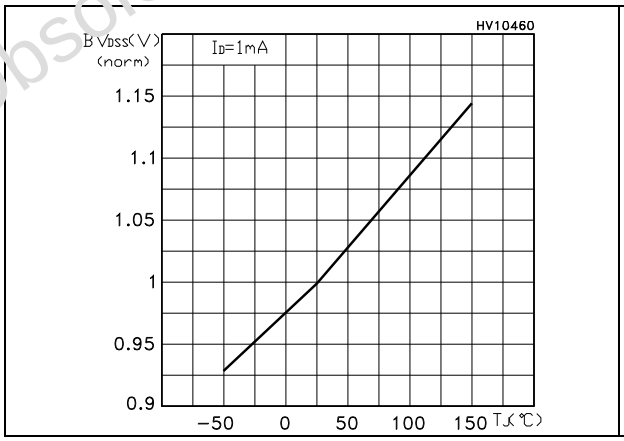
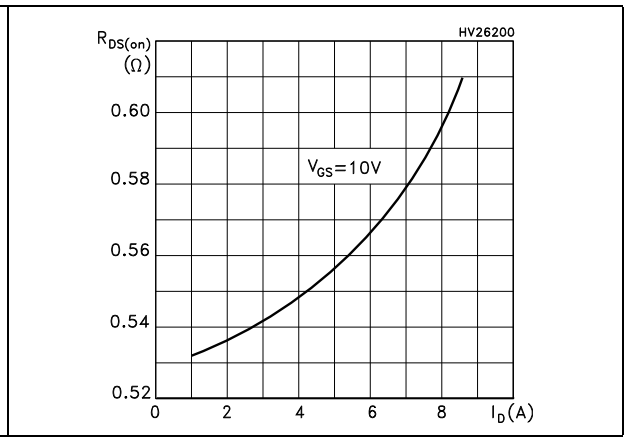


Figure 7. Static drain-source on resistance



Obsolete product(s) - Obsolete Product(s)

Figure 8. Gate charge vs gate-source voltage

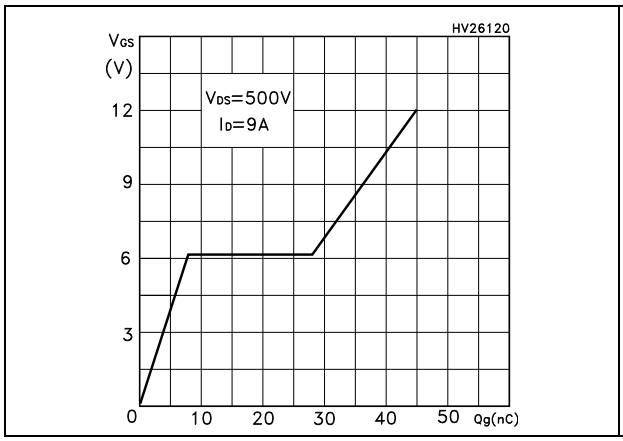


Figure 9. Capacitance variations

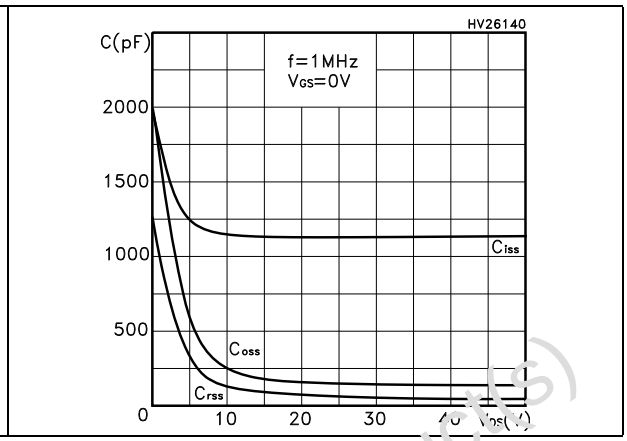


Figure 10. Normalized gate threshold voltage vs temperature

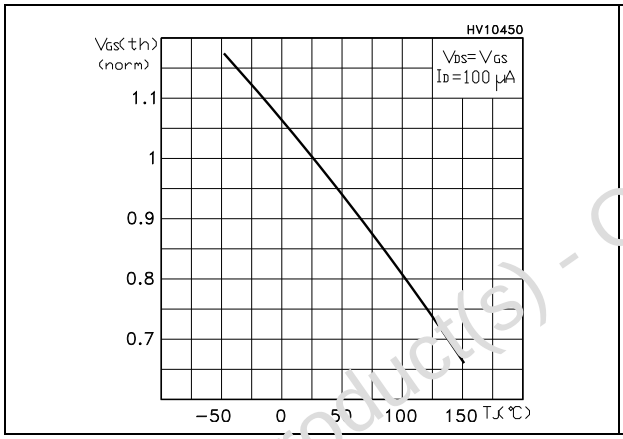


Figure 11. Normalized on resistance vs temperature

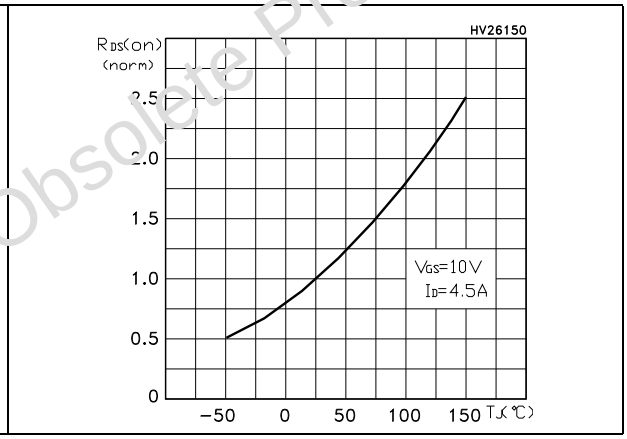


Figure 12. Source-drain diode forward characteristics

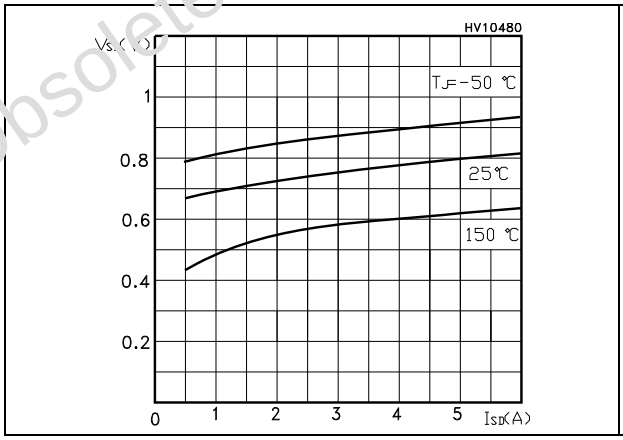
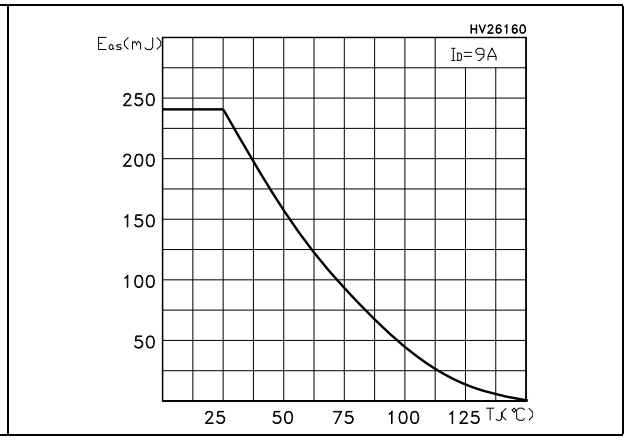


Figure 13. Maximum avalanche energy vs temperature



Obsolete Product(s) - Obsolete Product(s)

3 Test circuit

Figure 14. Switching times test circuit for resistive load

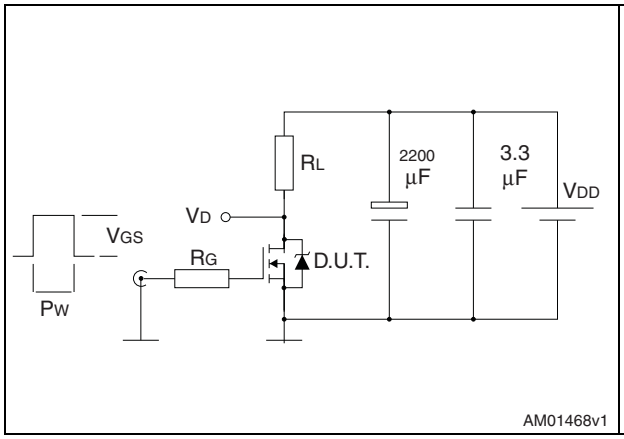


Figure 15. Gate charge test circuit

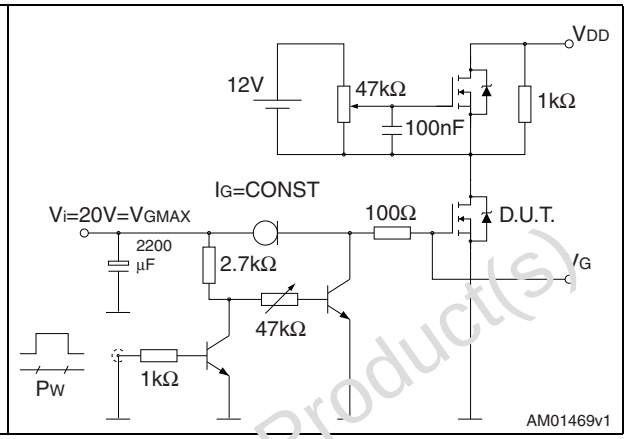


Figure 16. Test circuit for inductive load switching and diode recovery times

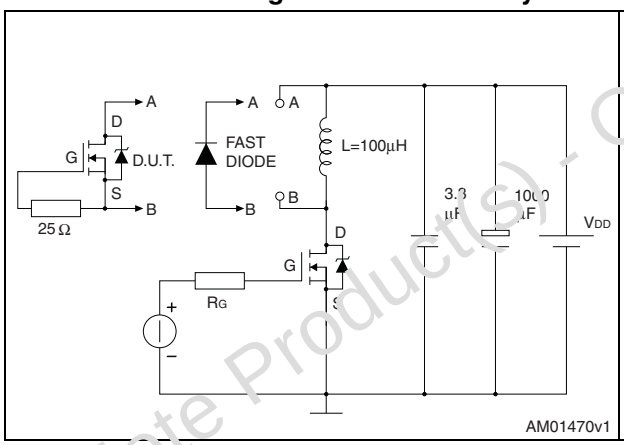


Figure 17. Unclamped inductive load test circuit

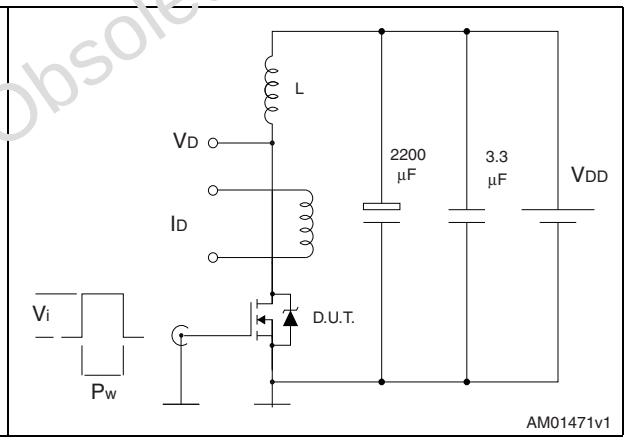


Figure 18. Unclamped inductive waveform

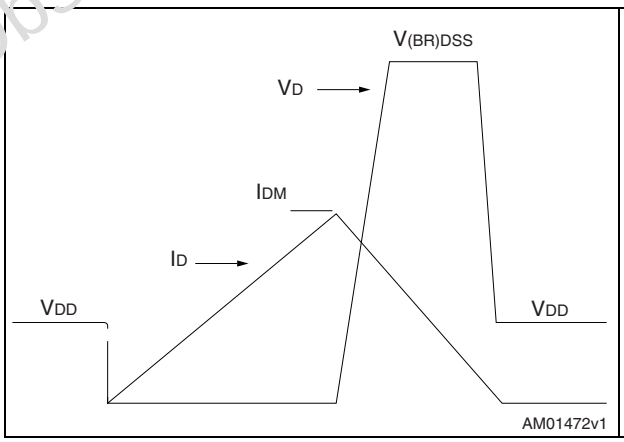
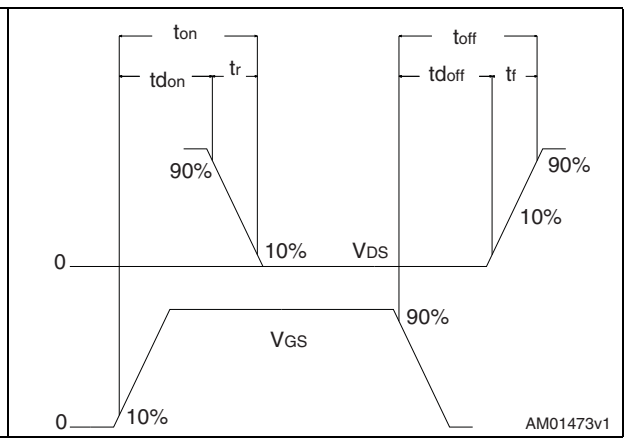


Figure 19. Switching time waveform



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4 Package mechanical data

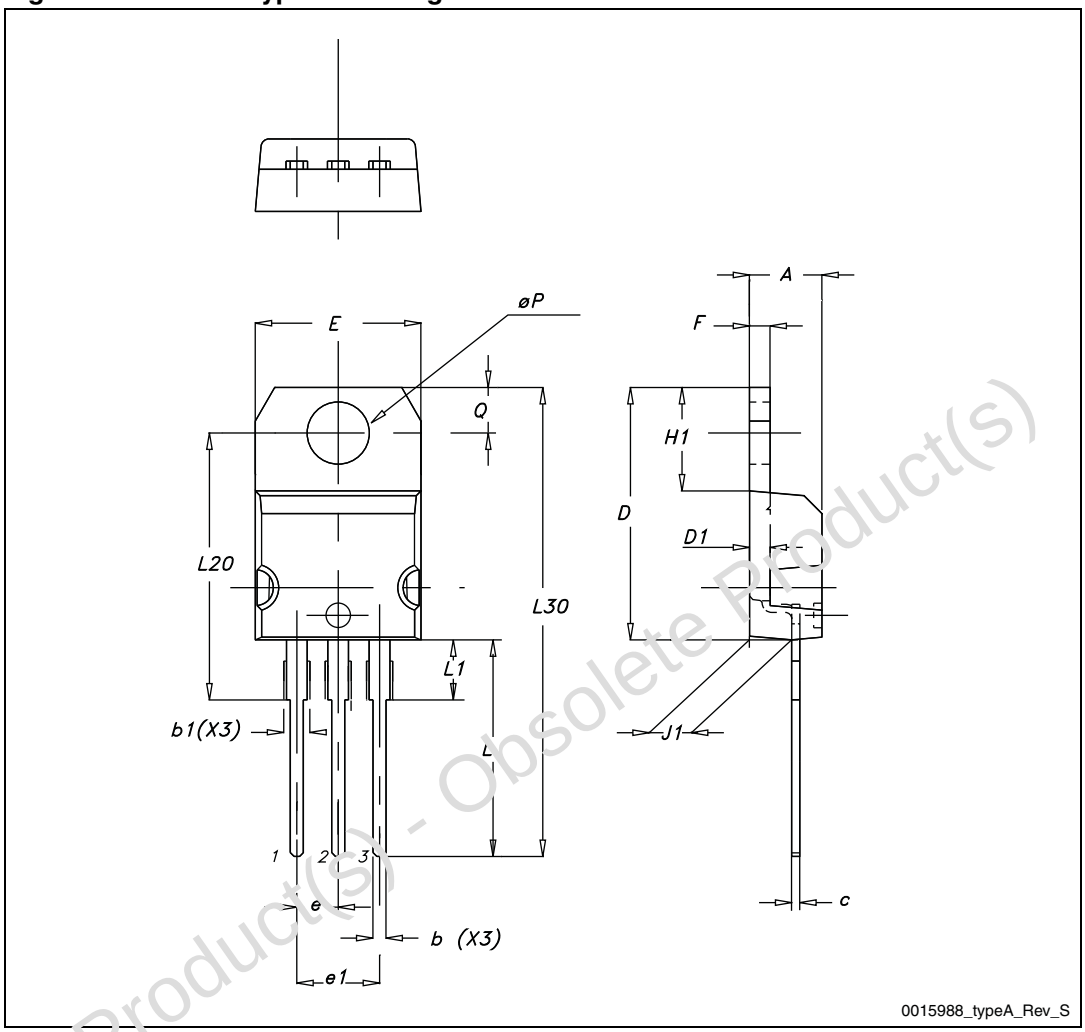
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Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Obsolete Product(s) - Obsolete Product(s)

Figure 20. TO-220 type A drawing



Obsolete Product(s) - Obsolete Product(s)

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
01-Jul-2005	1	First release.
08-Sep-2005	2	Inserted ecopack indication
15-Mar-2012	3	The part number STF10NK50Z has been moved to a separate datasheet.

Obsolete Product(s) - Obsolete Product(s)

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