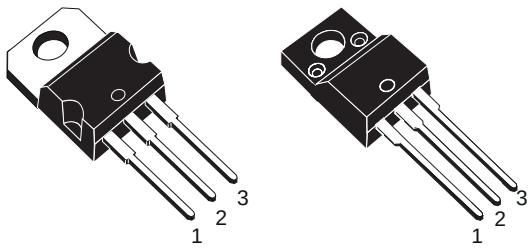
STP5NB40
STP5NB40FP

N-CHANNEL 400V - 1.47Ω - 4.7A TO-220/TO-220FP
PowerMesh™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP5NB40	400 V	< 1.8 Ω	4.7 A
STP5NB40FP	400 V	< 1.8 Ω	4.7 A

- TYPICAL R_{DS}(on) = 1.47 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

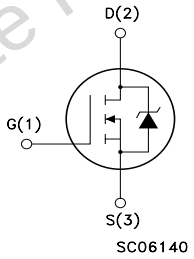


TO-220 **TO-220FP**

DESCRIPTION

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprieraty edge termination structure, gives the lowest $R_{DS(on)}$ per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITH MODE POWER SUPPLIES (SMPS)
- DC-AC CONVERTERS FOR WELDING EQUIPMENT

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP5NB40	STP5NB40FP	
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	400		V
V_{GS}	Gate- source Voltage	±30		V
I_D	Drain Current (continuos) at T_C = 25°C	4.7	4.7 (*)	A
I_D	Drain Current (continuos) at T_C = 100°C	3	3 (*)	A
I_{DM} (•)	Drain Current (pulsed)	19	19 (*)	A
P_{TOT}	Total Dissipation at T_C = 25°C	80	30	W
	Derating Factor	0.64	0.24	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	4	4	V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	V
T_{stg}	Storage Temperature	–65 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•)Pulse width limited by safe operating area (*)Limited only by maximum temperature allowed

(1)I_{SD} ≤4.7A, di/dt ≤200A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

Obsolete Product(s) - Obsolete Product(s)

THERMAL DATA

		TO-220	TO-220FP	
Rthj-case	Thermal Resistance Junction-case Max	1.56	4.1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5		°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	300		°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	4.7	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	200	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	400			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating			1	µA
		V_{DS} = Max Rating, T_C = 125 °C			50	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 2.3 A		1.47	1.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, I_D = 2.3 A		2.4		S
C_{iss}	Input Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		405		pF
C_{oss}	Output Capacitance			72		pF
C_{rss}	Reverse Transfer Capacitance			9		pF

Obsolete Product(s) - Obsolete Product(s)

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 200 V, I_D = 2.5 A		11		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 10 V (see test circuit, Figure 3)		8		ns
Q_g	Total Gate Charge	V_{DD} = 320V, I_D = 5 A,		14.5	20	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10V		7		nC
Q_{gd}	Gate-Drain Charge			5.1		nC

SWITCHING OFF

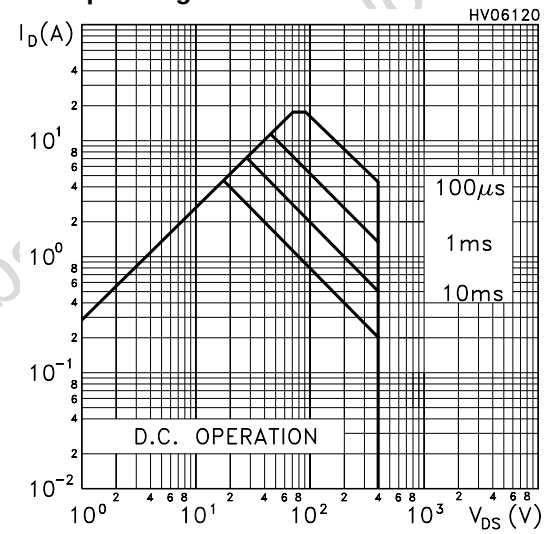
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	V_{DD} = 320V, I_D = 5 A,		9		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 10V (see test circuit, Figure 5)		6		ns
t_c	Cross-over Time			14		ns

SOURCE DRAIN DIODE

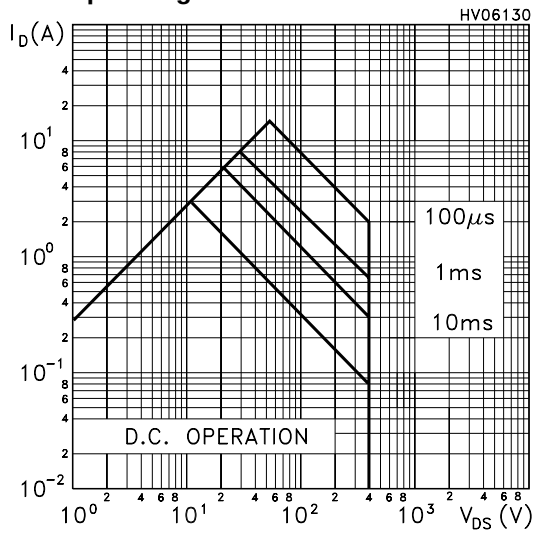
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				4.7	A
I_{SDM} (1)	Source-drain Current (pulsed)				19	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 4.7 A, V_{GS} = 0			1.6	V
t_{rr}	Reverse Recovery Time	I_{SD} = 5 A, di/dt = 100A/µs,		300		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 100V, T_j = 150°C (see test circuit, Figure 5)		1.6		µC
I_{RRM}	Reverse Recovery Current			10.5		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Safe Operating Area for TO-220

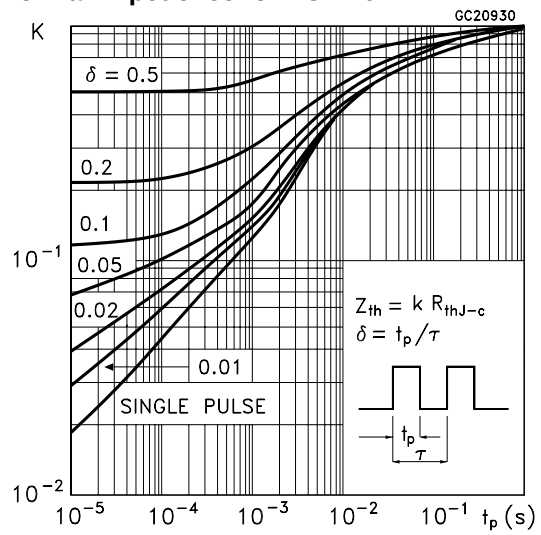


Safe Operating Area for TO-220FP

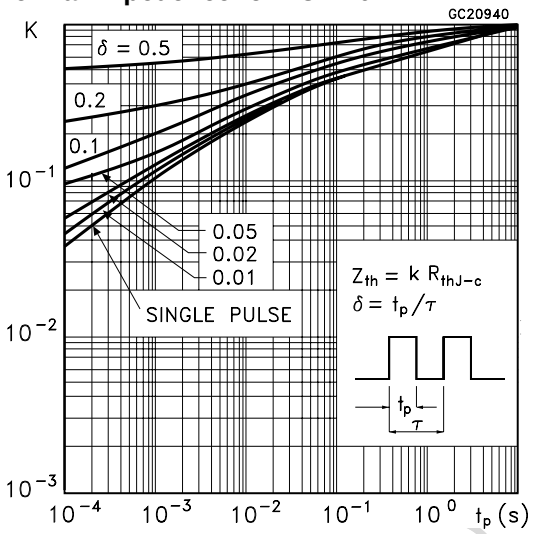


Obsolete Product(s) - Obsolete Product(s)

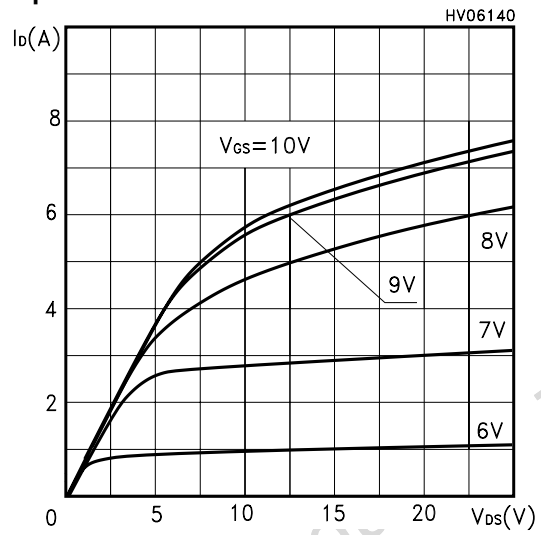
Thermal Impedence for TO-220



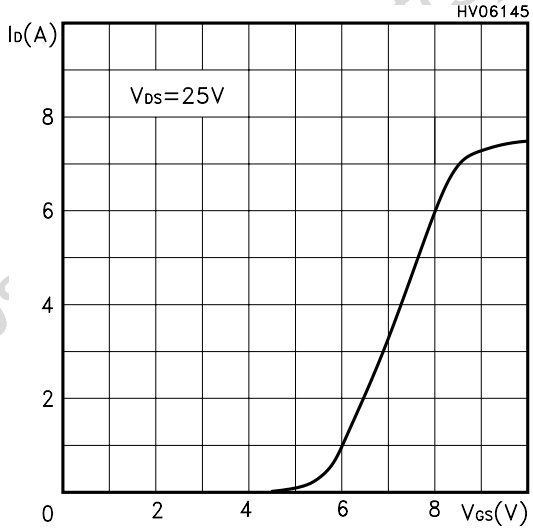
Thermal Impedence for TO-220FP



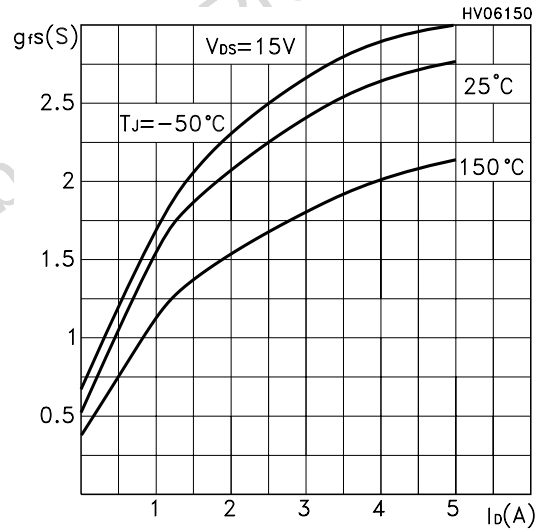
Output Characteristics



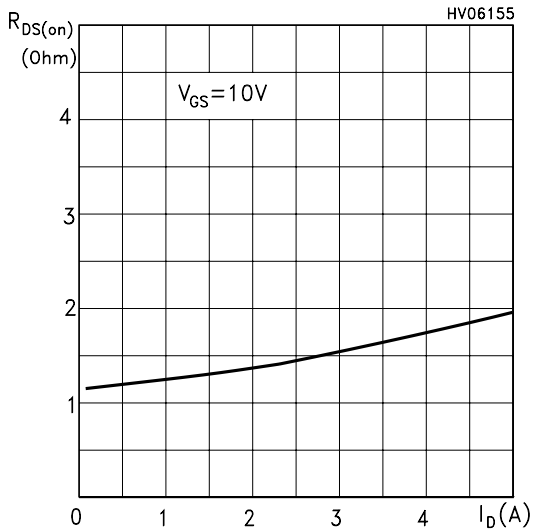
Transfer Characteristics



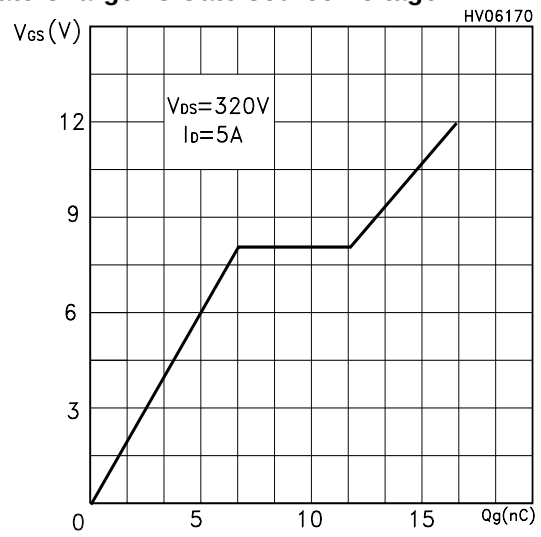
Transconductance



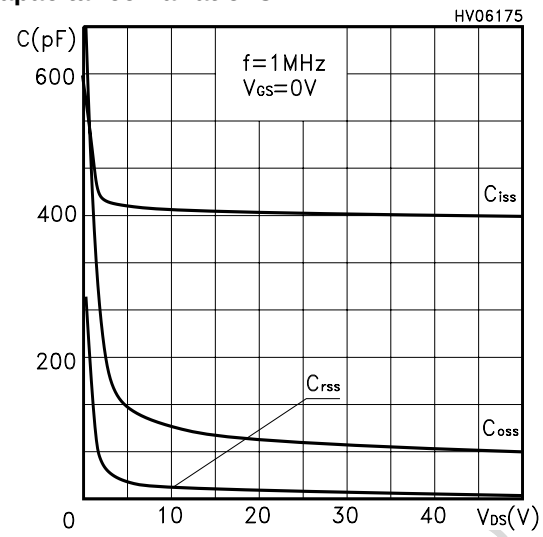
Static Drain-source On Resistance



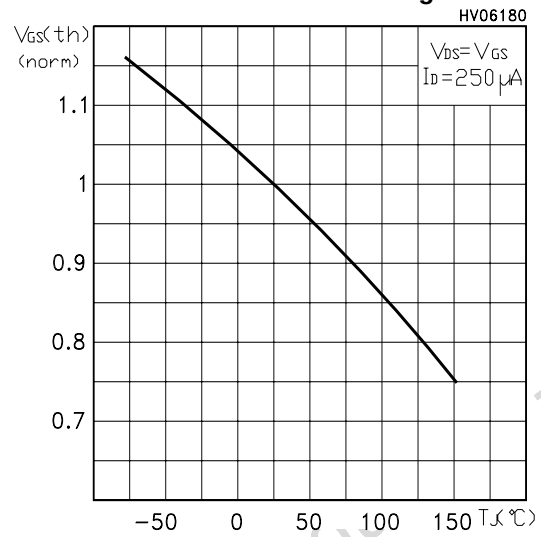
Gate Charge vs Gate-source Voltage



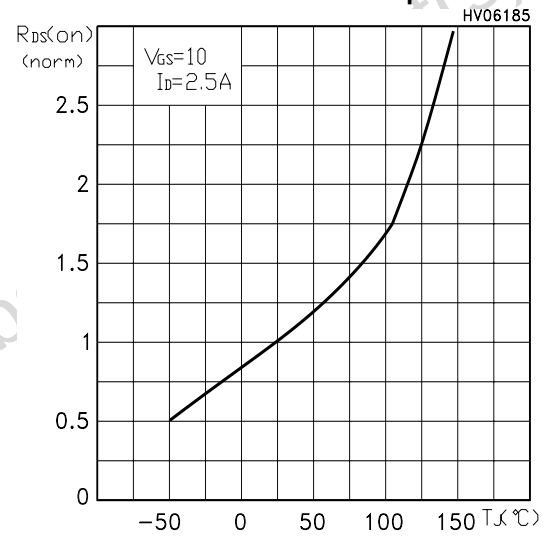
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

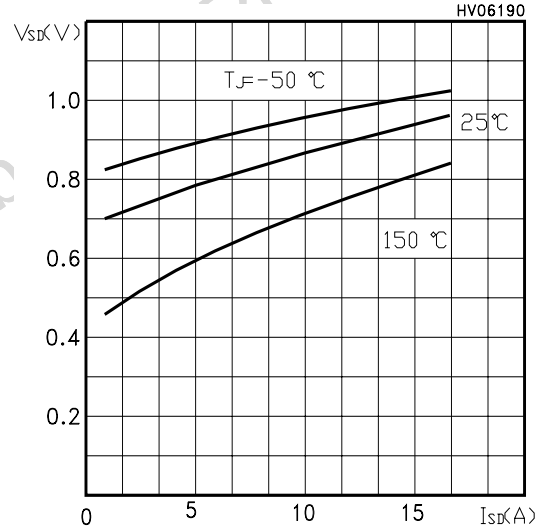


Fig. 1: Unclamped Inductive Load Test Circuit

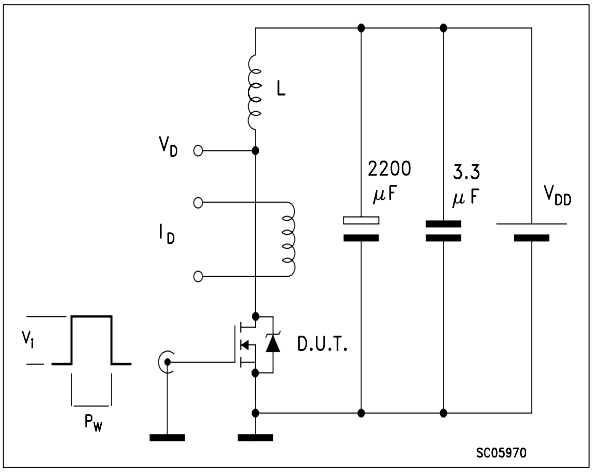


Fig. 2: Unclamped Inductive Waveform

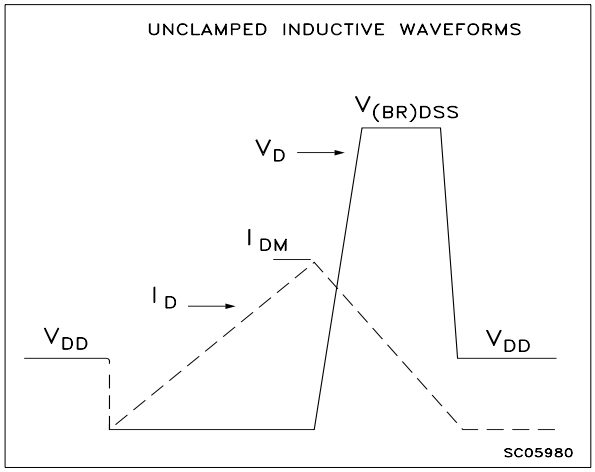


Fig. 3: Switching Times Test Circuit For Resistive Load

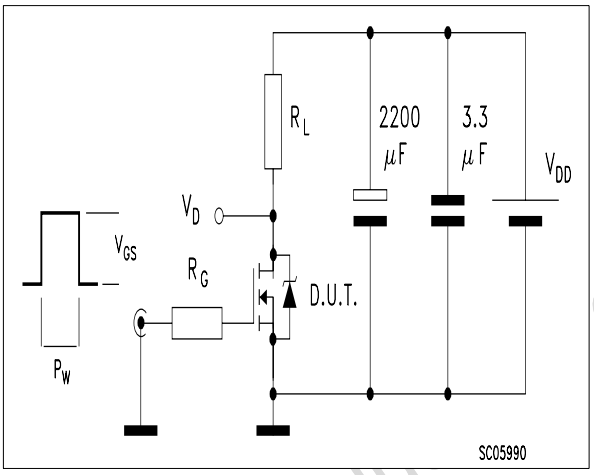


Fig. 4: Gate Charge test Circuit

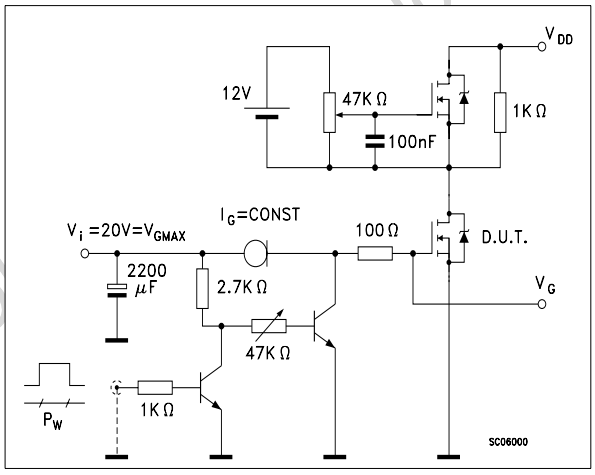
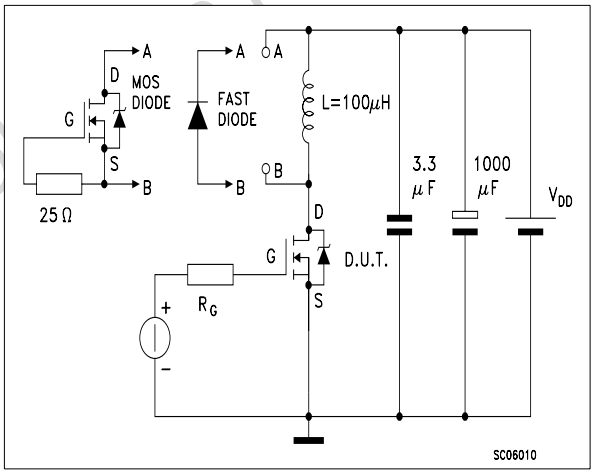
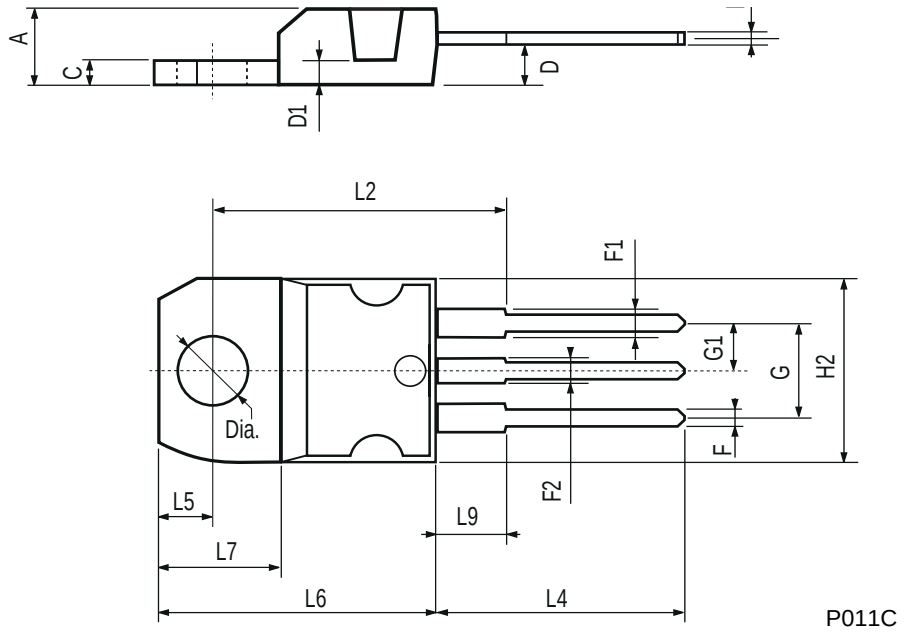


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



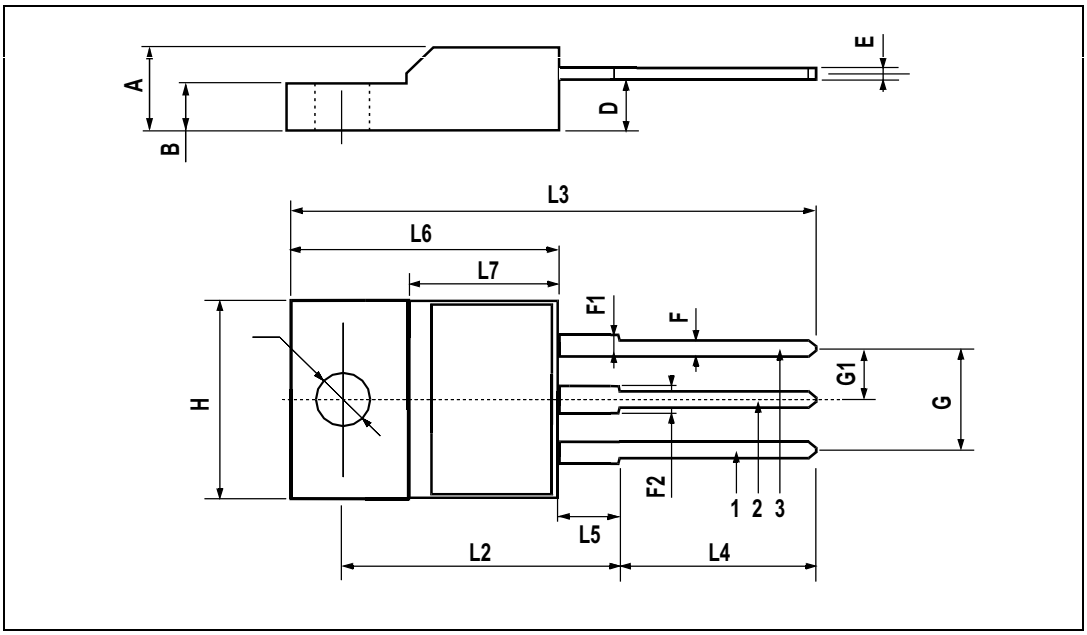
TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2001 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

http://www.st.com