STR1P2UH7

P-channel 20 V, 0.087 Ω typ., 1.4 A STripFET™ H7 Power MOSFET in a SOT-23 package

Datasheet - production data

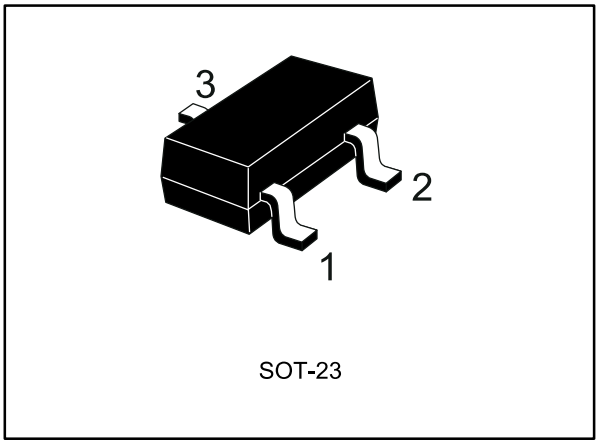
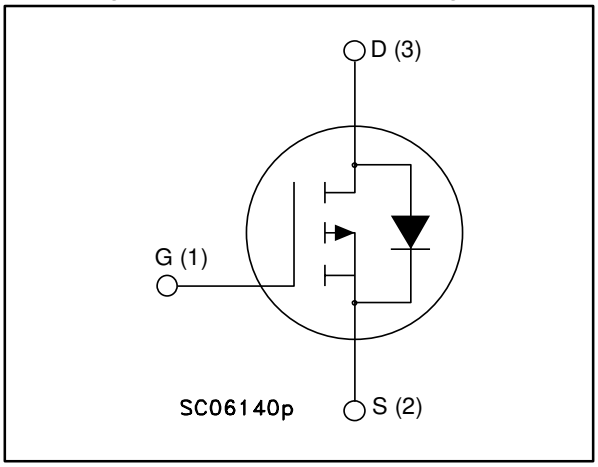


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STR1P2UH7	20 V	0.1 Ω @ 4.5	1.4 A

- Very low on-resistance
- Very low capacitance and gate charge
- High avalanche ruggedness

Applications

- Switching applications

Description

This P-channel Power MOSFET utilizes the STripFET H7 technology with a trench gate structure combined with extremely low on-resistance. The device also offers ultra-low capacitances for higher switching frequency operations.

Table 1: Device summary

Order code	Marking	Package	Packaging
STR1P2UH7	1L2U	SOT-23	Tape and reel

For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

This is information on a product in full production. www.st.com

Contents

1 Electrical ratings 3
2 Electrical characteristics 4
2.1 Electrical characteristics (curves) 6
3 Test circuits 8
4 Package mechanical data 9
4.1 SOT-23 package mechanical data 9
5 Revision history 11

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at T_{pcb} = 25 °C	1.4	A
I_D	Drain current (continuous) at T_{pcb} = 100 °C	0.9	A
I_{DM}(1)	Drain current (pulsed)	5.6	A
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	0.35	W
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

Notes:

(1)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max, single operation	357	°C/W

Notes:

(1)When mounted on 1inch² FR-4 board, 2 oz Cu



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	20			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 20 V, V_{GS} = 0			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 8 V, V_{DS} = 0			10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 4.5 V, I_D = 0.7 A		0.087	0.1	Ω
		V_{GS} = 2.5 V, I_D = 0.7 A		0.11	0.13	Ω
		V_{GS} = 1.8 V, I_D = 0.7 A		0.145	0.18	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 10 V, f = 1 MHz, V_{GS} = 0	-	510	-	pF
C_{oss}	Output capacitance		-	66	-	pF
C_{rss}	Reverse transfer capacitance		-	44	-	pF
Q_g	Total gate charge	V_{DD} = 10 V, I_D = 3 A, V_{GS} = 4.5 V (see *Figure 14: "Gate charge test circuit"*)	-	4.8	-	nC
Q_{gs}	Gate-source charge		-	0.7	-	nC
Q_{gd}	Gate-drain charge		-	0.8	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 10 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 4.5 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	9	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Fall time		-	19	-	ns



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 1 A, V_{GS} = 0	-	-	1	V
t_{rr}	Reverse recovery time	V_{DD} = 10 V di/dt = 100 A/µs, I_{SD} = 1 A T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	12.5		ns
Q_{rr}	Reverse recovery charge		-	5		nC
I_{RRM}	Reverse recovery current		-	0.8		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.



For the P-channel Power MOSFET the actual polarity of the voltages and the current must be reversed.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

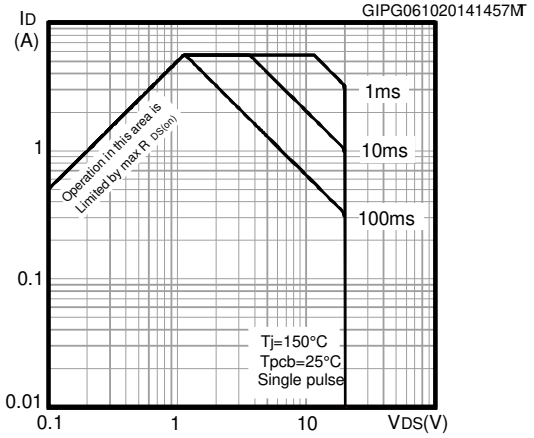


Figure 3: Thermal impedance

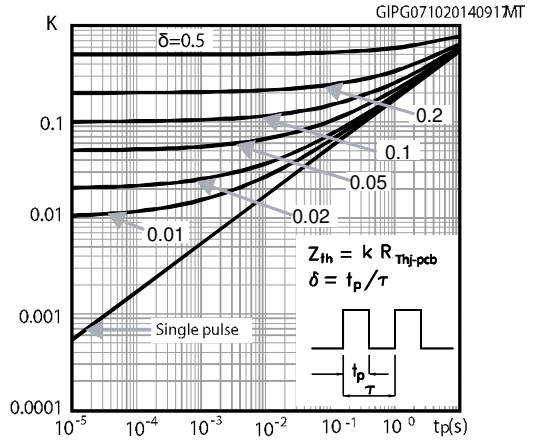


Figure 4: Output characteristics

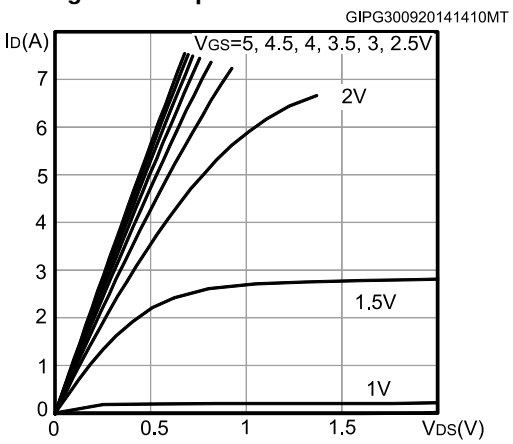


Figure 5: Transfer characteristics

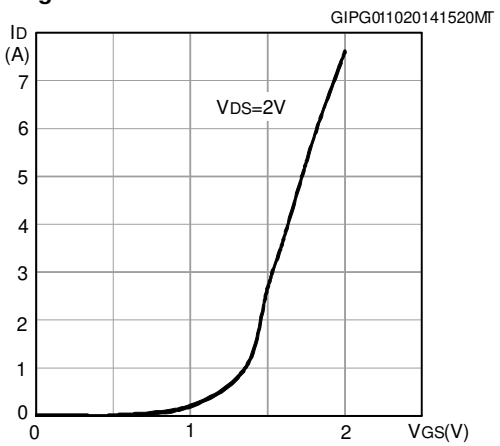


Figure 6: Gate charge vs gate-source voltage

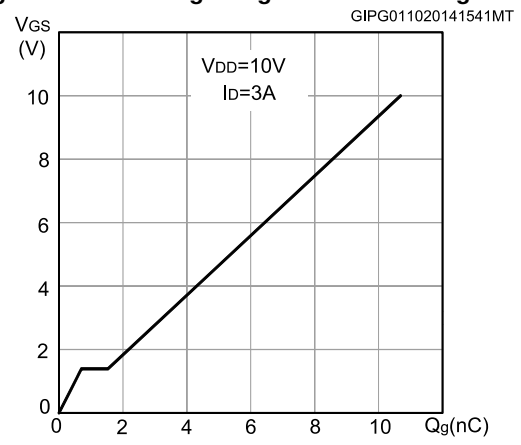


Figure 7: Static drain-source on-resistance

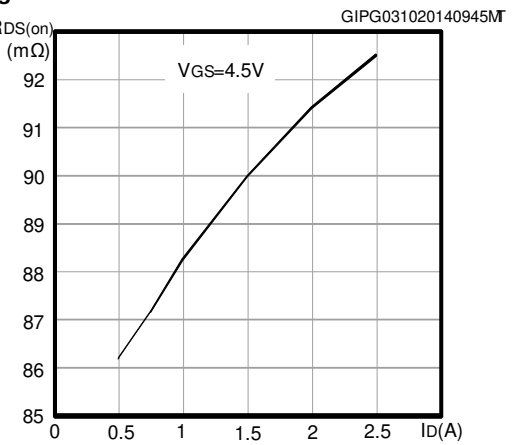


Figure 8: Capacitance variations

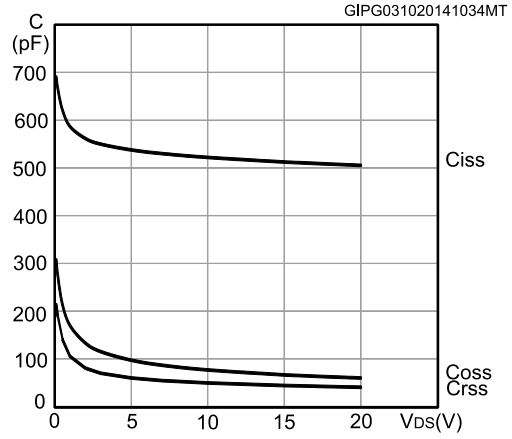


Figure 9: Normalized gate threshold voltage vs temperature

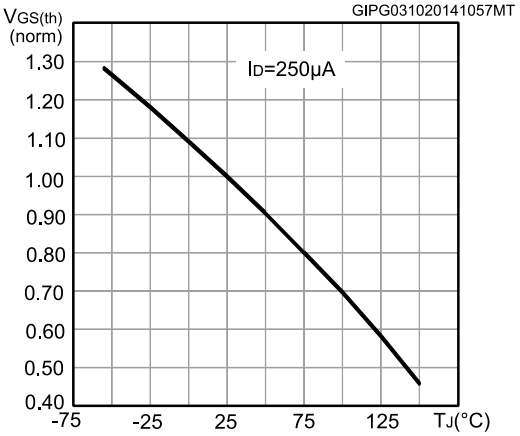


Figure 10: Normalized on-resistance vs temperature

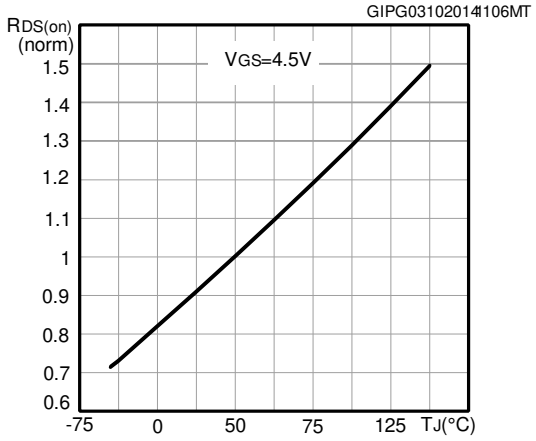


Figure 11: Normalized V(BR)DSS vs temperature

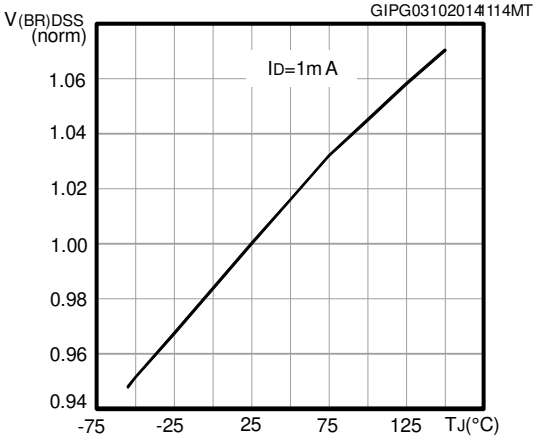
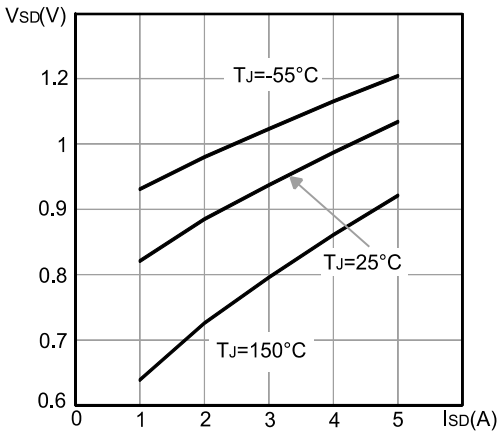


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

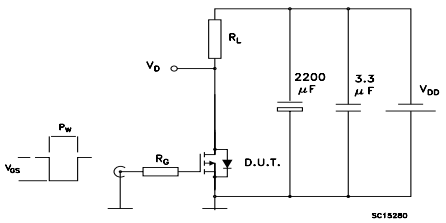


Figure 14: Gate charge test circuit

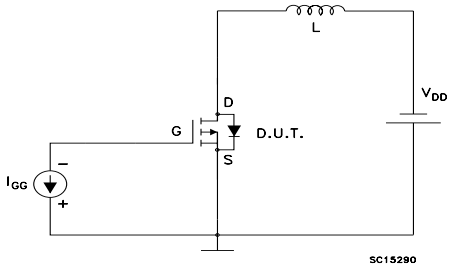
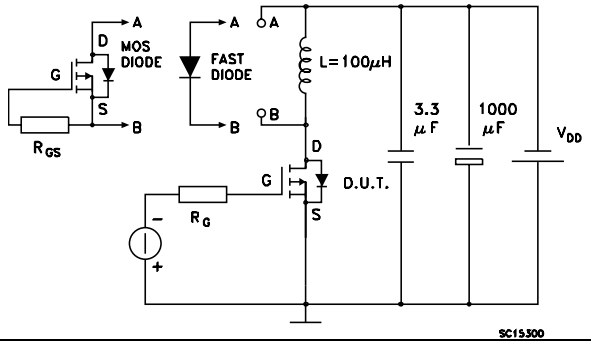


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 SOT-23 package mechanical data

Figure 16: SOT-23 mechanical drawing

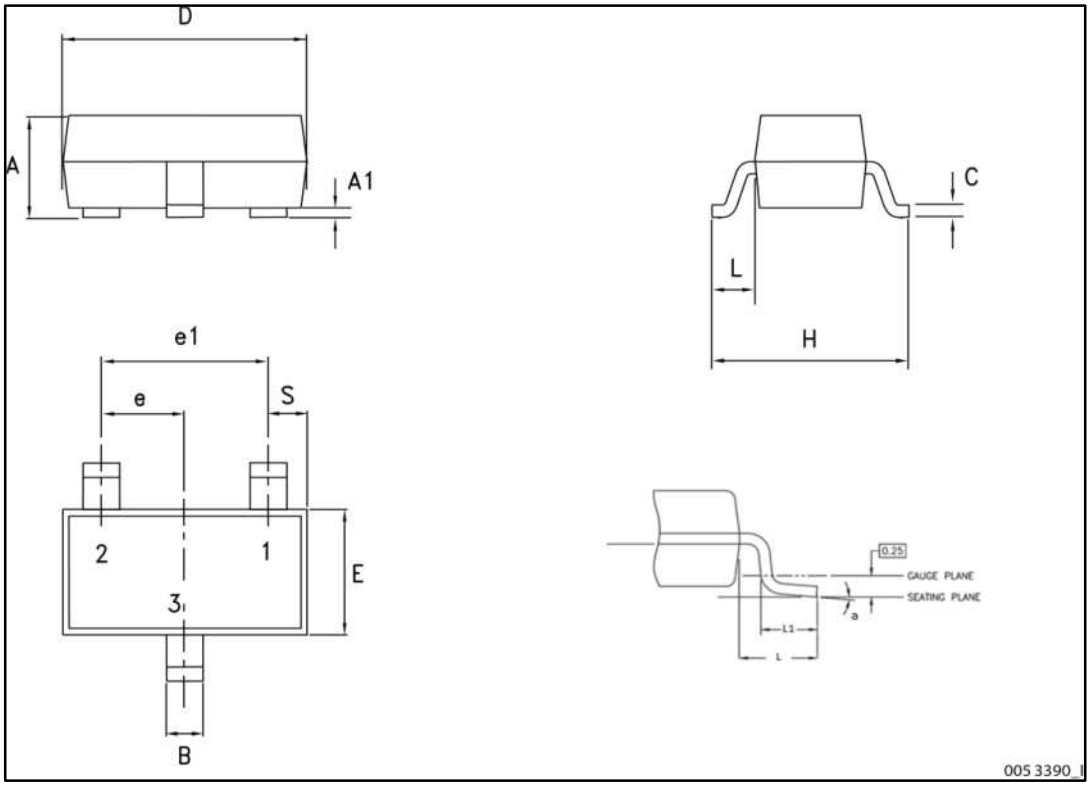
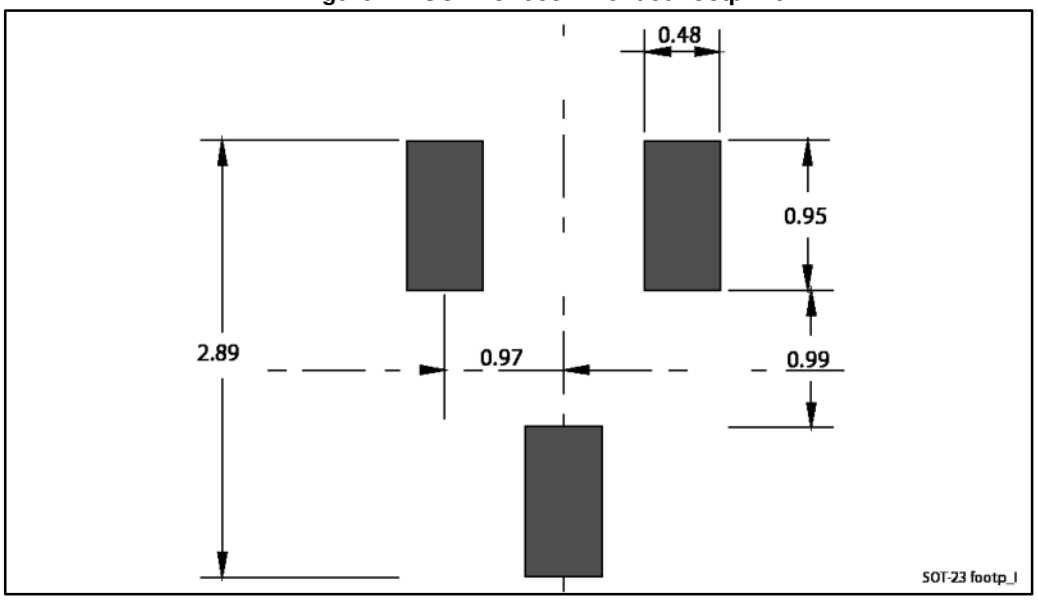


Table 8: SOT-23 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.89		1.40
A1	0		0.10
B	0.30		0.51
C	0.085		0.18
D	2.75		3.04
e	0.85		1.05
e1	1.70		2.10
E	1.20		1.75
H	2.10		3.00
L		0.60	
S	0.35		0.65
L1	0.25		0.55
a	0°		8°

Figure 17: SOT-23 recommended footprint



Dimensions are in mm.

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
18-Jul-2013	1	First release.
07-Oct-2014	2	Document status promoted from target data to preliminary data. Updated title, features and description in cover page. Updated *Section 2: "Electrical characteristics"*. Minor text changes.
05-Jun-2015	3	Document status promoted from preliminary to production data.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved