STS12N3LLH5

N-channel 30 V, 0.0068 Ω, 12 A, SO-8 STripFET™ V Power MOSFET

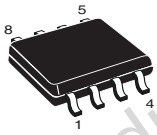
Datasheet — production data

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STS12N3LLH5	30 V	< 0.0075 Ω	12 A (1)

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses



SO-8

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

Figure 1. Internal schematic diagram

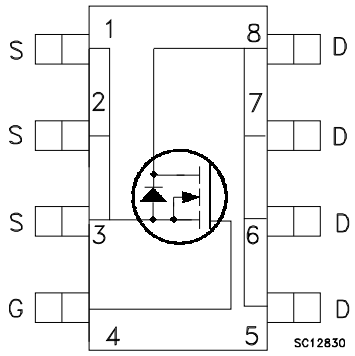


Table 1. Device summary

Order code	Marking	Package	Packaging
STS12N3LLH5	12D3L	SO-8	Tape and reel

Obsolete Product(s) - Obsolete Product(s)

This is information on a product in full production. www.st.com

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate-source voltage	+22/-20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	12	A
I_D (1)	Drain current (continuous) at T_C=100 °C	8.75	A
I_{DM} (2)	Drain current (pulsed)	48	A
P_{TOT} (2)	Total dissipation at T_C = 25 °C	2.7	W
	Derating factor	0.02	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according $R_{thj\text{-}pcb}$
2. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-ambient	47	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10sec

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating, V_{DS} =max rating @125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = +22/-20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 6 A V_{GS}= 4.5 V, I_D= 6 A		0.0068 0.0084	0.0075 0.0092	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0	-	1290 240 32		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 12 A V_{GS}= 4.5 V *Figure 14*	-	8 3.6 3.4		nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 6 A, R_G=4.7 Ω, V_{GS} =10 V *Figure 13*	-	8.6 11.2 32.4 6	-	ns ns ns ns

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Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	I_{SD} = 12 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD}= 25 V, Tj=150 °C	-	22 15 1.4		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

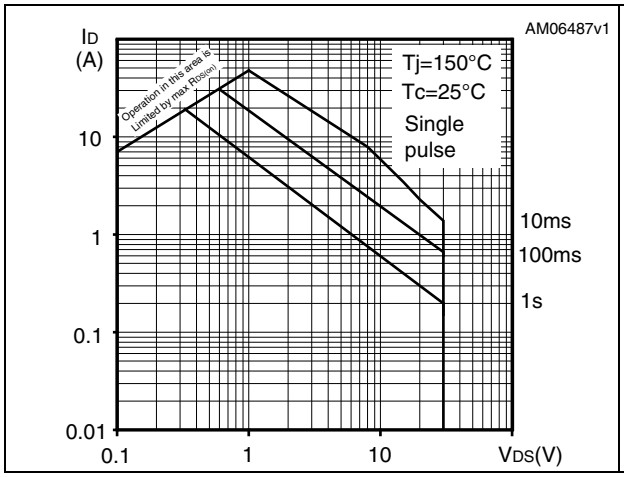


Figure 3. Thermal impedance

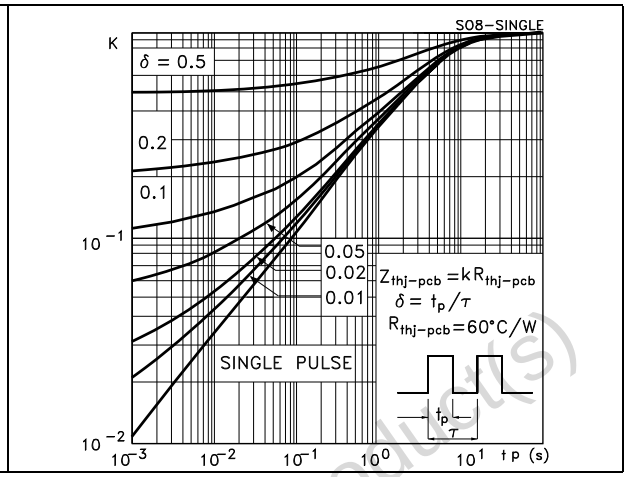


Figure 4. Output characteristics

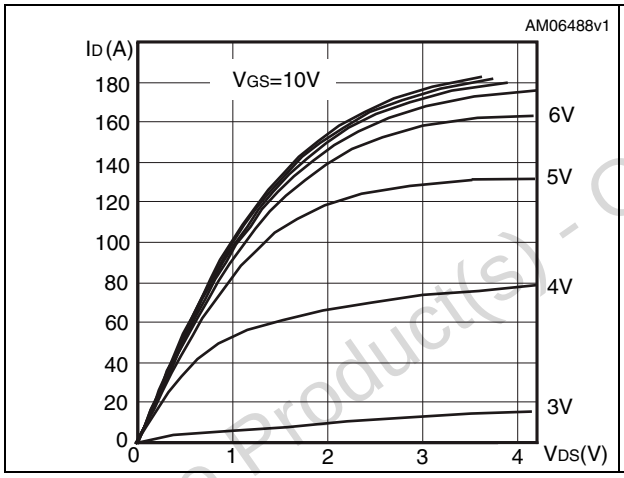


Figure 5. Transfer characteristics

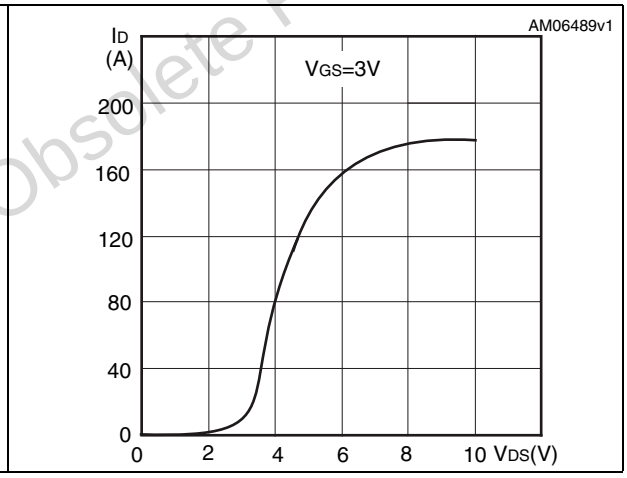


Figure 6. Normalized B_{VDSS} vs temperature

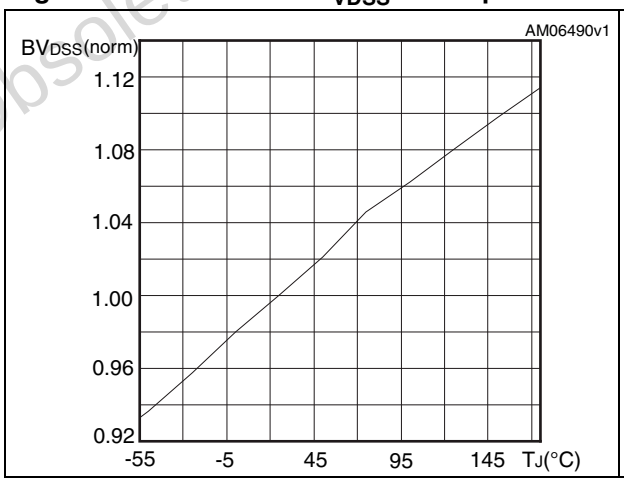
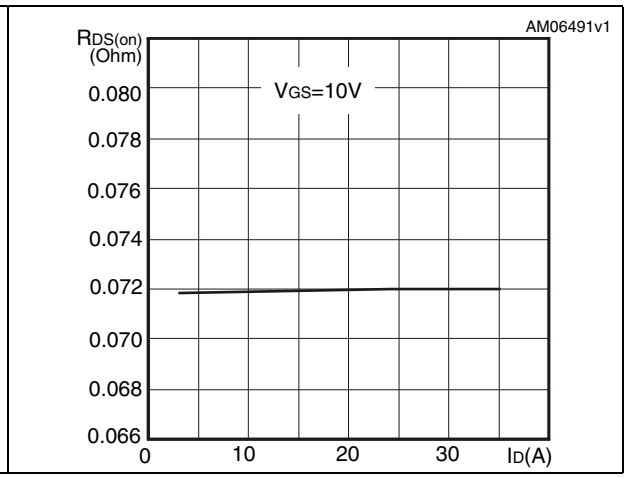


Figure 7. Static drain-source on-resistance



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Figure 8. Gate charge vs gate-source voltage

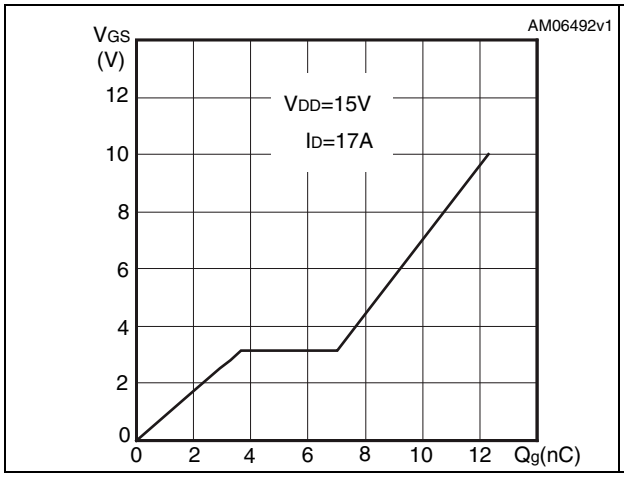


Figure 9. Capacitance variations

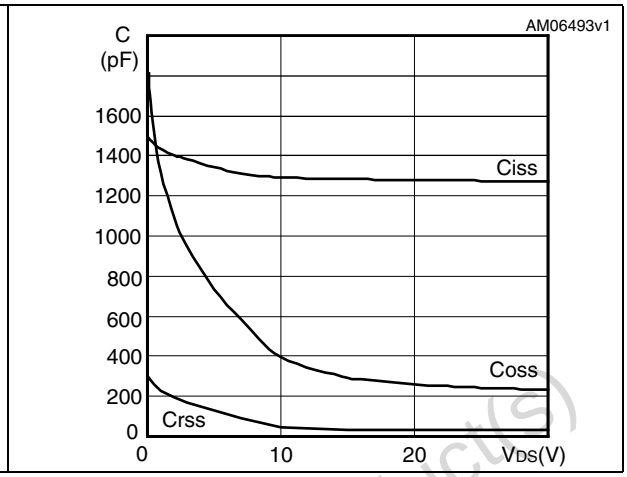


Figure 10. Normalized gate threshold voltage vs temperature

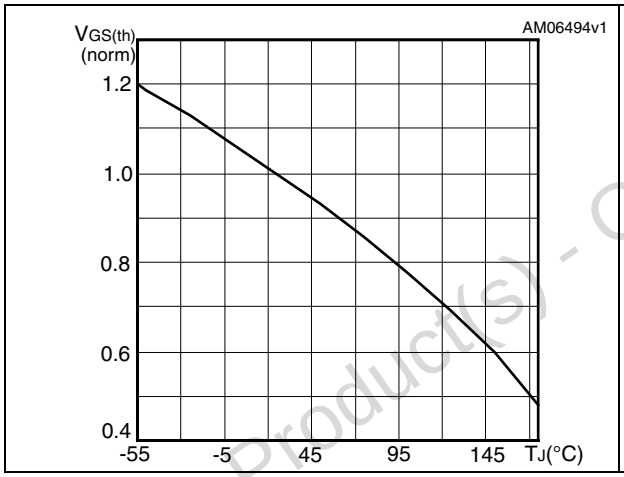


Figure 11. Normalized on-resistance vs temperature

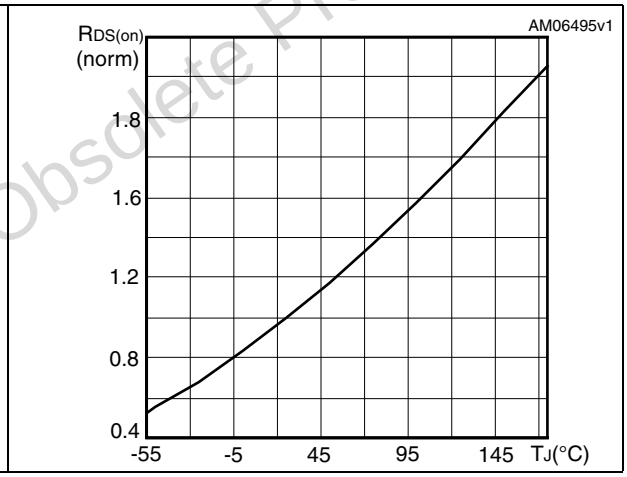
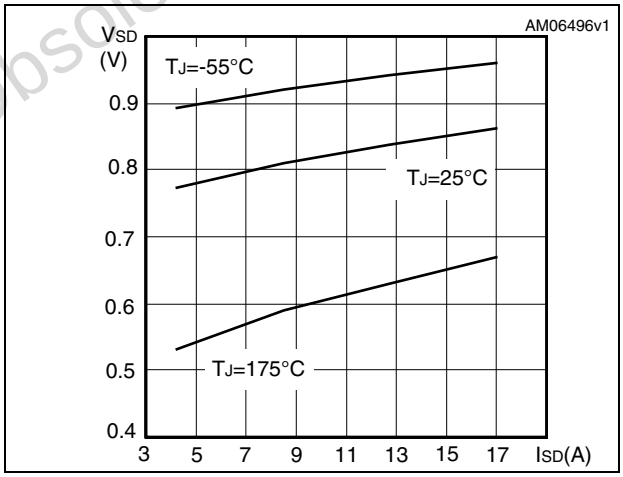


Figure 12. Source-drain diode forward characteristics



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3 Test circuits

Figure 13. Switching times test circuit for resistive load

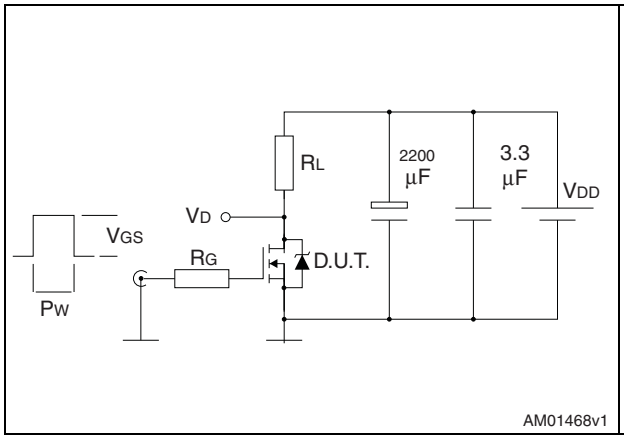


Figure 14. Gate charge test circuit

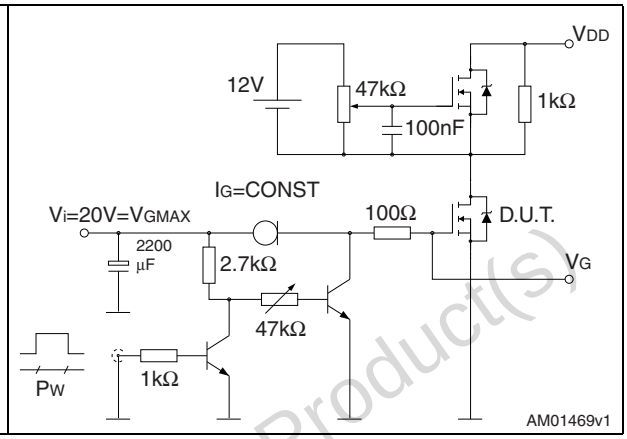


Figure 15. Test circuit for inductive load switching and diode recovery times

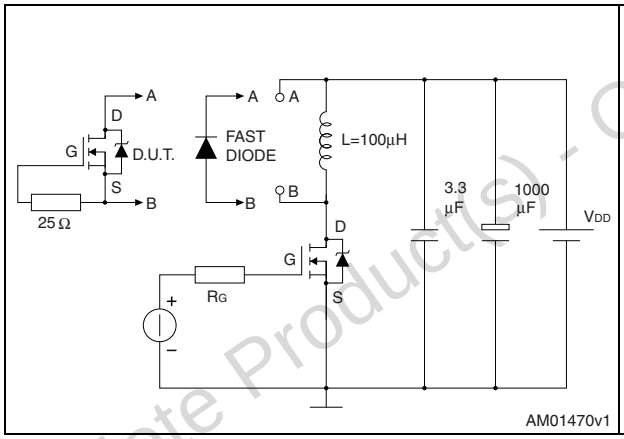


Figure 16. Unclamped inductive load test circuit

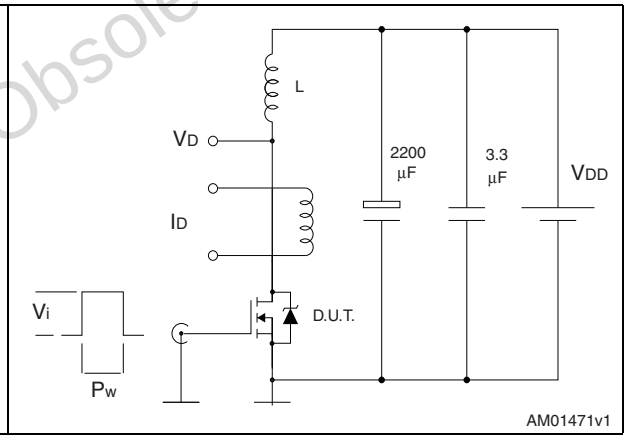


Figure 17. Unclamped inductive waveform

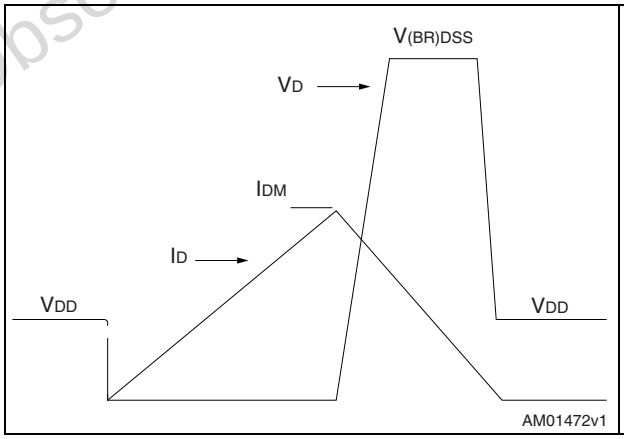
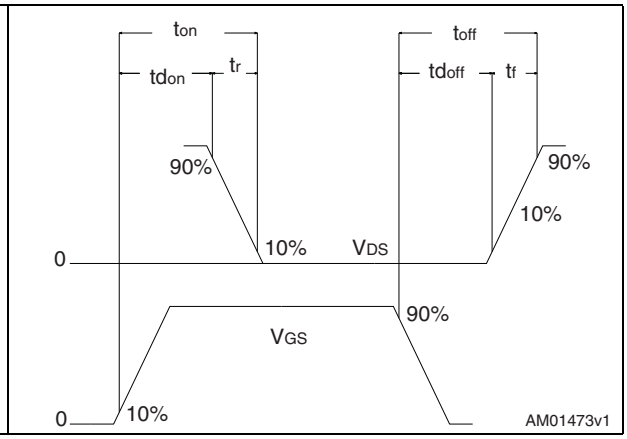


Figure 18. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

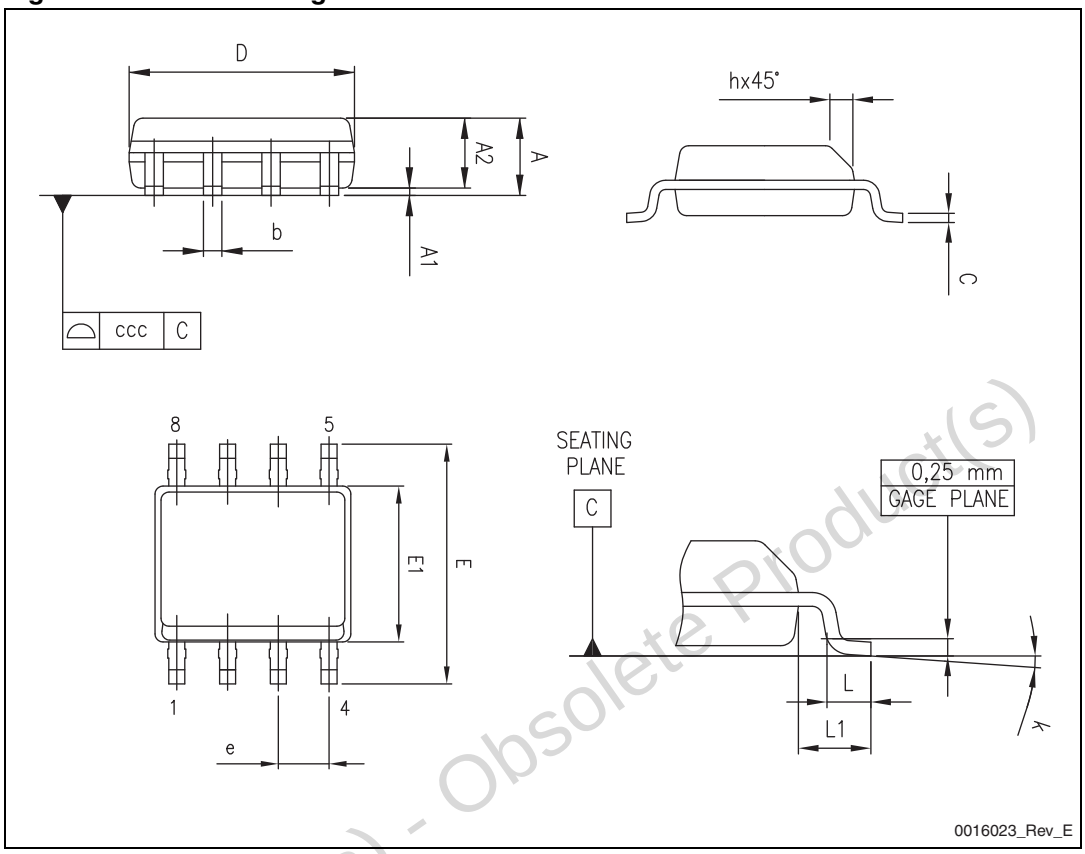
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Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

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Figure 19. SO-8 drawing



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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Feb-2010	1	First release.
01-Jul-2011	2	Datasheet status promoted from preliminary data to datasheet. Modified: *Table 2* and *4*.
07-Jun-2012	3	Updated mechanical data. Minor text changes.

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