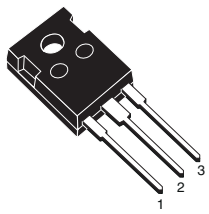
STW36NM60N

N-channel 600 V, 0.092 Ω, 29 A, MDmesh™ II Power MOSFET in TO-247

Features

Order code	V_{DSS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_W
STW36NM60N	650 V	< 0.105 Ω	29 A	210 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



TO-247

Application

- Switching applications
  - Automotive

Description

This device is made using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

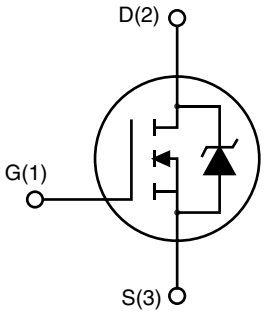


Table 1. Device summary

Order code	Marking	Package	Packaging
STW36NM60N	36NM60N	TO-247	Tape and reel

Contents

1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuits 8

4 Package mechanical data 9

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	29	A
I_D	Drain current (continuous) at T_C = 100 °C	18	A
I_{DM} (1)	Drain current (pulsed)	116	A
P_{TOT}	Total dissipation at T_C = 25 °C	210	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max.)	10.5	A
E_{AS}	Single pulse avalanche energy (Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.)	345	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating juncion temperature	150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 29$ A, di/dt $\leq$ 400 A/µs, V_{DS} peak $\leq V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.6	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	30	°C/W
T_l	Maximum lead temperature for soldering purposes	300	°C

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 14.5 A		0.092	0.105	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0	-	2722 173 1.75	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent Output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	458	-	pF
R_g	Gate input resistance	f =1MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	2.9	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 29 A, V_{GS} = 10 V *(see Figure 15)*	-	83.6 14 45	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 300 V, I_D = 14.5 A, R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 14)*	-	17 34 106 67	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		29 116	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 29 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD}= 60 V *(see Figure 19)*	-	408 8 39		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 29 A, di/dt = 100 A/µs V_{DD}= 60 V Tj = 150 °C *(see Figure 19)*	-	480 10 42		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

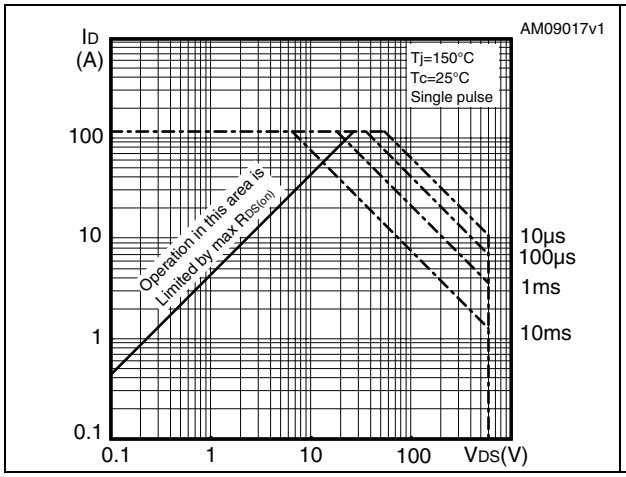


Figure 3. Thermal impedance

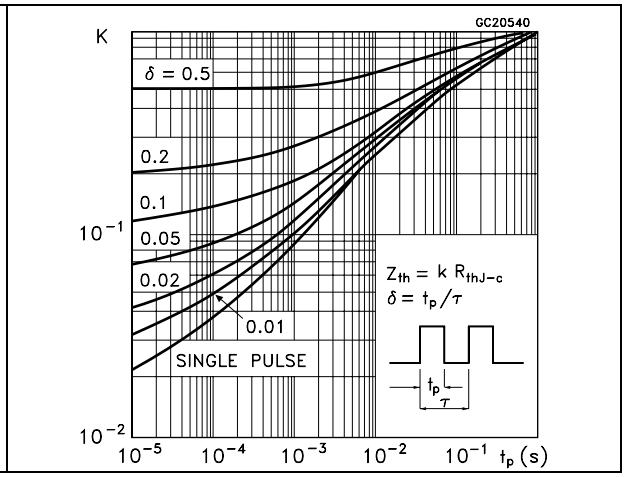


Figure 4. Output characteristics

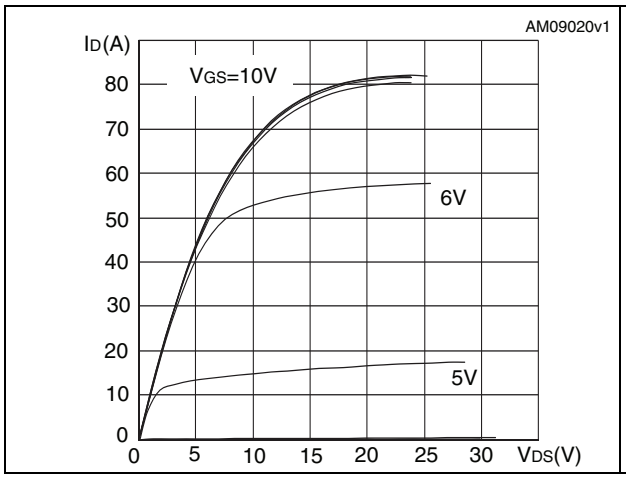


Figure 5. Transfer characteristics

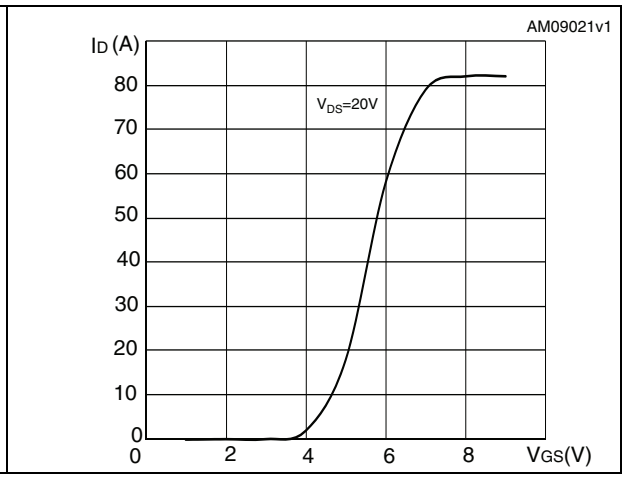


Figure 6. Gate charge vs gate-source voltage

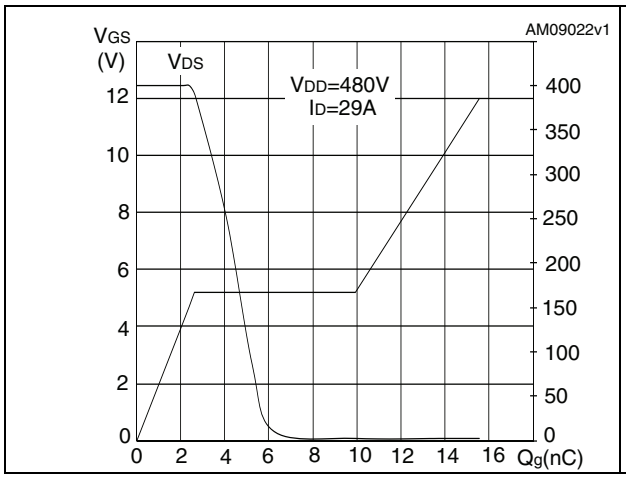


Figure 7. Static drain-source on resistance

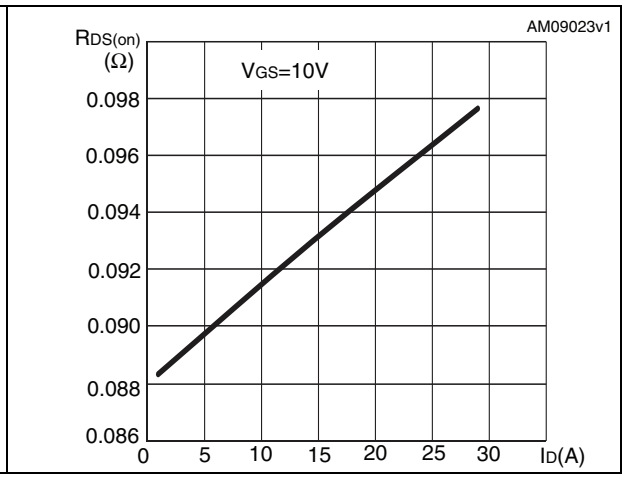


Figure 8. Capacitance variations

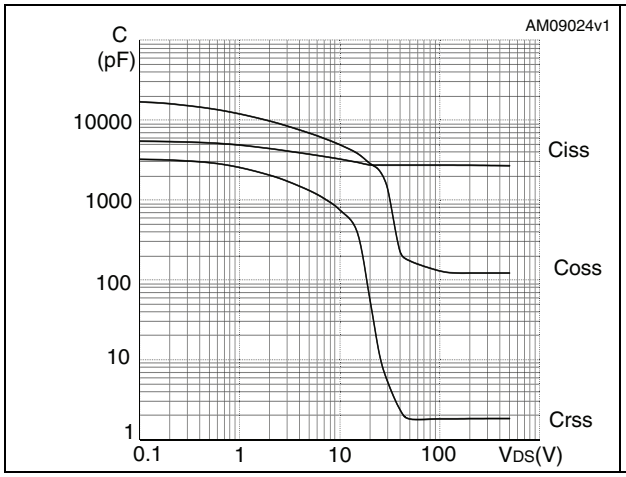


Figure 9. Output capacitance stored energy

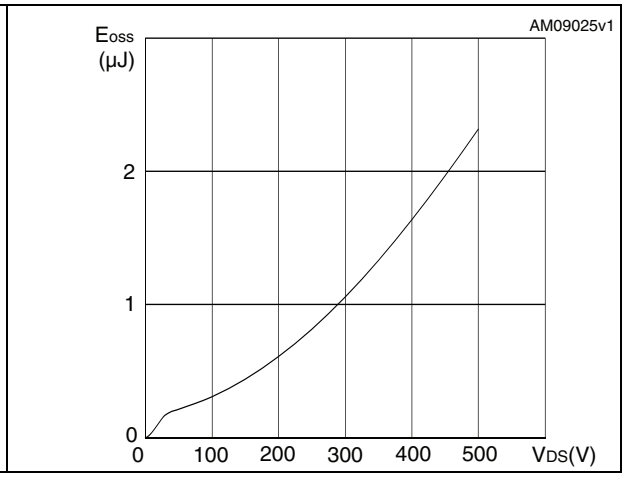


Figure 10. Normalized gate threshold voltage vs temperature

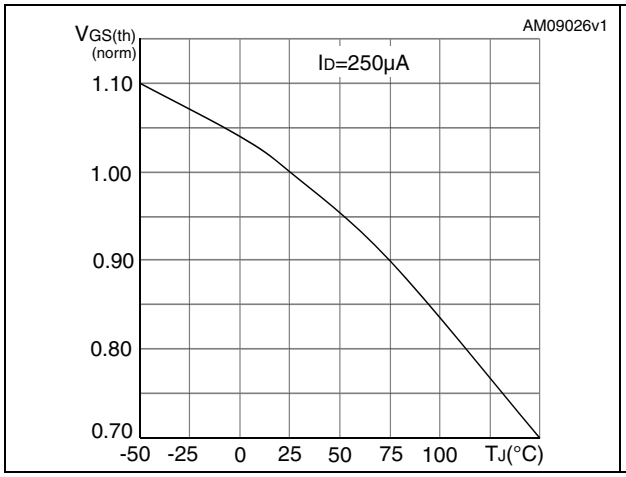


Figure 11. Normalized on resistance vs temperature

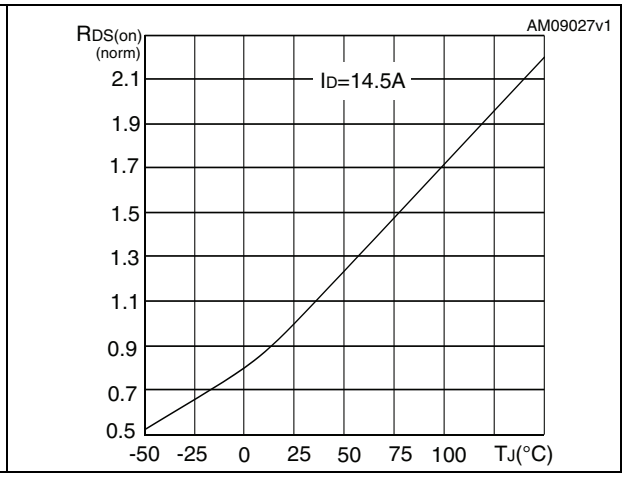


Figure 12. Normalized B_{VDSS} vs temperature

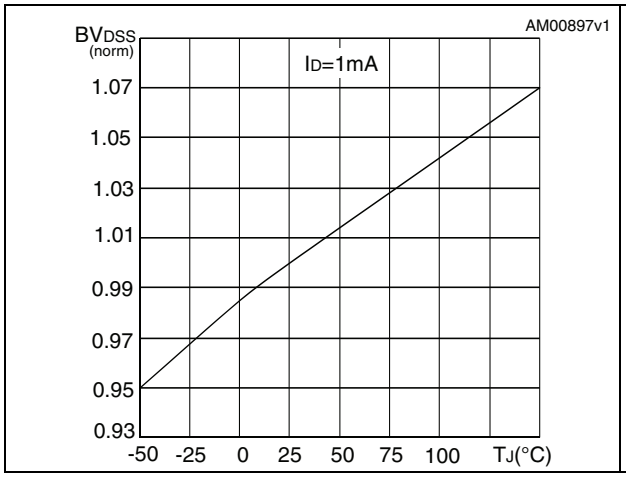
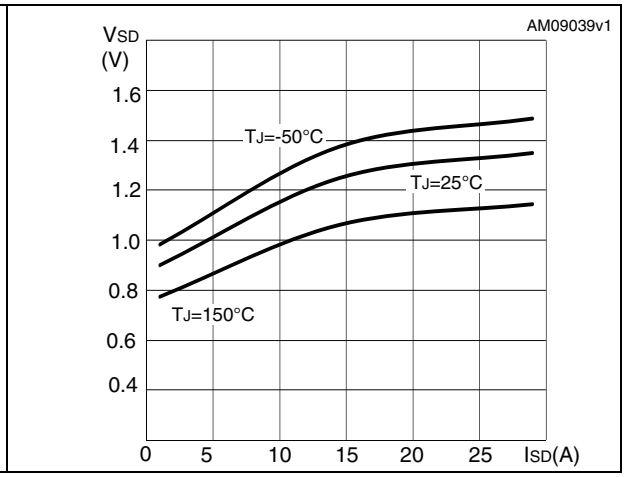


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

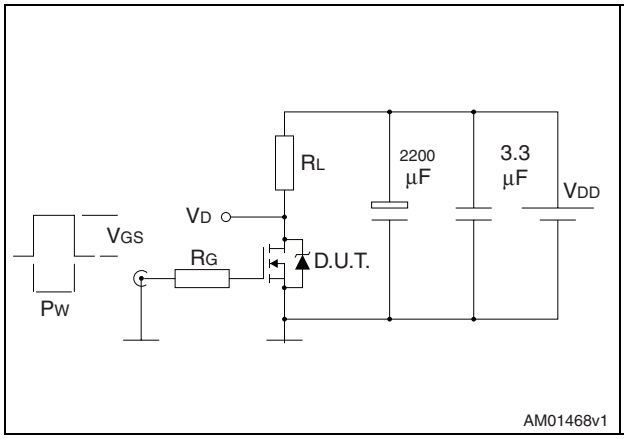


Figure 15. Gate charge test circuit

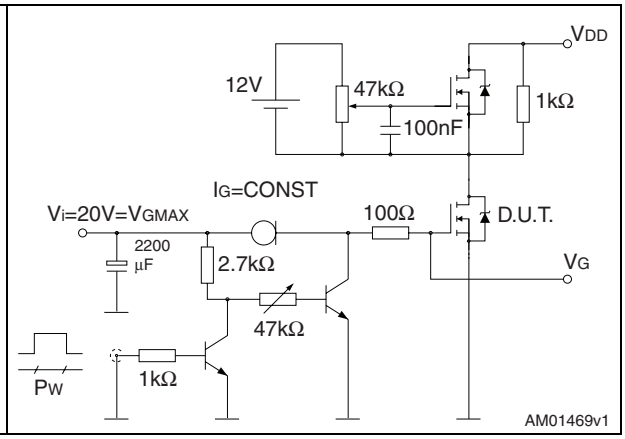


Figure 16. Test circuit for inductive load switching and diode recovery times

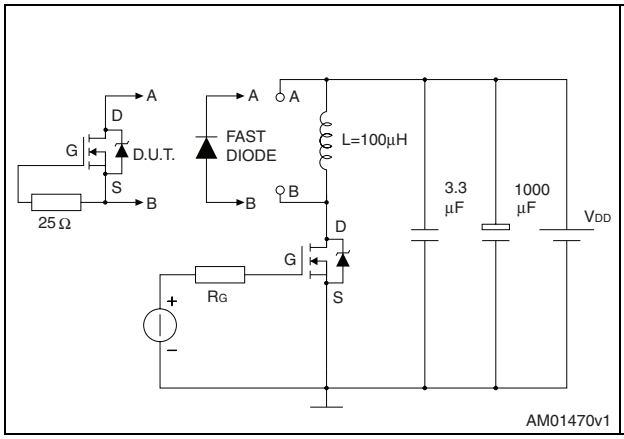


Figure 17. Unclamped inductive load test circuit

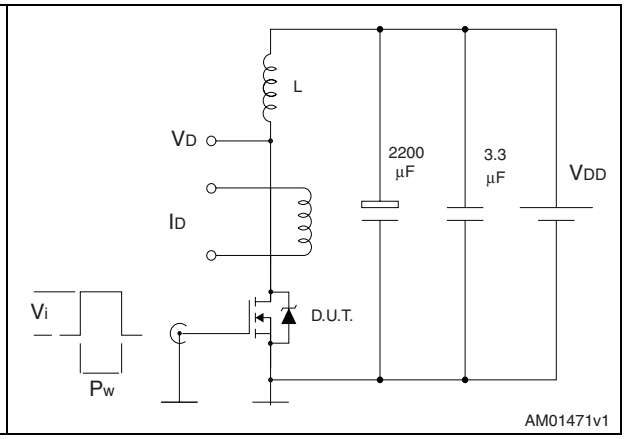


Figure 18. Unclamped inductive waveform

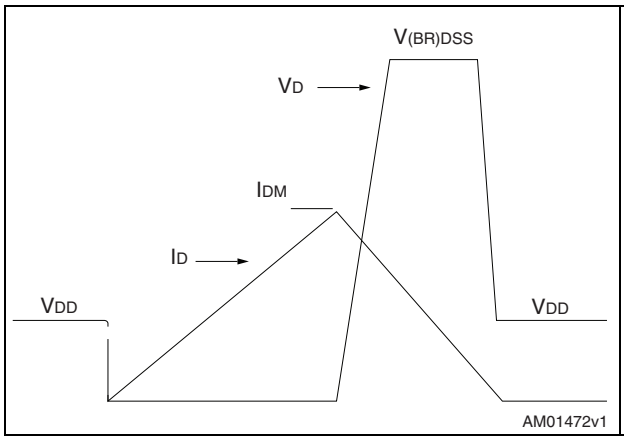
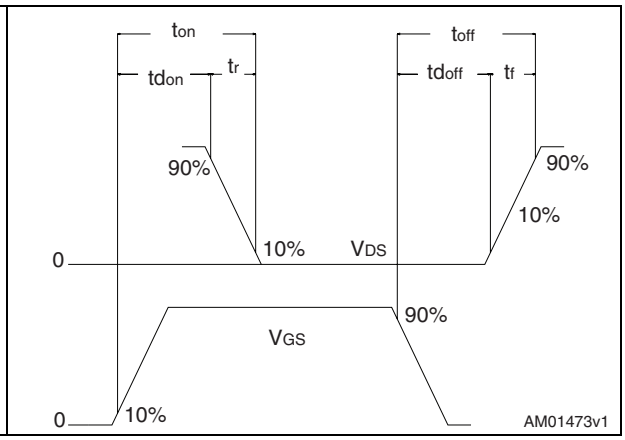


Figure 19. Switching time waveform



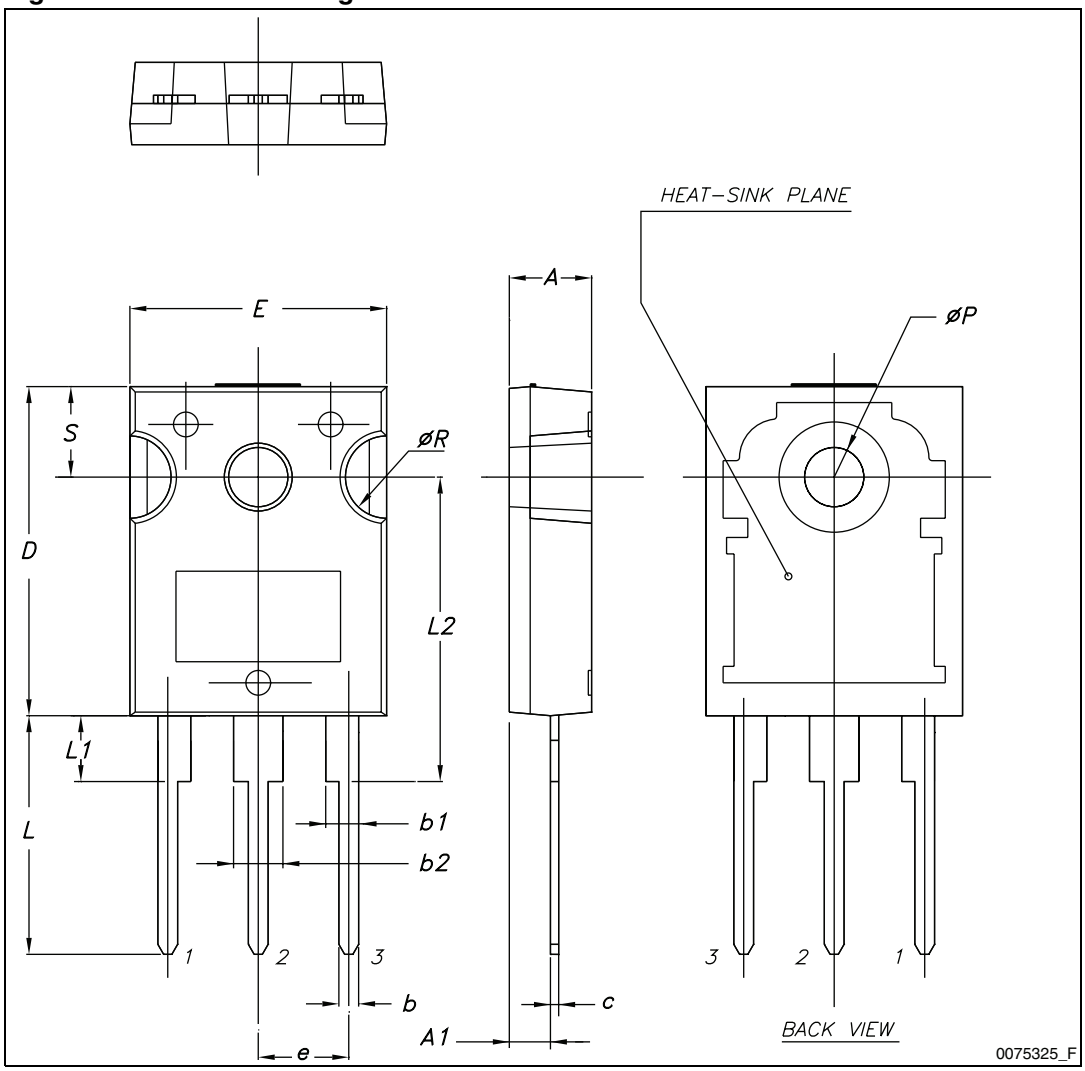
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 20. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jun-2011	1	First release.

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