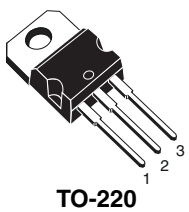
STP80NF06 - STB80NF06
STW80NF06

N-channel 60V - 0.0065Ω - 80A TO-220/D²PAK/TO-247
STripFET II™ Power MOSFET

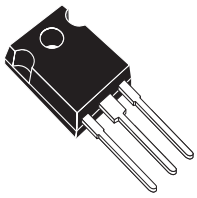
Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STB80NF06	60V	<0.008Ω	80A
STP80NF06	60V	<0.008Ω	80A
STW80NF06	60V	<0.008Ω	80A

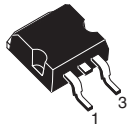
- 100% avalanche tested
- Low threshold drive



TO-220



TO-247

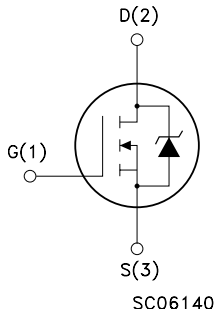


D²PAK

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STB80NF06T4	B80NF06	D²PAK	Tape & reel
STP80NF06	P80NF06	TO-220	Tube
STW80NF06	W80NF06	TO-247	Tube

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1 Electrical ratings 3

2 Electrical characteristics 4

2.1 Electrical characteristics (curves) 6

3 Test circuit 8

4 Package mechanical data 9

5 Revision history 13

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (v_{gs} = 0)	60	V
V_{GS}	Gate- source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C = 100°C	80	A
I_{DM} (2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25°C	300	W
	Derating factor	2	W/°C
E_{AS} (3)	Single pulse avalanche energy	870	mJ
T_{stg}	Storage temperature	– 65 to 175	°C
T_j	Max. operating junction temperature	175	

1. Current limited by wire bonding
2. Pulse width limited by safe operating area
3. Starting T_j= 25°C, I_D= 40A, V_{DD}=40V

Table 2. Thermal data

$R_{thj\text{-}case}$	Thermal resistance junction-case Max	0.5	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient Max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating			1	µA
		V_{DS}=Max rating, T_C=125°C			10	µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 40A		0.0065	0.008	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 2.5V, I_D=18A		20		S
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		3850		pF
C_{oss}	Output capacitance			800		pF
C_{rss}	Reverse transfer capacitance			250		pF
Q_g	Total gate charge	V_{DD} = 80V, I_D = 80A, V_{GS} = 10V		115	150	nC
Q_{gs}	Gate-source charge			24		nC
Q_{gd}	Gate-drain charge			46		nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 27V, I_D = 40A R_G = 4.7Ω V_{GS} = 10V (see Figure 13)		25		ns
t_r	Rise time			85		ns
$t_{d(off)}$	Turn-off-delay time	V_{DD} = 27V, I_D = 40A, R_G = 4.7Ω, V_{GS} = 10V (see Figure 13)		70		ns
t_f	Fall time			25		ns
$t_{d(off)}$	Off-voltage Rise Time	Vclamp =44V, I_D =80A R_G = 4.7Ω, V_{GS} = 10V (see Figure 15)		85		ns
t_f	Fall Time			75		ns
t_c	Cross-over Time			110		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				80	A
I_{SDM} (1)	Source-drain current (pulsed)				320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 80A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80A, V_{DD} = 50V di/dt = 100A/µs, T_j = 150°C (see Figure 15)		80 250 6.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

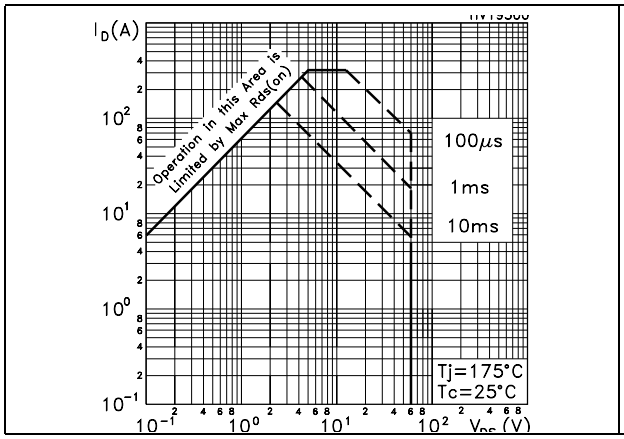


Figure 2. Thermal impedance

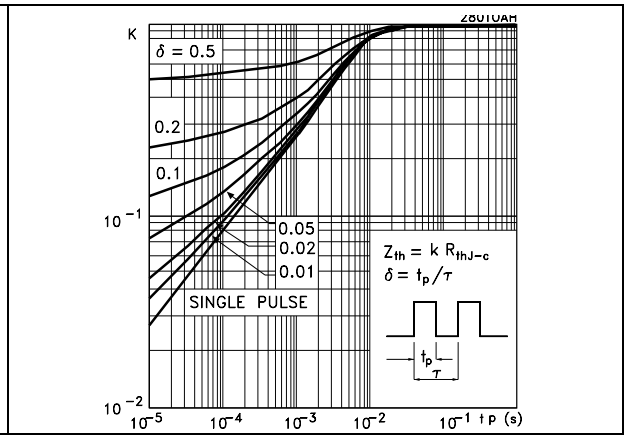


Figure 3. Output characteristics

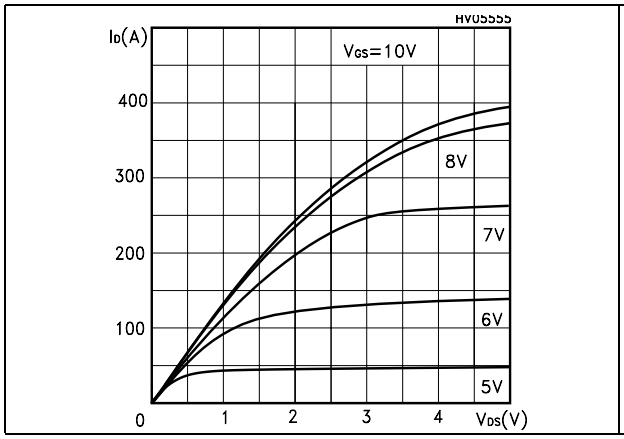


Figure 4. Transfer characteristics

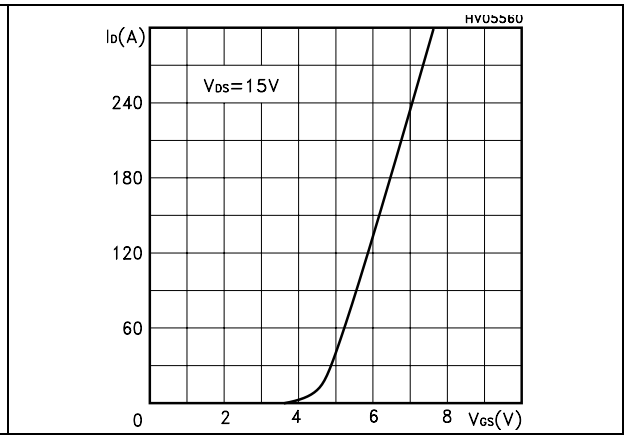


Figure 5. Transconductance

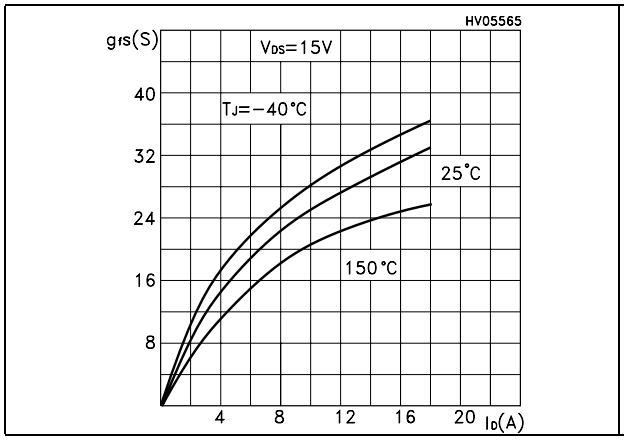


Figure 6. Static drain-source on resistance

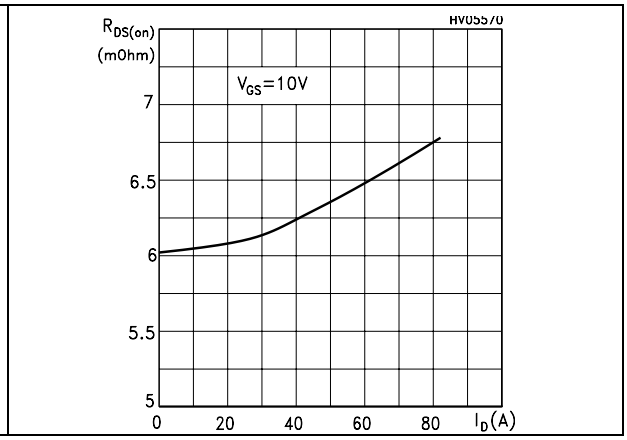


Figure 7. Gate charge vs. gate-source voltage

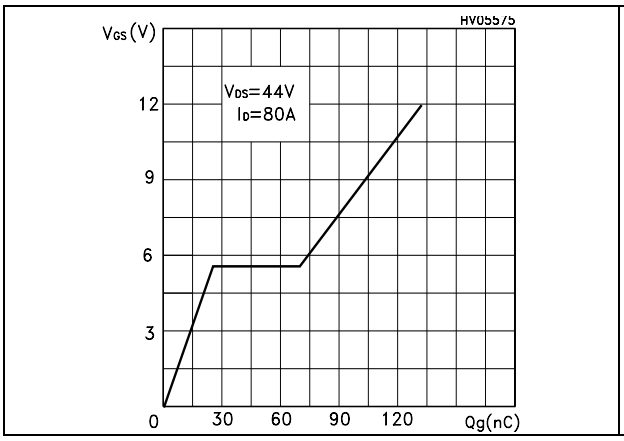


Figure 8. Capacitance variations

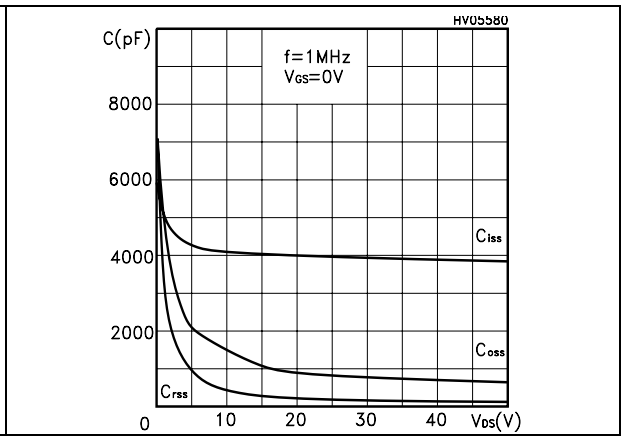


Figure 9. Normalized gate threshold voltage vs. temperature

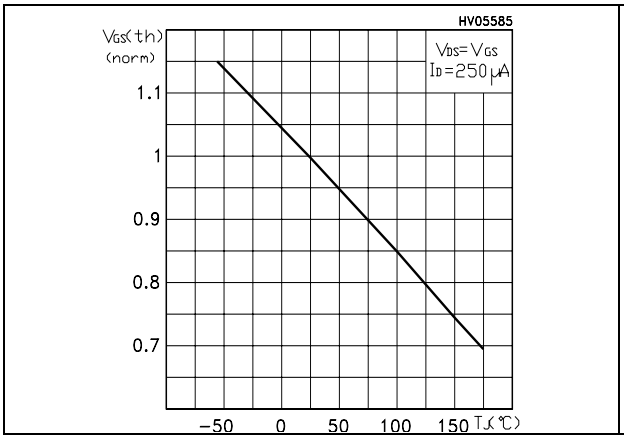


Figure 10. Normalized on resistance vs. temperature

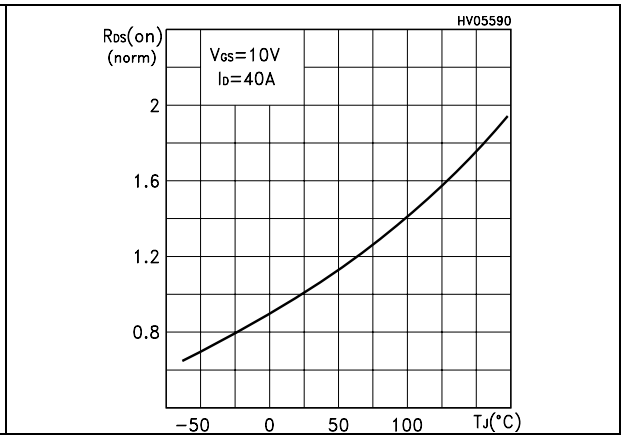


Figure 11. Source-drain diode forward characteristics

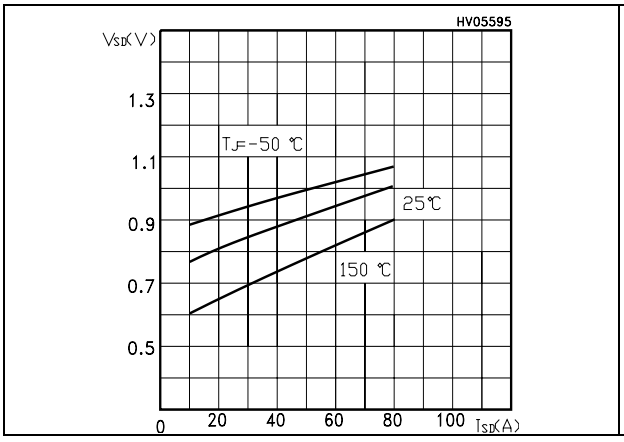
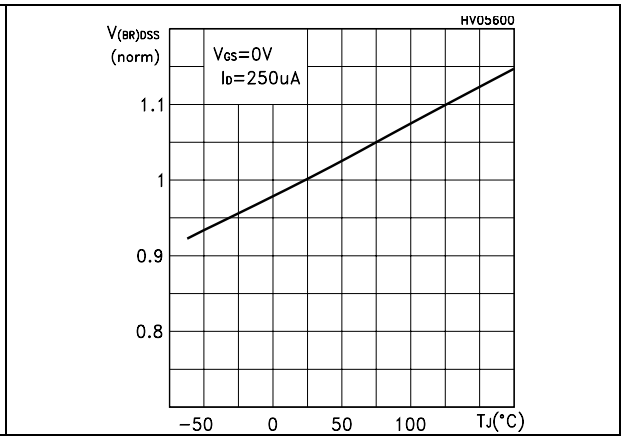


Figure 12. Normalized breakdown voltage vs. tj



3 Test circuit

Figure 13. Switching times test circuit for resistive load

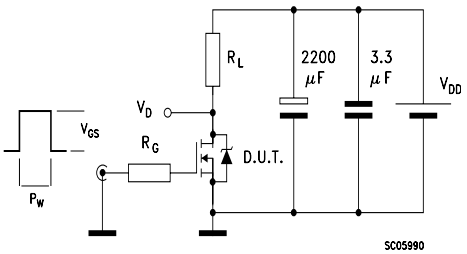


Figure 14. Gate charge test circuit

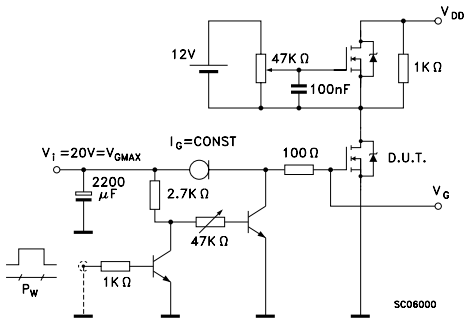


Figure 15. Test circuit for inductive load switching and diode recovery times

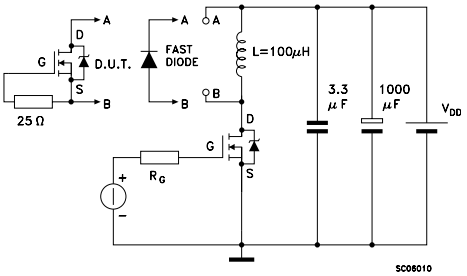


Figure 16. Unclamped Inductive load test circuit

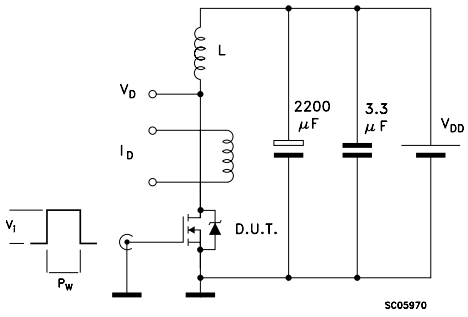


Figure 17. Unclamped inductive waveform

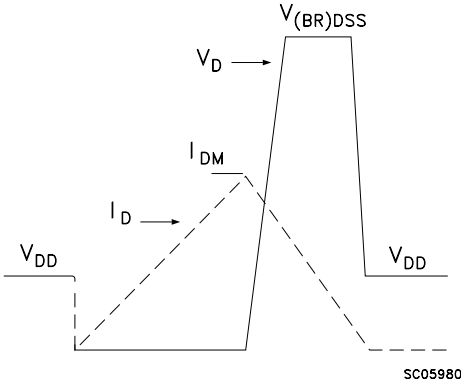
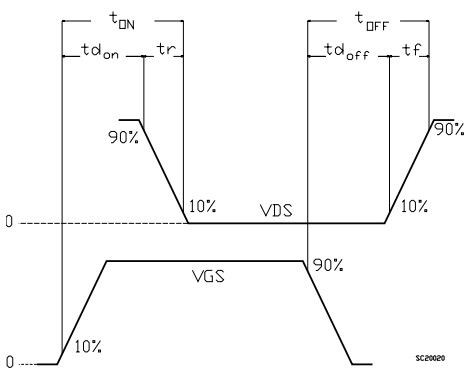


Figure 18. Switching time waveform

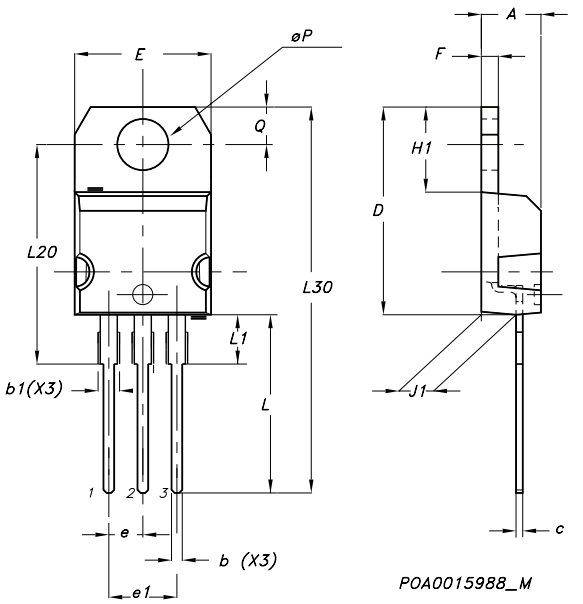


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

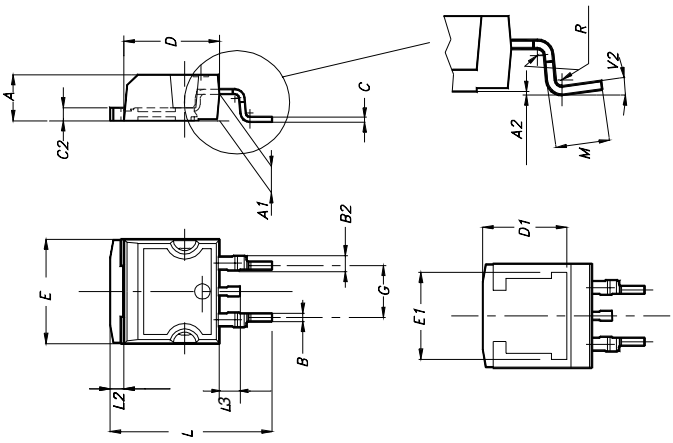
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



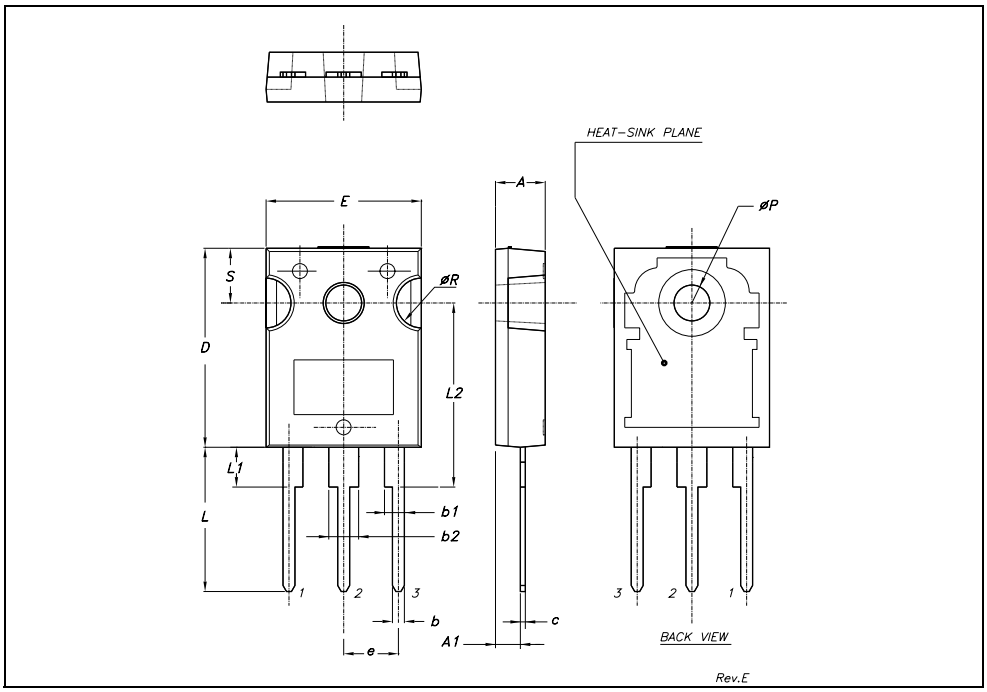
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	1	Complete version
21-Jun-2005	2	The word "STripFET" in the description title on the web was been corrected
17-Aug-2006	3	The document has been reformatted
31-Jan-2007	4	Typo mistake on *Table 1*.
03-May-2007	5	$R_{DS(on)}$ Max value has been changed

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