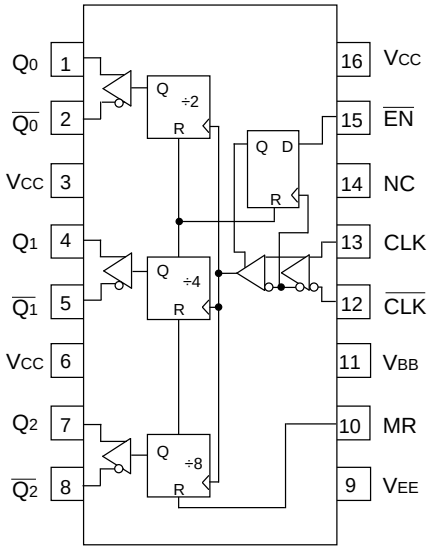
5V/3.3V ÷2, ÷4, ÷8 CLOCK GENERATION CHIP

- **3.3V and 5V power supply options**
- **50ps output-to-output skew**
- **Synchronous enable/disable**
- **Master Reset for synchronization**
- **Internal 75KΩ input pull-down resistors**
- **Available in 16-pin SOIC package**



TOP VIEW

÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL34/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34/Ls in a system.

Pin	Function
CLK	Differential Clock Inputs
$\overline{EN}$	Synchronous Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0	Differential ÷2 Outputs
Q_1	Differential ÷4 Outputs
Q_2	Differential ÷8 Outputs

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Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–2}$
X	X	H	Reset $Q_{0–2}$

NOTE:
Z = LOW-to-HIGH transition
ZZ = HIGH-to-LOW transition

EE = VEE (Min.) to VEE (Max.); VCC = GND

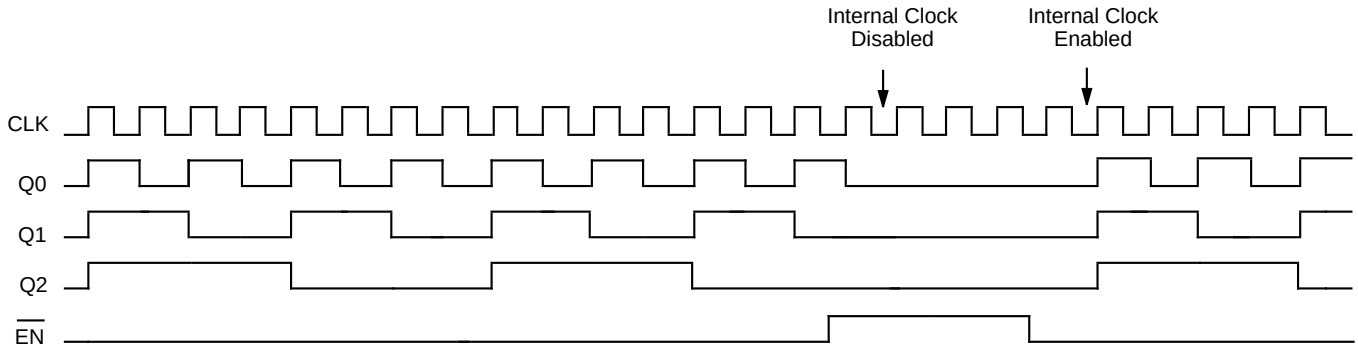
Symbol	Parameter		T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{EE}	Power Supply Current	10EL	—	—	49	—	—	49	—	—	49	—	—	49	mA
		100EL	—	—	49	—	—	49	—	—	49	—	—	54	
V_{BB}	Output Reference Voltage	10EL	–1.43	—	–1.30	–1.38	—	–1.27	–1.35	—	–1.25	–1.31	—	–1.19	V
		100EL	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	–1.38	—	–1.26	
I_{IH}	Input High Current		—	—	150	—	—	150	—	—	150	—	—	150	µA

NOTE:
1. Parametric values specified at: 5 volt Power Supply Range 100EL34 Series: -4.2V to -5.5V.
   10EL34 Series -4.75V to -5.5V.
   3 volt Power Supply Range 10/100EL34L Series: -3.0V to -3.8V.

VEE = VEE (Min.) to VEE (Max.); VCC = GND

Symbol	Parameter		T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK	960	1100	1200	960	1100	1200	960	1100	1200	960	1100	1200	ps
		MR	650	800	1010	650	800	1010	650	800	1010	650	800	1010	
t_{skew}	Within-Device Skew[2]		—	—	50	—	—	50	—	—	50	—	—	50	ps
t_S	Set-up Time $\overline{EN}$		400	—	—	400	—	—	400	—	—	400	—	—	ps
t_H	Hold Time $\overline{EN}$		200	—	—	200	—	—	200	—	—	200	—	—	ps
V_{PP}	Minimum Input Swing[3]		250	—	—	250	—	—	250	—	—	250	—	—	mV
V_{CMR}	Common Mode Range[4]		–1.3	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	–1.4	—	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)		275	400	525	275	400	525	275	400	525	275	400	525	ps

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   3 volt Power Supply Range 10/100EL34L Series: -3.0V to -3.8V.
2. Skew is measured between outputs under identical transitions.
3. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
4. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V – IV_{CMR} (min)I.



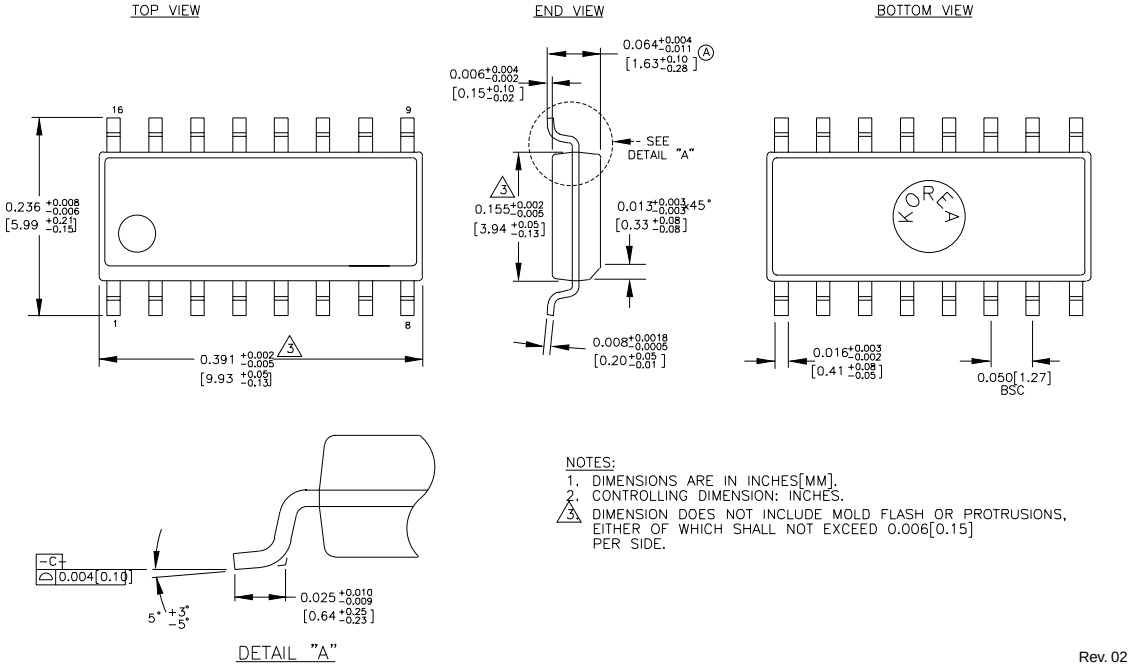
rnal dividers will maintain their state during the internal clock freeze and will return to clocking once the internal clocks are unfrozen. The outputs will transition to their next states in the same manner, time and relationship as they would have had the $\overline{EN}$ signal not been asserted.

3.3V

Ordering Code	Package Type	Operating Range	V_{EE} Range (V)
SY10EL34LZC	Z16-2	Commercial	-3.0 to -3.8
SY10EL34LZCTR	Z16-2	Commercial	-3.0 to -3.8
SY100EL34LZC	Z16-2	Commercial	-3.0 to -3.8
SY100EL34LZCTR	Z16-2	Commercial	-3.0 to -3.8

5V

Code	Type	Range	$_{EE}$ Range (V)
SY10EL34ZC	Z16-2	Commercial	-4.75 to -5.5
SY10EL34ZCTR	Z16-2	Commercial	-4.75 to -5.5
SY100EL34ZC	Z16-2	Commercial	-4.2 to -5.5
SY100EL34ZCTR	Z16-2	Commercial	-4.2 to -5.5



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Rev. 02

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