

3.3V ECL $\div 4$ Divider

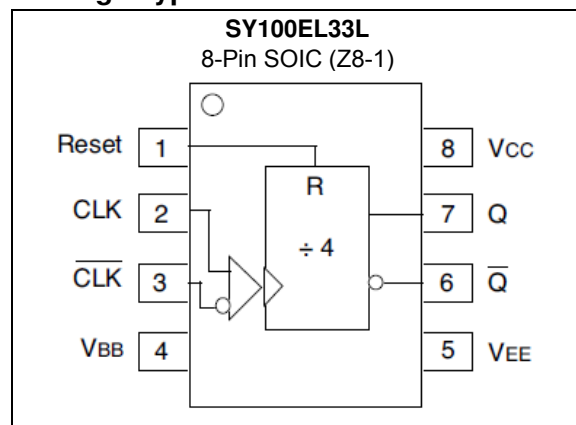
Features

- 3.3V Power Supply
- 640ps Propagation Delay (typical)
- 4.2 GHz Toggle Frequency (typical)
- High Bandwidth Output Transitions
- Internal 75 k Ω Input Pull-Down Resistors
- Available in 8-Pin SOIC Package

General Description

The SY100EL33L is an integrated $\div 4$ divider. The differential clock inputs and the V_{BB} allow a differential, single-ended or AC-coupled interface to the device. If used, the V_{BB} output should be bypassed to ground with a 0.01 μ F capacitor. Also note that the V_{BB} is designed to be used as an input bias on the EL33L only; the V_{BB} output has limited current sink and source capability. The Reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the Reset input allows for the synchronization of multiple EL33Ls in a system.

Package Type



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1).....	+8V
NECL Power Supply Voltage (V_{EE}) (Note 2).....	-8V
PECL Mode Input Voltage (V_{IN}) (Note 3).....	+6V
NECL Mode Input Voltage (V_{IN}) (Note 4).....	-6V
Continuous Output Current (I_{OUT}).....	50mA
Surge Output Current (I_{OUT}).....	100mA

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $V_{EE} = 0V$

2: $V_{CC} = 0V$

3: $V_{EE} = 0V$, $V_{IN} \leq V_{CC}$

4: $V_{CC} = 0V$, $V_{IN} \geq V_{EE}$

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics PECL: $V_{CC} = 3.0V$ to $3.8V$; $V_{EE} = 0V$; $T_A = -40^{\circ}C$ to $85^{\circ}C$, unless otherwise stated (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Power Supply Voltage	V_{CC}	3.0	3.3	3.8	V	
Power Supply Current	I_{EE}	—	27	33	mA	$T_A = -40^{\circ}C$ to $+25^{\circ}C$
		—	31	37		$T_A = +85^{\circ}C$
Output High Voltage (Note 2)	V_{OH}	$V_{CC} - 1.085$	$V_{CC} - 1.005$	$V_{CC} - 0.88$	V	$T_A = -40^{\circ}C$
		$V_{CC} - 1.025$	$V_{CC} - 0.955$	$V_{CC} - 0.88$		$T_A = 0^{\circ}C$ to $85^{\circ}C$
Output Low Voltage (Note 2)	V_{OL}	$V_{CC} - 1.830$	$V_{CC} - 1.695$	$V_{CC} - 1.555$	V	$T_A = -40^{\circ}C$
		$V_{CC} - 1.810$	$V_{CC} - 1.705$	$V_{CC} - 1.620$		$T_A = 0^{\circ}C$ to $85^{\circ}C$
Input High Voltage (Single Ended)	V_{IH}	$V_{CC} - 1.165$	—	$V_{CC} - 0.880$	V	
Input Low Voltage (Single Ended)	V_{IL}	$V_{CC} - 1.810$	—	$V_{CC} - 1.475$	V	
Output Reference Voltage	V_{BB}	$V_{CC} - 1.38$	—	$V_{CC} - 1.26$	V	
Input High Current	I_{IH}	—	—	150	μA	
Input Low Current	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL}$ (Min)

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2: Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0V$.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS**Electrical Characteristics NECL:** VEE = -3.8V to -3.0V; VCC = 0V; TA = -40°C to 85°C, unless otherwise stated (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Power Supply Voltage	VEE	-3.8	-3.3	-3	V	
Power Supply Current	IEE	—	27	33	mA	TA = -40°C to +25°C
		—	31	37		TA = +85°C
Output High Voltage (Note 2)	VOH	-1.085	-1.005	-0.88	V	TA = -40°C
		-1.025	-0.955	-0.88		TA = 0°C to 85°C
Output Low Voltage (Note 2)	VOL	-1.830	-1.695	-1.555	V	TA = -40°C
		-1.810	-1.705	-1.620		TA = 0°C to 85°C
Input High Voltage (Single Ended)	VIH	-1.165	—	-0.880	V	
Input Low Voltage (Single Ended)	VIL	-1.810	—	-1.475	V	
Output Reference Voltage	VBB	-1.380	—	-1.260	V	
Input High Current	IIH	—	—	150	μA	
Input Low Current	IIL	0.5	—	—	μA	VIN = VIL (Min)

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

2: Outputs are terminated through a 50 Ω resistor to VCC – 2.0V.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS⁽¹⁾**Electrical Characteristics:** VCC = 3.0V to 3.8V; VEE = 0V or VEE = -3.8V to -3.0V; VCC = 0V; TA = -40°C to 85°C, unless otherwise stated

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Condition
Maximum Toggle Frequency	f _{MAX}	3.8	4.2	—	GHz	
Prop. Delay CLK to Q	t _{PD}	490	630	770	ps	TA = -40°C
		540	630	720	ps	TA = 0°C
		550	640	730	ps	TA = +25°C
		590	670	760	ps	TA = +85°C
Propagation Delay RESET to Q	t _{PD}	310	460	610	ps	TA = -40°C
		360	460	560	ps	TA = 0°C to +25°C
		380	480	580	ps	TA = +85°C
Input Swing (Note 1)	V _{PP}	100	—	1000	mV	
Output Rise/Fall Time Q (20% to 80%)	t _r /t _f	100	225	350	ps	

Note 1: Input swing for which AC parameters are ensured.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T _A	-40	—	+85	°C	—
Storage Temperature	T _S	-65	—	+150	°C	—
Lead Temperature	T _{LEAD}	—	—	+260	°C	Soldering, 20 sec.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Reset	Asynchronous Reset
2, 3	CLK, /CLK	Clock Inputs
4	V _{BB}	Reference Voltage Output
5	V _{EE}	Negative Power Supply
6, 7	Q, /Q	Data Outputs
8	V _{CC}	Positive Power Supply

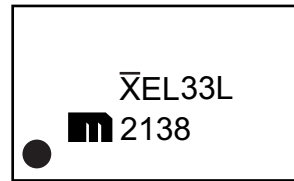
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

8-Lead SOIC*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

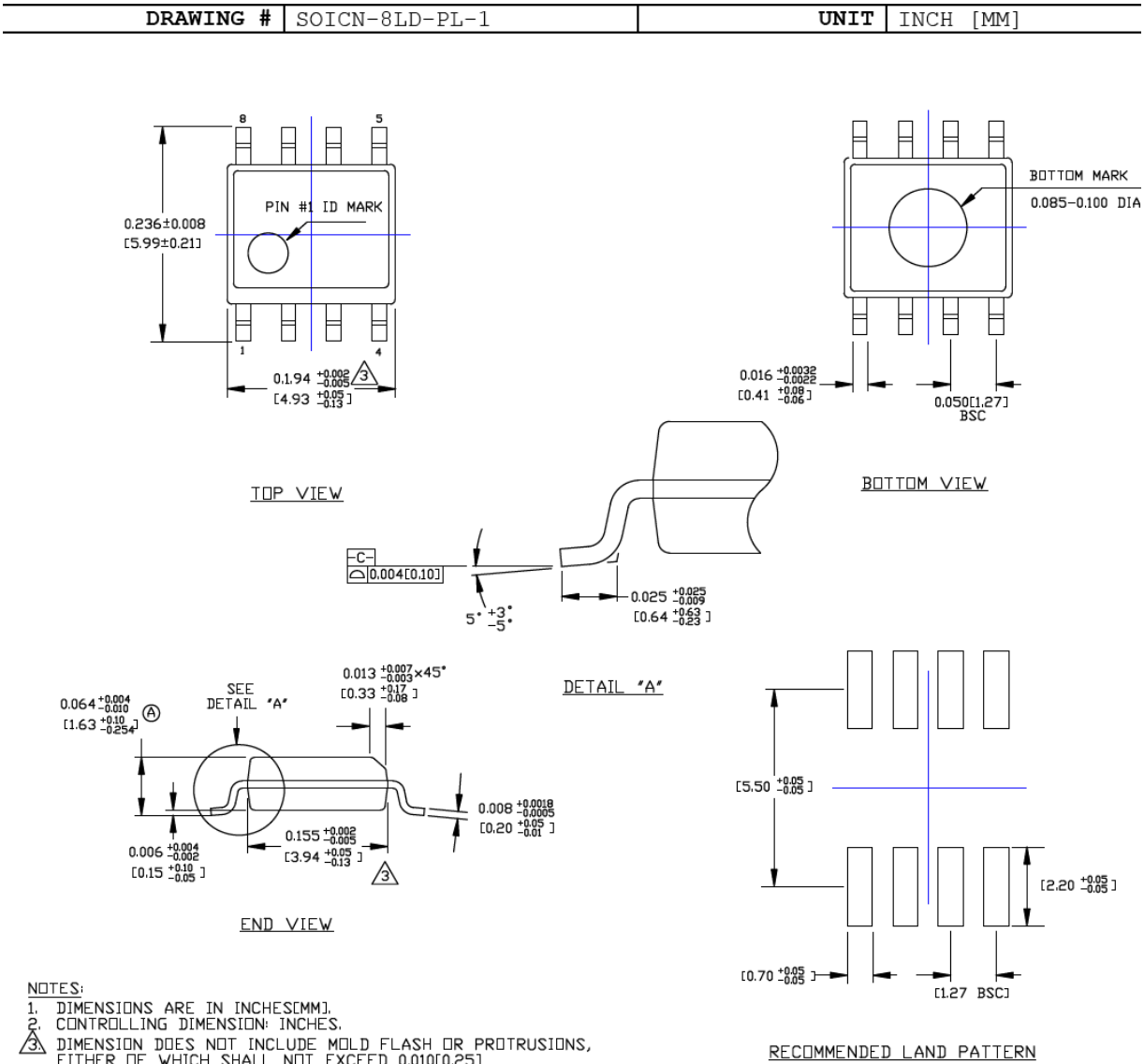
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (¯) and/or Overbar (¯) symbol may not be to scale.

8-Lead SOIC Package Outline and Recommended Land Pattern

TITLE

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>		X	X	-XX
Device		Package	Temperature Range	Special Processing
Device: 3.3V ÷ 4 Divider SY100EL33L				
Package Z = 8-Lead SOIC				
Temperature Range: G = -40°C to +85°C (Pb-Free NiPdAu)				
Special Processing: <blank>= 95/Tube TR = 1,000/Reel				
Note 1: Contact factory for die availability. Dice are ensured at T _A = 25°C, DC Electricals only. 2: Tape and Reel. 3: Pb-Free package is recommended for new designs.				

Examples:

a) SY100EL33LZG⁽³⁾ 8-Lead SOIC (Z8-1) package, -40°C to +85°C Industrial Temp. (Pb-Free NiPdAu), 95/Tube

b) SY100EL33LZG-TR^(2,3) 8-Lead SOIC (Z8-1) package, -40°C to +85°C Industrial Temp. (Pb-Free NiPdAu), 1,000/Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

APPENDIX A: REVISION HISTORY

Revision A (September 2018)

- Converted Micrel document SY100EL33L to Microchip data sheet DS20006076A.
- Minor text changes throughout.
- Removed all reference to the EOL SY10EL33 and SY100EL33 versions.

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