Si3471 Data Sheet

Autonomous Single Ethernet Port IEEE 802.3bt PoE PSE Device

The Si3471 is a fully autonomous Power over Ethernet (PoE) Power Sourcing Equipment (PSE) device. It is fully IEEE 802.3bt compliant and compatible with IEEE 802.3af and 802.3at. It is optimized for use in PSE mid-spans and injectors that do not require a host or MCU. The Si3471 integrates one Ethernet port with the IEEE-required powered device (PD) detection and classification functionality. In addition, it features powered device (PD) disconnect using dc sense algorithms and a robust multipoint detection algorithm. Intelligent protection circuitry includes input undervoltage detection, output current limit, and short-circuit protection. The Si3471 works autonomously and does not require a host or MCU to program it. The Si3471 is programmed for maximum available power by pulling its configration pins high or low.

Applications

- IEEE 802.3af, 802.3at, and 802.3bt Power Sourcing Equipment (PSE)
- Power over Ethernet Injectors
- Single Port Mid-Spans
- Power over Ethernet Switches
- IP Phone Systems
- Smartgrid Switches
- Ruggedized and Industrial Switches

KEY FEATURES

- Single Ethernet port PoE Power Sourcing Equipment (PSE) device
- IEEE 802.3bt compliant
- IEEE 802.3af and 802.3at compatible
- Multi-point detection
- Comprehensive fault protection circuitry includes:
  - Power undervoltage lockout
  - Output current limit and short-circuit protection
  - Thermal overload detection
- Operating temp range: –40 °C to +85 °C
- 38-pin 5 x 7 mm QFN package (RoHS-compliant)

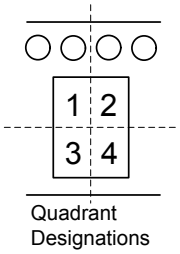
1. Ordering Guide

Table 1.1. Si3471 Ordering Guide

Ordering Part Number[1]	Product Revision	Package	Temperature Range (Ambient)
Si3471A-A02-IM	A02	38-pin, 5 x 7 mm QFN RoHS-compliant[2]	–40 to 85 °C

Note:

1. Add an “R” to the end of the part number for tape and reel option (e.g., Si3471A-A01-IM or Si3471A-A01-IMR).
2. Pin 1 is oriented in Quadrant 1 in the tape:



Quadrant Designations

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2. Summary of Operation

The Si3471 operates autonomously, without any external host or MCU control. All power on reset and brownout reset circuitry is internal. Upon V_{DD} and V_{DDA} being applied, an internal pull up sets the RESETb pin high, releasing the Si3471 from reset. The Si3471 then reads the PWRAVL pins and configures itself to grant the maximum class set by the PWRAVL pins. The multi-point detection algorithm runs until a valid PoE PD signature is detected and then proceeds with classification. If the Si3471 is configured to grant the class the PD requests, it internally sets the current limit to the class requested by the PD and proceeds to grant power. Otherwise, the Si3471 follows the IEEE 802.3bt specification for power demotion. The Si3471 automatically detects when a PD disconnects and restarts the detection process, continuously looking for a valid detection signature. If any error or fault condition occurs, the Si3471 removes power from the PD and automatically restarts the detection process.

The Si3471 includes an LED pin for driving a status indicator LED. If a status LED is not used, then the pin can be left floating. The LED operation is shown in the table below and is not configurable.

Table 2.1. LED Operation

LED Indication	Status
LED on, no blinking	Port successfully powered at requested power level
LED blinking slowly	Looking for a valid detection signature
LED blinking quickly	Error condition, such as port overload or loss of V_{PWR}

3. Typical Application Example

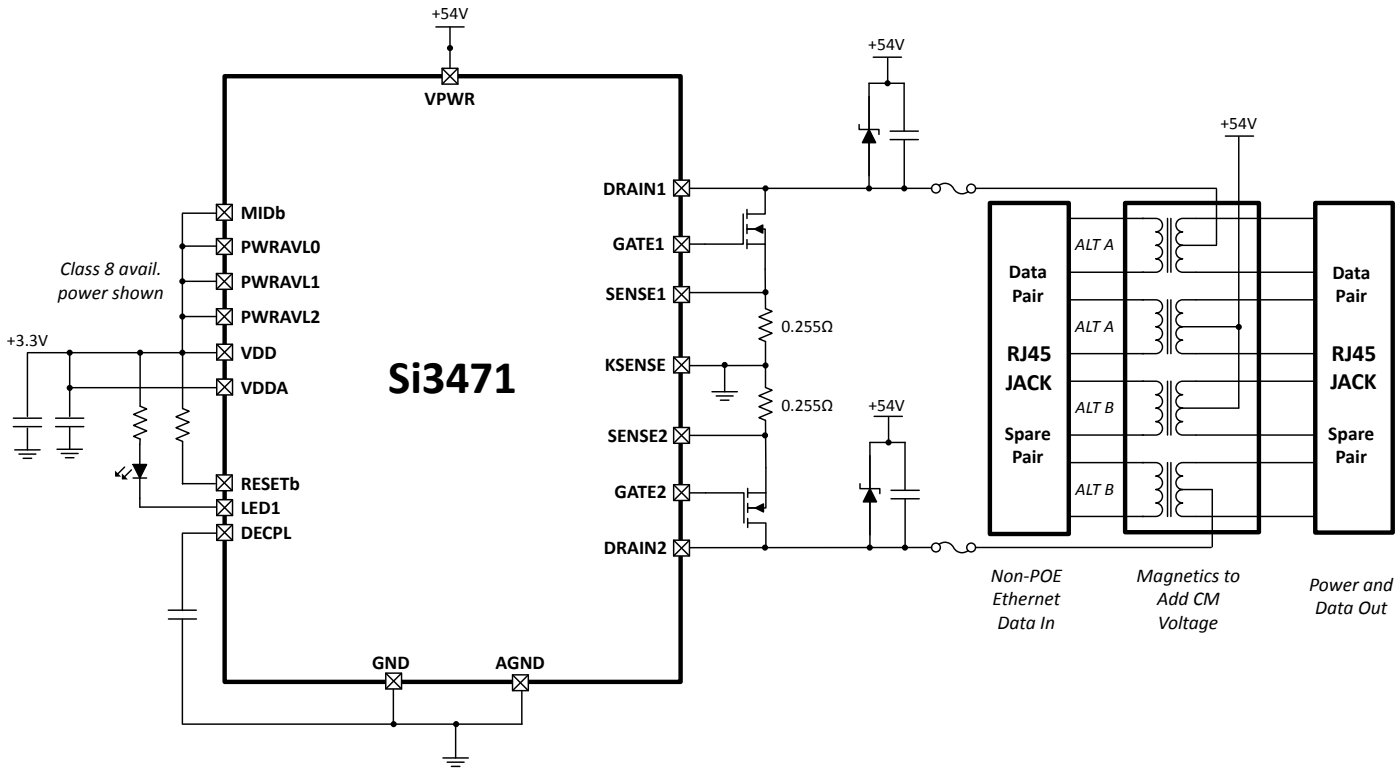


Figure 3.1. Typical 802.3bt Application Diagram

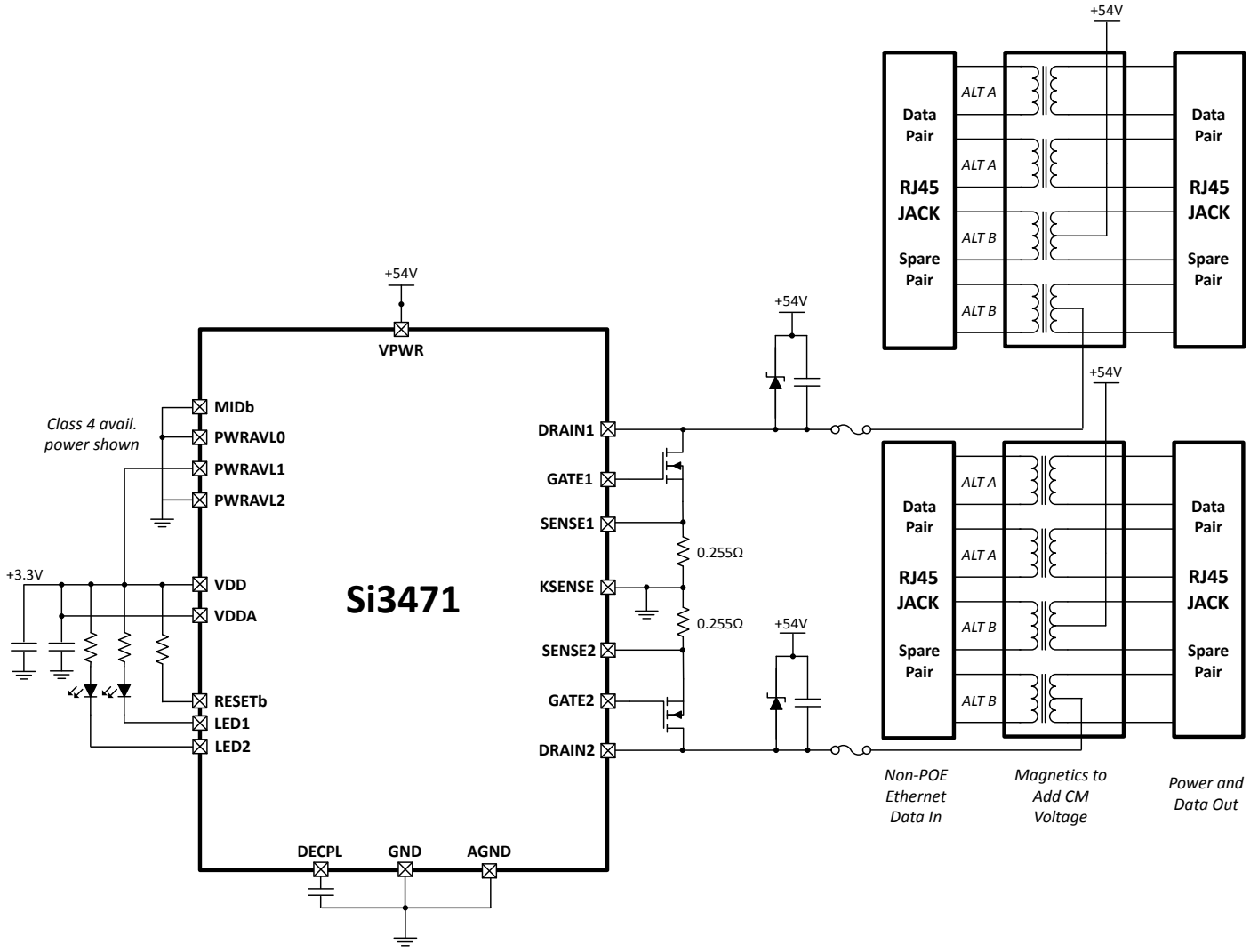


Figure 3.2. Typical 802.3at Midspan Application Diagram

4. Functional Block Diagram

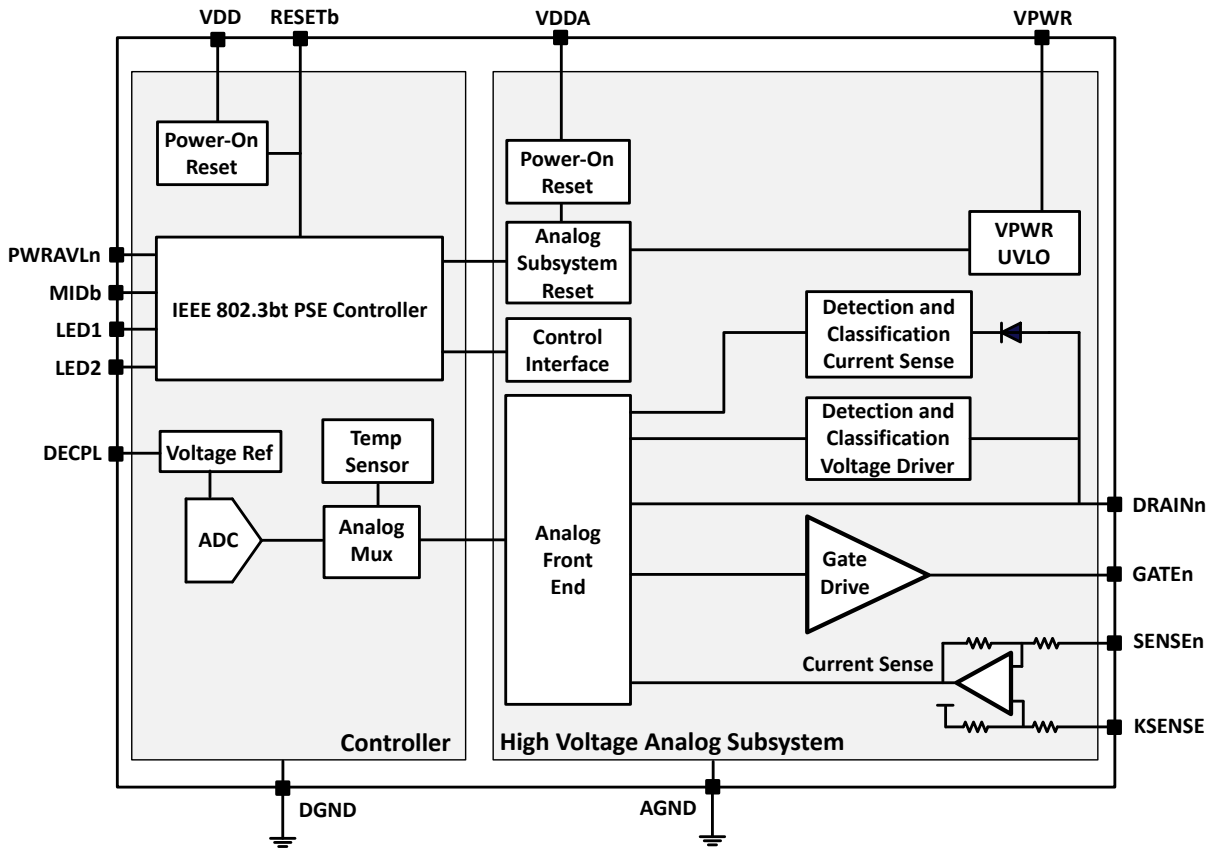


Figure 4.1. Si3471 Functional Block Diagram

5. Power Available Settings

The PWRAVL and MIDb pins configure the maximum allowable PD class that the Si3471 can power and set a power cutoff (P_{CUT}) setting. The Si3471 reads the PWRAVL and MIDb at power up, upon being released from reset, or after auto-clearing a UVLO or over-temperature event. The PWRAVL and MIDb are only read during these three conditions and cannot be dynamically adjusted while the Si3471 is operational. The Si3471 sets P_{CUT} in one of two operational modes: In one, the Si3471 sets P_{CUT} based solely on the available power of the PSE power supply disregarding the class of PD that may be attached. In the other, the Si3471 considers the class of the attached PD, and, if the PD class is lower than the class indicated by the PWRAVL pins, the Si3471 adjusts P_{CUT} to match the class of the attached PD. For each PWRAVL setting, the nominal P_{CUT} is set to 16% more than its maximum allowable PD class. For autonomous PoE injectors that require a more permissive P_{CUT}, choose a PWRAVL setting higher than the targeted PD class. For example, an injector designed to power a Class 6 PD (minimum required power of 60 W) can have a 87.2 W P_{CUT} by setting the PWRAVL[2:0] to 110b. While there are multiple options for increasing P_{CUT} for the lower classes of PDs, there is only one P_{CUT} option for powering Class 8 PDs. With PWRAVL[2:0] set to 111b, a P_{CUT} of 94 W was chosen so as to never exceed the IEEE .bt limit of 100 W, accounting for P_{CUT} measurement accuracy. The following table lists the maximum allowable classes of PDs and the P_{CUT} settings for 4-pair powering.

Table 5.1. Power Available Settings for 4-Pair Powering

PWRAVL[2:0]	MIDb	Maximum Allowable Single-Signature PD[1]	Maximum Allowable Dual-Signature PD[1]	Minimum PSE Power Required to Supply Maximum Allowable PD[1]	Nominal P_{CUT}	Maximum Power before P_{CUT} is Guaranteed
111b	H	Class 8	Class 5 + Class 5	90	95	99.8
110b	H	Class 7	Class 5 + Class 4	75	87.2	91.6
101b	H	Class 6	Class 4 + Class 4	60	70.4	73.9
100b	H	Class 5	Class 4 + Class 3	45	52.5	55.1
011b	H	Class 4	Class 3 + Class 3	30	36.2	38
000b	H	Class 8	Class 5 + Class 5	90	P_{CUT} is adjusted to whichever class is lower: The class indicated by the PWRAVL pins or the class of the attached PD.	
111b	L	Class 7	Class 5 + Class 4	75		
110b	L	Class 6	Class 4 + Class 4	60		
101b	L	Class 5	Class 4 + Class 3	45		
100b	L	Class 4	Class 3 + Class 3	30		

Note:

1. Total PSE power supply must be sized to account for target class of PD to be powered and to operate support circuitry including the Si3471.

For PWRAVL[2:0] settings 011b through 111b, the Si3471 will power Class 4 and higher PDs using all four pairs in the Ethernet cable. Using all four pairs reduces power loss in the cable, making the system more efficient. The Si3471 will always power Class 3 and lower PDs using just two pairs in the Ethernet cable. As such, the Si3471 can be configured to power lower-classes of PDs on up to two independent, 2-pair ports as shown in Figure 3.2 Typical 802.3at Midspan Application Diagram on page 6. If only one Ethernet port is used in two pair power operation, tie the unused SENSE pin and unused GATE pin to AGND and leave the unused DRAIN pin floating.

The IEEE 802.3bt specification provides allows powering a Class 4 PD using either 2-pairs or 4-pairs. The Si3471 will power a Class 4 PD using 4-pairs when PWRAVL[2:0] is set to 011b or higher, or it can power up to two Class 4 PDs over 2-pairs when PWRAVL[2:0] is set to 010b. Similar to P_{CUT} in 4-pair powering, 2-pair, per-port, P_{CUT} can be increased by choosing a higher PWRAVL setting. While there are multiple options for increasing P_{CUT} for Class 3 PDs, there is only one 2-pair P_{CUT} option for powering Class 4 PDs. With PWRAVL[2:0] set to 010b, a P_{CUT} of 36.2 W was chosen so as to never exceed the IEEE .at limit of 38.9 W, accounting for P_{CUT} measurement accuracy. The following table lists the maximum allowable classes of PDs and the P_{CUT} settings for 2-pair powering.

Table 5.2. Power Available Settings for 2-Pair Powering

PWRAVL[2:0]	MIDb1	Maximum Allowable PD (per Port)[1]	Minimum PSE Power Required to Supply Maximum Allowable PD[1]	Nominal P_{CUT} for PWRAVL[2:0] Setting (per Port)	Maximum Power before P_{CUT} is Guaranteed (per Port)
010b	1	Class 4	30 W	36.2 W	38.0 W
001b	1	Class 3	15.5 W	18.4 W	19.3 W

Note:

1. Total PSE power supply must be sized to account for target classes and number of PDs to be powered and to operate support circuitry including the Si3471.

6. Operational Sequences and Example Waveforms

The Si3471 follows the IEEE 802.3bt specification for detection, connection check, classification, and power on. The waveforms shown below illustrate Si3471 operation for single-signature and dual-signature PDs.

Si3471 Boot-up

Upon being released from reset (RESETb pulled high), the Si3471 boots up and reads the PWRAVL configuration pins and internally sets the maximum class. The Si3471 auto-clears UVLO and over-temperature events, which also triggers the Si3471 to read the PWRAVL pins.

Detection and Connection Check

After boot up, regardless of configuration, the Si3471 checks for a MOSFET fault. If a fault is found the Si3471 blinks the LED to signal an error condition and does not continue with detection and classification.

When configured for four-pair operation (PWRAVL[2:0] 111b, 110b, 101b, 100b, 011b), the Si3471 starts detection on one of the two pair sets. If a valid PD signature is found, the Si3471 executes a connection check on both pair sets. The connection check algorithm determines if a single signature or dual signature PD is connected. The Si3471 then performs detection on the second pair set to confirm a valid detection signature on both.

When configured for two-pair operation (PWRAVL[2:0] 010b, 001b), each pair set is connected to a different Ethernet port, and the Si3471 treats each independently of the other. Therefore, a connection check is not performed, and the Si3471 performs detection independently on each pair set/Ethernet port.

Classification and Power On—Four Pair, Single Signature

After two valid detection signatures and a single signature connection check, the Si3471 begins the classification and power-on sequence. The first step is a class probe to determine what power the PD is requesting. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset, and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS). The Si3471 then continues with the full classification sequence to notify the PD of the granted class. In the following figure, pair set A and pair set B the represent the primary and secondary pair sets. The Si3471 alternates which pair set detection begins on with each new detection and classification cycle.

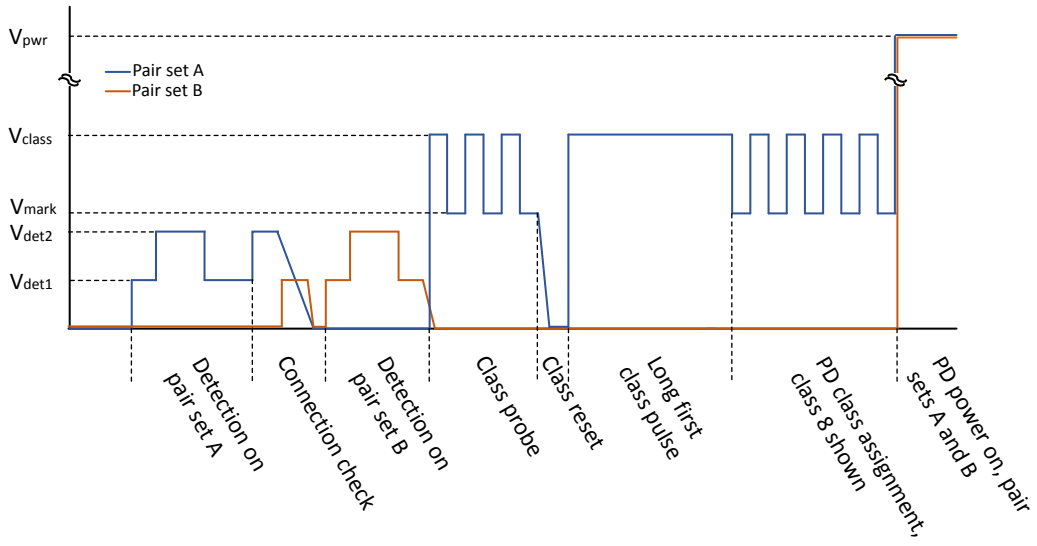


Figure 6.1. Example Waveform for 802.3bt Class 8 Single Signature Class 8

Classification and Power On—Four Pair, Dual Signature

After a valid detection signature and a dual signature connection check, the Si3471 begins the classification and power-on sequence for one of the pair sets. The first step is a class probe to determine what power the dual signature PD is requesting on one of the pair sets. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset, and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS). The Si3471 then continues with the full classification sequence to notify the PD of the granted class on one pair set. The figure below shows the classification waveform on one pair set for a Class 5 dual signature PD. Power is then applied to this pair set. The Si3471 then repeats the same procedure on the second pair set and applies power. In the following figure, Pair Set A and Pair Set B represent the primary and secondary pair sets. The Si3471 alternates which pair set detection begins with each new detection and classification cycle.

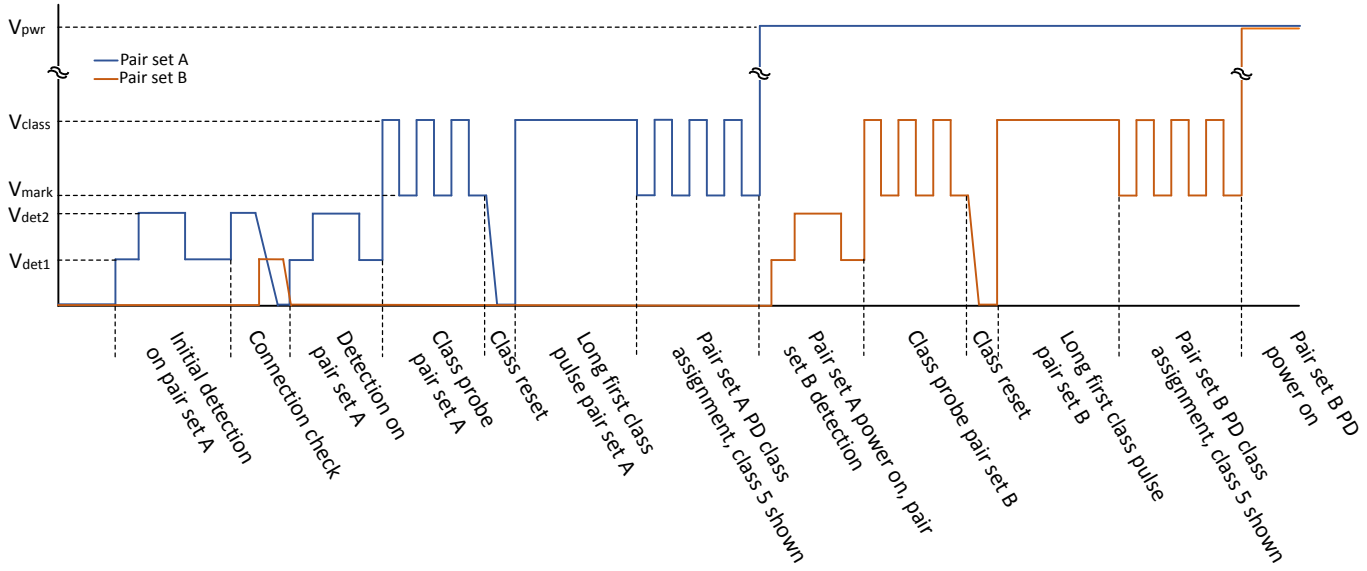


Figure 6.2. Example Waveform for 802.3bt Dual Signature PD, Class 5 on Both Pair Sets

Classification and Power On—Two Pair

After a valid detection signature, the Si3471 begins the classification and power-on sequence. The first step is a class probe to determine what power the PD is requesting. Regardless of the PWRAVL setting, the Si3471 always performs a class probe. Next, the PD is reset using a class reset, and the final classification and power-on sequence begins. The Si3471 always starts with a long first-class pulse to signal to the PD that it supports short maintain power signature (MPS) even in two-pair mode. The Si3471 then continues with the full classification sequence to notify the PD of the granted class. Finally, it powers on the PD.

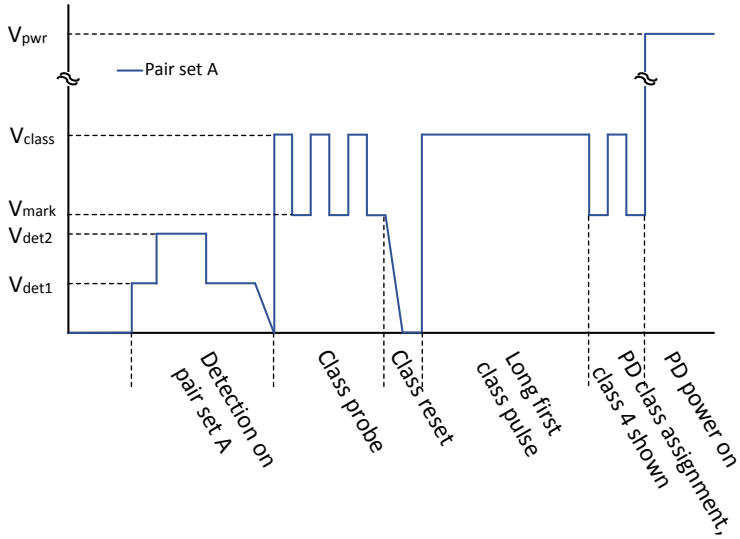


Figure 6.3. Example Waveform for 802.3at Two Pair Class 4

7. Reset Behavior

In a typical application, the Si3471's RESETb pin is tied to VDD through a pull up resistor. However, if the RESETb pin is not tied to VDD, several conditions apply. The Si3471's internal digital controller is responsible for resetting the analog subsystem. RESETb resets the Si3471's internal digital controller, which then reboots and resets the analog subsystem. If RESETb is held low, the internal digital controller is held in reset and does not reset the analog subsystem. Furthermore, if the Si3471 is providing power when RESETb is asserted, the analog subsystem will continue to provide power without any supervision or over-current protection from the digital controller. The time between the RESETb pulse and the analog subsystem being reset is specified by t_an_resetb in the diagram and table below. After the analog subsystem is reset, the Si3471 begins detection and classification based on the PWRAVL pin configuration. It is also possible to hold the Si3471 in reset such that it is powered but inactive.

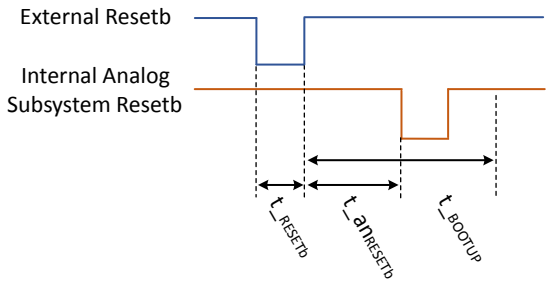


Figure 7.1. Reset Timing

Table 7.1. Reset Timing Characteristics

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Units
RESETb Pulse Width	t_{RESETb}		15	—	—	µs
Analog Subsystem Reset after RESETb deasserted	t_an_{RESETb}	If the Si3471 port is on, it will remain on for t_an_{RESETb} after the rising edge of RESETb.	—	—	300	µs
Boot up time	t_{BOOTUP}	Time from RESETb pulse end to first detection sequence.	—	45	—	ms

8. Electrical Characteristics

Table 8.1. Recommended Operating Conditions[1]

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
VPWR Input Supply Voltage	V_{PWR}	IEEE Type 3 when port is ON	50	—	57	V
		IEEE Type 4 when port is ON	52	—	57	V
VDD Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Operating Ambient Temperature[2]	T_{AMB}		–40	—	85	°C

Note:

1. All specification voltages are referenced with respect to DGND. These specifications apply over the recommended operating voltage and temperature ranges of the device unless noted otherwise.
2. The Si3471 includes internal thermal shutdown above 125 °C.

Table 8.2. Electrical Specifications

These specifications apply over the recommended operating voltage and temperature ranges of the device, specified in Table 8.1. Recommended Operating Conditions, unless otherwise noted. Typical performance is for T_A = 25 °C, V_{DD} = AGND + 3.3 V, AGND and DGND = 0 V, and V_{PWR} at 54 V. V_{PORTn}, V_{CLASS}, and V_{MARK} voltages are referenced with respect to V_{DRAIN}. All other voltages are referenced with respect to GND.

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Power Supply Voltages						
V_{PWR} Under Voltage Lock Out	V_{PWR_UVLO}	Level below which chip is not operational	43	45	50	V
V_{PWR} UVLO Input Voltage (to turn on)	V_{UVLO_ON}		43	45	—	V
V_{PWR} UVLO Input Voltage (to turn off)	V_{UVLO_OFF}		—	48	50	V
V_{DD} Under Voltage Lock Out	V_{DD_UVLO}	Voltage at which ports turn off	2.6	2.8	3.0	V
Hardware Reset Voltage	V_{RESET}	V_{DD} voltage causing reset	—	1.8	—	V
Power Supply Currents[1]						
V_{PWR} Supply Current	I_{VPWR}	During normal operation	—	2	5	mA
		V_{PWR} = 8 V, V_{DD} = 0 V	—	—	100	µA
VDD Supply Current	I_{DD}	During normal operation	—	17	25	mA
MOSFET Fault Specifications						
MOSFET Fault Detected	V_{PORT}	When V_{DRAIN} = V_{PWR}, if either condition is met, a MOSFET fault is detected	15	—	—	V
	I_{FET}		2.5	—	—	mA

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Detection Specifications						
Detection Short Circuit Current	I_{DET_SC}	Measured when Vdrain is shorted to V_{PWR}	—	3.0	4.9	mA
Detection voltage when RDET = 25.5 kΩ	V_{PORTn}	Primary detection voltage	2.8	4.0	—	V
		Secondary detection voltage	—	8.0	10.0	V
Signature Resistance	R_{GOOD}		—	25	—	kΩ
Minimum Signature Resistance @ PD	R_{DET_MIN}		15	17	19	kΩ
Maximum Signature Resistance @ PD	R_{DET_MAX}		26.5	30	33	kΩ
Reject Signature Capacitance	C_{REJECT}		—	—	10	µF
Classification Specifications						
Class Event Voltage	V_{CLASS}	0 mA < I_{CLASS} < 51 mA	15.5	—	20.5	V
Classification Short Circuit Current	I_{CLASS_SC}	Measured when Vdrain is shorted to V_{PWR}	55	—	95	mA
Classification Current Region	I_{CLASS_REGION}	Class Signature 0	0	—	5	mA
		Threshold between Class Signature 0 or 1	5	—	8	mA
		Class Signature 1	8	—	13	mA
		Threshold between Class Signature 1 or 2	13	—	16	mA
		Class Signature 2	16	—	21	mA
		Threshold between Class Signature 2 or 3	21	—	25	mA
		Class Signature 3	25	—	31	mA
		Threshold between Class Signature 3 or 4	31	—	35	mA
		Class Signature 4	35	—	45	mA
		Threshold between Class Signature 4 or invalid class	45	—	51	mA
Classification Mark Specifications						
Mark Event Voltage	V_{MARK}	Mark current between 0 and 5 mA	7	—	10	V
Mark Event Current Limitation	I_{MARK_LIM}		5	—	100	mA
Output Voltage						
Bias Current of DRAINn Pin	I_{DRAINn}	V_{DRAINn} = 0 V	—	–25	—	µA
Current Limit Detection Threshold	V_{DRAIN_ILIM}	Measured at V_{DRAIN} with respect to GND	—	—	3.00	V
Resistance from DRAIN to AGND	R_{DRAIN}		—	2.5	—	MΩ

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
Current Sense[2]						
Power Limit	P_{CUT}	PWRAVL[2:0] = 111b[3]	—	94	—	W
		PWRAVL[2:0] = 110b[3]	—	87.2	—	W
		PWRAVL[2:0] = 101b[3]	—	70.4	—	W
		PWRAVL[2:0] = 100b[3]	—	52.5	—	W
		PWRAVL[2:0] = 011b[3, 4]	—	36.2	—	W
		PWRAVL[2:0] = 010b[4]	—	36.2 (per port)	—	W
		PWRAVL[2:0] = 001b	—	18.4 (per port)	—	W
Parameter P_{CUT} Tolerance	P_{CUT}	All P_{CUT} settings	0	2.5	5	%
Current Limit[5, 6]	ILIM	Inrush, all assigned PD classes, Vport > 30 V	400	425	450	mA
		Inrush, all assigned PD classes, Vport < 30 V	60	—	—	mA
		Power-on, assigned PD Class 0, 1, 2, 3	—	425	—	mA
		Power-on, all other PD classes	—	1275	—	mA
Disconnect with power provided over two pairs[7]	$I_{PORT_DIS_2P}$	Current per pairset	—	6.5	—	mA
Disconnect with power provided over four pairs[7]	$I_{PORT_DIS_4P}$	Current per pairset. While powering over four pairs, if either pairset current is above this threshold, the PD is considered to be presenting the MPS signal.	—	3.5	—	mA

Parameter	Symbol	Test Condition/Note	Min	Typ	Max	Unit
MOSFET Gate Drive[8]						
Drive Current from GATEn Pin (Active)		GATEn pin active V_{GATEn} = AGND	–70	–50	–20	µA
Drive Current from GATEn Pin (Off)		GATEn pin shut off V_{GATEn} = AGND+ 5 V	—	50	—	mA
Voltage Difference between any GATEn and AGND Pin		I_{GATEn} = –1 µA	10	11.5	13	V
Digital Pin Characteristics						
Input Low Voltage	V_{IL}	PWRAVLn, RESETb, MIDb	—	—	0.3 x V_{DD}	V
Input High Voltage	V_{IH}	RESETb, PWRAVLn, MIDb	0.7 x V_{DD}	—	—	V
Input Leakage	I_{LK}	GND < V_{IN} < V_{DD}, RESETb, PWRAVLn, MIDb	–1.1	—	4	µA
Pullup Current to VDD	I_{PU}	RESETb, PWRAVLn, MIDb	—	–20	—	µA

Note:

1. Positive values indicate currents flowing into the device. Negative currents indicate current flowing out of the device.
2. Current sense resistor, R_{SENSE}, has a value of 0.255 Ω.
3. P_{CUT} is within 802.3bt specified unbalance limits.
4. Class 4 can be powered over either 4-pair or 2-pair power. When powered over 4-pair, the total current across both alternatives is used for P_{CUT} measurements. When powered over 2 pairs, P_{CUT} is calculated from the lone alternative.
5. Setting applies to each active alternative.
6. When powered in 4-pair mode, the ILIM value applies to each alternative; so, the total ILIM for the load is effectively doubled.
7. An MPS signal is considered present on an alternative when the current on that alternative is above these thresholds.
8. See "AN1228: FET Selection Guide for Si347x PSE Families" for detailed information on FET selection.

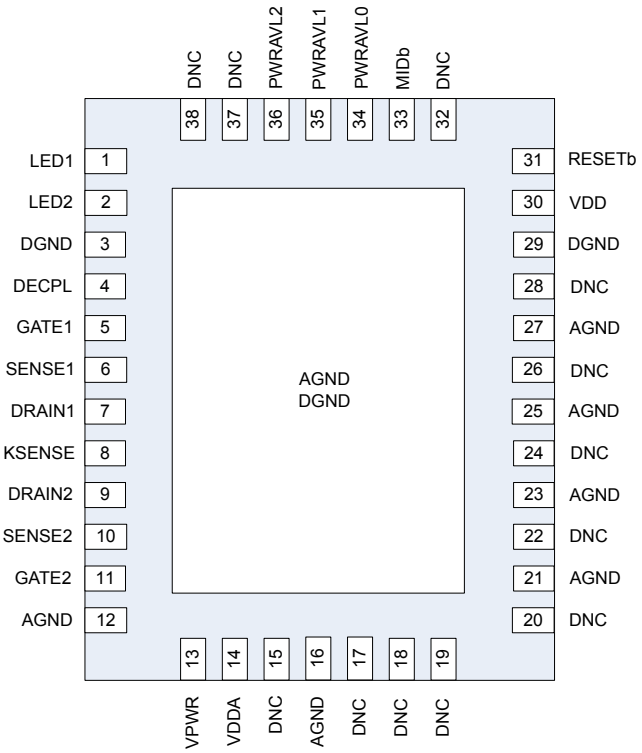
Table 8.3. Absolute Maximum Ratings[1]

Parameter	Range	Unit
Supply Voltage		
VDD	–0.3 to 4.0	V
VPWR	–0.3 to 80.0	V
DGND with Respect to AGND	0	V
Digital Signals		
All	–0.3 to 3.6	V
Analog Signals		
GATEn with Respect to AGND	–0.3 to 20.0	V
SENSEn with Respect to AGND	–0.3 to 3.0	V
DRAINn with Respect to AGND	–3 to 80	V
Temperature		
Junction[2]	+150	°C
Storage	–55 to +150	°C
Solder (10 seconds)	+300	°C

Note:

1. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. The Si3471 includes internal thermal shutdown above 125 °C.

9. Pin Descriptions



Pin	Name	Type	Description
1	LED1	Digital Output	Turns on an external LED when a PoE PD is connected and powered. When using Si3471 in 802.3at mode, LED1 turns on an external LED to indicate the status of Ethernet Port 1.
2	LED2	Digital Output	Leave floating when using Si3471 in 802.3bt mode. When using Si3471 in 802.3at mode, LED2 turns on an external LED to indicate the status of Ethernet Port 2.
15, 17, 18, 19, 20, 22, 24, 26, 28, 32, 37, 38	DNC	No Connect	No connections or nets allowed. Leave floating.
3, 29, ePAD	DGND	Digital Ground	Ground connection for 3.3 V digital supply (VDD). DGND and AGND are tied together inside the Si3471 package.
4	DECPL	Analog Input	Add a 0.1 µF capacitor between this pin and AGND.
5	GATE1	Analog Output	Gate drive outputs to external MOSFETs. Connect the GATEn outputs to the external MOSFET gate node gate. A 50 µA pull-up source is used to turn on the external MOSFET. When a current limit is detected, the GATEn voltage is reduced to maintain constant current through the external MOSFET. If the fault timer limit is reached, GATEn pulls down, shutting off the external MOSFET. GATEn will clamp to 11.5 V (typical) above AGND. If the port is unused, leave the GATEn pin disconnected or tie to AGND.
11	GATE2		
6	SENSE1	Analog Input	Current sense inputs for external MOSFETs. The SENSEn pin measures current through an external 0.255 Ω resistor tied between the AGND supply rail and the SENSEn input. If the voltage across the sense resistor subsequently triggers (the overcurrent limit), the voltage driven onto the GATEn pin is modulated to provide constant current through the external MOSFET. Tie the SENSEn pin to AGND when the port is not used.
10	SENSE2		

Pin	Name	Type	Description
7	DRAIN1	Analog input with 25 µA pull-up to VPWR	MOSFET drain output voltage sense. DRAINn pins should be left floating if the port is unused.
9	DRAIN2		
8	KSENSE	Analog Input	Kelvin point for accurate measurement of voltage across 0.255 Ω sense resistor
13	VPWR	Analog Power	Positive PoE voltage (+44 to +57 V) relative to AGND.
14	VDDA	Analog Power	3.3 V supply to the analog side; tied with VDD at the PCB level.
12, 16, 21, 23, 25, 27, ePAD	AGND	Analog Ground	Ground connection for VPWR supply. DGND and AGND are tied together inside the Si3471 package.
30	VDD	Digital Power	3.3 V digital supply (relative to DGND). Bypass VDD with a 0.1 µF capacitor to DGND as close as possible to the Si3471 power supply pins; tied with VDDA.
31	RESETb	Digital input with 20 µA pull-up to VDD	Active low device reset input. See 7. Reset Behavior for more information. If RESETb is not used, RESETb should be left floating.
33	MIDb	Digital Input	See 5. Power Available Settings for information on configuring MIDb. For 2-Pair operation, the Si3471 uses a 2-second detection back-off timing. Therefore, for 2-Pair operation, connect the port(s) to the ALT-B pair set(s).
34	PWRAVL0	Digital Input	Sets the maximum power available to the Si3471.
35	PWRAVL1		
36	PWRAVL2		

10. Package Outline: 38-Pin QFN

The figure below illustrates the package details for the Si3471. The table lists the values for the dimensions shown in the illustration. The Si3471 is packaged in an industry-standard, RoHS-compliant, 38-pin QFN package.

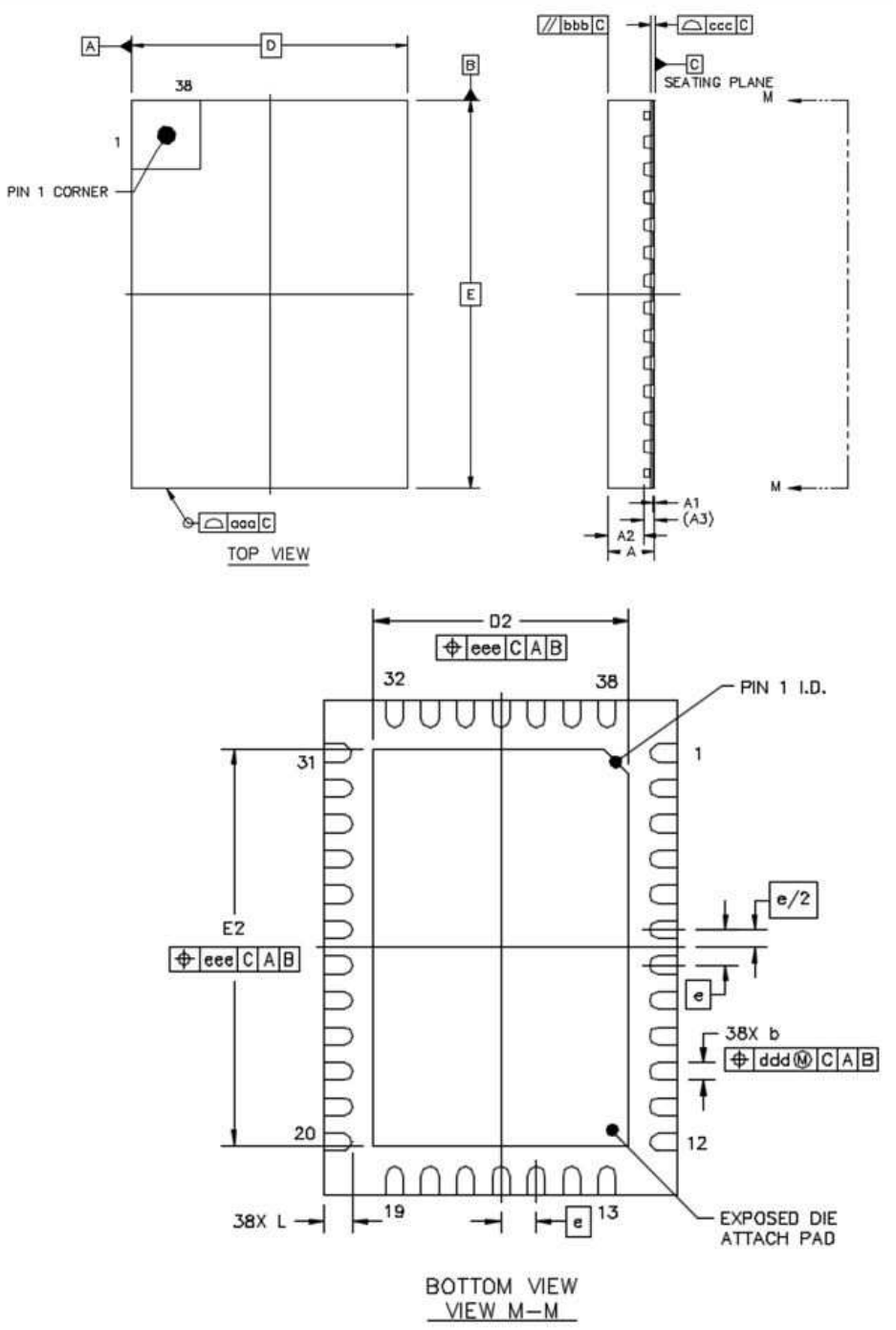


Figure 10.1. 38-Pin QFN Package

Table 10.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.035	0.05
A3		0.203 REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	6.90	7.00	7.10
D2	3.50	3.60	3.70
E2	5.50	5.60	5.70
e		0.50 BSC	
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. Land Pattern

The following figure illustrates the land pattern details for the Si3471. The table lists the values for the dimensions shown in the illustration. The stencil design and notes are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

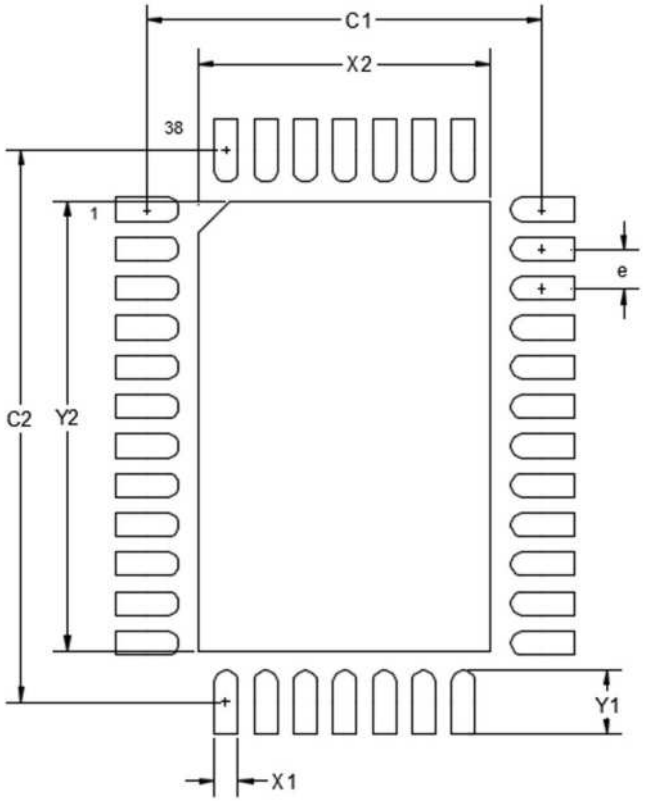


Figure 11.1. Si3471 Recommended Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Symbol	mm
C1	5.00
C2	7.00
e	0.50
X1	0.30
Y1	0.80
X2	3.70
Y2	5.70

Notes:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 3 x 5 array of 0.90 mm square openings on 1.10 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

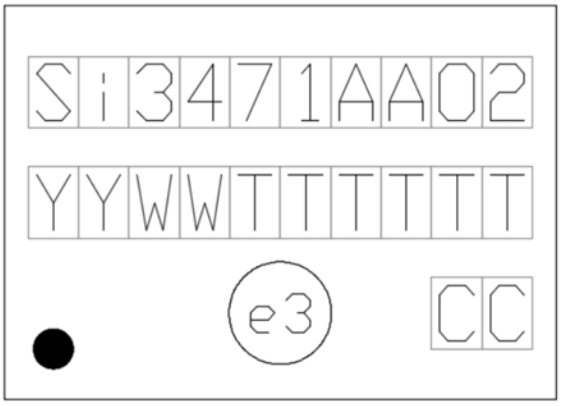


Figure 12.1. Si3471A Top Marking (QFN)

Table 12.1. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left-Justified	
Line 1 Mark Format:	Device Part Number	Si3471AA02
Line 2 Mark Format:	YY = Year WW = Work Week TTTTTT = Mfg Code	Year and Work Week of Assembly Manufacturing Code
Line 3 Mark Format:	Circle = 1.3 mm Diameter Country of Origin	“e3” Pb-Free Symbol TW = Taiwan

13. Revision History

Revision 1.0

May, 2021

- Updated 5. Power Available Settings.
- Updated 8. Electrical Characteristics.

Revision 0.6

May, 2020

- Updated 5. Power Available Settings.
- Updated 8. Electrical Characteristics.

Revision 0.5

March, 2020

- Initial release.

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