Si5018

SiPHY™ OC-48/STM-16 Clock and Data Recovery IC With FEC

Features

Complete high-speed, low-power, CDR solution includes the following:

- Supports OC-48 /STM-16 & FEC
- Low power—270 mW (typ OC-48)
- Small footprint: 4x4 mm
- DSPLL™ Eliminates external loop filter components
- 3.3 V tolerant control inputs
- Exceeds all SONET/SDH jitter specifications
- Jitter generation 3.0 mUI_{rms} (typ)
- Device powerdown
- Loss-of-lock indicator
- Single 2.5 V Supply



Ordering Information:

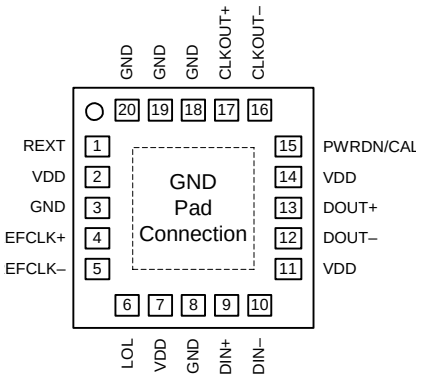
See page 17.

Applications

- SONET/SDH/ATM routers
- Add/drop multiplexers
- Digital cross connects
- SONET/SDH test equipment
- Optical transceiver modules
- SONET/SDH regenerators
- Board level serial links

Pin Assignments

Si5018

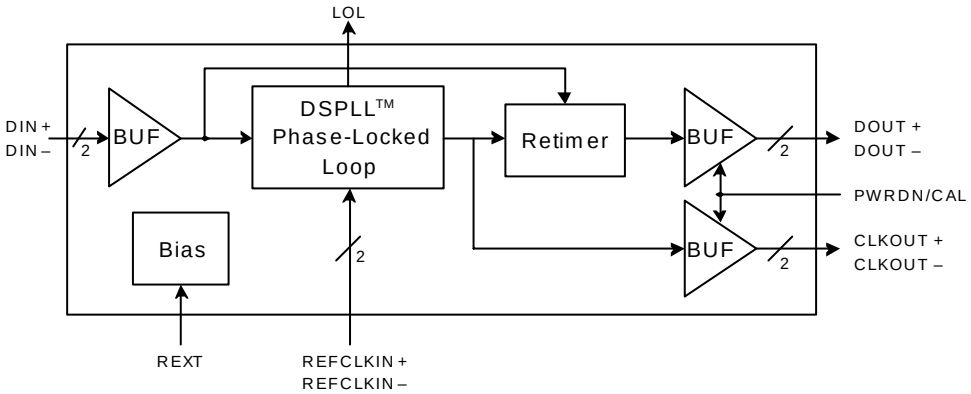


Description

The Si5018 is a fully-integrated low-power clock and data recovery (CDR) IC designed for high-speed serial communication systems. It extracts timing information and data from a serial input at OC-48/STM-16 data rates. In addition, support for 2.7 Gbps data streams is also provided for applications that employ forward error correction (FEC). DSPLL™ technology eliminates sensitive noise entry points thus making the PLL less susceptible to board-level interaction and helping to ensure optimal jitter performance.

The Si5018 represents a new standard in low jitter, low power, and small size for high speed CDRs. It operates from a single 2.5 V supply over the industrial temperature range (–40 to 85 °C).

Functional Block Diagram

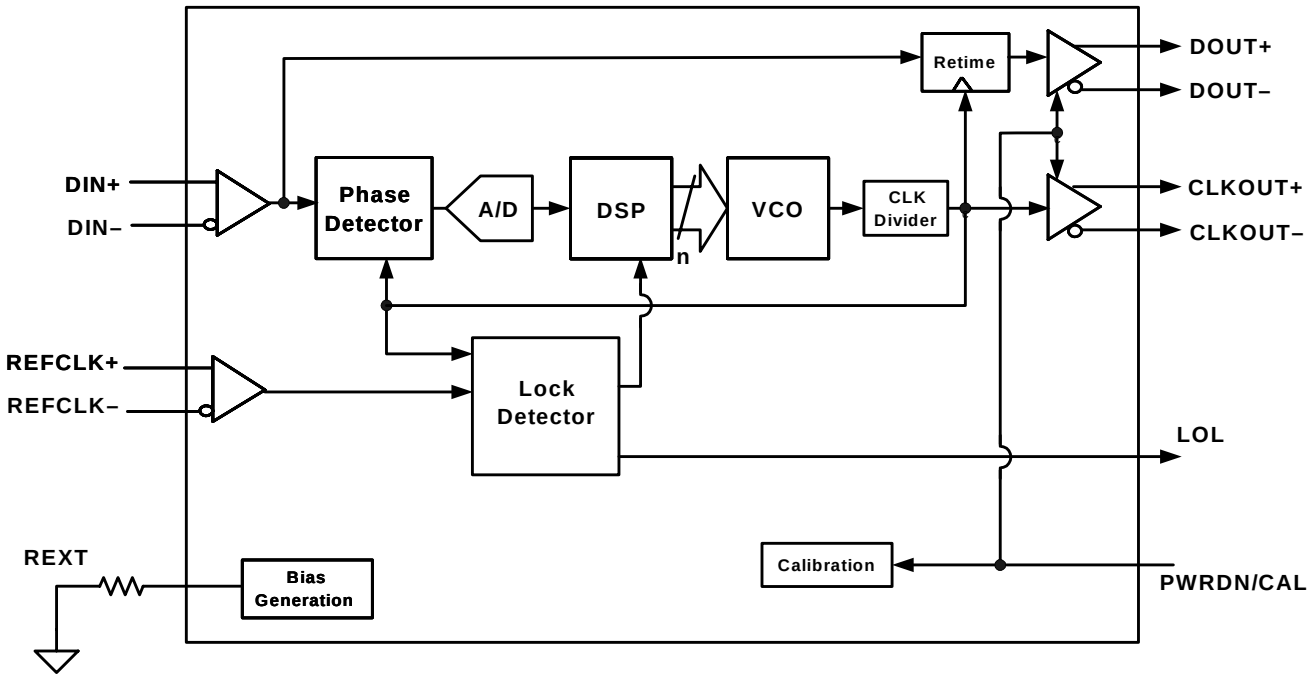


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TABLE OF CONTENTS

Section	Page
Detailed Block Diagram	**4**
Electrical Specifications	**5**
Typical Application Schematic	**9**
Functional Description	**10**
DSPLL™	10
PLL Self-Calibration	10
Reference Clock Detect	10
Forward Error Correction (FEC)	10
Lock Detect	10
PLL Performance	11
Powerdown	11
Device Grounding	12
Bias Generation Circuitry	12
Differential Input Circuitry	12
Differential Output Circuitry	14
Pin Descriptions: Si5018	**15**
Ordering Guide	**17**
Top Mark	**17**
Package Outline	**18**
4x4 mm 20L QFN Recommended PCB Layout	**19**
Document Change List	**20**
Contact Information	**22**

1. Detailed Block Diagram



2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A		–40	25	85	°C
Si5018 Supply Voltage[2]	V_{DD}		2.375	2.5	2.625	V

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. The Si5018 specifications are guaranteed when using the recommended application circuit (including component tolerance) shown in "Typical Application Schematic," on page 9.

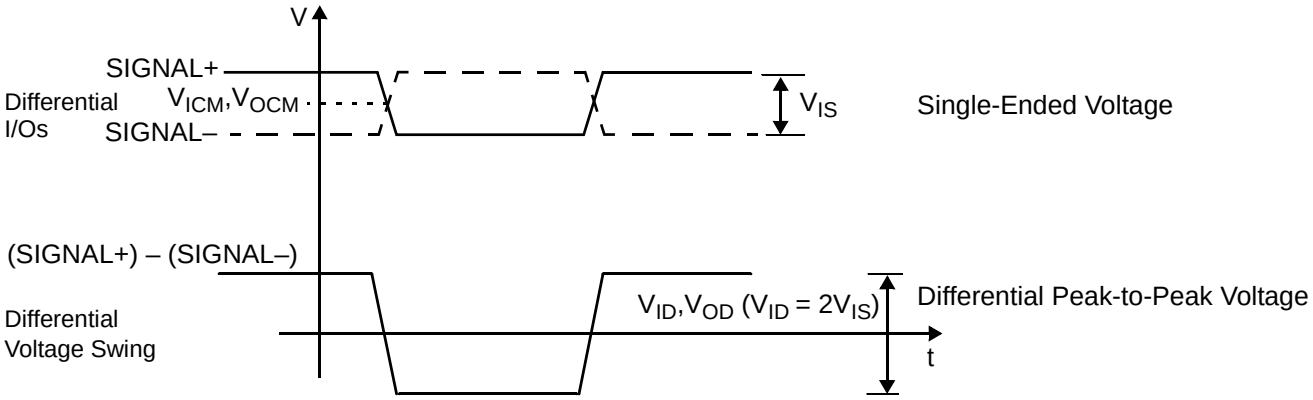


Figure 1. Differential Voltage Measurement (DIN, REFCLK, DOUT, CLKOUT)

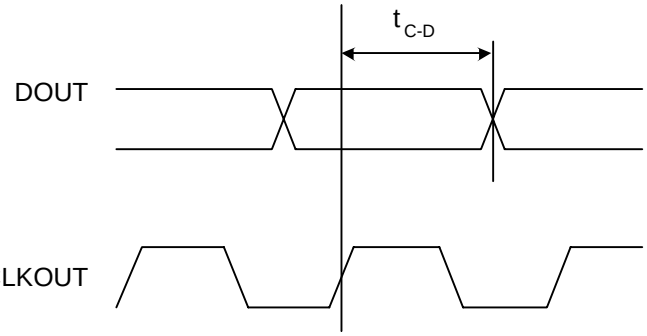


Figure 2. Differential Clock to Data Timing

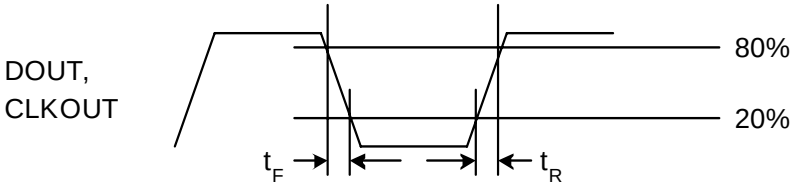


Figure 3. Differential DOUT and CLKOUT Rise/Fall Times

Table 2. DC Characteristics
(V_{DD} = 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	108	122	mA
Power Dissipation	P_D		—	270	320	mW
Common Mode Input Voltage (DIN, REFCLK)*	V_{ICM}	varies with V_{DD}	—	.80 x V_{DD}	—	V
Single Ended Input Voltage (DIN, REFCLK)*	V_{IS}	See Figure 1	200	—	750	mV_{PP}
Differential Input Voltage Swing (DIN, REFCLK)*	V_{ID}	See Figure 1	200	—	1500	mV_{PP}
Input Impedance (DIN, REFCLK)	R_{IN}	Line-to-Line	84	100	116	Ω
Differential Output Voltage Swing (DOUT) OC48	V_{OD}	100 Ω Load Line-to-Line	780	990	1260	mV_{PP}
Differential Output Voltage Swing (CLKOUT) OC48	V_{OD}	100 Ω Load Line-to-Line	550	900	1260	mV_{PP}
Output Common Mode Voltage (DOUT,CLKOUT)	V_{OCM}	100 Ω Load Line-to-Line	—	V_{DD} – 0.23	—	V
Output Impedance (DOUT,CLKOUT)	R_{OUT}	Single-ended	84	100	116	Ω
Output Short to GND (DOUT,CLKOUT)	$I_{SC(–)}$		—	25	31	mA
Output Short to V_{DD} (DOUT,CLKOUT)	$I_{SC(+)}$		–17.5	–14.5	—	mA
Input Voltage Low (LVTTL Inputs)	V_{IL}		—	—	.8	V
Input Voltage High (LVTTL Inputs)	V_{IH}		2.0	—	—	V
Input Low Current (LVTTL Inputs)	I_{IL}		—	—	10	µA
Input High Current (LVTTL Inputs)	I_{IH}		—	—	10	µA
Output Voltage Low (LVTTL Outputs)	V_{OL}	I_O = 2 mA	—	—	0.4	V
Output Voltage High (LVTTL Outputs)	V_{OH}	I_O = 2 mA	2.4	—	—	V
Input Impedance (LVTTL Inputs)	R_{IN}		10	—	—	kΩ
PWRDN/CAL Leakage Current	I_{PWRDN}	$V_{PWRDN} \geq 0.8$ V	15	25	35	µA

***Note:** The DIN and REFCLK inputs may be driven differentially or single-endedly. When driving single-endedly, the voltage swing of the signal applied to the active input must exceed the specified minimum Differential Input Voltage Swing (V_{ID} min), and the unused input must be ac coupled to ground. When driving differentially, the difference between the positive and negative input signals must exceed V_{ID} min. (Each individual input signal needs to swing only half of this range.) In either case, the voltage applied to any individual pin (DIN+, DIN–, REFCLK+, or REFCLK–) must not exceed the specified maximum Input Voltage Range (V_{IS} max).

Table 3. AC Characteristics (Clock and Data)
(V_A 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Clock Rate	f_{CLK}		2.4	—	2.7	GHz
Output Rise/Fall Time	t_R, t_F	Figure 3	—	80	110	ps
Clock to Data Delay FEC (2.7 GHz) OC-48	t_{C-D}	Figure 2	 225 225	 250 250	 270 270	ps
Input Return Loss		100 kHz–2.5 GHz 2.5 GHz–4.0 GHz	— —	16 13	— —	dB dB

Table 4. AC Characteristics (PLL Characteristics)
(V_A 2.5 V ±5%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Tolerance*	$J_{TOL(P–P)}$	f = 600 Hz	40	—	—	UI_{PP}
		f = 6000 Hz	4	—	—	UI_{PP}
		f = 100 kHz	4	—	—	UI_{PP}
		f = 1 MHz	.4	—	—	UI_{PP}
RMS Jitter Generation*	$J_{GEN(rms)}$	with no jitter on serial data	—	2.9	5.0	mUI
Peak-to-Peak Jitter Generation*	$J_{GEN(PP)}$	with no jitter on serial data	—	25	55	mUI
Jitter Transfer Bandwidth*	J_{BW}		—	—	2.0	MHz
Jitter Transfer Peaking*	J_P		—	0.03	0.1	dB
Acquisition Time	T_{AQ}	After falling edge of PWRDN/CAL	1.45	1.5	1.7	ms
		From the return of valid data	40	60	150	µs
Input Reference Clock Duty Cycle	C_{DUTY}		40	50	60	%
Input Reference Clock Frequency Tolerance	C_{TOL}		–100	—	100	ppm
Reference Clock Range			19.44	—	168.75	MHz
Frequency Difference at which Receive PLL goes out of Lock (REFCLK compared to the divided down VCO clock)	LOL		450	600	750	ppm
Frequency Difference at which Receive PLL goes into Lock (REFCLK compared to the divided down VCO clock)	LOCK		150	300	450	ppm

***Note:** Bellcore specifications: GR-253-CORE, Issue 2, December 1995. Using PRBS 2^{23} – 1 data pattern.

Table 5. Absolute Maximum Ratings

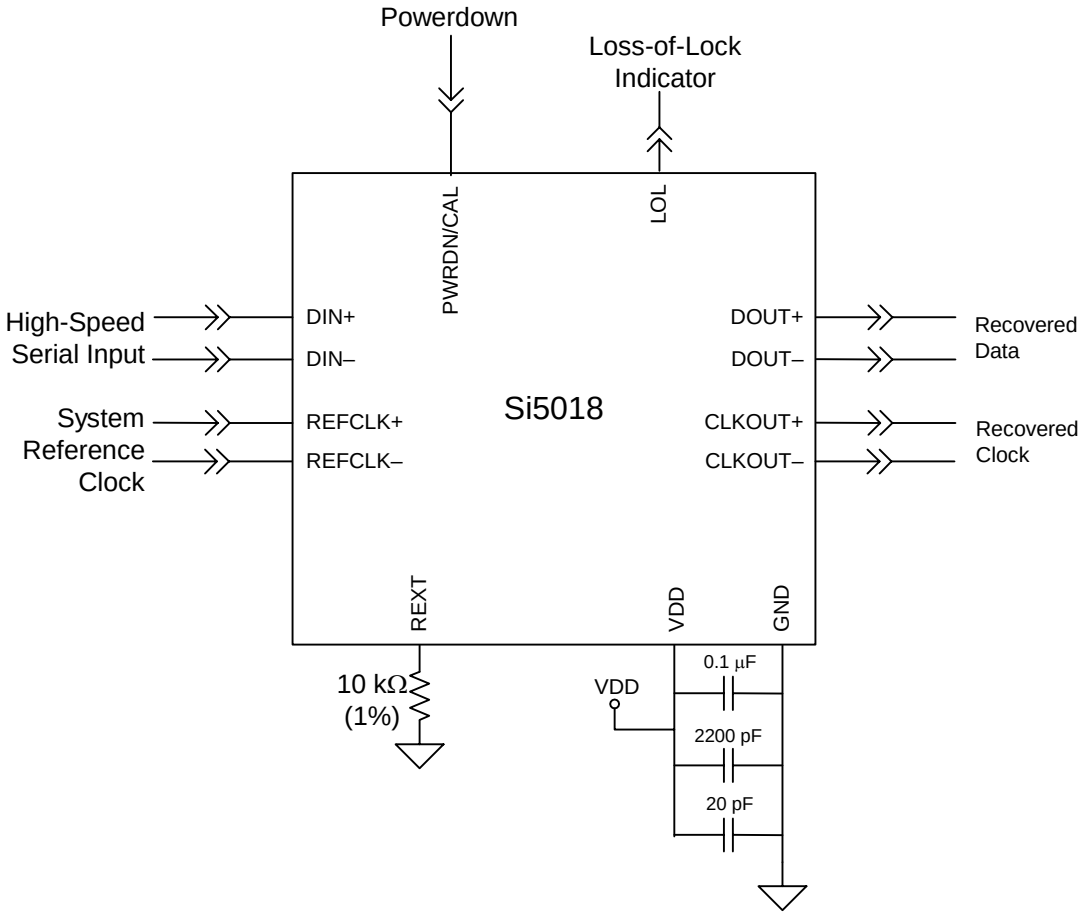
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 2.8	V
LVTTL Input Voltage	V_{DIG}	–0.3 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		1	kV

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	38	°C/W

3. Typical Application Schematic



4. Functional Description

The Si5018 utilizes a phase-locked loop (PLL) to recover a clock synchronous to the input data stream. This clock is used to retime the data, and both the recovered clock and data are output synchronously via current mode logic (CML) drivers. Optimal jitter performance is obtained by using Silicon Laboratories' DSPLL™ technology to eliminate the noise entry points caused by external PLL loop filter components.

4.1. DSPLL™

The phase-locked loop structure (shown in "Typical Application Schematic," on page 9) utilizes Silicon Laboratories' DSPLL™ technology to eliminate the need for external loop filter components found in traditional PLL implementations. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage-controlled oscillator (VCO). Because external loop filter components are not required, sensitive noise entry points are eliminated thus making the DSPLL less susceptible to board-level noise sources that make SONET/SDH jitter compliance difficult to attain.

4.2. PLL Self-Calibration

The Si5018 achieves optimal jitter performance by using self-calibration circuitry to set the loop gain parameters within the DSPLL. For the self-calibration circuitry to operate correctly, the power supply voltage must exceed 2.25 V when calibration occurs. For best performance, the user should force a self-calibration once the supply has stabilized on powerup.

A self-calibration can be initiated by forcing a high-to-low transition on the power-down control input, PWRDN/CAL, while a valid reference clock is supplied to the REFCLK input. The PWRDN/CAL input should be held high at least 1 μs before transitioning low to guarantee a self-calibration. Several application circuits that could be used to initiate a power-on self-calibration are provided in Silicon Laboratories' "AN42: Controlling DSPLL™ Self-Calibration for the Si5020/5018/5010 CDR Devices and Si531x Clock Multiplier/Regenerator Devices."

4.3. Reference Clock Detect

The Si5018 CDR requires an external reference clock applied to the REFCLK input for normal device operation. When REFCLK is absent, the LOL alarm will always be asserted when it has been determined that no activity exists on REFCLK, indicating the lock status of the PLL is unknown. Additionally, the Si5018 uses the reference clock to center the VCO output frequency at the OC-48/STM-16 data rate. The device will self-configure for operation with one of three reference clock frequencies. This eliminates the need to externally configure the device to operate with a particular reference clock.

The reference clock centers the VCO for a nominal output between 2.488 GHz and 2.7 GHz. The VCO frequency is centered at 16, 32, or 128 times the reference clock frequency. Detection circuitry continuously monitors the reference clock input to determine whether the device should be configured for a reference clock that is 1/16, 1/32, or 1/128 the nominal VCO output. Approximate reference clock frequencies are given in Table 7.

Table 7. Typical REFCLK Frequencies

OC-48/ STM-16 (2.488 GHz)	OC-48/STM-16 w/ 15/14 FEC (2.666 GHz)	Ratio of VCO to REFCLK
19.44 MHz	20.83 MHz	128
77.76 MHz	83.31 MHz	32
155.52 MHz	166.63 MHz	16

4.4. Forward Error Correction (FEC)

The Si5018 supports FEC in SONET OC-48 (SDH STM-16) applications for data rates up to 2.7 Gbps. In FEC applications, the appropriate reference clock frequency is determined by dividing the input data rate by 16, 32, or 128. For example, if an FEC code is used that produces a 2.7 Gbps data rate, the required reference clock would be 168.75 MHz, 84.375 MHz, or 21.09 MHz.

4.5. Lock Detect

The Si5018 provides lock-detect circuitry that indicates whether the PLL has achieved frequency lock with the incoming data. The circuit compares the frequency of a divided-down version of the recovered clock with the frequency of the applied reference clock (REFCLK). If the recovered clock frequency deviates from that of the reference clock by the amount specified in Table 4 on page 7**,** the PLL is declared out of lock, and the loss-of-lock (LOL) pin is asserted high. In this state, the PLL will periodically try to reacquire lock with the incoming data stream. During reacquisition, the recovered clock may drift over a ±600 ppm range relative to the applied reference clock, and the LOL output alarm may toggle until the PLL has reacquired frequency lock. Due to the

low noise and stability of the DSPLL, under the condition where data is removed from the inputs, there is the possibility that the PLL will not drift enough to render an out-of-lock condition.

If REFCLK is removed, the LOL output alarm is always asserted when it has been determined that no activity exists on REFCLK, indicating the frequency lock status of the PLL is unknown.

Note: LOL is not asserted during PWRDN/CAL.

4.6. PLL Performance

The PLL implementation used in the Si5018 is fully compliant with the jitter specifications proposed for SONET/SDH equipment by Bellcore GR-253-CORE, Issue 2, December 1995 and ITU-T G.958.

4.6.1. Jitter Tolerance

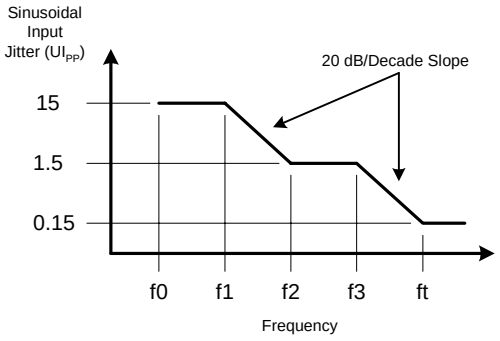
The Si5018's tolerance to input jitter exceeds that of the Bellcore/ITU mask shown in Figure 4. This mask defines the level of peak-to-peak sinusoid jitter that must be tolerated when applied to the differential data input of the device.

4.6.2. Jitter Transfer

The Si5018 is fully compliant with the relevant Bellcore/ ITU specifications related to SONET/SDH jitter transfer. Jitter transfer is defined as the ratio of output signal jitter to input signal jitter as a function of jitter frequency (see Figure 5). These measurements are made with an input test signal that is degraded with sinusoidal jitter whose magnitude is defined by the mask in Figure 4.

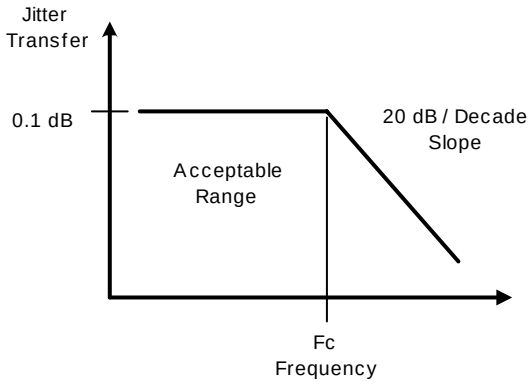
4.6.3. Jitter Generation

The Si5018 exceeds all relevant specifications for jitter generation proposed for SONET/SDH equipment. The jitter generation specification defines the amount of jitter that may be present on the recovered clock and data outputs when a jitter free input signal is provided. The Si5018 generates less than 3.0 mUI_{rms} of jitter when presented with jitter free input data.



SONET Data Rate	F0 (Hz)	F1 (Hz)	F2 (Hz)	F3 (kHz)	Ft (kHz)
OC- 48	10	600	6000	100	1000

Figure 4. Jitter Tolerance Specification



SONET Data Rate	Fc (kHz)
OC- 48	2000

Figure 5. Jitter Transfer Specification

4.7. Powerdown

The Si5018 provides a powerdown pin, PWRDN/CAL, that disables the output drivers (DOUT, CLKOUT). When the PWRDN/CAL pin is driven high, the positive and negative terminals of CLKOUT and DOUT are each tied to VDD through 100 Ω on-chip resistors. This feature is useful in reducing power consumption in applications that employ redundant serial channels. When PWRDN/CAL is released (set to low) the digital logic resets to a known initial condition, recalibrates the DSPLL, and will begin to lock to the data stream.

4.8. Device Grounding

The Si5018 uses the GND pad on the bottom of the 20-

pin micro leaded package (MLP) for device ground. This pad should be connected directly to the analog supply ground. See Figures 10 and 11 for the ground (GND) pad location.

4.9. Bias Generation Circuitry

The Si5018 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 10 kΩ (1%) resistor connected between REXT and GND.

4.10. Differential Input Circuitry

The Si5018 provides differential inputs for both the high speed data (DIN) and the reference clock (REFCLK) inputs. An example termination for these inputs is shown in Figure 6. In applications where direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The DIN and REFCLK input amplifiers require an input signal with a minimum differential peak-to-peak voltage listed in Table 2 on page 6.

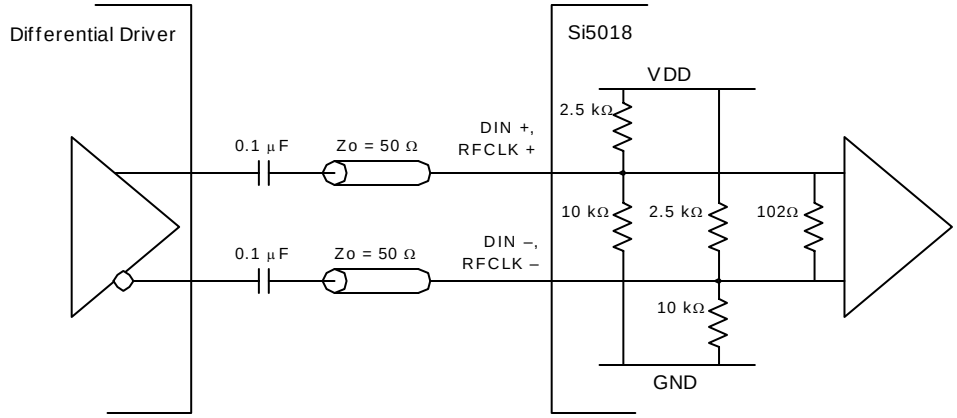


Figure 6. Input Termination for DIN and REFCLK (AC Coupled)

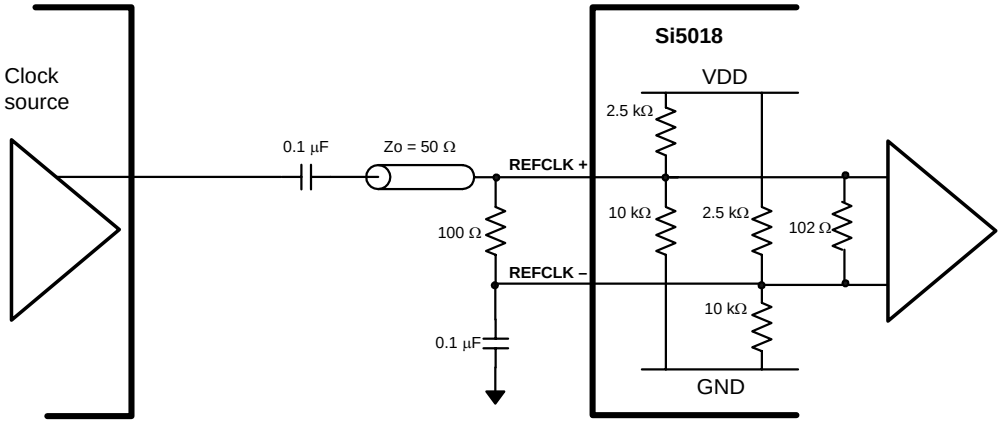


Figure 7. Single-Ended Input Termination for REFCLK (AC Coupled)

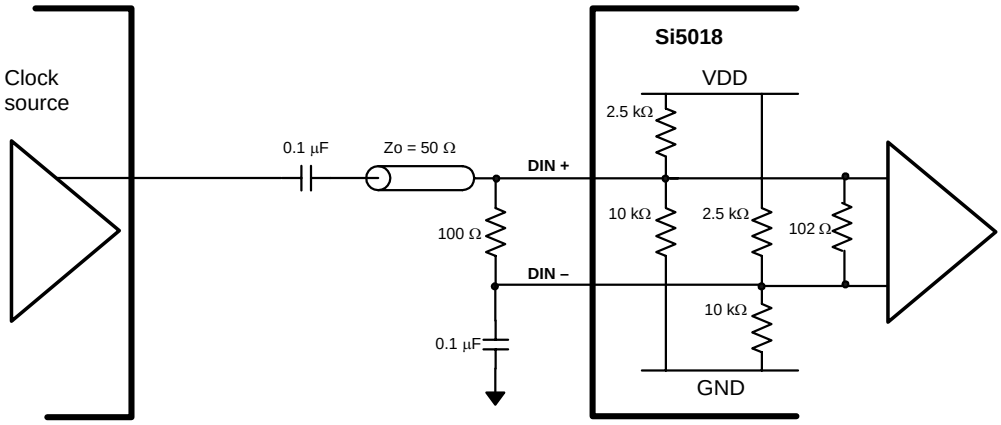


Figure 8. Single-Ended Input Termination for DIN (AC Coupled)

4.11. Differential Output Circuitry

The Si5018 utilizes a current mode logic (CML) architecture to output both the recovered clock (CLKOUT) and data (DOUT). An example of output termination with ac coupling is shown in Figure 9. In applications in which direct dc coupling is possible, the 0.1 μF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is listed in Table 2 on page 6.

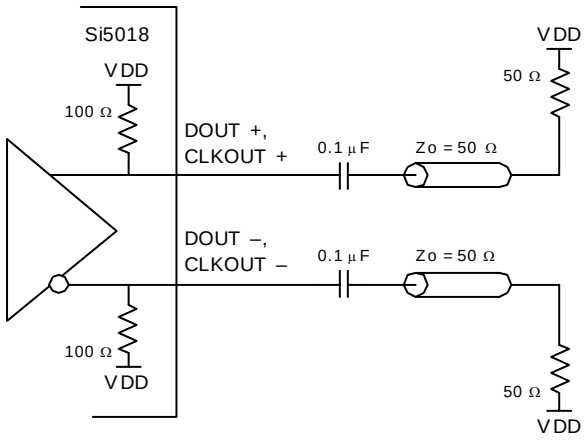


Figure 9. Output Termination for DOUT and CLKOUT (AC Coupled)

5. Pin Descriptions: Si5018

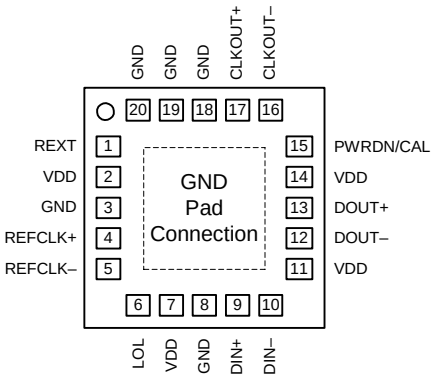


Figure 10. Si5018 Pin Configuration

Table 8. Si5018 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	REXT			**External Bias Resistor.** This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 10 kΩ (1%) resistor.
4 5	REFCLK+ REFCLK–	I	See Table 2	**Differential Reference Clock.** The reference clock sets the initial operating frequency used by the onboard PLL for clock and data recovery. Additionally, the reference clock is used to derive the clock output when no data is present.
6	LOL	O	LVTTL	**Loss-of-Lock.** This output is driven high when the recovered clock frequency deviates from the reference clock by the amount specified in Table 4 on page 7.
9 10	DIN+ DIN–	I	See Table 2	**Differential Data Input.** Clock and data are recovered from the differential signal present on these pins.
12 13	DOUT– DOUT+	O	CML	**Differential Data Output.** The data output signal is a retimed version of the data recovered from the signal present on DIN. It is phase aligned with CLKOUT and is updated on the rising edge of CLKOUT.

Table 8. Si5018 Pin Descriptions (Continued)

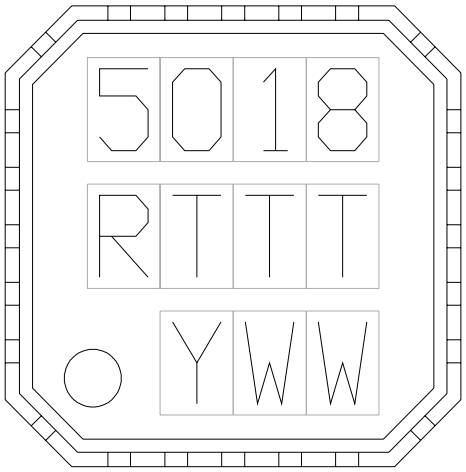
Pin #	Pin Name	I/O	Signal Level	Description
15	PWRDN/CAL	I	LVTTL	**Powerdown.** To shut down the high-speed outputs and reduce power consumption, hold this pin high. For normal operation, hold this pin low. **Calibration.** To initiate an internal self-calibration, force a high-to-low transition on this pin. (See "PLL Self-Calibration," on page 10.) **Note:** This input has a weak internal pulldown.
16 17	CLKOUT– CLKOUT+	O	CML	**Differential Clock Output.** The output clock is recovered from the data signal present on DIN. In the absence of data, the output clock is derived from REFCLK.
2, 7, 11, 14	VDD		2.5 V	**Supply Voltage.** Nominally 2.5 V.
3, 8, 18, 19, 20, and GND Pad	GND		GND	**Supply Ground.** Nominally 0.0 V. The GND pad found on the bottom of the 20-pin micro leaded package (see Figure 11) must be connected directly to supply ground.

6. Ordering Guide

Part Number	Package	Voltage	Pb-Free	Temperature
Si5018-X-GM	20-Lead QFN	2.5	Yes	–40 to 85 °C

1. "X" denotes product revision.
2. Add an "R" at the end of the device to denote tape and reel option; 2500 quantity per reel.
3. These devices use a NiPdAu pre-plated finish on the leads that is fully RoHS6 compliant while being fully compatible with both leaded and lead-free card assembly processes.

7. Top Mark



Silicon Labs Part Number	Die Revision (R)	Assembly Date (YWW)
Si5018-B-GM	B	Y = Last digit of current year WW = Work week

8. Package Outline

Figure 11 illustrates the package details for the Si5018. Table 9 lists the values for the dimensions shown in the illustration.

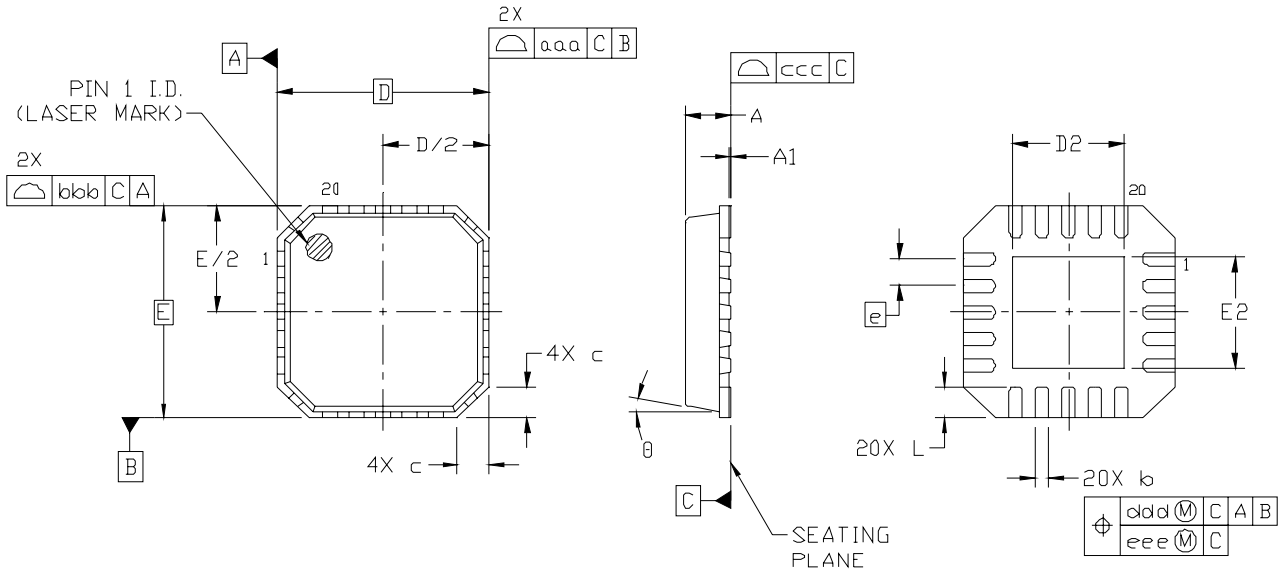


Figure 11. 20-pin Quad Flat No-Lead (QFN)

Table 9. Package Dimensions

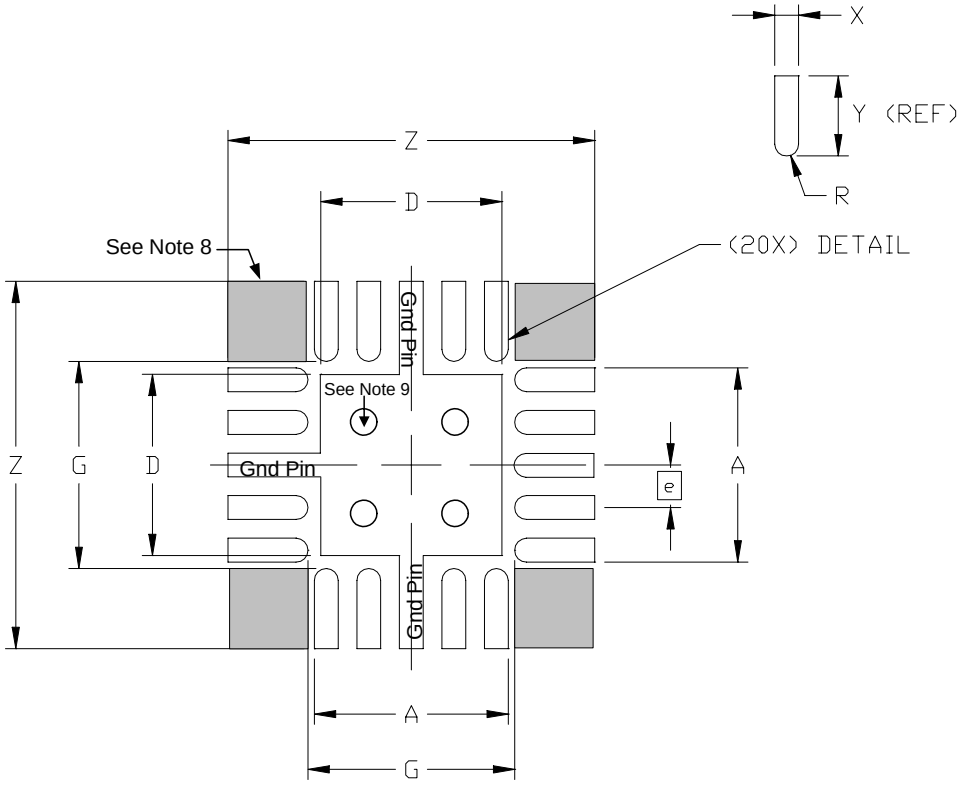
Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	—	—	0.60
D		4.00 BSC	
D2	1.95	2.10	2.25
e		0.50 BSC	
E		4.00 BSC	

Symbol	Millimeters		
	Min	Nom	Max
E2	1.95	2.10	2.25
L	0.50	0.60	0.70
θ	0°	—	12°
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-1.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

9. 4x4 mm 20L QFN Recommended PCB Layout



Symbol	Parameter	Dimensions		
		Min	Nom	Max
A	Pad Row/Column Width/Length	2.23	2.25	2.28
D	Thermal Pad Width/Height	2.03	2.08	2.13
e	Pad Pitch	—	0.50 BSC	—
G	Pad Row/Column Separation	2.43	2.46	2.48
R	Pad Radius	—	0.12 REF	—
X	Pad Width	0.23	0.25	0.28
Y	Pad Length	—	0.94 REF	—
Z	Pad Row/Column Extents	4.26	4.28	4.31

Notes:

1. All dimensions listed are in millimeters (mm).
2. The perimeter pads are to be Non-Solder Mask Defined (NSMD). Solder mask openings should be designed to leave 60-75 mm separation between solder mask and pad metal, all the way around the pad.
3. The center thermal pad is to be Solder Mask Defined (SMD).
4. Thermal/Ground vias placed in the center pad should be no less than 0.2 mm (8 mil) diameter and tented from the top to prevent solder from flowing into the via hole.
5. The stencil aperture should match the pad size (1:1 ratio) for the perimeter pads. A 3x3 array of 0.5 mm square stencil openings, on a 0.65 mm pitch, should be used for the center thermal pad.
6. A stencil thickness of 5 mil is recommended. The stencil should be laser cut and electropolished, with trapezoidal walls to facilitate paste release.
7. A “No-Clean”, Type 3 solder paste should be used for assembly. Nitrogen purge during reflow is recommended.
8. Do not place any signal or power plane vias in these “keep out” regions.
9. Suggest four 0.38 mm (15 mil) vias to the ground plane.

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Added "Top Mark," on page 17.
- Updated "Package Outline," on page 18.
- Added "4x4 mm 20L QFN Recommended PCB Layout," on page 19.

Revision 1.1 to Revision 1.2

- Made minor note corrections to "4x4 mm 20L QFN Recommended PCB Layout," on page 19.

Revision 1.2 to Revision 1.3

- Updated "Ordering Guide," on page 17.
- Updated "Package Outline," on page 18.

NOTES:

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