Bidirectional I²C Isolators with Unidirectional Digital Channels

Features

- Independent, bidirectional SDA and SCL isolation channels
  - Open drain outputs with 35 mA sink current
  - Supports I²C clocks up to 1.7 MHz
- Unidirectional isolation channels support additional system signals (Si8405)
- Up to 2500 V_{RMS} isolation
- UL, CSA, VDE recognition
- 60-year life at rated working voltage
- High electromagnetic immunity
- Wide operating supply voltage
  - 3.0 to 5.5 V
- Wide temperature range
  - –40 to +125 °C max
- Transient immunity 25 kV/µs
- RoHS-compliant packages
  - SOIC-8 narrow body
  - SOIC-16 narrow body



Ordering Information:
See page 25.

Applications

- Isolated I²C, SMBus
- Isolated digital power supply communications
- Power over Ethernet
- Motor Control Systems
- Hot-swap applications
- Intelligent Power systems

Description

The Si840x series of isolators are single-package galvanic isolation solutions for I²C and SMBus serial port applications. These products are based on Skyworks Solutions proprietary RF isolation technology and offer shorter propagation delays, lower power consumption, smaller installed size, and more stable operation with temperature and age versus opto couplers or other digital isolators.

All devices in this family include hot-swap, bidirectional SDA and SCL isolation channels with open-drain, 35 mA sink capability and operate to a maximum frequency of 1.7 MHz. The 8-pin version (Si8400/01) supports bidirectional SDA and SCL isolation; the Si8402 supports bidirectional SDA and unidirectional SCL isolation, and the 16-pin version (Si8405) features two unidirectional isolation channels to support additional system signals, such as an interrupt or reset. All versions contain protection circuits to guard against data errors if an unpowered device is inserted into a powered system.

Small size, low installed cost, low power consumption, and short propagation delays make the Si840x family the optimum solution for isolating I²C and SMBus serial ports.

Safety Regulatory Approval

- UL 1577 recognized
  - Up to 2500 V_{RMS} for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Not Recommended for New Designs

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1. Electrical Specifications

Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Ambient Temperature Under Bias	T_A	–40	—	125	°C
Supply Voltage (Revision A)[3]	V_{DD}	–0.5	—	5.75	V
Supply Voltage (Revision B)[3]	V_{DD}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive (non-I^2C channels)	I_O	—	—	±10	mA
Side A output current drive (I^2C channels)	I_O	—	—	±15	mA
Side B output current drive (I^2C channels)	I_O	—	—	±75	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.
3. See "7.Ordering Guide" on page 25 for more information.

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Table 2. Si840x Power Characteristics*

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C (See Figures 2 and 16 for test diagrams.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8400/01/02 Supply Current						
AVDD current BVDD current	Idda Iddb	All channels = 0 dc	— —	4.2 3.9	6.3 5.9	mA mA
AVDD current BVDD current	Idda Iddb	All channels = 1 dc	— —	2.3 1.9	3.5 2.9	mA mA
AVDD current BVDD current	Idda Iddb	All channels = 1.7 MHz	— —	3.2 2.9	4.8 4.4	mA mA
Si8405 Supply Current						
AVDD current BVDD current	Idda Iddb	All non-I^2C channels = 0 All I^2C channels = 1	— —	3.2 2.9	4.8 4.4	mA mA
AVDD current BVDD current	Idda Iddb	All non-I^2C channels = 1 All I^2C channels = 0	— —	6.2 6.0	9.3 9.0	mA mA
AVDD current BVDD current	Idda Iddb	All non-I^2C channels = 5 MHz All I^2C channels = 1.7 MHz	— —	4.7 4.5	7.1 6.8	mA mA

***Note:** All voltages are relative to respective ground.

Table 3. Si8400/01/02/05 Electrical Characteristics for Bidirectional I^2C Channels[1]

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Logic Levels Side A						
Logic Input Threshold[2]	I^2CV_T (Side A)		450	—	780	mV
Logic Low Output Voltages[3]	I^2CV_{OL} (Side A)	ISDAA = ISCLA = 3.0 mA	650	—	910	mV
		ISDAA = ISCLA = 0.5 mA	550	—	825	mV
Input/Output Logic Low Level Difference[4]	$I^2C\Delta V$ (Side A)		50	—	—	mV
Logic Levels Side B						
Logic Low Input Voltage	I^2CV_{IL} (Side B)		—	—	0.8	V
Logic High Input Voltage	I^2CV_{IH} (Side B)		2.0	—	—	V
Logic Low Output Voltage	I^2CV_{OL} (Side B)	ISCLB = 35 mA	—	—	400	mV
SCL and SDA Logic High Leakage	Isdaa, Isdab Iscla, Isclb	SDAA, SCLA = VSSA SDAB, SCLB = VSSB	—	2.0	10	µA
Pin capacitance SDAA, SCLA, SDAB, SDBB	CA CB		— —	10 10	— —	pF pF

Notes:

1. All voltages are relative to respective ground.
2. V_{IL} < 0.450 V, V_{IH} > 0.780 V.
3. Logic low output voltages are 910 mV max from –10 to 125 °C at 3.0 mA.
   Logic low output voltages are 955 mV max from –40 to 125 °C at 3.0 mA.
   Logic low output voltages are 825 mV max from –10 to 125 °C at 0.5 mA.
   Logic low output voltages are 875 mV max from –40 to 125 °C at 0.5 mA.
   See “AN375: Design Considerations for Isolating an I^2C Bus or SMBus” for additional information.
4. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
5. Side A measured at 0.6 V.

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Table 3. Si8400/01/02/05 Electrical Characteristics for Bidirectional I²C Channels[1] (Continued)
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Specifications (Measured at 1.40 V Unless Otherwise Specified)						
Maximum I²C bus Frequency	Fmax		—	—	1.7	MHz
Propagation Delay						
5 V Operation						
Side A to side B rising[5]	Tphab	No bus capacitance,	—	25	29	ns
Side A to side B falling[5]	Tplab	R1 = 1400,	—	15	22	ns
Side B to side A rising	Tphba	R2 = 499,	—	20	30	ns
Side B to side A falling	Tplba	See Figure 2	—	9.0	12	ns
3.3 V Operation						
Side A to side B rising[5]	Tphab		—	28	35	ns
Side A to side B falling[5]	Tplab	R1 = 806	—	13	18	ns
Side B to side A rising	Tphba	R2 = 499	—	20	40	ns
Side B to side A falling	Tplba		—	10	15	ns
Pulse width distortion		No bus capacitance,				
5 V		R1 = 1400,				
Side A low to Side B low[5]	PWDAB	R2 = 499,	—	9.0	15	ns
Side B low to Side A low	PWDBA	See Figure 2	—	11	20	ns
3.3 V						
Side A low to Side B low[5]	PWDAB	R1 = 806,	—	15	22	ns
Side B low to Side A low	PWDBA	R2 = 499	—	11	30	ns

Notes:
1. All voltages are relative to respective ground.
2. V_{IL} < 0.450 V, V_{IH} > 0.780 V.
3. Logic low output voltages are 910 mV max from –10 to 125 °C at 3.0 mA.
   Logic low output voltages are 955 mV max from –40 to 125 °C at 3.0 mA.
   Logic low output voltages are 825 mV max from –10 to 125 °C at 0.5 mA.
   Logic low output voltages are 875 mV max from –40 to 125 °C at 0.5 mA.
   See “AN375: Design Considerations for Isolating an I²C Bus or SMBus” for additional information.
4. $I^2C\Delta V$ (Side A) = I^2CV_{OL} (Side A) – I^2CV_T (Side A). To ensure no latch-up on a given bus, $I^2C\Delta V$ (Side A) is the minimum difference between the output logic low level of the driving device and the input logic threshold.
5. Side A measured at 0.6 V.

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Table 4. Electrical Characteristics for Unidirectional Non-I²C Digital Channels (Si8402/05)
3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	AVDD, BVDD –0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Timing Characteristics						
Maximum Data Rate			0	—	10	Mbps
Minimum Pulse Width			—	—	40	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	20	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	12	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	20	ns
Channel-Channel Skew	t_{PSK}		—	—	10	ns
Output Rise Time	t_r	C_3 = 15 pF See Figure 1 and Figure 2	—	4.0	6.0	ns
Output Fall Time	t_f	C_3 = 15 pF See Figure 1 and Figure 2	—	3.0	4.3	ns

Notes:
1. The nominal output impedance of a non-I²C isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.

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Table 5. Electrical Characteristics for All I²C and Non-I²C Channels

3.0 V < VDD < 5.5 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	AVDD, BVDD rising	2.15	2.3	2.5	V
VDD Negative-going Lockout Hysteresis	VDDH–	AVDD, BVDD falling	45	75	95	mV
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Shut Down Time from UVLO	t_{SD}		—	3.0	—	µs
Start-up Time*	t_{START}		—	15	40	µs
***Note:** Start-up time is the time period from the application of power to valid data at the output.						

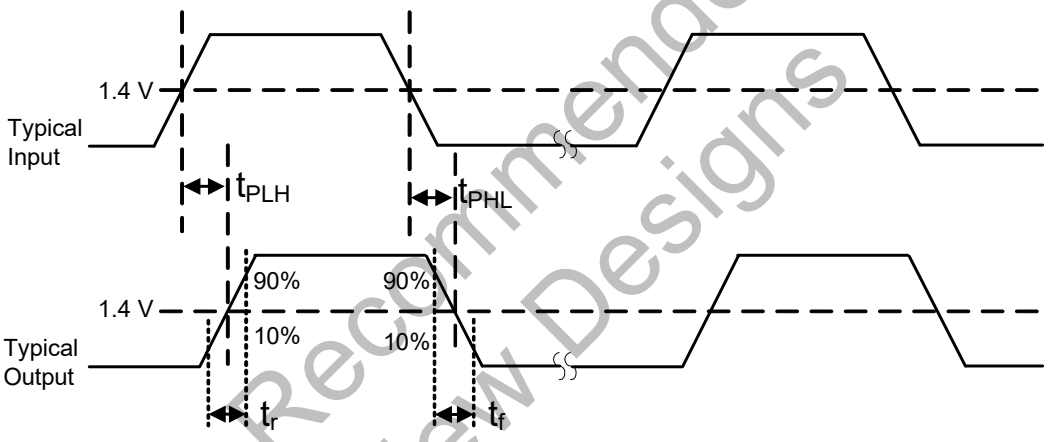


Figure 1. Propagation Delay Timing (Non-I²C Channels)

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1.1. Test Circuits

Figure 2 depicts the timing test diagram.

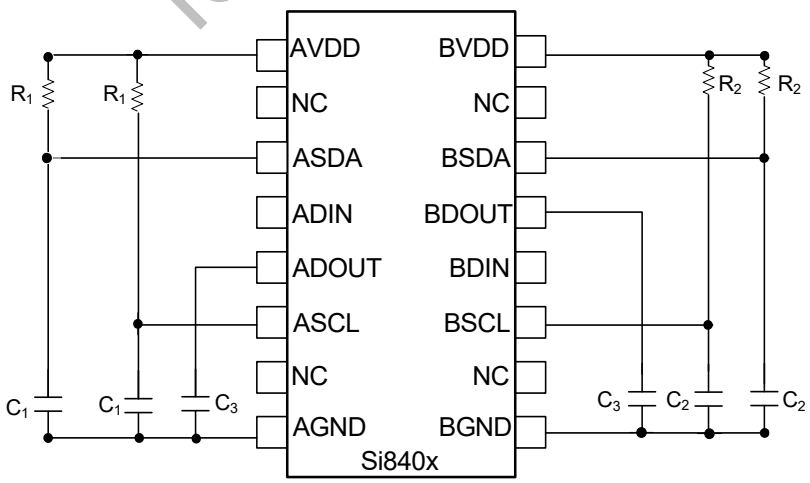


Figure 2. Simplified Timing Test Diagram

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 300 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 130 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 2500 V_{RMS} isolation voltage for basic insulation.
***Note:** Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. For more information, see "7.Ordering Guide" on page 25.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			NB SOIC-8	NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(1O1)		4.9	4.9	mm
Nominal External Tracking (Creepage)[1]	L(1O2)		4.01	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.008	0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.040	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:
1. The values in this table correspond to the nominal creepage and clearance values as detailed in “8. Package Outline: 8-Pin Narrow Body SOIC” and “10. Package Outline: 16-Pin Narrow Body SOIC”. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-8 package and 4.7 mm minimum for the NB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 package and 3.9 mm minimum for the NB SOIC-16 package.
2. To determine resistance and capacitance, the Si840x, SO-16, is converted into a 2-terminal device. Pins 1–8 (1-4, SO-8) are shorted together to form the first terminal and pins 9–16 (5–8, SO-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

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Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

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Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
Case Temperature	T_S		150	150	°C
Safety Input Current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), 140 °C/W (NB SOIC-8) AVDD, BVDD = 5.5 V, T_J = 150 °C, T_A = 25 °C	160	210	mA
Device Power Dissipation[2]	P_D		220	275	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 3 and Figure 4.
2. The Si840x is tested with AVDD, BVDD = 5.5 V; T_J = 150 ºC; C_1, C_2 = 0.1 µF; C_3 = 15 pF; R1, R2 = 3kΩ; input 1 MHz 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	NB SOIC-8	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		140	105	°C/W

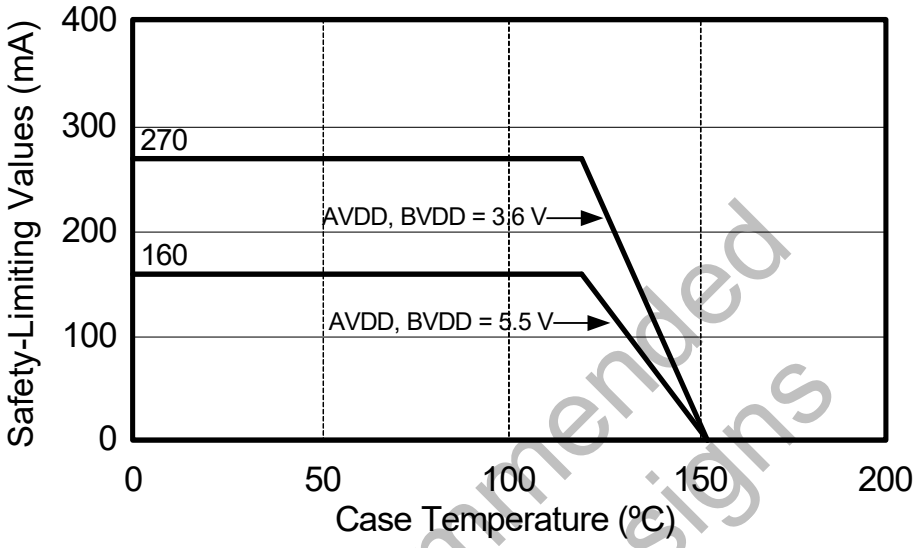


Figure 3. NB SOIC-8 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

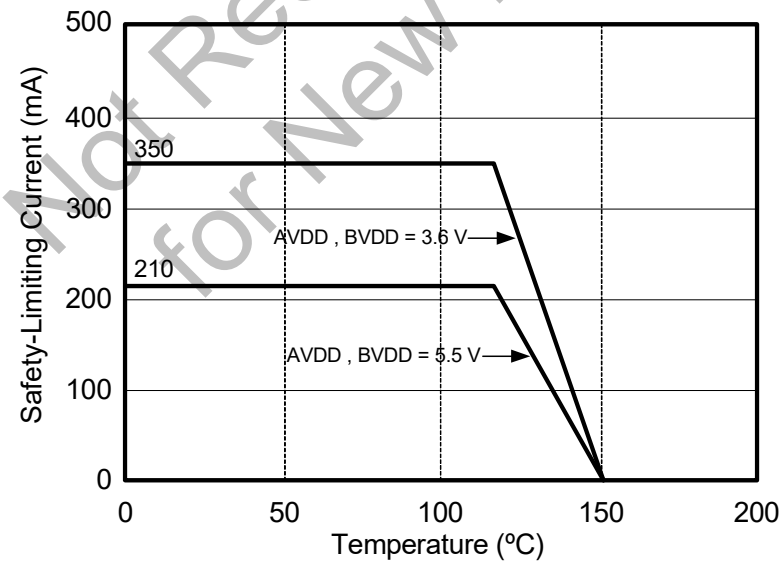


Figure 4. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

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2. Functional Description

2.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single unidirectional Si84xx channel is shown in Figure 5.

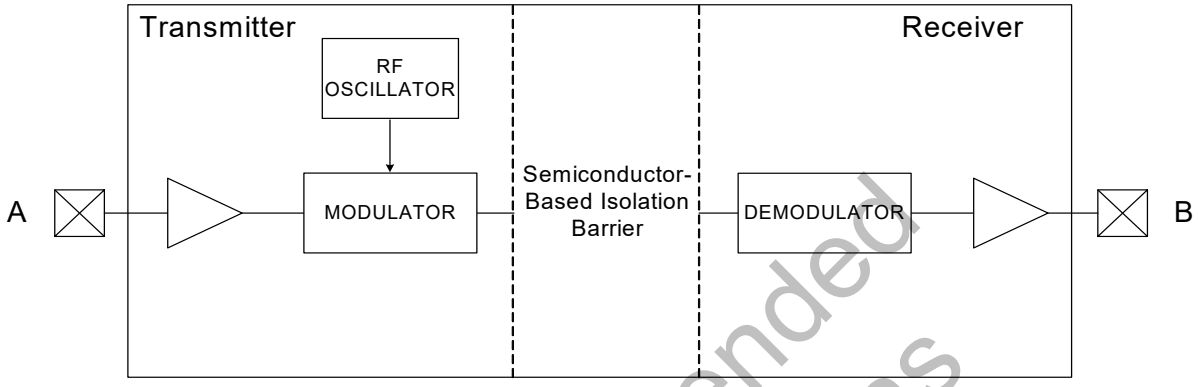


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

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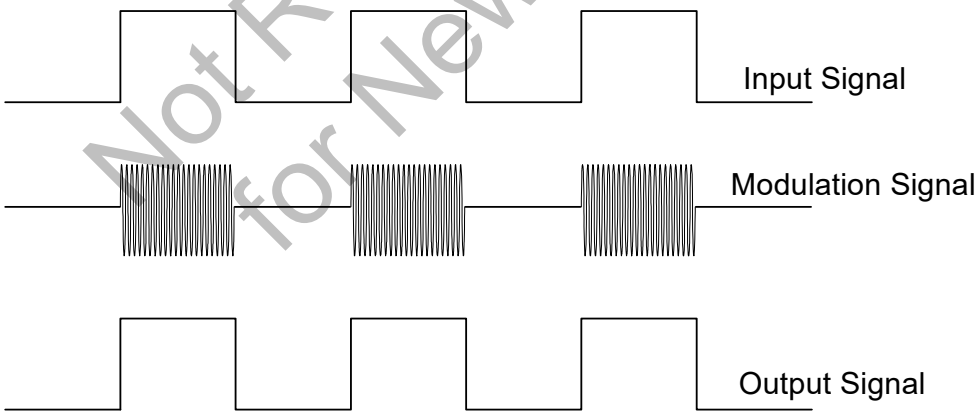


Figure 6. Modulation Scheme

3. Device Operation

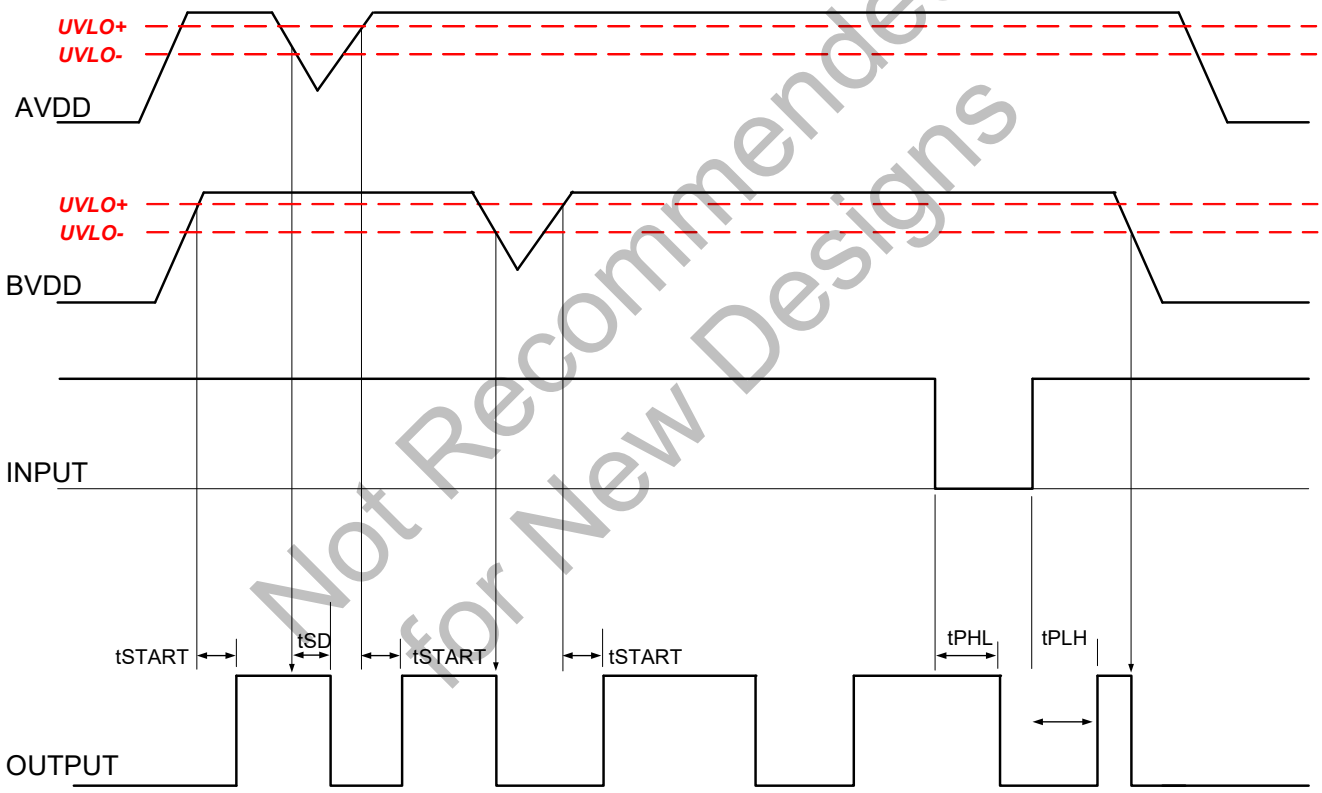
Device behavior during start-up, normal operation, and shutdown is shown in Figure 7, where UVLO+ and UVLO– are the positive-going and negative-going thresholds respectively. Refer to Table 12 to determine outputs when power supply (VDD) is not present.

3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own under voltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when AVDD falls below $AVDD_{UVLO-}$ and exits UVLO when AVDD rises above $AVDD_{UVLO+}$. Side B operates the same as Side A with respect to its BVDD supply.



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Figure 7. Device Behavior during Normal Operation

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 6 on page 9 and Table 7 on page 9 detail the working voltage and creepage/clearance capabilities of the Si84xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

3.3.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 Ω resistors in series with the VDD supply voltage source and 50 to 300 Ω resistors in series with the digital inputs/outputs (see Figure 8). For more details, see "5.Errata and Design Migration Guidelines" on page 22.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 Ω resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 3, “Si8400/01/02/05 Electrical Characteristics for Bidirectional I2C Channels[1],” on page 5. and Table 4, “Electrical Characteristics for Unidirectional Non-I2C Digital Channels (Si8402/05),” on page 7.

3.3.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

3.3.3. Output Pin Termination

The nominal output impedance of an non-I^2C isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “3.3.1. Supply Bypass” above.

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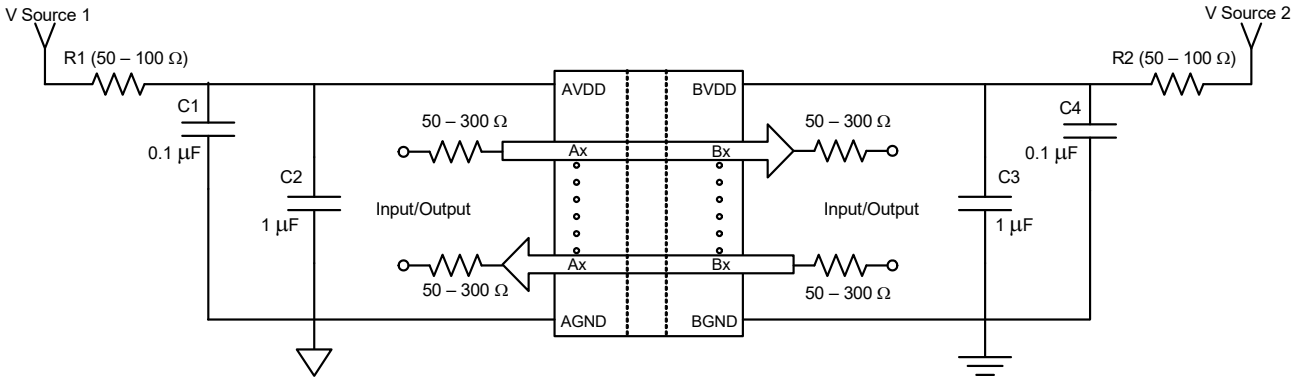


Figure 8. Recommended Bypass Components for the Si84xx Digital Isolator Family

3.4. Input and Output Characteristics for Non-I²C Digital Channels

The Si84xx inputs and outputs for unidirectional channels are standard CMOS drivers/receivers. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. Table 12 details powered and unpowered operation of the Si84xx's non-I²C digital channels.

Table 12. Si84xx Operation Table

V_I Input[1,2]	VDDI State[1,3,4]	VDDO State[1,3,4]	V_O Output[1,2]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low.
3. Powered (P) state is defined as 3.0 V < VDD < 5.5 V.
4. Unpowered (UP) state is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. For I²C channels, the outputs for a given side go to Hi-Z when power is lost on the opposite side.

Not Recommended for New Designs

3.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 2, 3, 4, and 5 for actual specification limits.

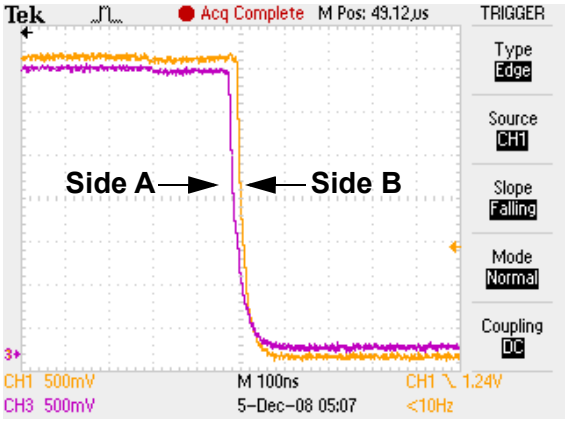


Figure 9. I²C Side A Pulling Down (1100 Ω Pull-Up)

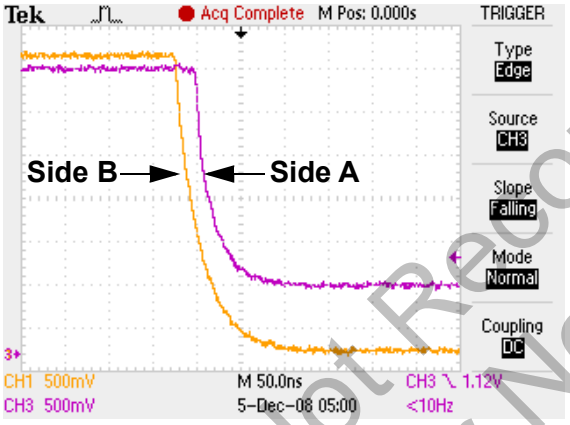


Figure 10. I²C Side B Pulling Down

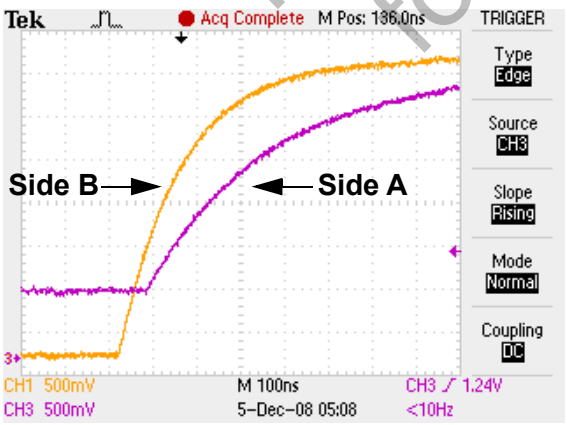


Figure 11. I²C Side B Pulling Up, Side A Following

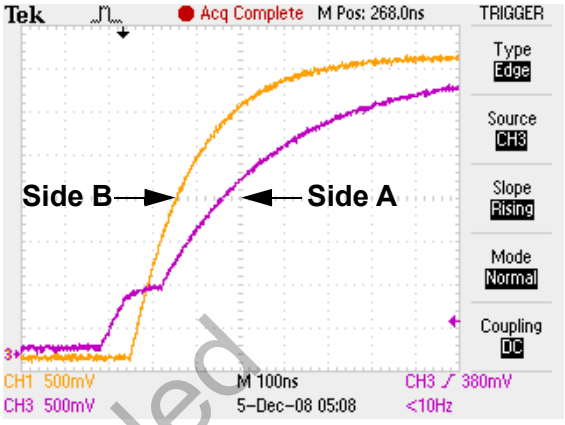


Figure 12. I²C Side A Pulling Up, Side B Following

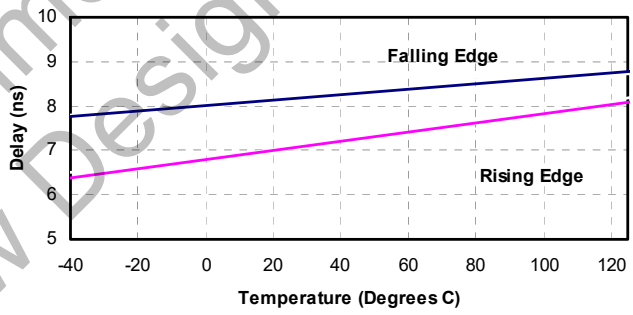


Figure 13. Non I²C Channel Propagation Delay vs. Temperature

Not Recommended for New Designs

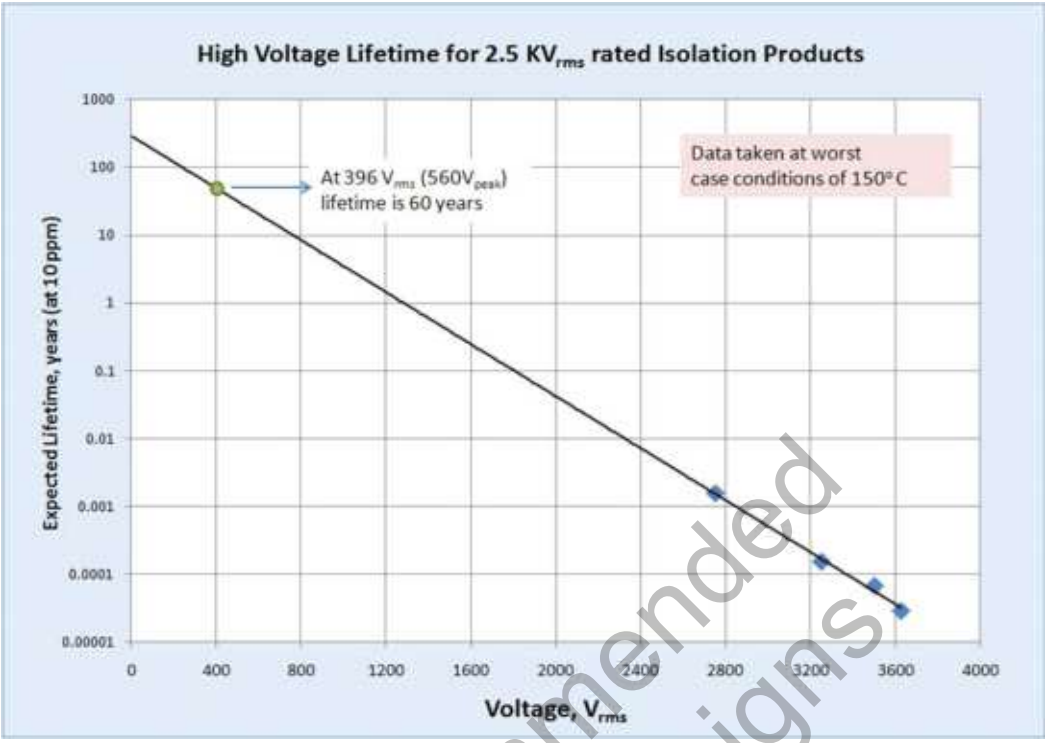


Figure 14. Si84xx Time-Dependent Dielectric Breakdown

Not Recommended for New Designs

4. Typical Application Overview

4.1. I²C Background

In many applications, I²C, SMBus, and other digital power supply communications, including those for bus power management, the interfaces require galvanic isolation for safety or ground loop elimination. For example, Power over Ethernet (PoE) applications typically use an I²C interface for communication between the PoE power sourcing device (PSE), and the earth ground referenced system controller. Galvanic isolation is required both by standard and also as a practical matter to prevent ground loops in Ethernet connected equipment.

The physical interface consists of two wires: serial data (SDA) and serial clock (SCL). These wires are connected to open collector drivers that serve as both inputs and outputs. At first glance, it appears that SDA and SCL can be isolated simply by placing two unidirectional isolators in parallel, and in opposite directions. However, this technique creates feedback that latches the bus line low when a logic low asserted by either master or slave. This problem can be remedied by adding anti-latch circuits, but results in a larger and more expensive solution. The Si840x products offer a single-chip, anti-latch solution to the problem of isolating I²C/SMBus applications and require no external components except the I²C/SMBus pull-up resistors. In addition, they provide isolation to a maximum of 2.5 kV_{RMS}, support I²C clock stretching, and operate to a maximum I²C bus speed of 1.7 Mbps.

4.2. I²C Isolator Operation

Without anti-latch protection, bidirectional I²C isolators latch when an isolator output logic low propagates back through an adjacent isolator channel creating a stable latched low condition on both sides. Anti-latch protection is typically added to one side of the isolator to avoid this condition (the “A” side for the Si8400/01/02/05).

The following examples illustrate typical circuit configurations using the Si8400/01/02/05.

Not Recommended for New Designs

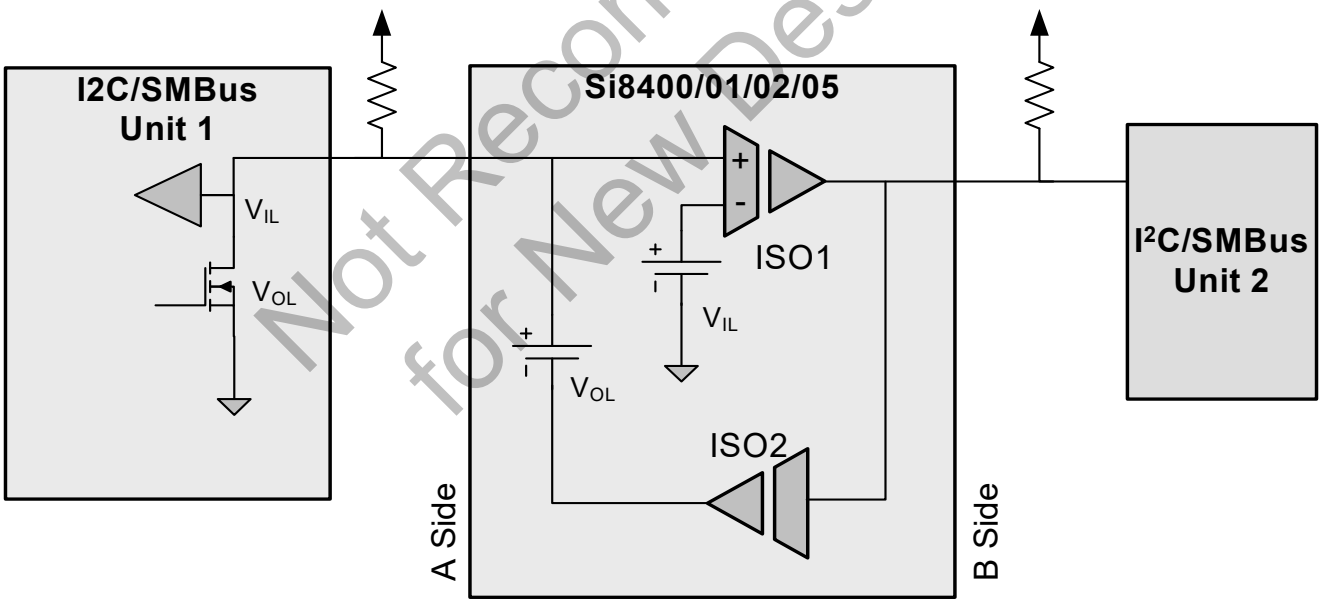


Figure 15. Isolated Bus Overview (Bidirectional Channels)

The “A side” output low (V_{OL}) and input low (V_{IL}) levels are designed such that the isolator V_{OL} is greater than the isolator V_{IL} to prevent the latch condition.

4.3. I²C Isolator Design Constraints

Table 13 lists the design constraints.

Table 13. Design Constraints

Design Constraint	Data Sheet Values	Effect of Bus Pull-up Strength and Temperature
To prevent the latch condition, the isolator output low level must be greater than the isolator input low level.	Isolator V_{OL} 0.8 V typical Isolator V_{IL} 0.6 V typical Input/Output Logic Low Level Difference ΔVSDA1, ΔVSCL1 = 50 mV minimum	This is normally guaranteed by the isolator data sheet. However, if the pull up strength is too weak, the output low voltage will fall and can get too close to the input low logic level. These track over temperature.
The bus output low must be less than the isolator input low logic level.	Bus V_{OL} = 0.4 V maximum Isolator V_{IL} = 0.45 V minimum	If the pull up strength is too large, the devices on the bus might not pull the voltage below the input low range. These have opposite temperature coefficients. Worst case is hot temperature.
The isolator output low must be less than the bus input low.	Bus V_{IL} 0.3 x V_{DD} = 1.0 V minimum for V_{DD} = 3.3 V Isolator V_{OL} = 0.825 V maximum, (0.5 mA pullup, –10 to 125 °C)	If the pull up strength is too large, the isolator might not pull below the bus input low voltage. Si8400/01/05 Vol: –1.8 mV/C CMOS buffer: –0.6 mV/C This provides some temperature tracking, but worst case is cold temperature.

Not Recommended for New Designs

4.4. I²C Isolator Design Considerations

The first step in applying an I²C isolator is to choose which side of the bus will be connected to the isolator A side. Ideally, it should be the side which:

1. Is compatible with the range of bus pull up specified by the manufacturer. For example, the Si8400/01/02/05 isolators are normally used with a pull up of 0.5 mA to 3 mA.
2. Has the highest input low level for devices on the bus. Some devices may specify an input low of 0.9 V and other devices might require an input low of 0.3 x Vdd. Assuming a 3.3 V minimum power supply, the side with an input low of 0.3 x Vdd is the better side because this side has an input low level of 1.0 V.
3. Have devices on the bus that can pull down below the isolator input low level. For example, the Si840x input level is 0.45 V. As most CMOS devices can pull to within 0.4 V of GND this is generally not an issue.
4. Has the lowest noise. Due to the special logic levels, noise margins can be as low as 50 mV.

The Si840x isolators are not compatible with devices that have a logic low of 0.8 V. For this situation, a discrete circuit can be used. See “AN352: Low-Cost, High-Speed I²C Isolation with Digital Isolators” for additional information.

Figures 16, 17, 18, and 19 illustrate typical circuit configurations using the Si8400, Si8401, Si8402 and Si8405.

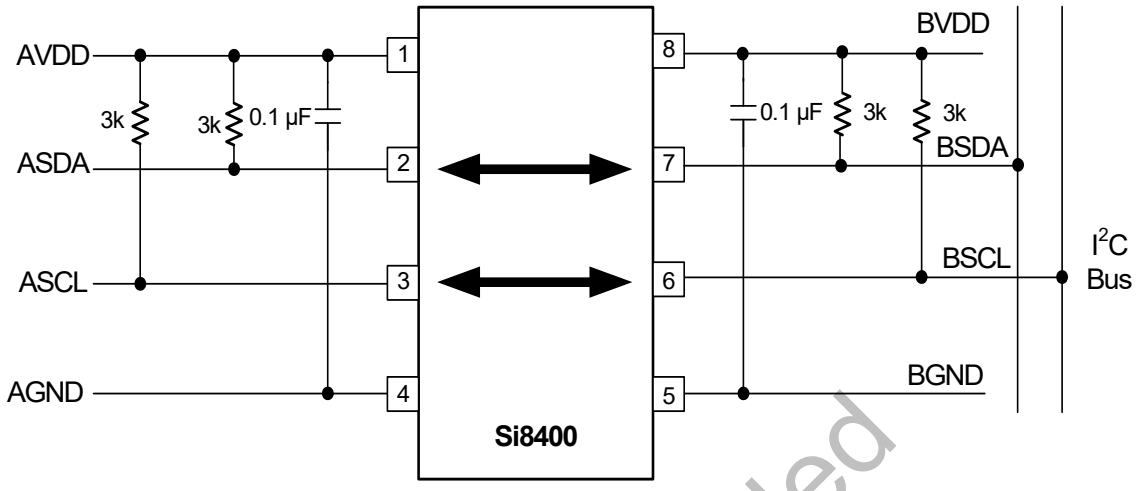


Figure 16. Typical Si8400 Application Diagram

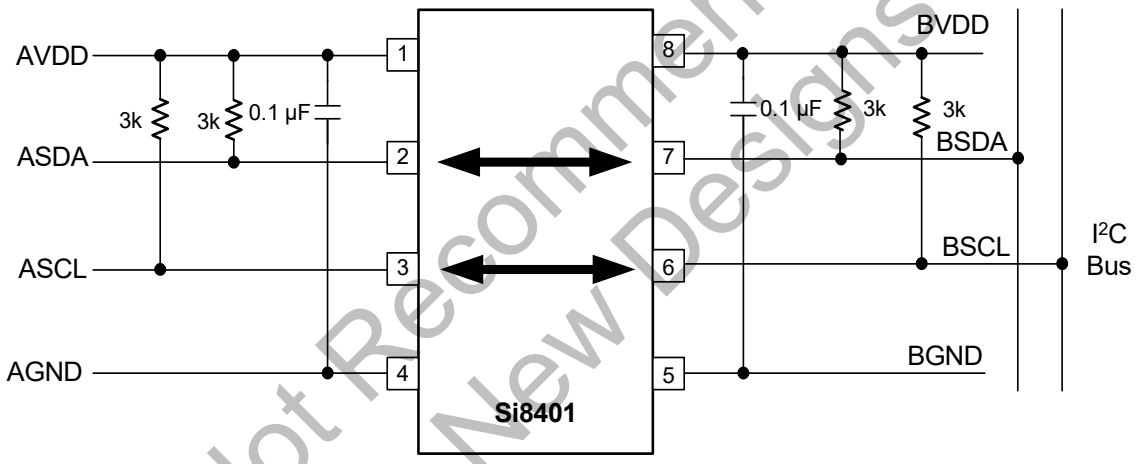


Figure 17. Typical Si8401 Application Diagram

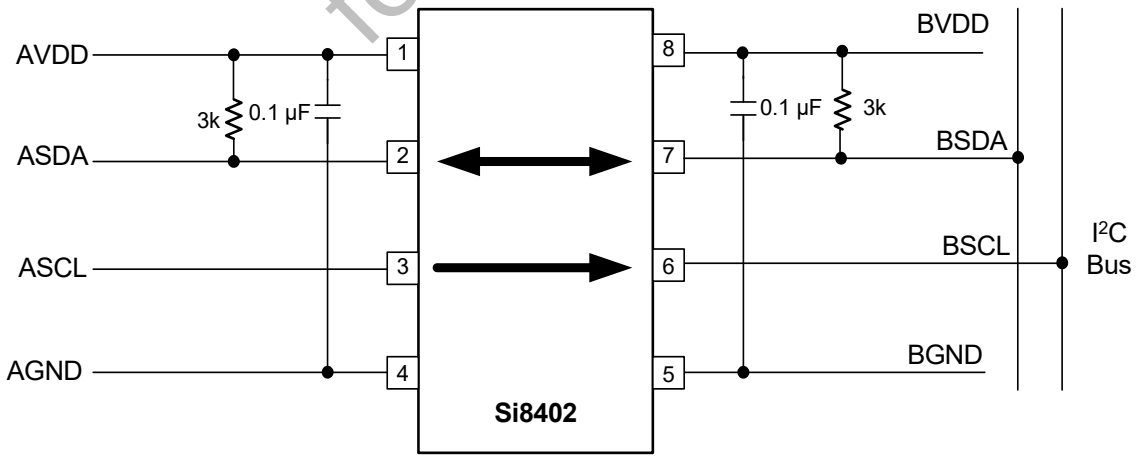


Figure 18. Typical Si8402 Application Diagram

Not Recommended for New Designs

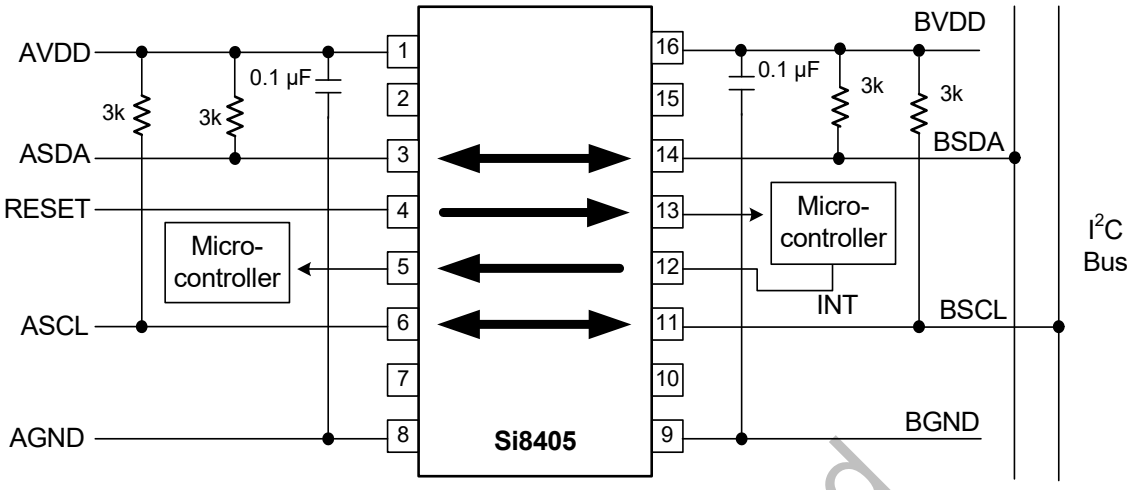


Figure 19. Typical Si8405 Application Diagram

Not Recommended for New Designs

5. Errata and Design Migration Guidelines

The following errata apply to Revision A devices only. See "7.Ordering Guide" on page 25 for more details. No errata exist for Revision B devices.

5.1. Power Supply Bypass Capacitors (Revision A and Revision B)

When using the Si840x isolators with power supplies ≥ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a ≥ 4.5 V supply). Although rise time is power supply dependent, ≥ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

5.1.1. Resolution

For recommendations on resolving this issue, see "3.3.1.Supply Bypass" on page 14. Additionally, refer to "7.Ordering Guide" on page 25 for current ordering information.

Not Recommended for New Designs

6. Pin Descriptions

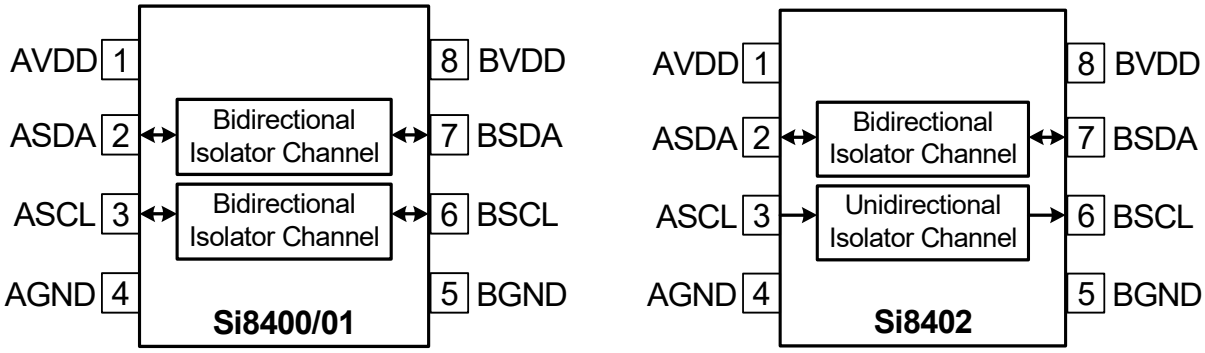


Table 14. Si8400/01/02 in SO-8 Package

Pin	Name	Description
1	AVDD	Side A power supply terminal; connect to a source of 3.0 to 5.5 V.
2	ASDA	Side A data (open drain) input or output.
3	ASCL	Side A clock input or output. Open drain I/O for Si8400/01. Standard CMOS input for Si8402.
4	AGND	Side A ground terminal.
5	BGND	Side B ground terminal.
6	BSCL	Side B clock input or output. Open drain I/O for Si8400/01. Push-pull output for Si8402.
7	BSDA	Side B data (open drain) input or output.
8	BVDD	Side B power supply terminal; connect to a source of 3.0 to 5.5 V.

Not Recommended for New Designs

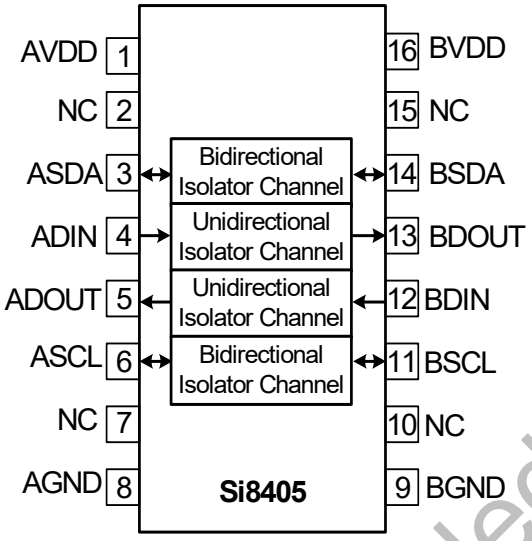


Table 15. Si8405 in Narrow-Body SO-16 Package

Pin	Name	Description
1	AVDD	Side A Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.
2	NC	No connection.
3	ASDA	Side A Data (open drain) Input or Output.
4	ADIN	Side A Standard CMOS Digital Input (non I^2C).
5	ADOUT	Side A Digital Push-Pull Output (non I^2C).
6	ASCL	Side A Clock (open drain) Input or Output.
7	NC	No connection.
8	AGND	Side A Ground Terminal.
9	BGND	Side B Ground Terminal.
10	NC	No connection.
11	BSCL	Side B Clock (open drain) Input or Output.
12	BDIN	Side B Standard CMOS Digital Input (non I^2C).
13	BDOUT	Side B Digital Push-Pull Output (non I^2C).
14	BSDA	Side B Data (open drain) Input or Output.
15	NC	No connection.
16	BVDD	Side B Power Supply Terminal. Connect to a source of 3.0 to 5.5 V.

Not Recommended for New Designs

7. Ordering Guide

These devices are not recommended for new designs. Please see the Si860x datasheet for replacement options.

Table 16. Ordering Guide[1]

Ordering Part Number (OPN)	Alternative Part Number (APN)	Number of Bidirectional I^2C Channels	Max I^2C Bus Speed (MHz)	Number of Unidirectional Channels	Max Data Rate of Non-I^2C Unidirectional Channels (Mbps)	Isolation Ratings	Package
Revision B Devices[2]							
Si8400AA-B-IS	Si8600AB-B-IS	2	1.7	0	—	1 kV_{RMS}	NB SOIC-8
Si8400AB-B-IS	Si8600AB-B-IS	2	1.7	0	—	2.5 kV_{RMS}	NB SOIC-8
Si8401AA-B-IS	Si8602AB-B-IS	1	1.7	1	—	1 kV_{RMS}	NB SOIC-8
Si8401AB-B-IS	Si8602AB-B-IS	1	1.7	1	—	2.5 kV_{RMS}	NB SOIC-8
Si8402AB-B-IS	Si8602AB-B-IS	1	1.7	1	10	2.5 kV_{RMS}	NB SOIC-8
Si8405AA-B-IS1	Si8605AB-B-IS1	2	1.7	1 forward 1 reverse	10	1 kV_{RMS}	NB SOIC-16
Si8405AB-B-IS1	Si8605AB-B-IS1	2	1.7	1 forward 1 reverse	10	2.5 kV_{RMS}	NB SOIC-16
Revision A Devices[2]							
Si8400AA-A-IS	Si8600AB-B-IS	2	1.7	0	—	1 kV_{RMS}	NB SOIC-8
Si8400AB-A-IS	Si8600AB-B-IS	2	1.7	0	—	2.5 kV_{RMS}	NB SOIC-8
Si8405AA-A-IS1	Si8605AB-B-IS1	2	1.7	1 forward 1 reverse	10	1 kV_{RMS}	NB SOIC-16
Si8405AB-A-IS1	Si8605AB-B-IS1	2	1.7	1 forward 1 reverse	10	2.5 kV_{RMS}	NB SOIC-16

Notes:

1. All packages are RoHS-compliant. Moisture sensitivity level is MSL2A with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.
2. Revision A and Revision B devices are supported for existing designs.

Not Recommended for New Designs

8. Package Outline: 8-Pin Narrow Body SOIC

Figure 20 illustrates the package details for the Si840x in an 8-pin SOIC (SO-8). Table 17 lists the values for the dimensions shown in the illustration.

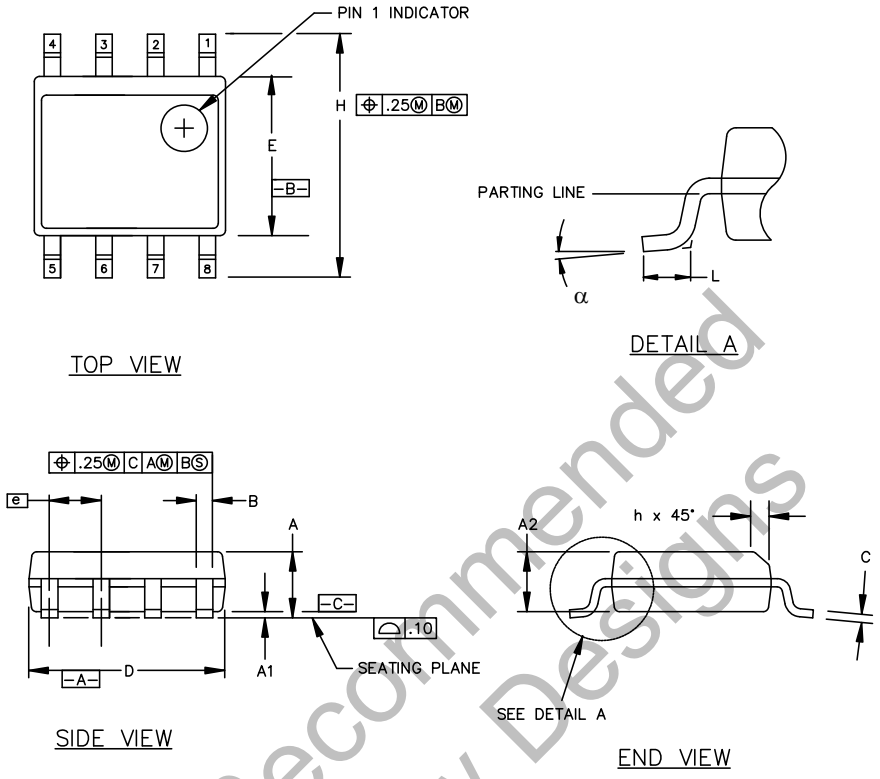


Figure 20. 8-pin Small Outline Integrated Circuit (SOIC) Package

Table 17. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

Not Recommended for New Designs

9. Land Pattern: 8-Pin Narrow Body SOIC

Figure 21 illustrates the recommended land pattern details for the Si840x in an 8-pin narrow-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

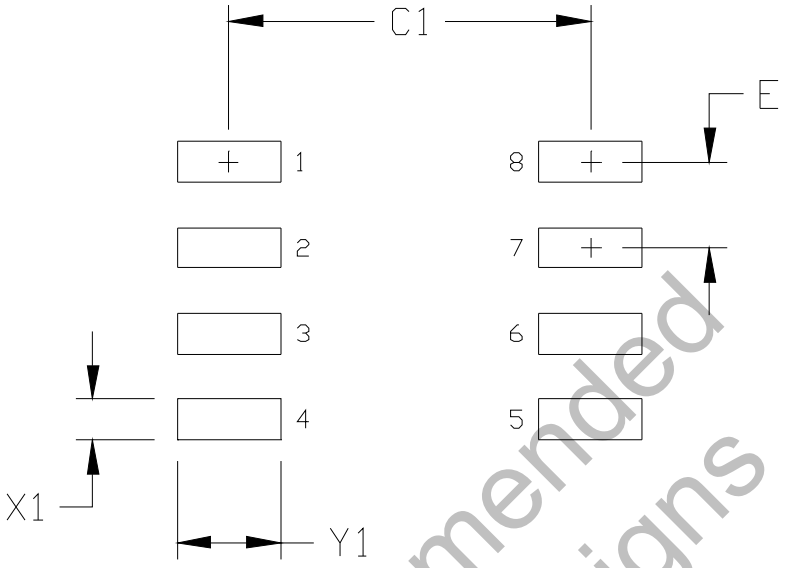


Figure 21. PCB Land Pattern: 8-Pin Narrow Body SOIC

Table 18. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

Not Recommended for New Designs

10. Package Outline: 16-Pin Narrow Body SOIC

Figure 22 illustrates the package details for the Si840x in a 16-pin narrow-body SOIC (SO-16). Table 19 lists the values for the dimensions shown in the illustration.

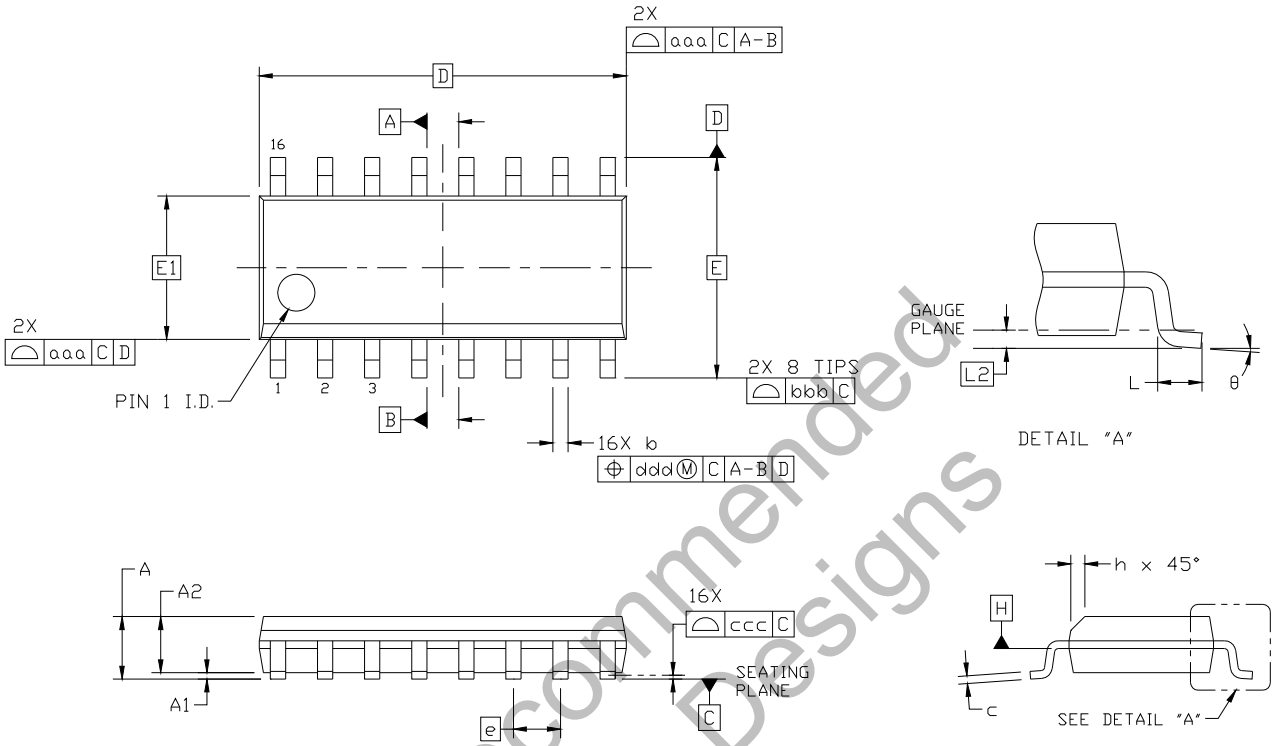


Figure 22. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 19. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Not Recommended for New Designs

Table 19. Package Diagram Dimensions (Continued)

Dimension	Min	Max
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

11. Land Pattern: 16-Pin Narrow Body SOIC

Figure 23 illustrates the recommended land pattern details for the Si840x in a 16-pin narrow-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

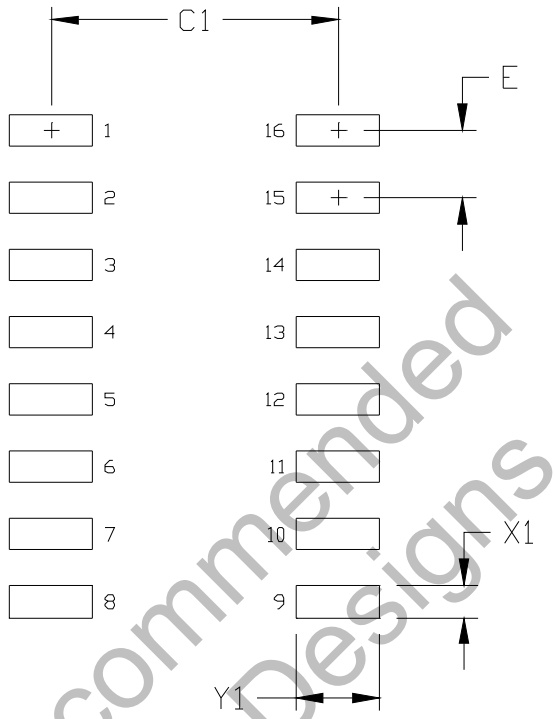


Figure 23. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 20. 16-Pin Narrow Body SOIC Land Pattern Dimensions

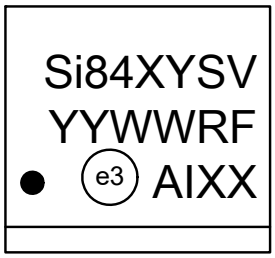
Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

Not Recommended for New Designs

12. Top Marking: 8-Pin Narrow Body SOIC

12.1. 8-Pin Narrow Body SOIC Top Marking



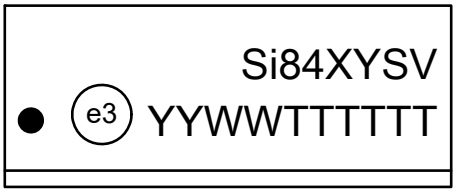
12.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator I^2C Product Series: ■ XY = Channel Configuration • 00 = Bidirectional SCL and SDA channels • 01/02 = Bidirectional SDA channel; Unidirectional SCL channel ■ S = Speed Grade • A = 1.7 Mbps ■ V = Isolation rating • A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Work week	Assigned by assembly contractor. Corresponds to the year and work week of the mold date.
	R = Product Rev F = Wafer Fab	First two characters of the manufacturing code from Assembly.
Line 3 Marking:	Circle = 1.1 mm Diameter Left-Justified	“e3” Pb-Free Symbol
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the manufacturing code from assembly.

Not Recommended for New Designs

13. Top Marking: 16-Pin Narrow Body SOIC

13.1. 16-Pin Narrow Body SOIC Top Marking



13.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options	Si84 = Isolator product series ■ XY = Channel Configuration • 05 = Bidirectional SCL, SDA; 1- forward and 1-reverse unidirectional channel ■ S = Speed Grade • A = 1.7 Mbps ■ V = Isolation rating • A = 1 kV; B = 2.5 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	"e3" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	"e3" Pb-Free Symbol.

Not Recommended for New Designs

Document Change List

Revision 0.1 to Revision 1.0

- Updated document to reflect availability of Revision B silicon.
- Updated Tables 2, 3, 4, and 5.
  - Updated all supply currents and timing parameters.
  - Revised logic low output voltage specifications in Table 3.
- Updated Table 1.
  - Updated absolute maximum supply voltage.
- Updated Table 7.
  - Updated clearance and creepage dimensions.
- Updated "5.Errata and Design Migration Guidelines" on page 22.
- Updated "7.Ordering Guide" on page 25.

Revision 1.0 to Revision 1.1

- Updated Table 4.
  - Updated Note 1 to reflect output impedance of 85 Ω.
  - Updated rise and fall time specifications.
- Updated Table 5.
  - Updated CMTI value.
- Updated “7. Ordering Guide”.
- Added Si8401 device configuration throughout document.

Revision 1.1 to Revision 1.2

- Updated document throughout to include MSL improvements to MSL2A.
- Updated "7.Ordering Guide" on page 25.
  - Updated Note 1 in ordering guide table to reflect improvement and compliance to MSL2A moisture sensitivity level.

Revision 1.2 to Revision 1.3

- Added Si8402 throughout document. Clarified description of Si8401’s BSCL pin to indicate pin type is an open output, whereas the Si8402’s BSCL pin is a push-pull CMOS pin.
- Updated "7.Ordering Guide" on page 25 to include Si8402.
- Moved Table 1 to page 4.
- Updated Tables 6, 7, 8, and 9.
- Updated Table 12 footnotes.
- Added Figure 14, “Si84xx Time-Dependent Dielectric Breakdown,” on page 17.
- Added Figure 18, “Typical Si8402 Application Diagram,” on page 20.

Revision 1.3 to Revision 1.4

- Updated "3.3.1.Supply Bypass" on page 14.
- Added Figure 8, “Recommended Bypass Components for the Si84xx Digital Isolator Family,” on page 14.
- Updated "5.1.Power Supply Bypass Capacitors (Revision A and Revision B)" on page 22.

Revision 1.4 to Revision 1.5

- Updated "7.Ordering Guide" on page 25 to include new title note and “ Alternative Part Number (APN)” column.

Revision 1.5 to Revision 1.6

- Updated part numbers on page 1 and in pin descriptions images.

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