Features

- **Fully Integrated TX/RX with VCO**
- **Fast Settling Synthesizer**
- **Unlimited Multi-slot Operation with Advanced Closed-loop Modulation**
- **No Mechanical Tuning Required**
- **Low Current Consumption**
- **Auxiliary Voltage Regulator On-chip (3.2 V to 4.6 V)**
- **Supply-voltage Range 3 V to 4.6 V (Regulated)**
- **Ramp-signal Generator for Power Ramping and Power Control of External SiGe Power Amplifier (T7024 and T7026)**
- **Supports Multiple Reference Clocks (10.368 MHz/13.824 MHz/20.736 MHz/27.648 MHz)**
- **TX Preamplifier with 3 dBm Output Power at 2.45 GHz**
- **Few Low-cost External Components**

Electrostatic sensitive device.
Observe precautions for handling.

2.4 GHz WDECT/ISM Single-chip Transceiver

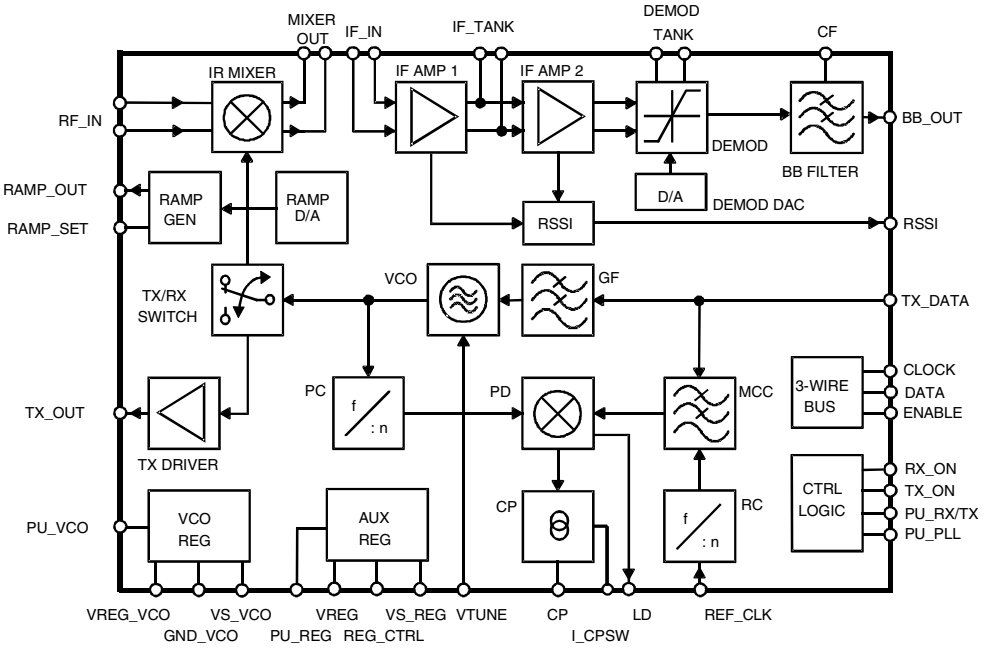
T2802

Preliminary

Description

The T2802 is an RF IC for low-power applications in the 2.45 GHz ISM band. The QFN48-packaged IC is a complete transceiver including image rejection mixer, IF amplifier, FM demodulator, baseband filter, RSSI, TX preamplifier, power-ramping generator for power amplifiers, integrated synthesizer, fully integrated VCO, TX filter and modulation compensation circuit for advanced closed-loop modulation concept. No mechanical tuning is necessary in production.

Figure 1. Block Diagram



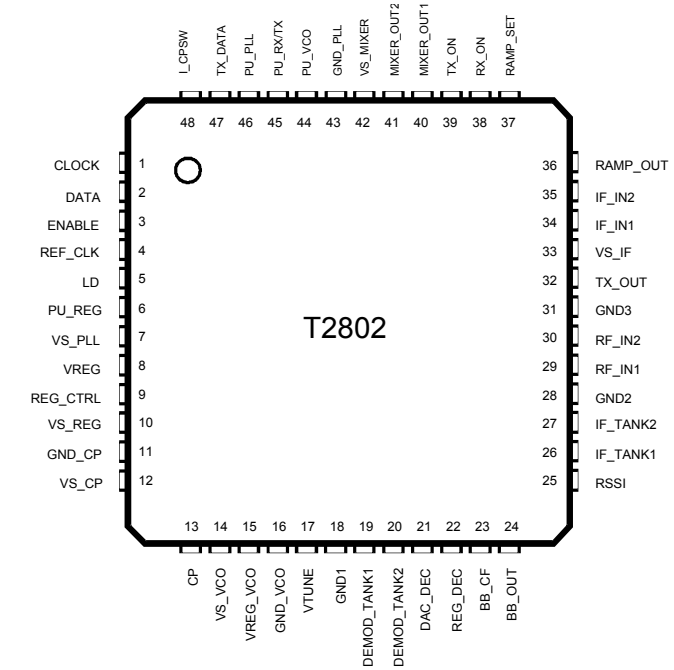
Rev. 4509F–DECT–10/03

Table 1. Functional Block Description

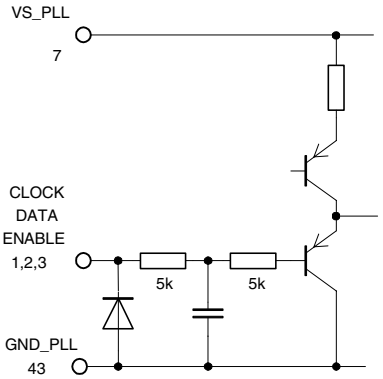
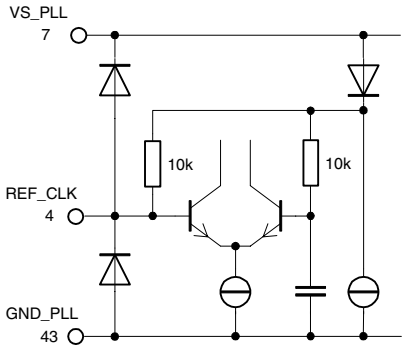
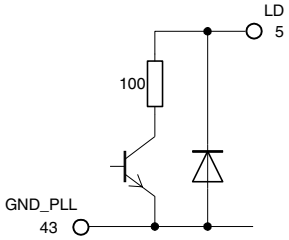
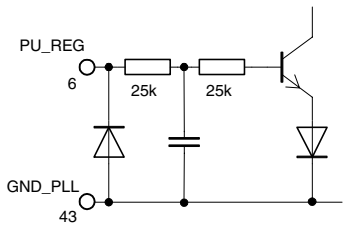
Name	Description
AUX REG	Auxiliary voltage regulator
BBF	Baseband filter
CP	Charge pump
DAC	D/A converter for demodulator tuning
DEMOD	Demodulator
GF	Gaussian filter for transmit data
IF AMP1	1st intermediate frequency amplifier
IF AMP2	2nd intermediate frequency amplifier
IR MIXER	Image rejection mixer
MCC	Modulation compensation circuit
PC	Programmable counter
PD	Phase detector
RAMP GEN	Ramp-signal generator
RC	Reference counter
RSSI	Received signal-strength indicator
TX DRIVER	Buffer amplifier for TX_OUT
TX/RX SWITCH	Switches VCO signal to IR MIXER respectively TX DRIVER
VCO	Voltage-controlled oscillator
VCO REG	Voltage regulator for VCO

Pin Configuration

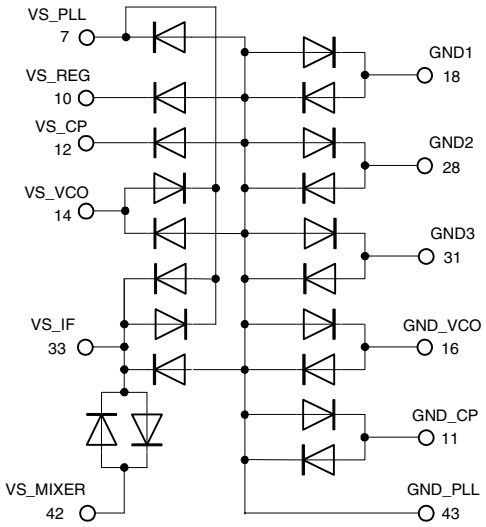
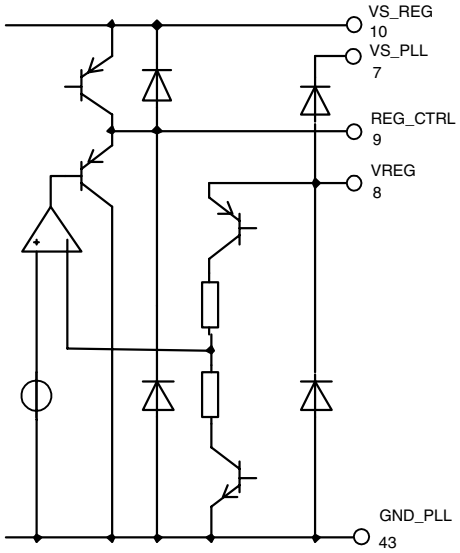
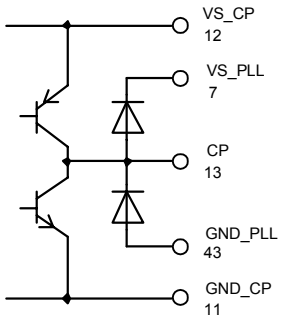
Figure 2. Pinning QFN48



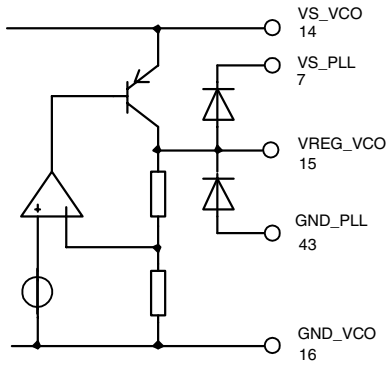
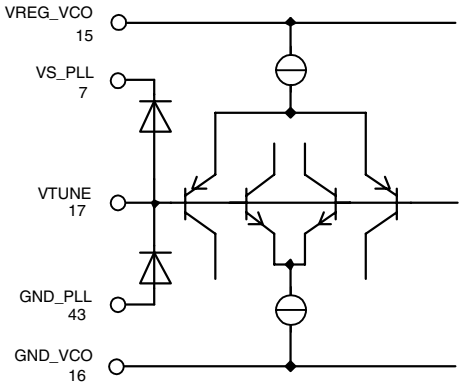
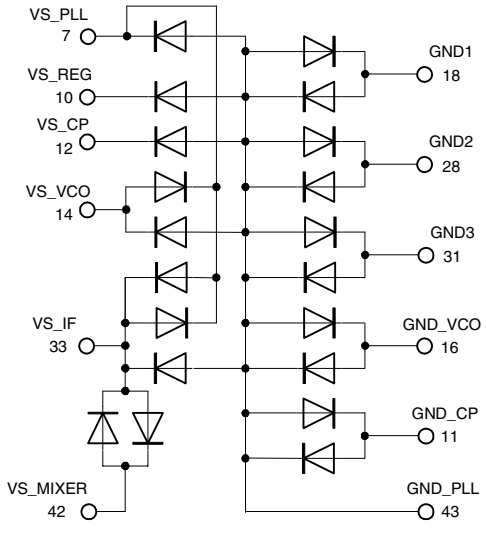
Pin Description

Pin	Symbol	Function	Configuration
1	CLOCK	3-wire-bus: Clock input	
2	DATA	3-wire-bus: Data input	
3	ENABLE	3-wire-bus: Enable input	
4	REF_CLK	Reference-frequency input	
5	LD	Lock-detect output	
6	PU_REG	Power-up input for auxiliary voltage regulator	

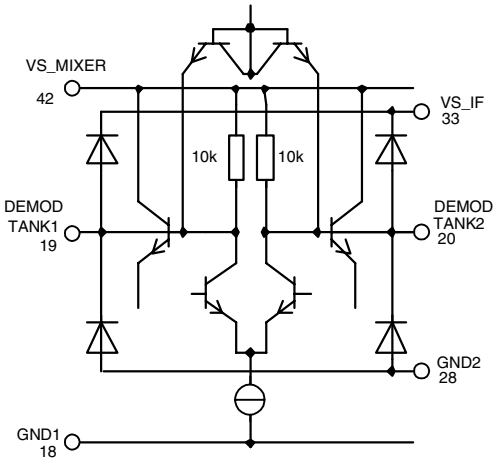
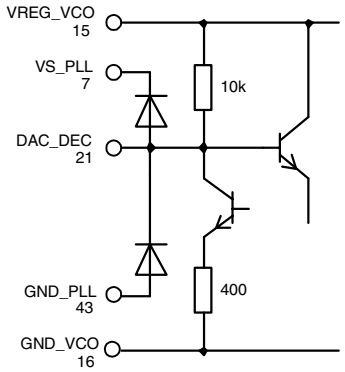
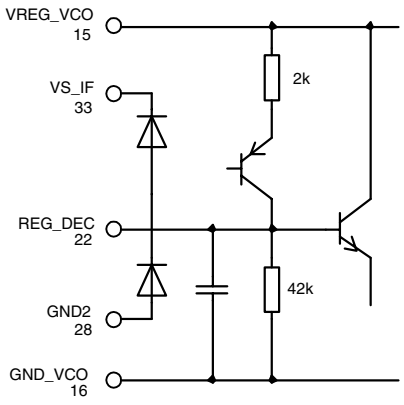
Pin Description (Continued)

Pin	Symbol	Function	Configuration
7	VS_PLL	PLL supply voltage	
8	VREG	Auxiliary voltage-regulator output	
9	REG_CTRL	Auxiliary voltage-regulator control output	
10	VS_REG	Auxiliary voltage-regulator supply voltage	
11	GND_CP	Charge-pump ground	
12	VS_CP	Charge-pump supply voltage	
13	CP	Charge-pump output	

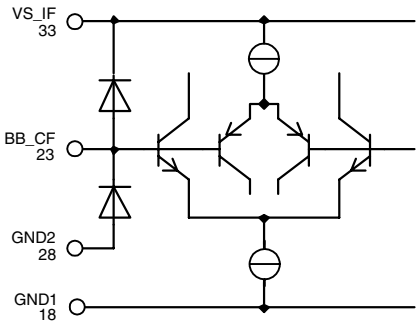
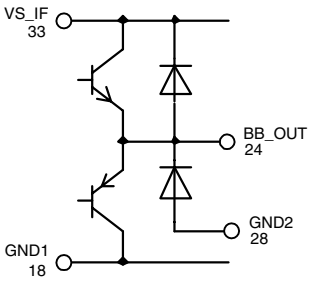
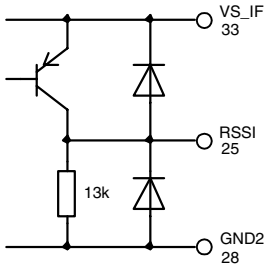
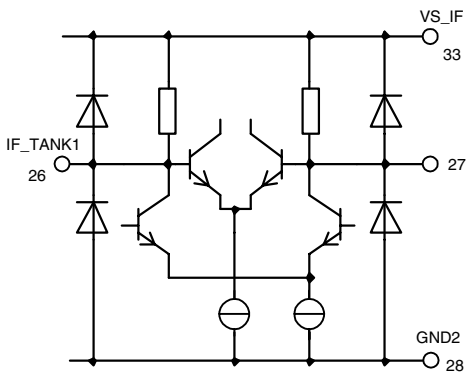
Pin Description (Continued)

Pin	Symbol	Function	Configuration
14	VS_VCO	VCO voltage-regulator supply voltage	
15	VREG_VCO	VCO voltage-regulator control output	
16	GND_VCO	VCO ground	
17	VTUNE	VCO tuning voltage input	
18	GND1	Ground	

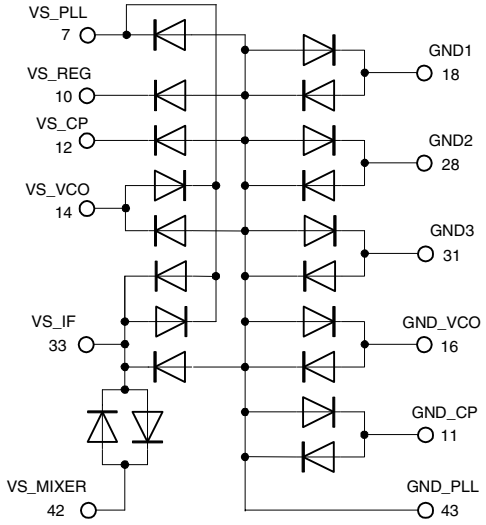
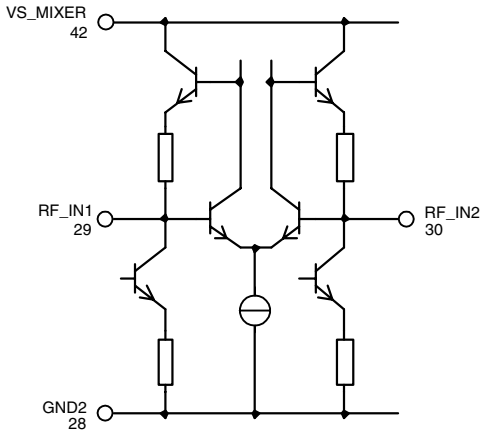
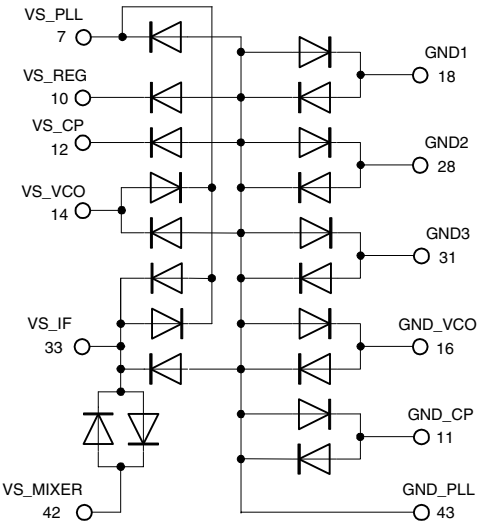
Pin Description (Continued)

Pin	Symbol	Function	Configuration
19	DEMOD_TANK1	Demodulator tank circuit	
20	DEMOD_TANK2	Demodulator tank circuit	
21	DAC_DEC	Decoupling PIN for VCO_DAC	
22	REG_DEC	Decoupling PIN for VCO_REG	

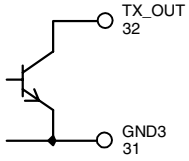
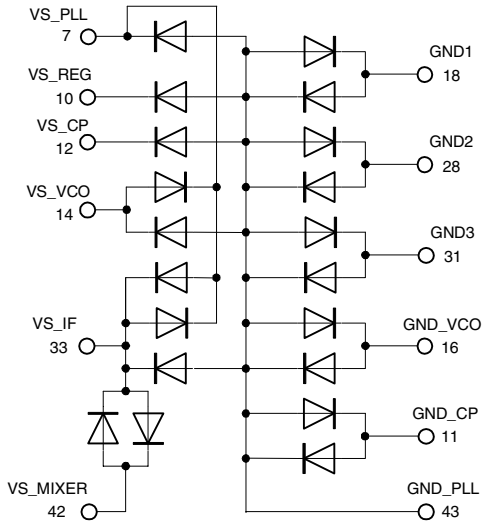
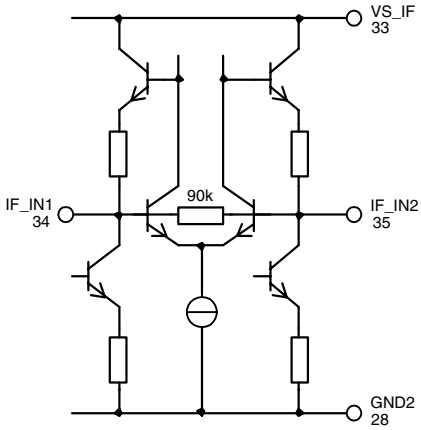
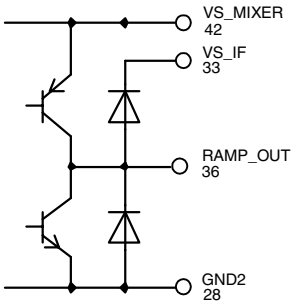
Pin Description (Continued)

Pin	Symbol	Function	Configuration
23	BB_CF	Baseband filter corner-frequency control input	
24	BB_OUT	Baseband filter output	
25	RSSI	Received signal strength indicator output	
26	IF_TANK1	IF tank circuit	
27	IF_TANK2	IF tank circuit	

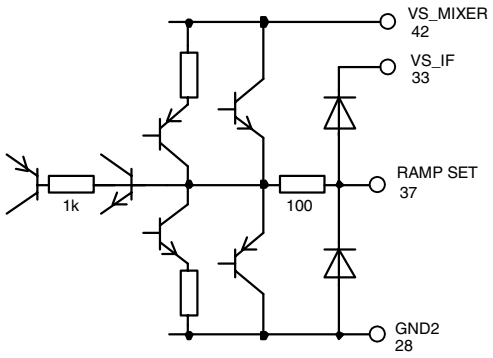
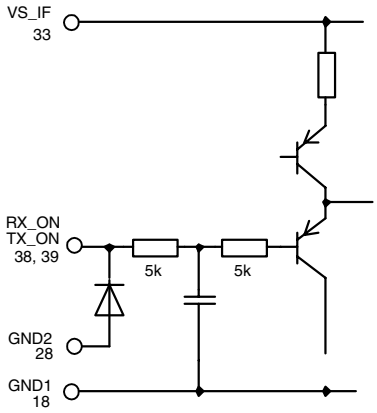
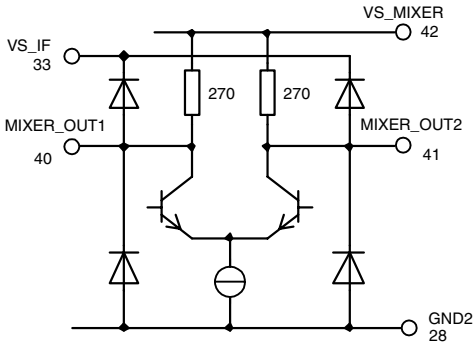
Pin Description (Continued)

Pin	Symbol	Function	Configuration
28	GND2	Ground	
29 30	RF_IN1 RF_IN2	RF input of image reject mixer RF input of image reject mixer	
31	GND3	Ground	

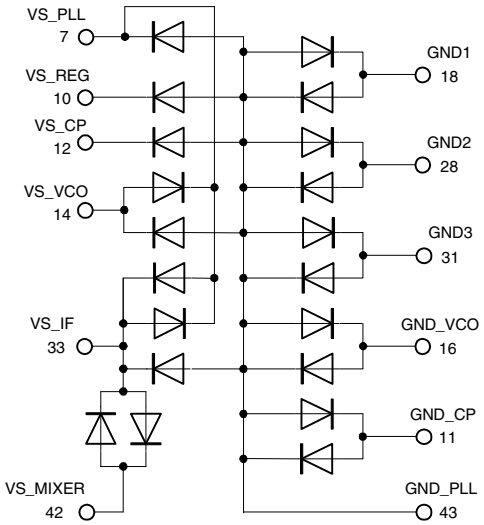
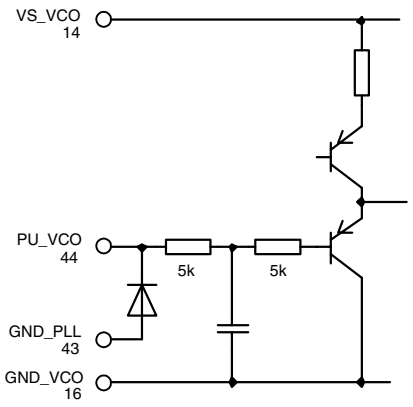
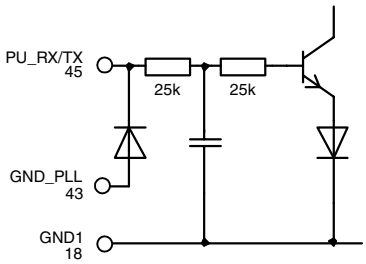
Pin Description (Continued)

Pin	Symbol	Function	Configuration
32	TX_OUT	TX driver amplifier output for PA	
33	VS_IF	IF amplifier supply voltage	
34 35	IF_IN1 IF_IN2	IF input of IF amplifier IF input of IF amplifier	
36	RAMP_OUT	Ramp-generator output for PA power ramping	

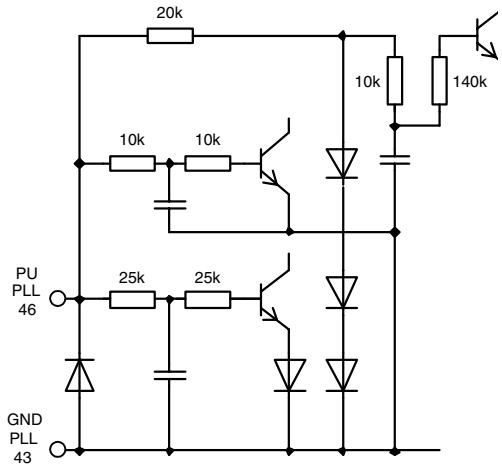
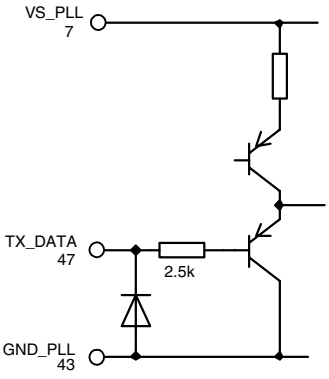
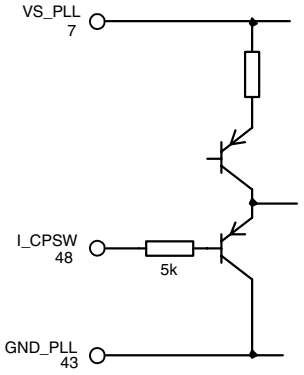
Pin Description (Continued)

Pin	Symbol	Function	Configuration
37	RAMP_SET	Slew-rate setting of ramping signal	
38 39	RX_ON TX_ON	RX control input TX control input	
40 41	MIXER_OUT1 MIXER_OUT2	Mixer output to SAW filter Mixer output to SAW filter	

Pin Description (Continued)

Pin	Symbol	Function	Configuration
42	VS_MIXER	Mixer supply voltage	
43	GND_PLL	PLL ground	
44	PU_VCO	VCO power-up input	
45	PU_RX/TX	RX/TX power-up input	

Pin Description (Continued)

Pin	Symbol	Function	Configuration
46	PU_PLL	PLL power-up input	
47	TX_DATA	TX data input of Gaussian filter and modulation-compensation circuit	
48	I_CPSW	Charge-pump current control input	

Functional Description

Receiver

The RF signal at RF_IN is fed to an image rejection mixer IR_MIXER with its differential outputs MIXER_OUT1 and MIXER_OUT2 driving an IF-SAW filter at 110.592 MHz or 112.32 MHz. The IF amplifiers IF_AMP1 and IF_AMP2 with an external IF_TANK and an integrated RSSI function feed the signal to the demodulator DEMOD working at $f = f_{IF}/2$ (≈55 MHz) and finally to an integrated baseband filter BB. For demodulator tunning in production an integrated 5-bit digital-to-analog (D/A) converter is provided to control the on-chip varicap diode.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian Filter GF and fed to the fully integrated VCO operating at twice the output frequency. After modulation the signal is frequency-divided by 2 and fed via a TX/RX SWITCH to the TX_DRIVER. This bus-controlled driver amplifier supplies typically +3 dBm output power at TX_OUT. A ramp-signal generator RAMP_GEN, providing a ramp signal at RAMP_OUT for the external power amplifier, is integrated. The slope of the ramp signal is controlled by a capacitor at the RAMP_SET pin.

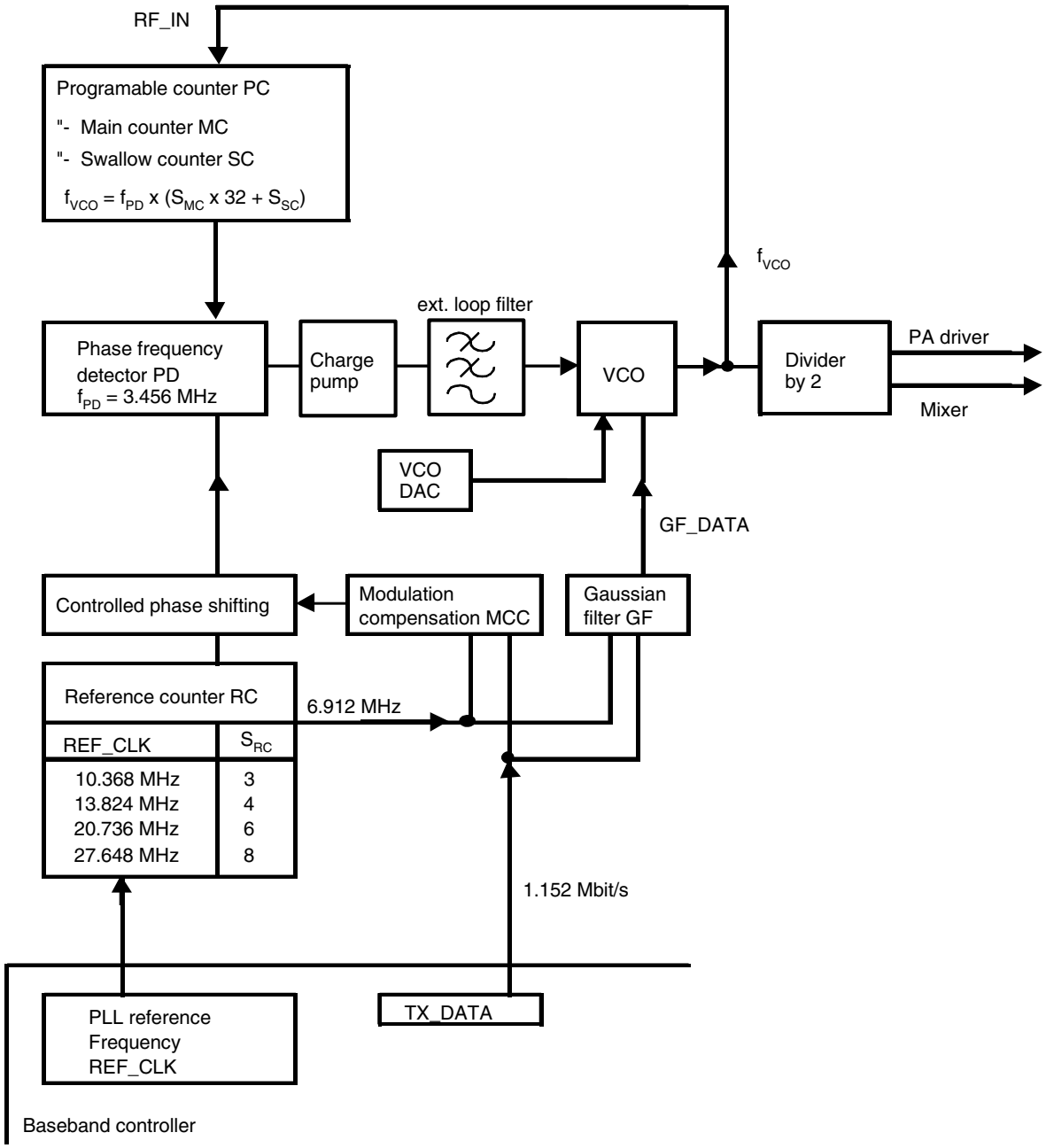
Synthesizer

The IR_MIXER, the TX_DRIVER and the programmable counter PC are driven by the fully integrated VCO (including on-chip inductors and varactors). A 3-bit digital-to-analog converter is used to pretune the frequency. The output signal is frequency-divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD (f_{PD} = 3.456 MHz). Unlimited multislot operation is possible by using the integrated advanced closed-loop modulation concept based on the modulation compensation circuit MCC.

Power Supply

An integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

Figure 3. PLL Principle



The following table shows the LO frequencies for RX and TX for the DECT band plus additional channels for the extended DECT band. Intermediate frequencies of 110.592 MHz and 112.32 MHz are supported.

Table 1. LO Frequencies

Mode	f_{IF}/MHz	Channel	f_{ANT}/MHz	f_{VCO}/MHz	S_{MC}	S_{SC}
TX		C0	2401.920	2401.920	43	14
		C1	2403.648	2403.648	43	15
		...	...	...	...	...
		C45	2479.680	2479.680	44	27
		C46	2481.408	2498.688	44	28
RX	110.592 (for 10.368 MHz/ 20.736 MHz REF_CLK recommended)	C0	2401.920	2291.328	41	14
		C1	2403.648	2293.056	41	15
		...	...	...	...	...
		C45	2479.680	2369.088	42	27
		C46	2481.408	2370.816	42	28
RX	112.320 (for 13.824 MHz/ 27.648 MHz REF_CLK recommended)	C0	2401.920	2289.600	41	13
		C1	2403.648	2291.328	41	14
		...	...	...	...	...
		C45	2479.680	2367.360	42	26
		C46	2481.408	2369.088	42	27

Formula

TX: $f_{ANT} = f_{VCO} = 1.728\ MHz \times (32 \times S_{MC} + S_{SC})$

RX: $f_{ANT} = 1.728\ MHz \times (32 \times S_{MC} + S_{SC}) + f_{IF}$

Control Signals

Table 2. Control Signals — Functions

Signal	Functions
I_CPSW	Charge pump current control
PU_REG	Activates AUX voltage regulator supplying the complete transceiver
PU_VCO	Activates VCO voltage regulator which supplies only the VCO
PU_RX/TX	Activates RX/TX blocks
PU_PLL	Activates PLL circuits: PC, PD, CP, RC
RX_ON	Activates RX circuits: BBF, DEMOD, IF AMP, IR MIXER
TX_ON	Activates TX circuits: TX-DRIVER, RAMP GEN, Starts RAMP SIGNAL at RAMP OUT
Data Word 1 Bit D10	Activates GF in TX mode
Data Word 1 Bit D9	Activates MCC in TX mode

Table 3. Control Signals — Modes

Modes	TX Mode	RX Mode	RSSI Only
PU_REG	1	1	1
PU_VCO	1	1	1
PU_RX/TX	1	1	1
PU_PLL	1	1	1
RX_ON	0	1	1
TX_ON	1	0	1
BB filter	OFF	ON	OFF
Demodulator	OFF	ON	OFF
IF amplifiers and RSSI	OFF	ON	ON
IR mixer	OFF	ON	ON
RX switch	OFF	ON	ON
TX switch	ON	OFF	OFF
TX driver	ON	OFF	OFF
Ramp generator	ON	OFF	OFF
Programmable counter	ON	ON	ON
Voltage-controlled oscillator	ON	ON	ON
Gaussian filter	ON	OFF	OFF
Phase detector/charge pump	ON	ON	ON
Modulation compensation circuit	ON	OFF	OFF
Reference counter	ON	ON	ON
Typical current consumption at V_S = 3.2 V	58 mA	85 mA	82 mA

Serial Programming Bus

The transceiver is programmed by the 3-wire bus (CLOCK, DATA and ENABLE).

After the setting enable signal to low condition on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. When the enable signal has returned to high condition, the programmed information is loaded into the addressed latches according to the address bit condition (last bit). Additional leading bits are ignored and there is no check made how many pulses arrived during enable low condition. During enable low condition the bus current is increased to speed up the bus logic.

To keep all information in the registers during standby, DATA_HOLD must be set to high condition. In this case the power-down current is below 100 µA.

The programming of the transceiver is separated into two data words. Data word 1 controls mainly the channel information together with settings, which are closely related with the channel. Dataword 2 holds setup information, which is adjusted during production.

Data Word 1

MSB																					LSB
Data bits																					Address bit
D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A0
RC		SC					MC			VS	X	MCC	GFCS			VCODAC				CPCS		GF	

D11 = x: do not care

Data Word 2

E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	A0
PA		DEMODDAC/RAMPDAC					MCCS			TEST			0

Data Word 1 Programs

PLL Settings

With the Reference Counter bits D21 - D22

RC (Reference Counter)			
D22	**D21**	**S_{RC}**	**REF_CLK**
0	0	3	10.368 MHz
0	1	4	13.824 MHz
1	0	6	20.736 MHz
1	1	8	27.648 MHz

With the Main Counter bits D13 - D15

MC (Main Counter)			
D15	**D14**	**D13**	**S_{MC}**
0	0	0	40
0	0	1	41
...	...	...	...
1	1	0	46
1	1	1	47

With the Swallow Counter bits D16 - D20

SC (Swallow Counter)					
D20	**D19**	**D18**	**D17**	**D16**	**S_{SC}**
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

VCO Selection

With bit D12

VCO Selection	
D12	**VCO Mode**
0	RX-VCO
1	TX-VCO

Gaussian Filter On/Off

With bit D0
GF is used only in TX mode.

D0	GF (Gaussian Filter)
0	OFF
1	ON

Modulation Compensation Circuit On/Off

With bit D10
MCC is used only in TX mode.

D10	MCC (Modulation Compensation Circuit)
0	OFF
1	ON

GFCS Adjustment

With bits D7 - D9
Only in TX mode effective for setting the frequency deviation of the modulation.

GFCS (Gaussian Filter Settings)			
D9	**D8**	**D7**	**GFCS**
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

VCO_DAC Adjustment

With bits D3 - D6
Used to pretune the VCO frequency in case of production tolerances of the device.

Pretune DAC Voltage				
D6	**D5**	**D4**	**D3**	**f_{VCO}/%**
0	0	0	0	-5
0	0	0	1	...
0	0	1	0	...
...	...	...	...	...
1	1	0	1	...
1	1	1	0	...
1	1	1	1	5

CPCS Adjustment

With bits D1 - D2
Used to adjust the charge pump current. This can be used to compensate the change of the tuning sensitivity over frequency and device tolerances.

CPCS (Charge-pump Current Settings)		
D2	**D1**	**CPCS**
0	0	-1
0	1	0
1	0	1
1	1	2

Data Word 2 Programs

DEMODDAC Adjustment

With bits E6 - E10
Only in RX mode effective. Used to tune the demodulator center frequency and allows to compensate tolerances of external components and the T2802.

Demod DAC Voltage					
E10	**E9**	**E8**	**E7**	**E6**	**$f_{IFcenter}$ %**
0	0	0	0	0	-5
0	0	0	0	1	...
0	0	0	1	0	...
...	...	...	...	...	...
1	1	1	0	1	...
1	1	1	1	0	...
1	1	1	1	1	5

RAMPDAC Adjustment for TX Mode

With bits E6 - E10
Only in TX mode effective. Used to control the power of the external PA by adjusting the ramping voltage.

RAMPDAC Voltage (at Pin 36 RAMP_OUT)					
E10	**E9**	**E8**	**E7**	**E6**	**V_{RAMP_OUT}**
0	0	0	0	0	1.1 V
0	0	0	0	1	...
0	0	0	1	0	...
...	...	...	...	...	...
1	0	1	1	1	1.68 V
1	1	0	0	0	1.7 V
...	...	...	...	...	...
1	1	1	1	0	...
1	1	1	1	1	1.7 V

MCCS Adjustment

With bits E3 - E5
Only in TX mode effective. Adjusts the modulation compensation circuit for closed-loop modulation. This adjustment is done with a test sequence of a long stream of ‚1' - ‚0'. The correct setting is achieved if the modulation is not affected by the PLL.

MCCS (Modulation Compensation Settings)			
E5	**E4**	**E3**	**MCCS**
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

TEST Mode Settings

With bits E0 - E2
In normal operation Lock detect output is used. All other settings are for test only.

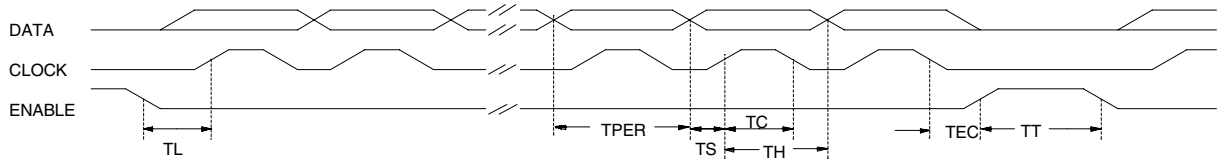
E2	E1	E0	Signal at Lock Detect Output	CP Mode
0	0	0	Lock detect	Active
0	0	1	PC out/2	Active
0	1	0	RC out/2	Active
0	1	1	MCCTEST: RC out divided by 512	Active
1	0	0	Lock detect	High imp.
1	0	1	PC out/2	High imp.
1	1	0	RC out/2	High imp.
1	1	1	GFTEST: RC out	High imp.

Output Power Settings

With bits E11 - E12

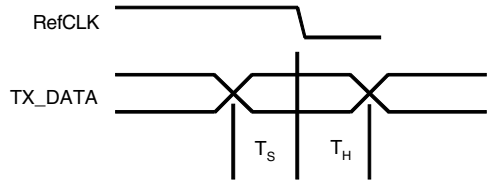
PA (Output Power Settings)		
E12	**E11**	**PA**
0	0	-21 dBm
0	1	-11 dBm
1	0	-4 dBm
1	1	+3 dBm

Figure 4. 3-Wire Bus Protocol Timing Diagram



Description	Symbol	Minimum Value	Unit
Clock period	TPER	125	ns
Set time data to clock	TS	60	ns
Hold time data to clock	TH	60	ns
Clock pulse width	TC	125	ns
Set time enable to clock	TL	200	ns
Hold time enable to data	TEC	0	ns
Time between two protocols	TT	250	ns

Figure 5. TX DATA Timing



Set-up time TX DATA	TS	> 8 ns
Hold time TX DATA	TH	> 8 ns

When using REFCLK = 10.368 MHz, TS and TH must be considered for falling and rising edge of REFCLK

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages refer to GND

Parameters	Pin	Symbol	Min.	Max.	Unit
Supply voltage regulator	10	V_{S_REG}	3.2	4.7	V
Supply voltage	7, 12, 14, 33, 42	V_S	3.0	4.7	V
Logic input voltage	1, 2, 3, 38, 39, 44-48	V_{IN}	-0.3	V_S	V
Junction temperature		T_{jmax}		150	°C
Storage temperature		T_{stg}	-40	150	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	25	K/W

Handling

Do not operate this part near strong electrostatic fields. This IC meets class 1 ESD test requirement (HBM in accordance to EIA/JESD22-A114-A (October 97) and class A ESD test requirement (MM) in accordance to EIA/JESD22-A115A.

Operating Range

Parameters	Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage regulator	10	V_{S_REG}	3.2	3.6	4.6	V
Supply voltage	7, 14, 33, 42	V_S	2.9	3.0	4.6	V
Supply voltage charge pump	12	V_{SCP}	V_S		4.6	V
Ambient temperature		T_{amb}	-25		+85	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
IR Mixer (Pins 29, 30, 40 and 41)						
Input impedance	Single ended, pins 29 or 30	Z_{in}		110 + j12		Ω
Image rejection ratio	Pins 40 and 41	IRR		20		dB
DSB noise figure	Single ended, pins 29 or 30	NFDSB= NFSSB		10		dB
Conversion gain	R_{load} = 200 Ω	G_{conv}		11		dB
Input intercept point	Single ended, pins 29 or 30	IIP3		-7		dBm
Output impedance	Differential, pins 40 and 41	Z_{out}		175 + j145		Ω
IF Amplifier (Pins 26, 27, 34 and 35)						
Input impedance	Differential, pins 34 and 35	Z_{in}		1200 - j480		Ω
Lower cut-off frequency		fl_{3dB}		90		MHz
Upper cut-off frequency		fu_{3dB}		130		MHz
Power gain		Gp		85		dB
Bandwidth of external tank circuit	Pins 26 and 27	BW3dB		10		MHz
Noise figure		NF		9		dB
RSSI (Pins 25, 34 and 35)						
RSSI sensitivity	At IF_IN1,2; pins 34 and 35	P_{min}		20		dBµV
RSSI compression	At IF_IN1,2; pins 34 and 35	P_{max}		100		dBµV
RSSI dynamic range		DR		80		dB
RSSI resolution	Slope of the RSSI has to be steady	Acc		±2		dB
RSSI rise time	P_{in} = 30 to 100 dBµV, pin 25	t_r		1		µs
RSSI fall time	P_{in} = 100 to 30 dBµV, pin 25	t_f		1		µs
Quiescent output voltage	At P_{in} < 20 dBµV at IF_IN1, IF_IN2, Pin 25	I_{out}		0.4		V
Maximum output voltage	At P_{in} = 100 dBµV at IF_IN1, IF_IN2, Pin 25	I_{out}		1.9		V
FM Demodulator, BB-filter (Pins 19, 20, 23 and 24)						
Co-channel rejection ratio	At P_{in} = -75 dBm at IR-mixer input	CCRR		10		dB
Sensitivity	Quality factor of external tank circuit approximately 20, $f_{res} = F_{IF}/2$, pin 24	S		0.5		V/MHz
Amplitude of recovered signal	Nominal deviation of signal ±288 kHz, pin 24	A		450		mVpp
Corner frequency	Pin 23: C = 68 pF	f_c		680		kHz
Output voltage DC range	Pin 24	V_{outDC}	1		V_S - 1	V
DEMOD_DAC range	See bus protocol E6 to E10	$\Delta f_{IFcenter}$		±5		%

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
VCOs						
Frequency range	TX-VCO, D12 (VS) = 1 RX-VCO, D12 (VS) = 0	f_{vco} f_{vco}	2400 2289		2500 2389	MHz MHz
Tuning gain		G_{tune}		70		MHz/V
Frequency control voltage range	Pin 17	V_{tune}	0.4		2.8	V
VCO_DAC range	See bus protocol D3 ... D6	$\Delta f_{vco,DAC}$		±5		%
PLL						
Scaling factor prescaler		S_{PSC}		32/33		
Scaling factor main counter		S_{MC}		40 - 47		
Scaling factor swallow counter		S_{SC}	0		31	
External reference input frequency	AC coupled sinewave, pin 4	f_{REF_CLK}		10.368 13.824 20.736 27.648		MHz MHz MHz MHz
External reference input voltage	AC coupled sinewave, pin 4	V_{REF_CLK}	50		250	mV_{RMS}
Scaling factor reference counter		S_{RC}		3/4/6/8		
Charge Pump (Pin 13)						
Output current	$V_{CP} = V_{VS_CP}/2$, I_CPSW = '1', Pin 48	I_{CP_nom}		7.5		mA
Output current	$V_{CP} = V_{VS_CP}/2$, I_CPSW = '0', Pin 48	I_{CP_nom}		1.2		mA
Current scaling	$I_{CP} = I_{CP_nom} + CPCS \times I_{CP_step}$ (see bus protocol D1 ... D2)	I_{CP_step}		0.2		mA
Leakage current		I_L		±100		pA
Gaussian Transmit Filter (Gaussian Shape B × T = 0.5)						
Tx data filter clock	6 taps in filter	f_{TXFCLK}		6.912		MHz
Frequency deviation		GF_{FM_nom}		±400		kHz
Frequency deviation scaling	$GF_{FM} = GF_{FM_nom} \times GFCS$ (see bus protocol D7 ... D9)	GFCS	60		130	%
Modulation Compensation Circuit						
Oversampling		OVS		6		
Digital sum variation		DSV			85	
Current scaling factor	See bus protocol E3 ... E5	MCCS	60		130	%
TX Driver (Pin 32)						
Maximum output power	At L = 5.6 nH, pin 32 (see bus protocol E11 - E12)	P_{TX}		3		dBm
Minimum output power	At L = 5.6 nH, pin 32 (see bus protocol E11 - E12)	P_{TX}		-21		dBm

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

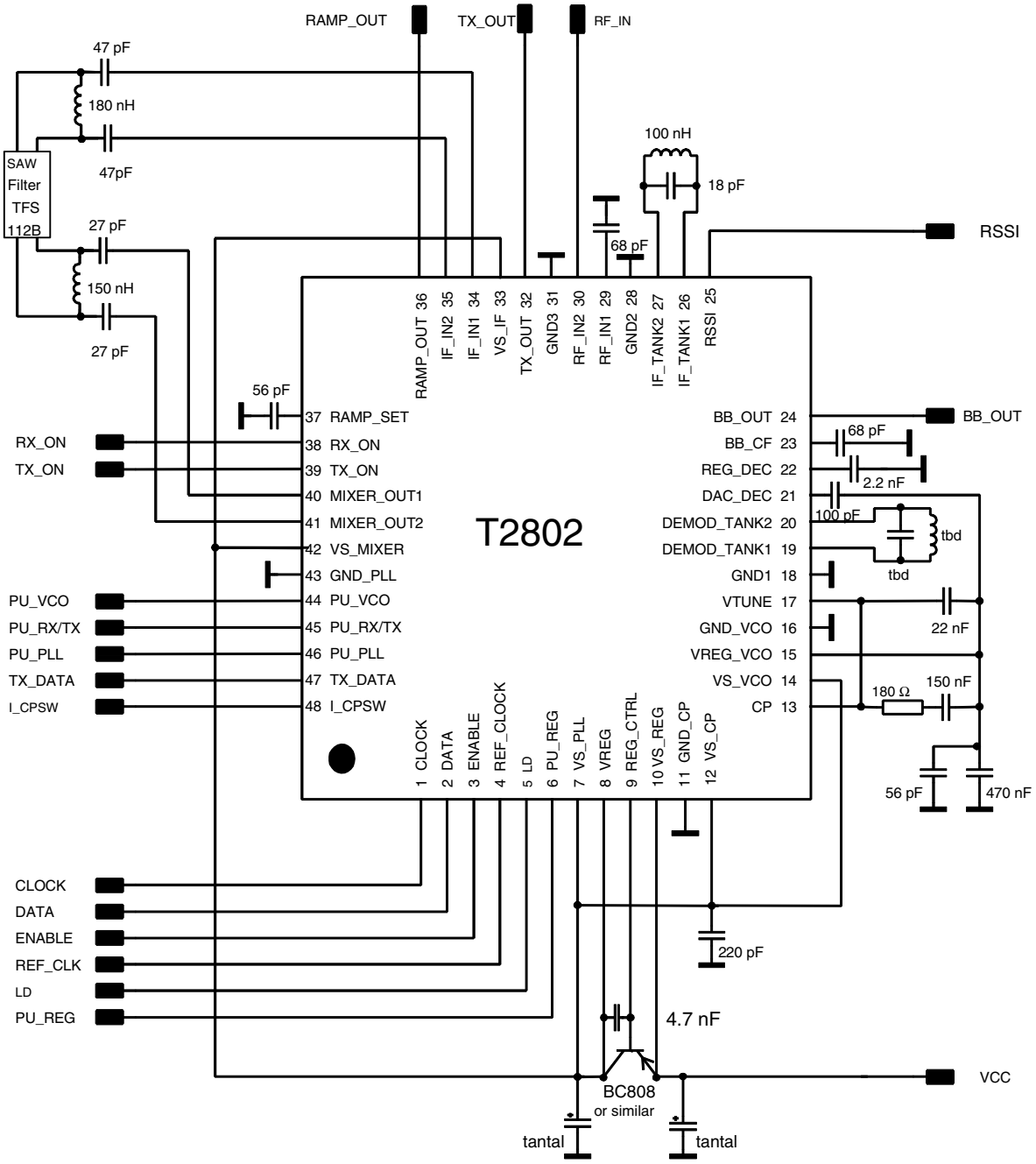
Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
RF leakage	In RX mode	P_{leak}			-47	dBm
Output impedance	At L = 5.6 nH, 2.5 GHz, pin 32	Z_{OUT}		13 + j40		Ω
Ramp Generator (Pins 36 and 37)						
Minimum output voltage	Pin 36 and 37	V_{min}		0.7		V
Maximum output voltage	See bus protocol E6 - E10	V_{max}	1.1		1.8	V
Rise time	C_{ramp} = 270 pF at pin 37	t_r		5		µs
Fall time	C_{ramp} = 270 pF at pin 37	t_f		5		µs
Lock Detect and Test Mode Output (Pin 5)						
Lock detect output, test mode output	locked = '1', unlocked = '0' test modes (see bus protocol E0 ... E2)	LD				
Leakage current	V_{OH} = 4.6 V	I_L			5	µA
Saturation voltage	I_{OL} = 0.5 mA	V_{SL}			0.4	V
Auxiliary Regulator (Pins 8, 9 and 10)						
Output voltage	V_{SREG} = 3 V, pin 8	V_{REG}	2.9	3.0	3.1	V
Supply voltage rejection	$V_{Pin10} = V_{DC} + 0.1\ V_{pp}$ f_{Pin10} = 0.1 to 10 kHz C_{Pin8} = 100 nF	SVR		TBD		dB
VCO Regulator (Pins 14, 15 and 12)						
Output voltage	V_{SVCO} = 3 V, pin 15	V_{REG_VCO}	2.6	2.7	2.8	V
3-wire Bus						
Clock		f_{Clock}			6.912	MHz
Logic Input Levels (CLOCK, DATA, ENABLE, RX_ON, TX_ON, PU_VCO, TX_DATA, DATA_HOLD) (Pins 1, 2, 3, 38, 39, 44, 47 and 48)						
High input level	= '1'	V_{iH}	1.5			V
Low input level	= '0'	V_{iL}			0.5	V
High input current	= '1'	I_{iH}	-5		5	µA
Low input current	= '0'	I_{iL}	-5		5	µA
Standby Control (Pins 6, 45 and 46)						
Power Up PU_REG = '1' PU_RX/TX = '1' PU_PLL = '1' High input level	Pin 6 Pin 45 Pin 46	V_{PU_REG} $V_{PU_RX/TX}$ V_{PU_PLL}	2.0			V
Standby PU_REG = '0' PU_RX/TX = '0' PU_PLL = '0' Low input level	Pin 6 Pin 45 Pin 46	$V_{PU_REG,OFF}$ $V_{PU_RX/TX,OFF}$ $V_{PU_PLL,OFF}$			0.7	V

Electrical Characteristics (Continued)

Test conditions (unless otherwise specified): V_{S_REG} = 3.2 V, T_{amb} = 25°C

Parameters	Test Conditions/Pins	Symbol	Min.	Typ.	Max.	Unit
Power Up						
PU_REG = '1' PU_RX/TX = '1'	V_{PU} = 3 V, pin 6 V_{PU} = 4.6 V, pin 45	I_{PU_REG} $I_{PU_RX/TX}$	20 60	30 80	40 100	µA µA
PU_PLL = '1' High input current	V_{PU} = 3 V, pin 46 V_{PU} = 4.6 V	I_{PU_PLL}	100 200	125 300	150 400	µA µA
Standby PU_xxxx = '0' Low input current	V_{PU} = 0 V, pin 6 V_{PU} = 0.5 V, pins 45, 46	$I_{PU,OFF}$			0.1 1	µA µA
Settling Time V_S = 0 → active operation	Switched from V_S = 0 to V_S = 3V	t_{soa}		< 10		µs
Settling Time standby → active operation	Switched from PU = '0' to PU = '1'	t_{ssa}		< 10		µs
Settling Time active operation → standby	Switched from PU = '1' to standby	t_{sas}		< 2		µs
Power Supply (Pins 7, 10, 12, 14, 33 and 42)						
Total supply current	RX	I_S		85		mA
	RSSI only	I_S		82		mA
	TX	I_S		54		mA
	TX (MCC, GF active)	I_S		58		mA
Standby current	PU_RX/TX = GND	I_S			10	µA
Supply current CP	V_{VS_CP} = 3 V, PLL in lock condition, Pin 13	I_{CP}		1		µA

Figure 6. Typical Application Circuit

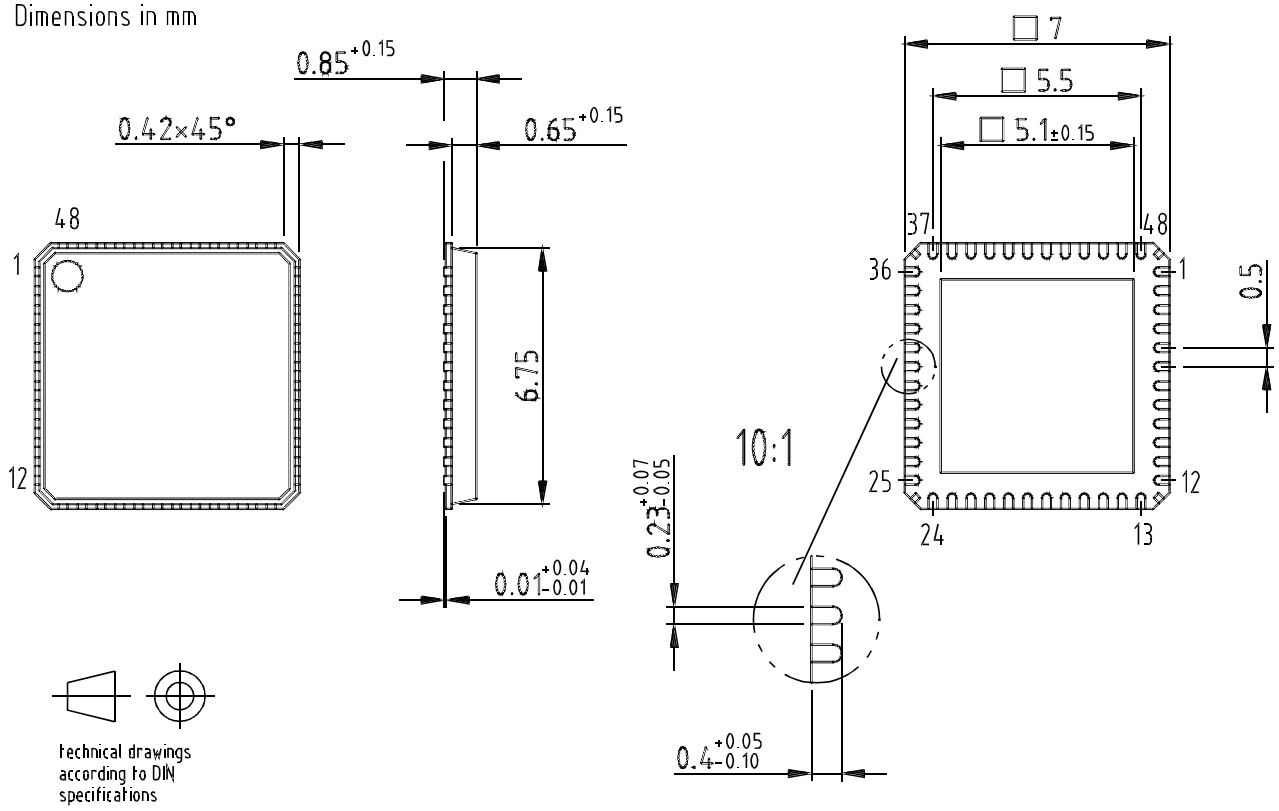


Ordering Information

Extended Type Number	Package	Remarks
T2802-PLQ	QFN48	Taped and reeled

Package Information

Package: QFN 48 - 7x7
Exposed pad 5.1x5.1
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm



Drawing-No.: 6.543-5068.01-4
Issue: 3; 24.01.03

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