DATA SHEET

TDA1599
IF amplifier/demodulator for FM radio receivers

Product specification
File under Integrated Circuits, IC01

May 1994

Philips
Semiconductors

PHILIPS

IF amplifier/demodulator for FM radio receivers

TDA1599

FEATURES

- Balanced limiting amplifier
- Balanced coincidence demodulator
- Two open-collector stop pulse outputs for microcomputer tuning control
- Simulated behaviour of a ratio detector (internal field strength and detuning dependent voltage for dynamic AF signal muting)
- Mono/stereo blend field strength indication control voltage
- AFC output
- 3-state mode switch for FM-MUTE-ON, FM-MUTE-OFF and FM-OFF
- Internal compensation of AF signal total harmonic distortion (THD)
- Built-in hum and ripple rejection circuits.

GENERAL DESCRIPTION

The TDA1599 provides IF amplification, symmetrical quadrature demodulation and level detection for quality home and car FM radio receivers and is suitable for mono and stereo reception. It may also be applied to common front ends, stereo decoders and AM receiver circuits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)	7.5	8.5	12	V
I_P	supply current ($I_2 = I_7 = 0$)	–	20	26	mA
V_i	IF input sensitivity for limiting on pin 20 (RMS value)	14	22	35	μV
V_o	AF output signal on pin 4 (RMS value)	180	200	220	mV
S/N	signal-to-noise ratio (f_m = 400 Hz; $\Delta f = \pm 75$ kHz)	–	82	–	dB
THD	total harmonic distortion (f_m = 1 kHz; $\Delta f = \pm 75$ kHz)	–	0.1	0.3	%
	with K2 adjustment and FM-MUTE-OFF	–	0.07	0.25	%
T_{amb}	operating ambient temperature	–40	–	+85	°C

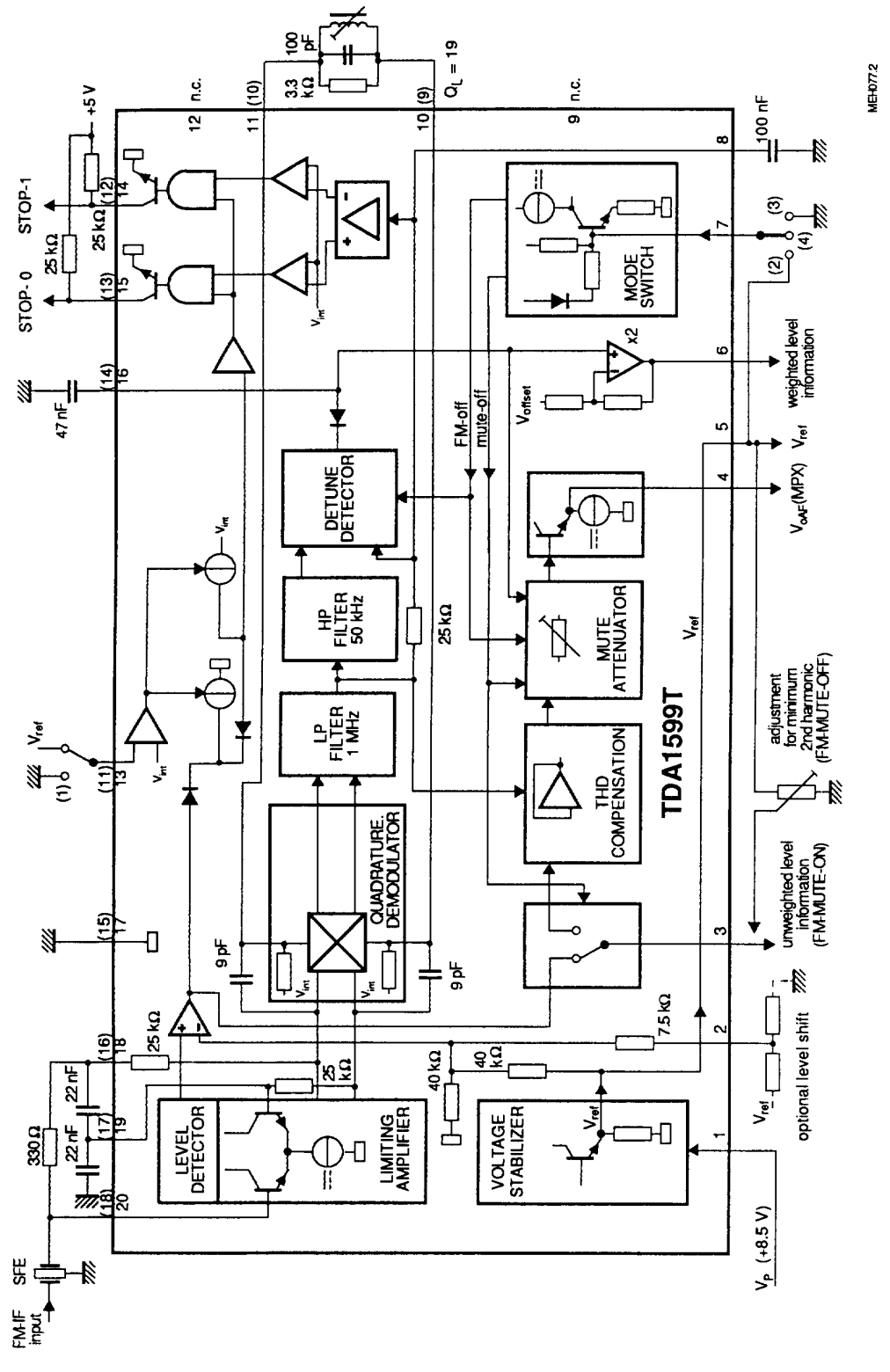
All pin numbers mentioned in this data sheet refer to the SO-version (TDA1599T) unless otherwise specified.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1599	18	DIL	plastic	SOT102(1)
TDA1599T	20	mini-pack	plastic	SOT163A(2)

Notes

1. SOT102-1; 1996 August 29.
2. SOT163-1; 1996 August 29.



(1) to connect pin 13 (11) to ground is only allowed to measure the current on pin 16 (14)
(2) FM-MUTE-OFF
(3) FM-OFF
(4) FM-MUTE-ON

Fig.1 Block diagram and application circuit (TDA1599 pinning in parenthesis).

PINNING; note 1

SYMBOL	PIN	DESCRIPTION
V_P	1 (1)	supply voltage (+8.5 V)
LVA	2 (2)	level adjustment for stop condition
ULV	3 (3)	unweighted level output / K2 adjustment
V_{oAF}	4 (4)	audio frequency output (MPX signal)
V_{REF}	5 (5)	reference voltage output
WLV	6 (6)	weighted level output
MODE	7 (7)	mode switch input
DDV	8 (8)	detune detector voltage
n.c.	9 (–)	not connected
DEMI1	10 (9)	demodulator input 1
DEMI2	11 (10)	demodulator input 2
n.c.	12 (–)	not connected
TSW	13 (11)	tau switch input
ST1	14 (12)	STOP-1, stop pulse output 1
ST0	15 (13)	STOP-0, stop pulse output 0
MUTE	16 (14)	muting voltage
GND	17 (15)	ground (0 V)
LFB1	18 (16)	IF limiter feedback 1
LFB2	19 (17)	IF limiter feedback 2
V_{iIF}	20 (18)	IF signal input

Note

1. SO-version TDA1599T; pinning for DIL-version in parenthesis.

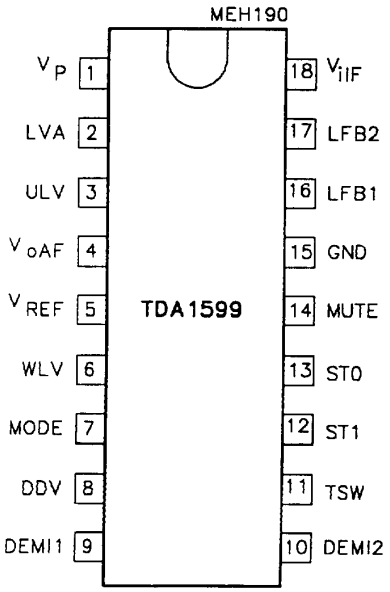


Fig.2 Pin configuration for DIL-version.

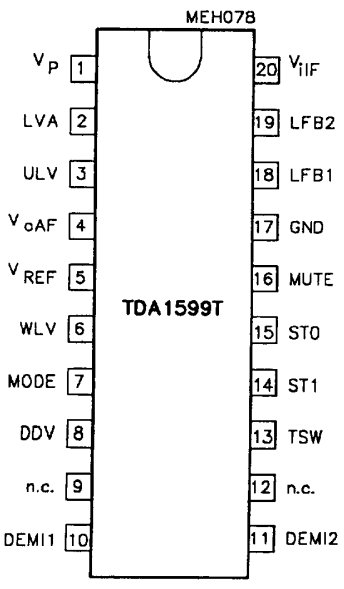


Fig.3 Pin configuration for SO-version.

FUNCTIONAL DESCRIPTION

The limiter amplifier has five stages of IF amplification using balanced differential limiter amplifiers with emitter follower coupling.

Decoupling of the stages from the supply voltage line and an internal high-ohmic DC feedback loop give a very stable IF performance. The amplifier gain is virtually independent of changes in temperature.

The FM demodulator is fully balanced and compromises two cross-coupled differential amplifiers. The quadrature detection of the FM signal is performed by direct feeding of one differential amplifier from the limiter amplifier output, and the other via an external 90 degrees phase shifting network. The demodulator has a good stability and a small zero-cross-over shift. The bandwidth on the demodulator output is restricted by an internal low-pass filter to approximately 1 MHz.

Non-linearities, which are introduced by demodulation, are compensated by the THD compensation circuit. For this reason, the demodulator resonance circuit (between pins 10 and 11) must have a loaded Q-factor of 19.

Consequently, there is no need for the demodulator tuned circuit to be adjusted for minimum distortion. Adjustment criterion is a symmetrical stop pulse. The control voltage for the mute attenuator (pin 16) is derived from the values of the level detector and the detuning detector output signals. The mute attenuator has a fast attack and a slow decay determined by the capacitor on pin 16. The AF signal is fed via the mute attenuator to the output (pin 4). A weighted control voltage (pin 6) is obtained from the mute attenuator control voltage via a buffer amplifier that introduces an additional voltage shift and gain.

The level detector generates a voltage output signal proportional to the amplitude of the input signal. The unweighted level detector output signal is available in FM-MUTE-ON condition (mode switch).

The open-collector tuning stop output voltages STOP-0 and STOP-1 (pins 15 and 14) are derived from the detuning and the input signal level. The pins 14 and 15 may be tied together, if only one tuning-stop output is required.

LIMITING VALUES (TDA1599T PINNING)

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	–0.3	+13	V
V_{n1}	voltage at pins 2, 4, 5, 6, 10, 11 and 16	–0.3	+10	V
V_{n2}	voltage at pins 7, 3, 8, 14, 15, 18, 19 and 20	–0.3	V_P	V
V_{13}	voltage on pin 13	–	6	V
$I_{14, 15}$	current at pins 14 and 15	–	2	mA
P_{tot}	total power dissipation	–	360	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–40	+85	°C
V_{ESD}	electrostatic handling; note 1			
	all pins except 5 and 7	–	±2000	V
	pin 5	–	+800	V
			–2000	V
	pin 7	–	+1000	V
			–2000	V

Note to the limiting values

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	
	SOT102	80 K/W
	SOT163A	90 K/W

CHARACTERISTICS (TDA1599T PINNING)

V_P = 8.5 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 μs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 1)		7.5	8.5	12	V
I_P	supply current	$I_2 = I_7 = 0$	–	20	26	mA
Mode switch input						
I_7	input current for FM-MUTE-ON		–	0	–	mA
V_7	input voltage for FM-MUTE-ON		2.4	2.8	3.2	V
	input voltage for FM-MUTE-OFF		$0.9V_{REF}$	–	–	V
	input voltage for FM-OFF	AF attenuation > 60 dB	–	–	1.4	V
IF amplifier and demodulator						
Z_i	demodulator input impedance between pins 10 and 11		25	40	55	kΩ
C_i	demodulator input capacitance between pins 10 and 11		–	6	–	pF
AF output (pin 4)						
R_o	output resistance		–	400	–	Ω
V_4	DC output level	$V_{IIF} \leq 5$ μV RMS on pin 20	2.75	3.1	3.45	V
RR_{1000}	power supply ripple rejection on pin 4	f = 1000 Hz; V_{ripple} = 50 mV RMS	33	36	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9;				
		$V_{14, 15} \geq 3.5$ V	250	–	–	μV
		$V_{14, 15} \leq 0.3$ V	–	–	50	μV
$V_{14, 15}$	output voltage	$I_{14, 15}$ = 1 mA	–	–	0.3	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	I_5 = –1 mA	3.3	3.7	4.1	V
R_5	output resistance	I_5 = –1 mA	–	40	80	Ω
TC	temperature coefficient		–	3.3	–	mV/VK

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
External muting						
V_{16}	muting voltage at $I_2 = 0$	$V_{20} \leq 5$ μV RMS; Fig.12	1.45	1.75	2.05	V
		$V_{20} = 1$ mV RMS	3.0	3.45	3.9	V
S	steepness of control voltage (slope: 100 μV ≤ V_{20} ≤ 100 mV) 20 Δlog V_{20} = 20 dB (ΔV_{16} / Δlog V_{20})		–	0.85	–	V/dec
Internal mute α = 20 log ($\Delta V_{4(FM\text{-}MUTE\text{-}OFF)}$/ $\Delta V_{4(FM\text{-}MUTE\text{-}ON)}$)						
α	mute voltage	$V_{16} \geq V_{REF}$	–	0	–	dB
		$V_{16} = 0.77V_{REF}$	1.5	–	4.5	dB
		$V_{16} = 0.55V_{REF}$	–	20	–	dB
I_{16}	current for capacitor (pin 16)					
	charge current	$V_{13} = 0$ V	–	–8	–	μA
	discharge current	$V_{13} = 0$ V	–	+120	–	μA
	charge current	$V_{13} = V_{REF}$	–	–100	–	μA
	discharge current	$V_{13} = V_{REF}$	–	+120	–	μA
Level detector						
R_6	output resistance		–	–	500	Ω
V_6	output voltage at $I_2 = 0$	$V_{20} \leq 5$ μV RMS; Fig.14	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
		±200 kHz detuning	1.2	1.5	1.8	V
	output voltage at $V_2 = V_5$	$V_{20} \leq 5$ μV RMS	–	–	0.3	V
ΔV_6	output voltage at detuning	±45 kHz detuning	–	–	0.2	V
TC	temperature coefficient		–	3.3	–	mV/VK
Δf	detuning frequency	$V_6 = 1.8$ V; Fig.13	90	–	160	kHz
S	steepness of control voltage (slope: 50 μV ≤ V_{20} ≤ 50 mV) 20 Δlog V_{20} = 20 dB (ΔV_6 / Δlog V_{20})		1.4	1.7	2.0	V/dec
$\Delta V_6/\Delta f$	slope of output voltage at detuning	$\Delta f = 125 \pm 20$ kHz	–	35	–	mV/kHz
S	level shift adjustments					
	range by pin 2	$\pm\Delta V_6/V_{REF}$	0.42	0.5	–	V/V
	gain	$-\Delta V_6/\Delta V_2$	–	1.7	–	V/V
	range by pin 2	$\pm\Delta V_{16}/V_{REF}$	0.21	0.25	–	V/V
	gain	$-\Delta V_{16}/\Delta V_2$	–	0.85	–	V/V

OPERATING CHARACTERISTICS (TDA1599T PINNING)

V_P = 7.5 to 12 V; T_{amb} = +25 °C; FM-MUTE-ON (I_7 = 0); f_{IF} = 10.7 MHz; deviation ±22.5 kHz with f_m = 400 Hz; V_i = 10 mV RMS at pin 20; de-emphasis of 50 μs; tuned circuit at pins 10 and 11 aligned for symmetrical stop pulses; measurements taken in Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
IF amplifier and demodulator						
V_i	input signal for start of limiting (–3 dB) (RMS value; pin 20)	$V_7 = V_{REF}$; FM-MUTE-OFF	14	22	35	μV
	input signal for signal-to-noise ratio (RMS value)	f = 250 to 15000 Hz				
	S/N = 26 dB	$V_7 = V_{REF}$	–	15	–	μV
	S/N = 46 dB	$V_7 = V_{REF}$	–	60	–	μV
S/N	signal-to-noise ratio	deviation ±75 kHZ	–	82	–	dB
V_o	AF output signal (RMS value; pin 4)		180	200	220	mV
THD	total harmonic distortion	deviation ±75 kHz;				
	without de-emphasis	f_m = 1 kHz; I_7 = 0				
	without detuning		–	0.1	0.3	%
	±25 kHz detuning		–	–	0.6	%
	compensated via pin 3	$V_7 = V_{REF}$	–	0.07	0.25	%
ΔV_4	K2 adjustment ($\Delta V_4 = V_4(V_3 = 0) - V_4(V_3 = V_{REF})$)		10	–	–	mV
α_{AM}	AM suppression on pin 4	$V_7 = V_{REF}$; m = 30%				
	V_i = 0.3 to 1000 mV RMS	on pin 20	46	55	–	dB
	V_i = 1 to 300 mV RMS	on pin 20	60	65	–	dB
Dynamic mute attenuation α = 20 log ($\Delta V_{4(FM\text{-}MUTE\text{-}OFF)}/\Delta V_{4(FM\text{-}MUTE\text{-}ON)}$)						
α	dynamic mute attenuation	deviation ±75 kHz; f_m = 100 kHz; V_2 = 1 V	–	14	–	dB
Tuning stop detector						
Δf	detuning frequency for STOP-0	on pin 15; Fig.11				
	for $V_{15} \geq 3.5$ V		–	–	+14.0	kHz
	for $V_{15} \leq 0.3$ V		+22.0	–	–	kHz
Δf	detuning frequency for STOP-1	on pin 14; Fig.10				
	for $V_{14} \geq 3.5$ V		–	–	–14.0	kHz
	for $V_{14} \leq 0.3$ V		–22.0	–	–	kHz
V_{20}	dependence on input voltage for STOP-0 and STOP-1 (RMS value)	Fig.9;				
		$V_{14, 15} \geq 3.5$ V	250	–	–	μV
		$V_{14, 15} \leq 0.3$ V	–	–	50	μV
R_8	internal low-pass resistance of detune detector		12	25	50	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_8	voltage on capacitor	$I_7 = 0$; $V_i \leq 5$ μV RMS on input pin 20	–	2.2	–	V
Level detector ($I_2 = 0$)						
V_6	output voltage	$V_{20} \leq 5$ μV RMS	0.1	–	1.1	V
		$V_{20} = 1$ mV RMS	3.0	–	4.2	V
Reference voltage source (pin 5)						
V_{REF}	reference output voltage	$I_5 = -1$ mA	3.3	3.7	4.1	V

Operation with AM-IF

Level and stop information (on pins 6,13, 14, 15 and 16) is provided for the modes FM-MUTE-ON and FM-MUTE-OFF. This information is also available in the FM-OFF mode when an AM-IF signal is input (for example 455 kHz). This can also provide a valid detuning information when a suitable AM-IF resonance circuit is provided for demodulator (Fig.18).

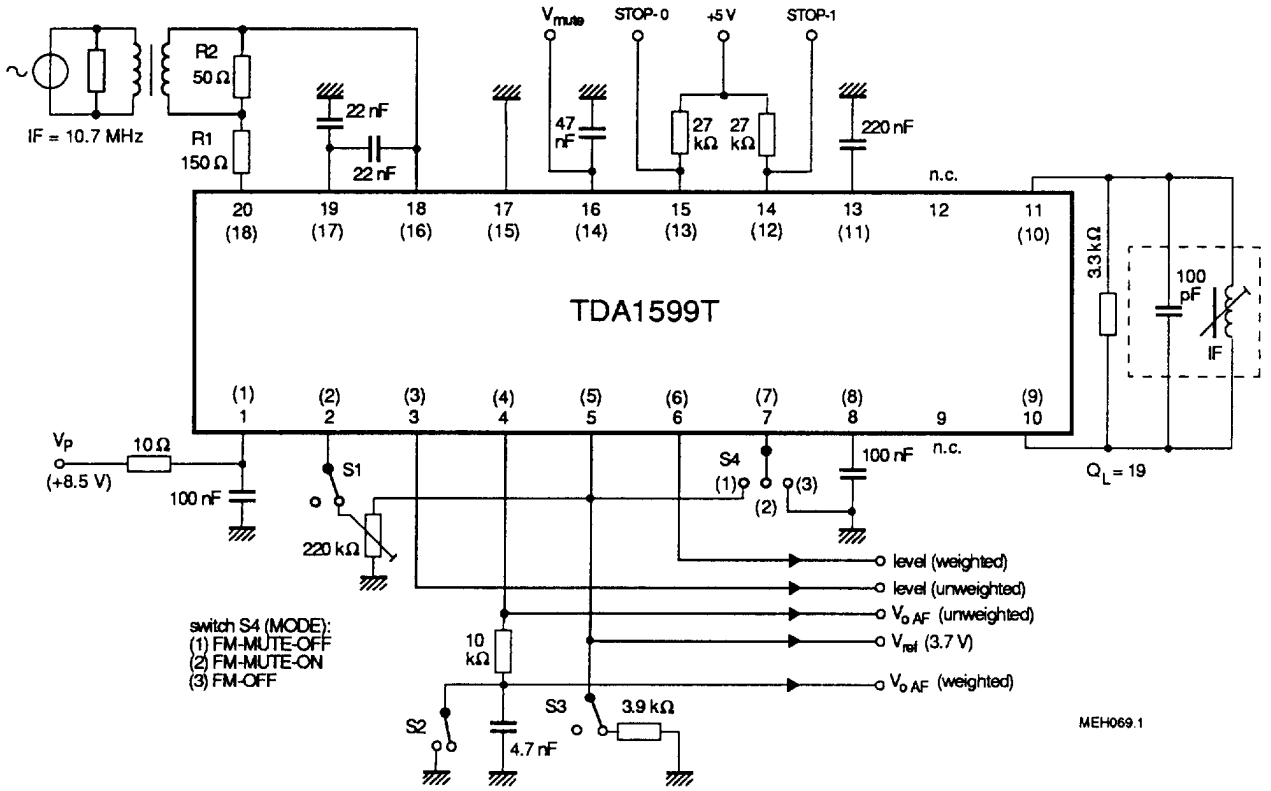
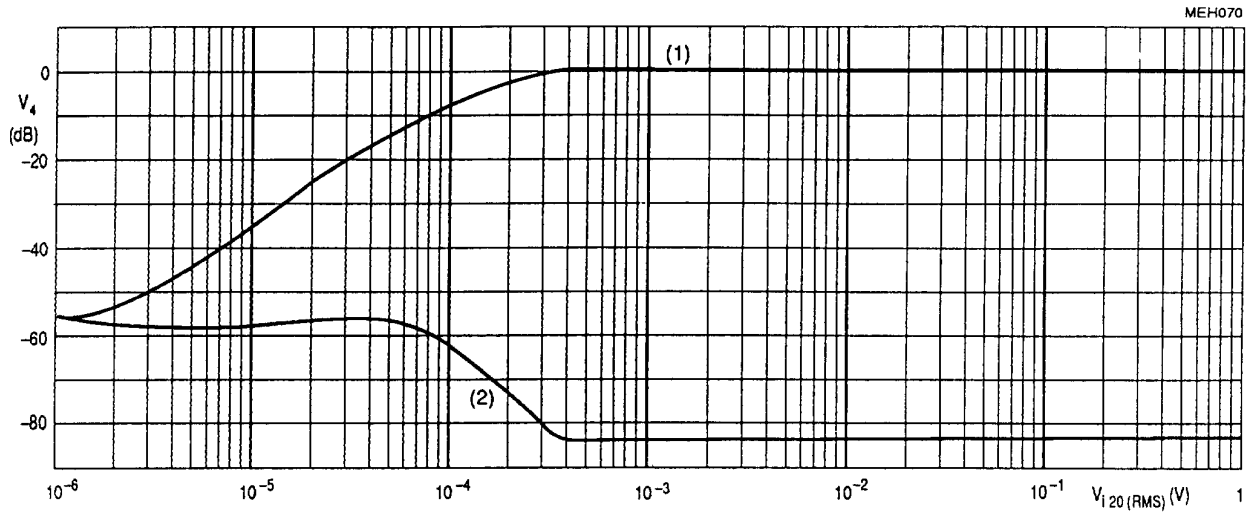
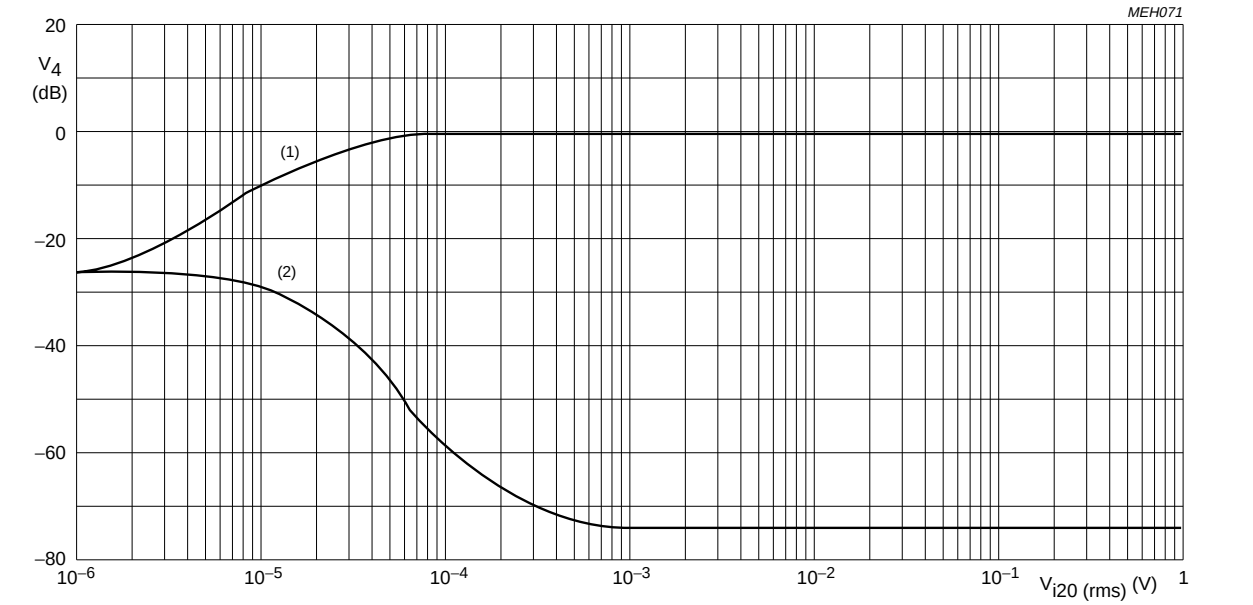


Fig.4 Test circuit (TDA1599 pinning in parenthesis).



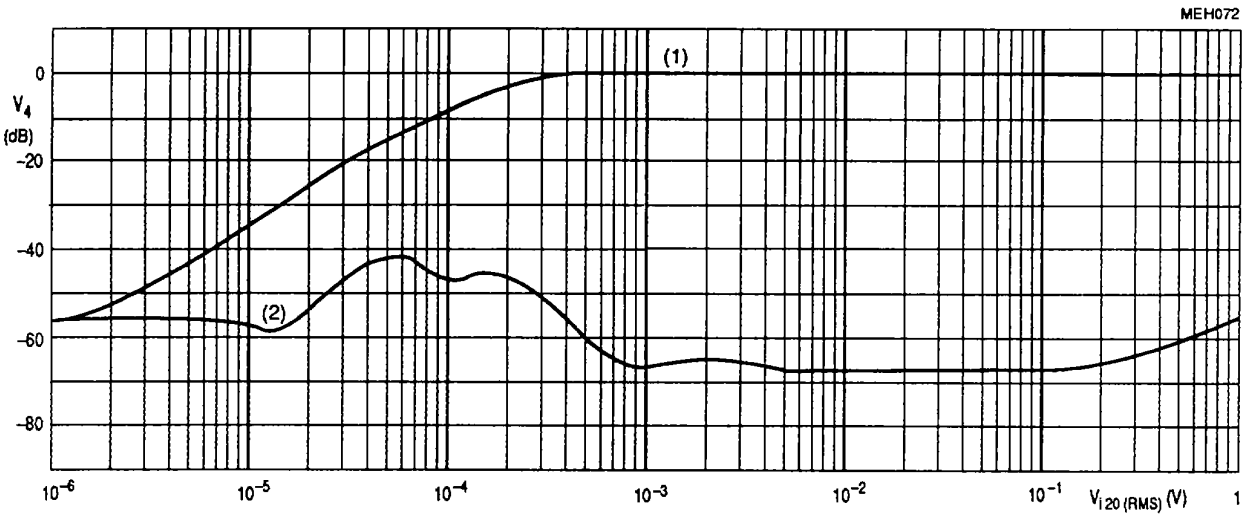
(1) audio signal
(2) noise

Fig.5 FM-MUTE-ON: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



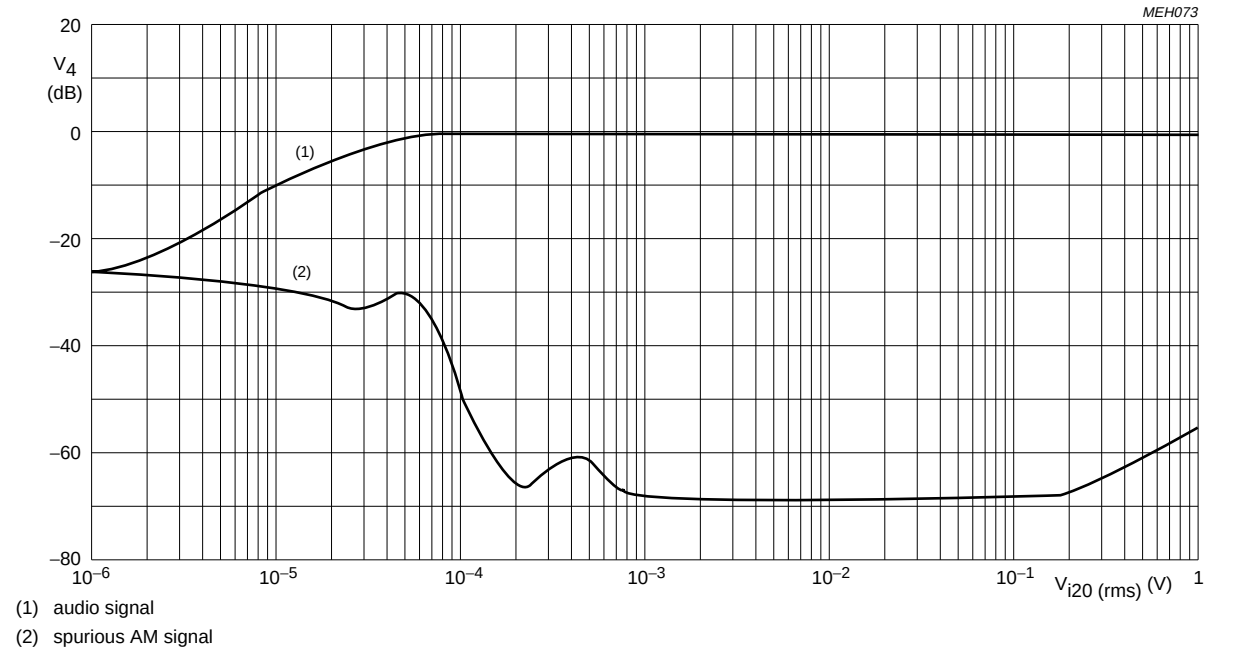
(1) audio signal
(2) noise

Fig.6 FM-MUTE-OFF: Audio signal and noise as functions of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; de-emphasis 50 μs.



(1) audio signal
(2) spurious AM signal

Fig.7 FM-MUTE-ON: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.



(1) audio signal
(2) spurious AM signal

Fig.8 FM-MUTE-OFF: Typical AM suppression as a function of the input signal V_{iIF} (pin 20) with $\Delta f = \pm 22.5$ kHz; $f_m = 1$ kHz; AM with $f_m = 400$ Hz; m = 0.3 and 250 to 15000 Hz bandwidth.

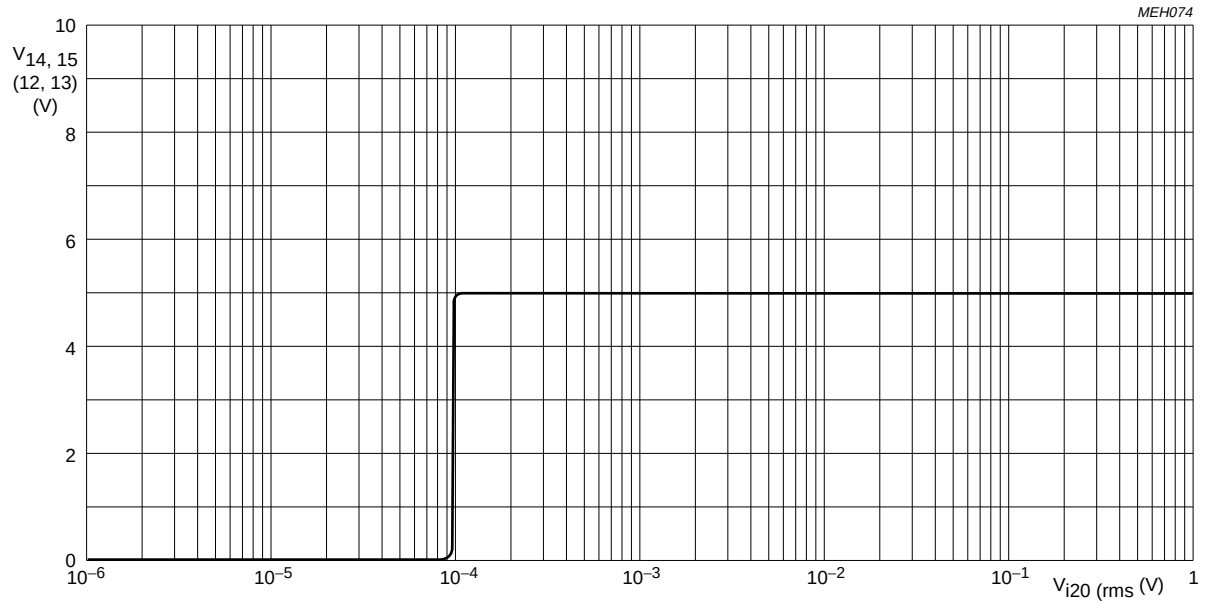


Fig.9 STOP-0 and STOP-1 output voltage dependent on input signal V_{iIF} (pin 20).

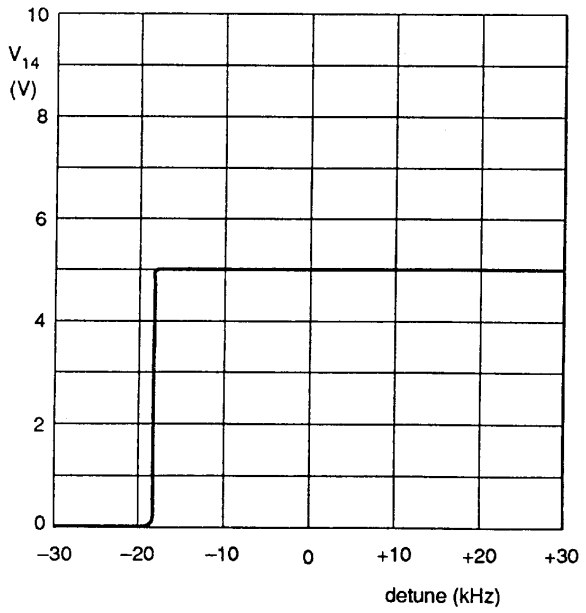


Fig.10 STOP-1 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

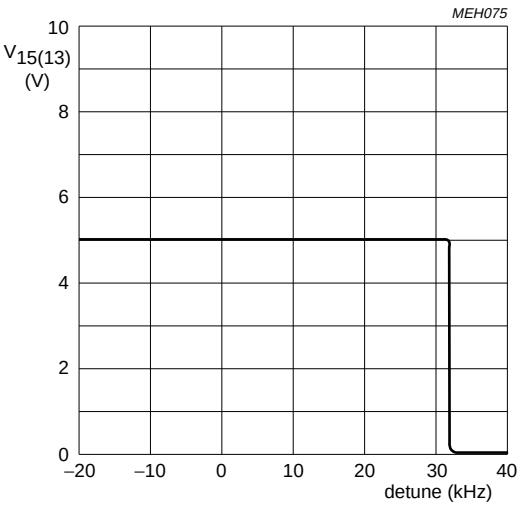


Fig.11 STOP-0 output voltage dependent on V_{iIF} = 10 mV RMS (pin 20).

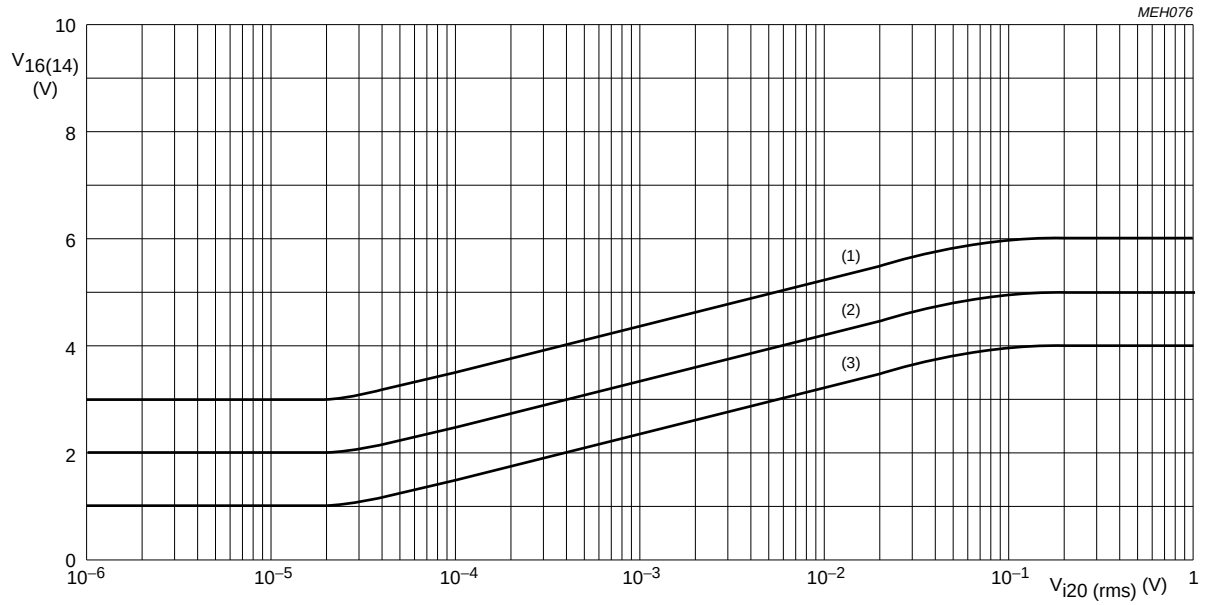


Fig.12 External mute voltage V_{16} dependent on input signal V_{iIF} (pin 20); typical adjusting range.

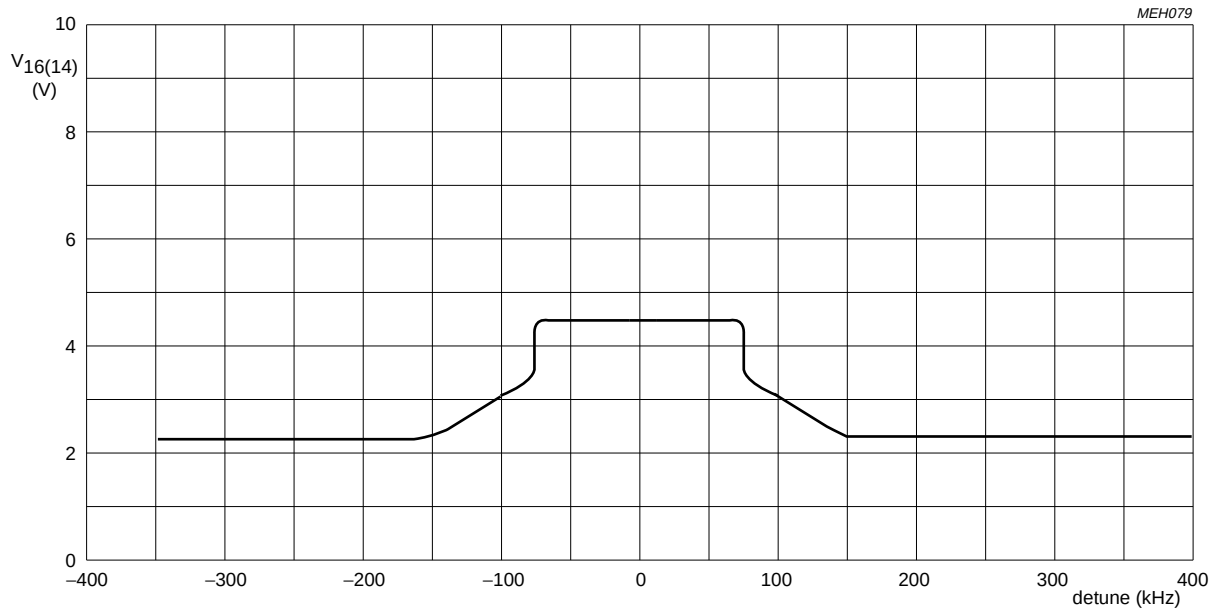


Fig.13 Mute voltage V_{16} dependent on detuning; V_{iIF} = 10 mV RMS.

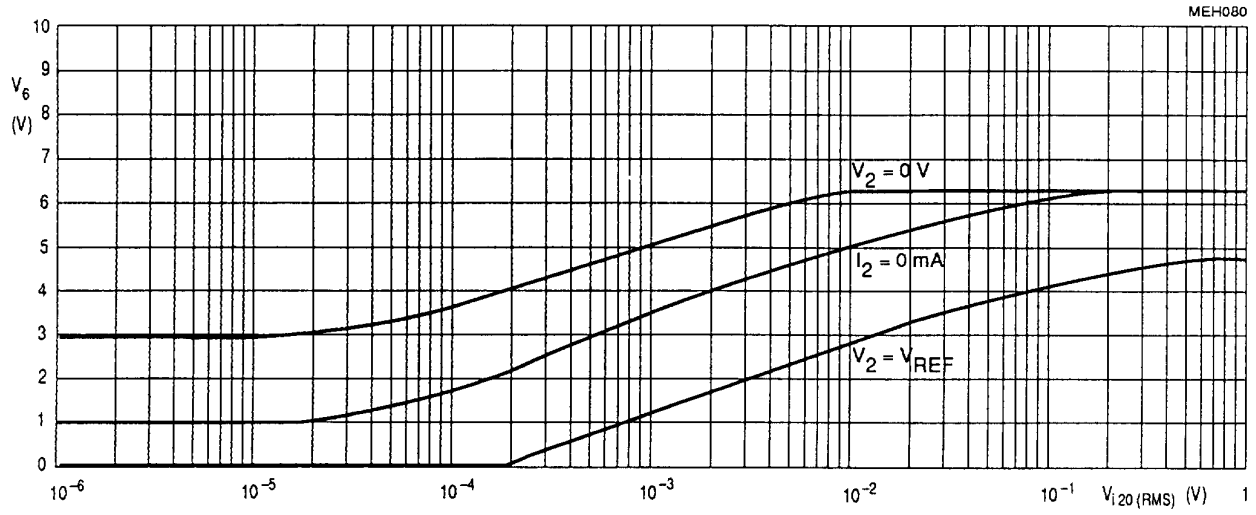


Fig.14 Control voltage V_6 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

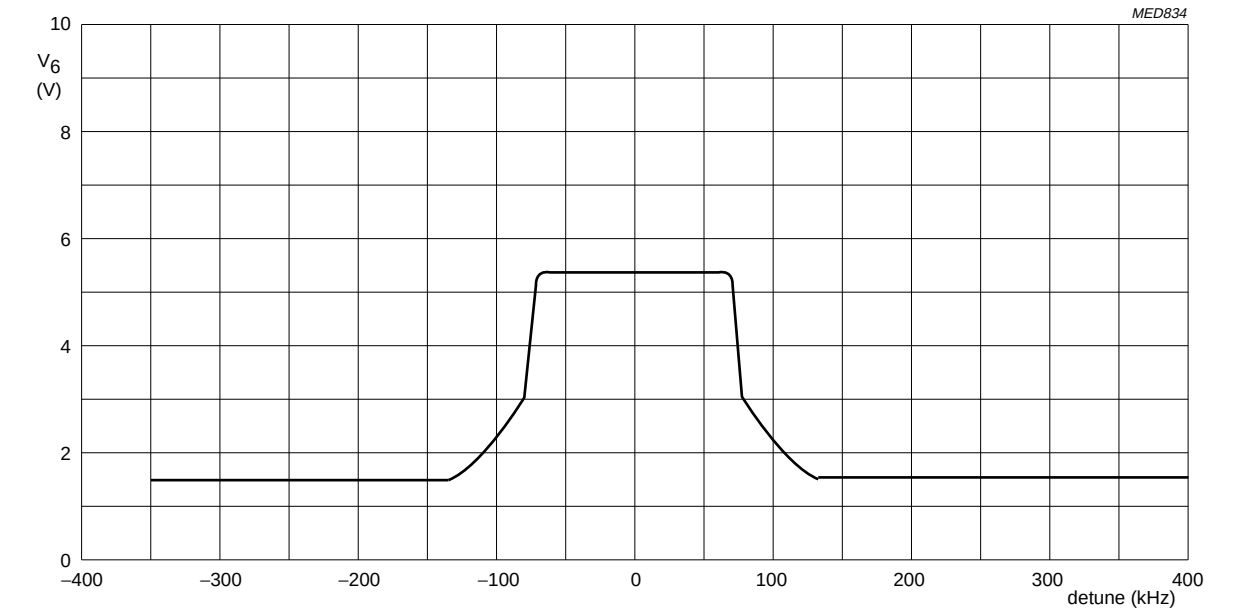


Fig.15 Control voltage V_6 dependent on detuning; V_{iIF} = 10 mV RMS.

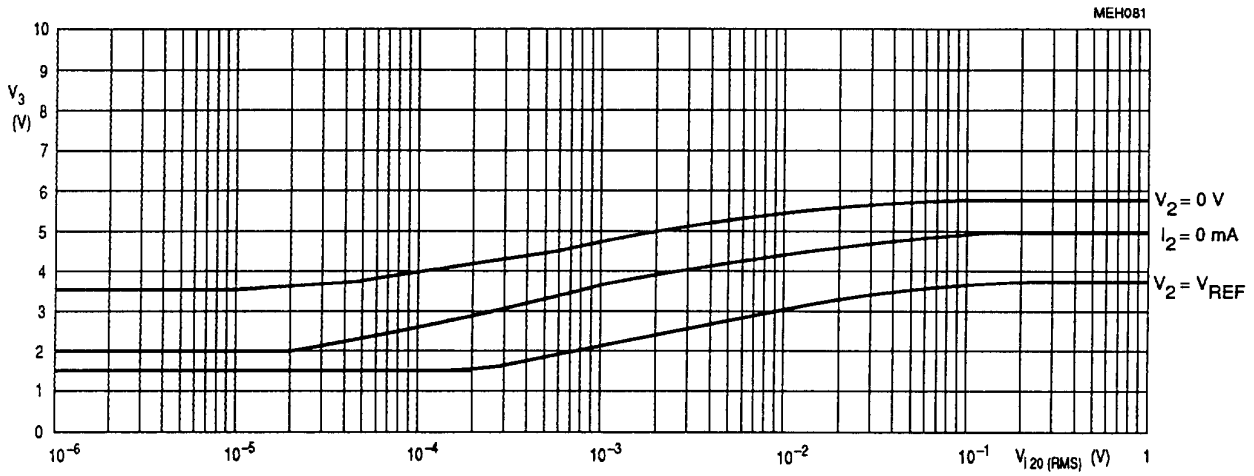


Fig.16 Level output voltage V_3 dependent on input signal V_{iIF} (pin 20); typical adjusting range.

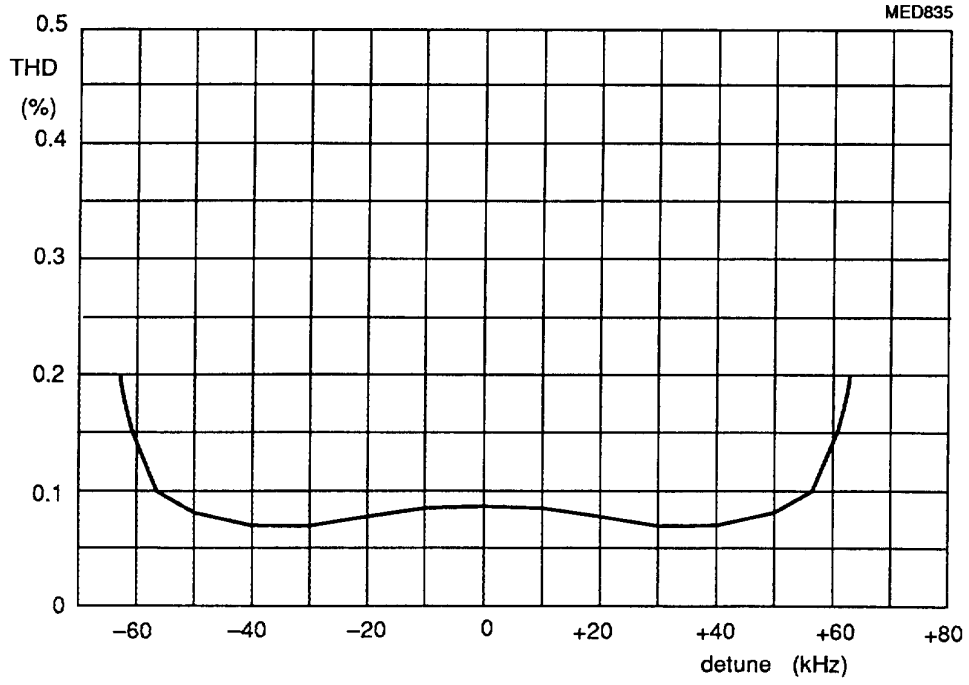


Fig.17 Total harmonic distortion dependent on detuning at FM-MUTE-ON; deviation ±75 kHz; f_m = 1 kHz; V_{iIF} = 10 mV.

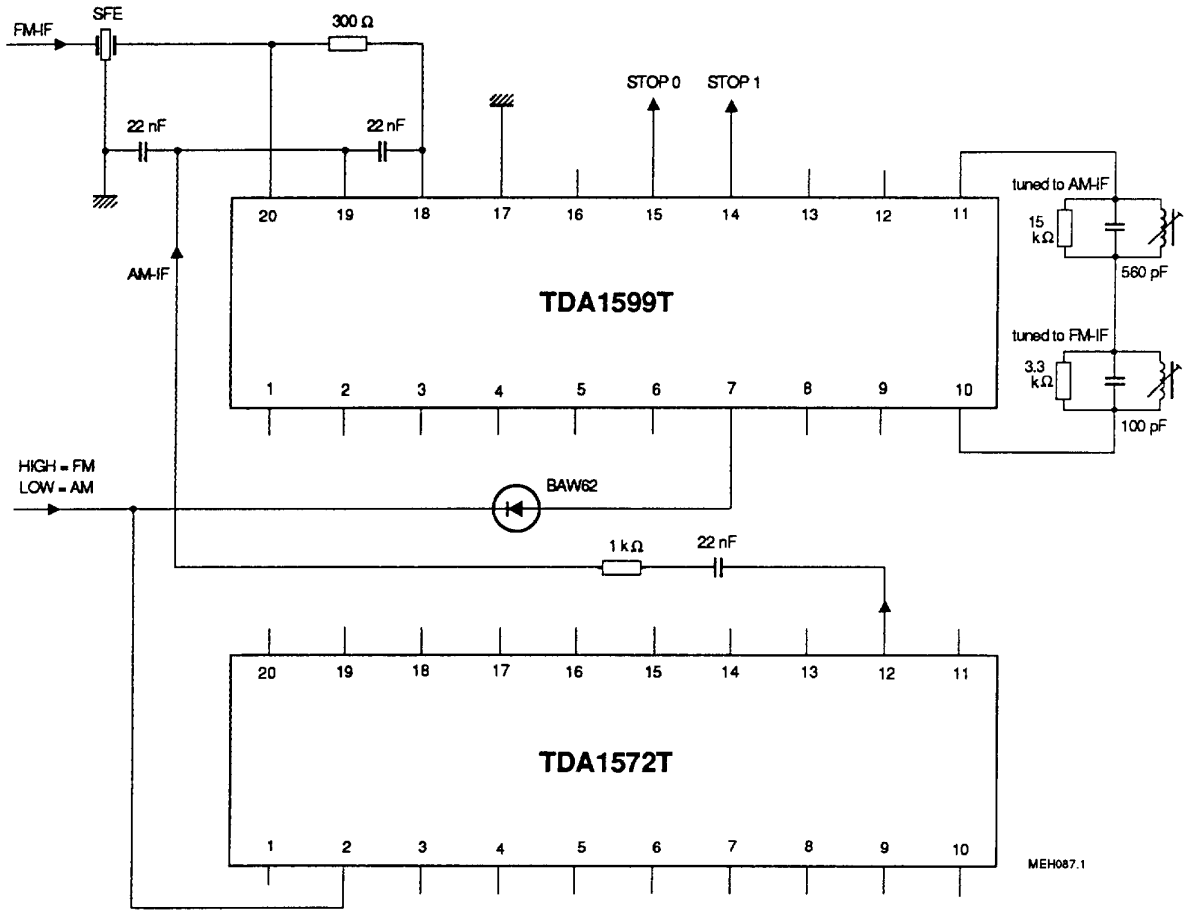


Fig.18 Interface for AM stop pulse application (SO-version).

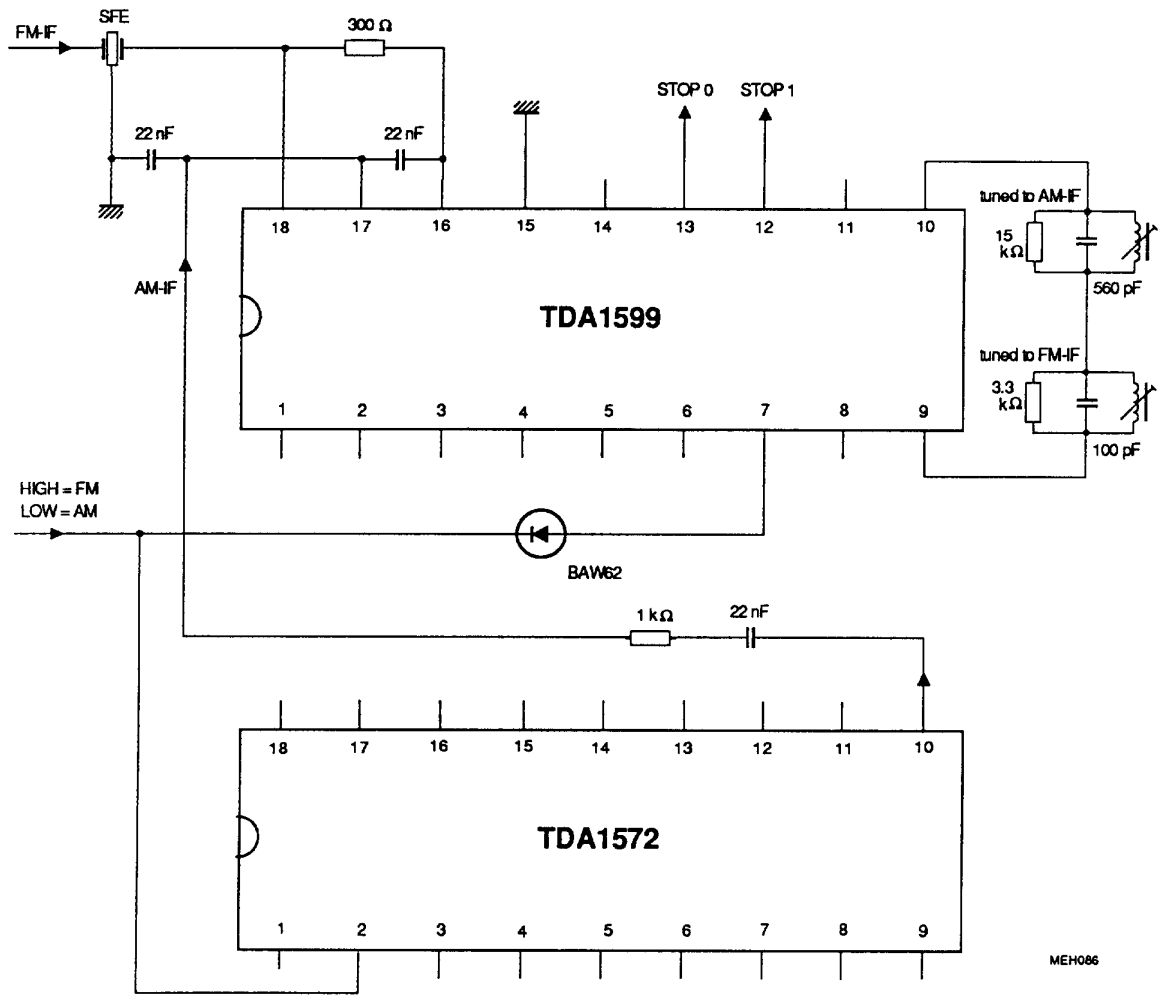
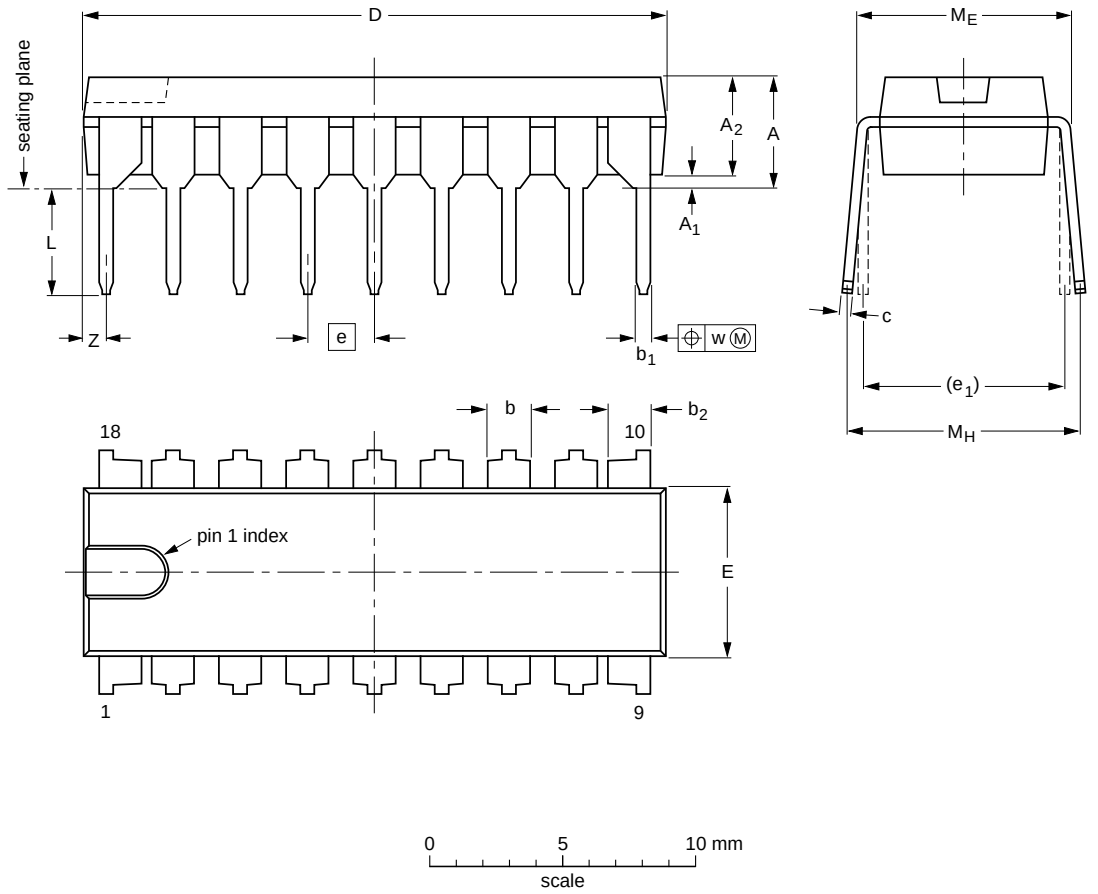


Fig.19 Interface for AM stop pulse application (DIL-version).

PACKAGE OUTLINES

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

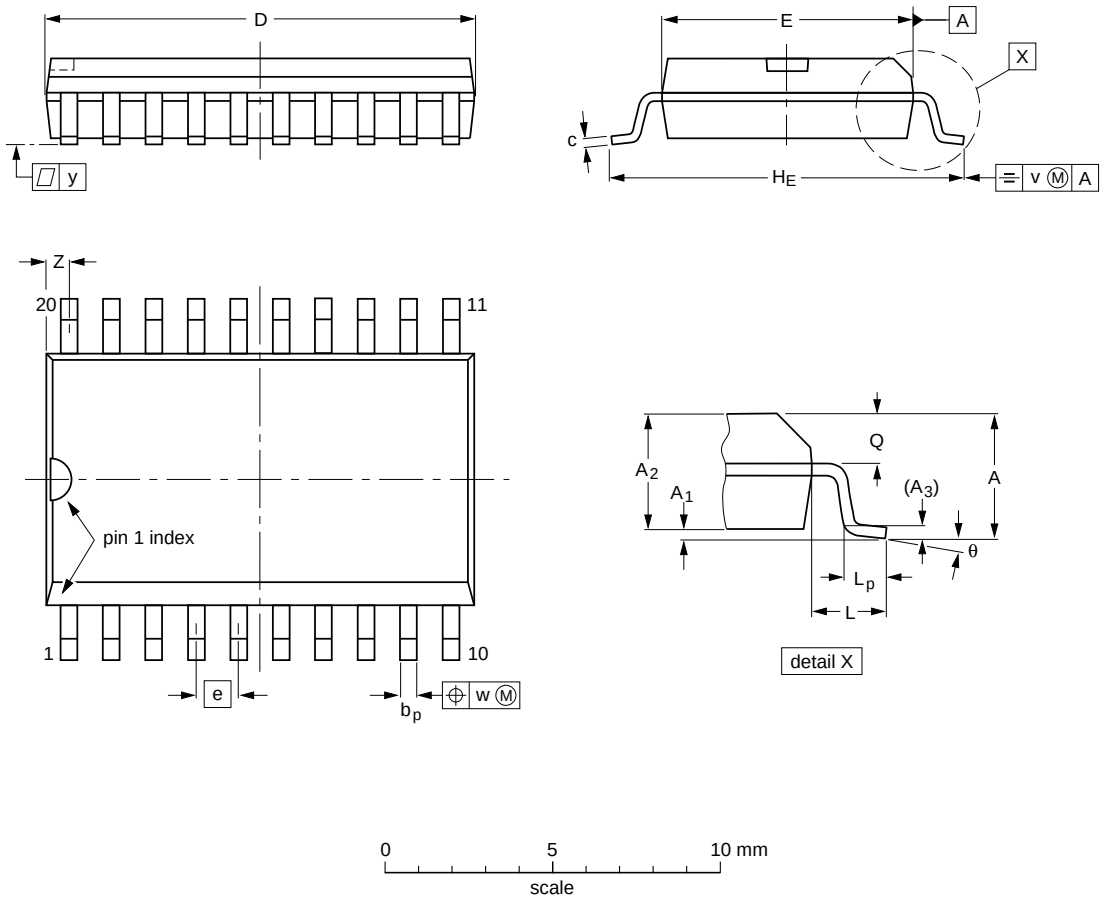
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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