TJA1041A

High-speed CAN transceiver

Rev. 04 — 29 July 2008 Product data sheet

1. General description

The TJA1041A provides an advanced interface between the protocol controller and the physical bus in a Controller Area Network (CAN) node. The TJA1041A is primarily intended for automotive high-speed CAN applications (up to 1 Mbit/s). The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller. The TJA1041A is fully compatible to the ISO 11898 standard, and offers excellent ElectroMagnetic Compatibility (EMC) performance, very low power consumption, and passive behavior when supply voltage is off. The advanced features include:

- Low-power management, supporting local and remote wake-up with wake-up source recognition and the capability to control the power supply in the rest of the node
- Several protection and diagnosis functions including short circuits of the bus lines and first battery connection
- Automatic adaptation of the I/O-levels, in line with the supply voltage of the controller

2. Features

2.1 Optimized for in-vehicle high-speed communication

- Fully compatible with the ISO 11898 standard
- Communication speed up to 1 Mbit/s
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with wide common-mode range, offering high ElectroMagnetic Immunity (EMI)
- Passive behavior when supply voltage is off
- Automatic I/O-level adaptation to the host controller supply voltage
- Recessive bus DC voltage stabilization for further improvement of EME behavior
- Listen-only mode for node diagnosis and failure containment
- Allows implementation of large networks (more than 110 nodes)

2.2 Low-power management

- Very low-current in Standby and Sleep mode, with local and remote wake-up
- Capability to power down the entire node, still allowing local and remote wake-up
- Wake-up source recognition

2.3 Protection and diagnosis (detection and signalling)

- TXD dominant clamping handler with diagnosis

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- RXD recessive clamping handler with diagnosis
- TXD-to-RXD short circuit handler with diagnosis
- Overtemperature protection with diagnosis
- Undervoltage detection on pins V_{CC}, $V_{I/O}$ and V_{BAT}
- Automotive environment transient protected bus pins and pin V_{BAT}
- Short circuit proof bus pins and pin SPLIT (to battery and to ground)
- Bus line short circuit diagnosis
- Bus dominant clamping diagnosis
- Cold start diagnosis (first battery connection)

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	DC voltage on pin V_{CC}	operating range	4.75	-	5.25	V
$V_{I/O}$	DC voltage on pin $V_{I/O}$	operating range	2.8	-	5.25	V
I_{BAT}	V_{BAT} input current	normal or pwon/listen-only mode	15	30	40	µA
		standby mode; V_{CC} > 4.75 V; $V_{I/O}$ = 2.8 V; V_{INH} = V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
		sleep mode; V_{INH} = V_{CC} = $V_{I/O}$ = 0 V; V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
V_{CANH}	DC voltage on pin CANH	0 V < V_{CC} < 5.25 V; no time limit	–27	-	+40	V
V_{CANL}	DC voltage on pin CANL	0 V < V_{CC} < 5.25 V; no time limit	–27	-	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	0 V < V_{CC} < 5.25 V; no time limit	–27	-	+40	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM) [1]				
		pins CANH, CANL and SPLIT	–6	-	+6	kV
		pins TXD, RXD, $V_{I/O}$ and $\overline{STB}$	–3	-	+3	kV
		all other pins	–4	-	+4	kV
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	40	-	255	ns
T_{vj}	virtual junction temperature		–40	-	+150	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor (6 kV level with pin GND connected to ground).

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4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1041AT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
TJA1041AU	-	bare die; 1920 × 3190 × 380 µm	-

5. Block diagram

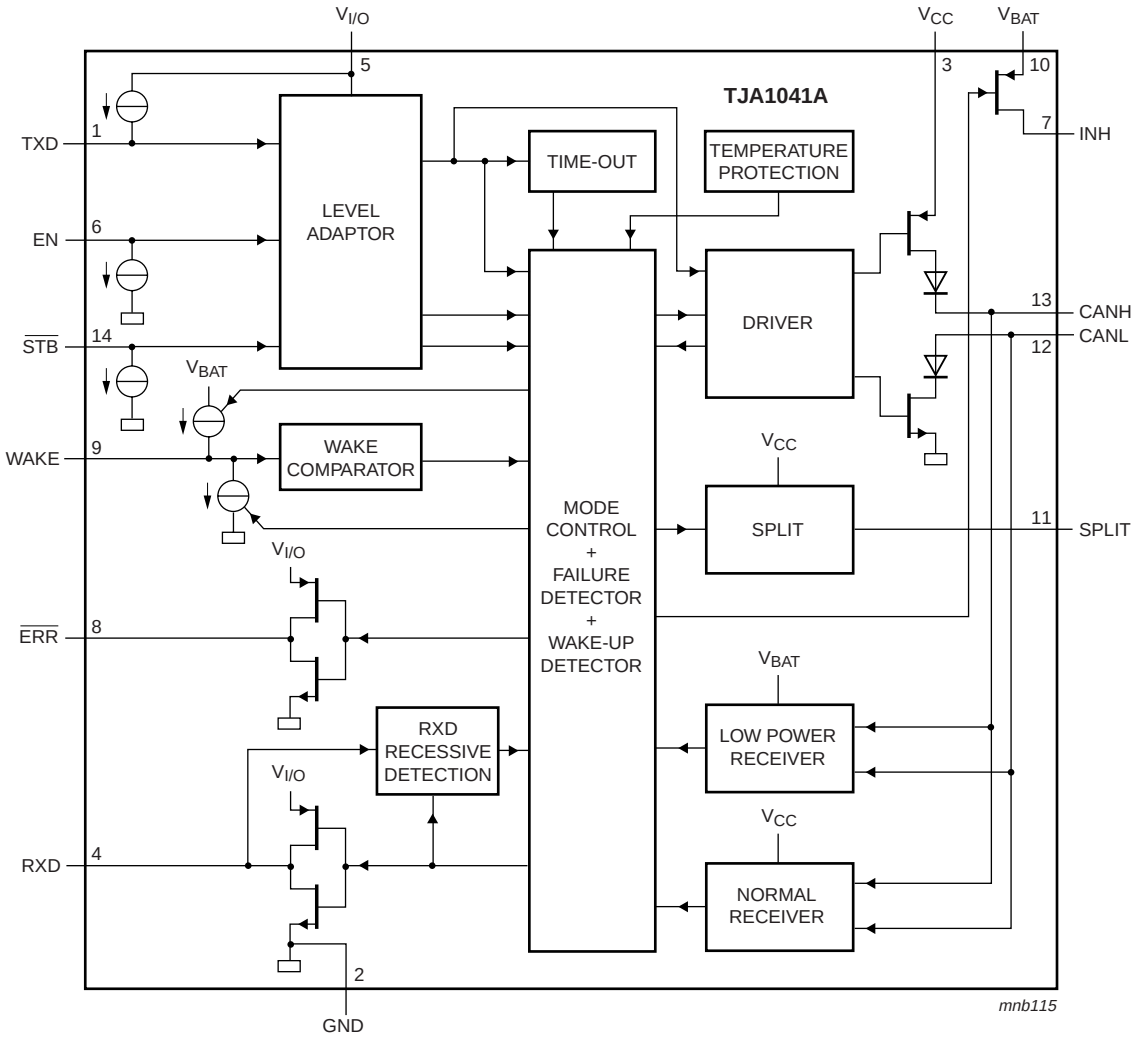


Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

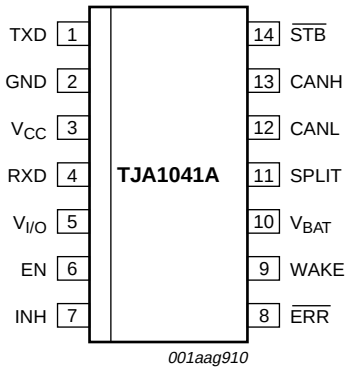


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD	1	transmit data input
GND	2	ground
V_{CC}	3	transceiver supply voltage input
RXD	4	receive data output; reads out data from the bus lines
$V_{I/O}$	5	I/O-level adapter voltage input
EN	6	enable control input
INH	7	inhibit output for switching external voltage regulators
$\overline{ERR}$	8	error and power-on indication output (active LOW)
WAKE	9	local wake-up input
V_{BAT}	10	battery voltage input
SPLIT	11	common-mode stabilization output
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
$\overline{STB}$	14	standby control input (active LOW)

7. Functional description

The primary function of a CAN transceiver is to provide the CAN physical layer as described in the ISO 11898 standard. In the TJA1041A this primary function is complemented with a number of operating modes, fail-safe features and diagnosis features, which offer enhanced system reliability and advanced power management functionality.

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7.1 Operating modes

The TJA1041A can be operated in five modes, each with specific features. Control pins $\overline{STB}$ and EN select the operating mode. Changing between modes also gives access to a number of diagnostics flags, available via pin $\overline{ERR}$. The following sections describe the five operating modes. Table 4 shows the conditions for selecting these modes. Figure 3 illustrates the mode transitions when V_{CC}, $V_{I/O}$ and V_{BAT} are present.

Table 4. Operating mode selection

Control pins		Internal flags			Operating mode	Pin INH
$\overline{STB}$	EN	UV_{NOM}	UV_{BAT}	pwon; wake-up		
X	X	set	X	X[1]	Sleep mode[2]	floating
		cleared	set	one or both set	Standby mode	H
				both cleared	no change from Sleep mode	floating
					Standby mode from any other mode	H
L	L	cleared	cleared	one or both set	Standby mode	H
				both cleared	no change from Sleep mode	floating
					Standby mode from any other mode	H
L	H	cleared	cleared	one or both set	Standby mode	H
				both cleared	no change from Sleep mode	floating
					Go-to-sleep command mode from any other mode[3]	H[3]
H	L	cleared	cleared	X	Pwon/Listen-only mode	H
H	H	cleared	cleared	X	Normal mode[4]	H

[1] Setting the pwon flag or the wake-up flag will clear the UV_{NOM} flag.

[2] The transceiver directly enters Sleep mode and pin INH is set floating when the UV_{NOM} flag is set (so after the undervoltage detection time on either V_{CC} or $V_{I/O}$ has elapsed before that voltage level has recovered).

[3] When Go-to-sleep command mode is selected for longer than the minimum hold time of the go-to-sleep command, the transceiver will enter Sleep mode and pin INH is set floating.

[4] On entering Normal mode the pwon flag and the wake-up flag will be cleared.

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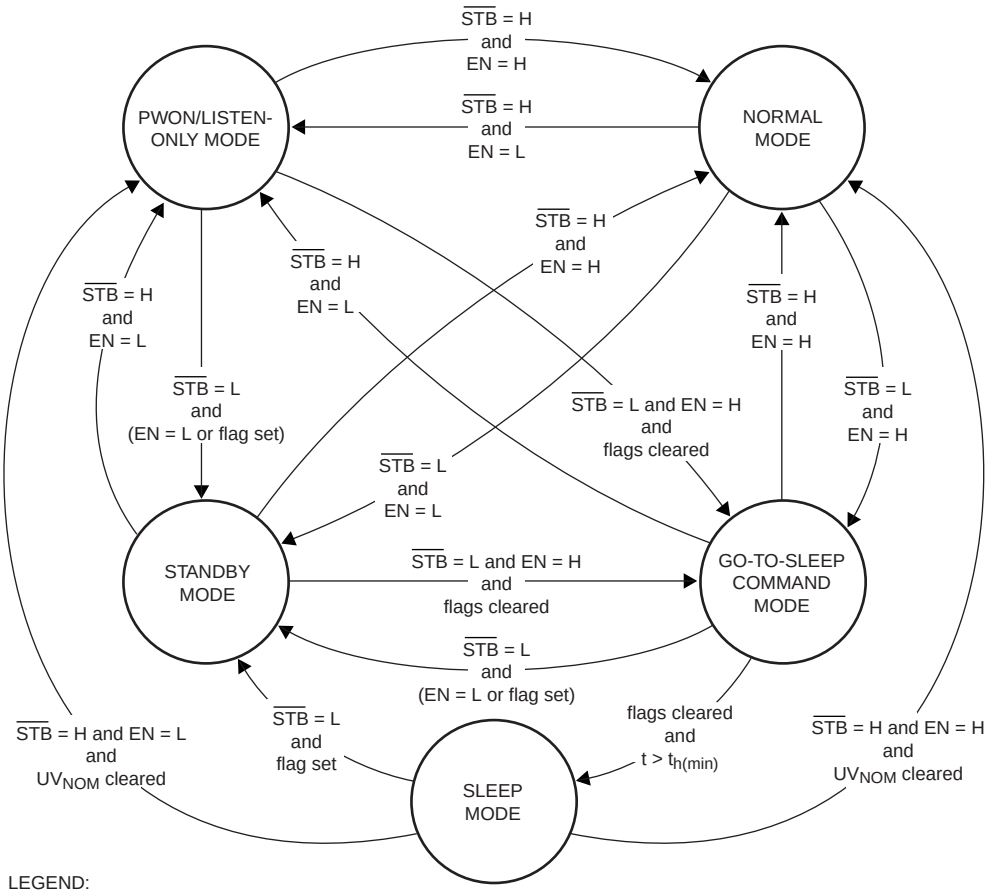


Fig 3. Mode transitions when V_{CC}, $V_{I/O}$ and V_{BAT} are present

7.1.1 Normal mode

Normal mode is the mode for normal bidirectional CAN communication. The receiver will convert the differential analog bus signal on pins CANH and CANL into digital data, available for output to pin RXD. The transmitter will convert digital data on pin TXD into a differential analog signal, available for output to the bus pins. The bus pins are biased at $0.5V_{CC}$ (via $R_{i(cm)}$). Pin INH is active, so voltage regulators controlled by pin INH (see Figure 4) will be active too.

7.1.2 Pwon/Listen-only mode

In Pwon/Listen-only mode the transmitter of the transceiver is disabled, effectively providing a transceiver listen-only behavior. The receiver will still convert the analog bus signal on pins CANH and CANL into digital data, available for output to pin RXD. As in Normal mode the bus pins are biased at $0.5V_{CC}$, and pin INH remains active.

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7.1.3 Standby mode

The Standby mode is the first-level power saving mode of the transceiver, offering reduced current consumption. In Standby mode the transceiver is not able to transmit or receive data and the low-power receiver is activated to monitor bus activity. The bus pins are biased at ground level (via $R_{i(cm)}$). Pin INH is still active, so voltage regulators controlled by this pin INH will be active too.

Pins RXD and $\overline{ERR}$ will reflect any wake-up requests (provided that $V_{I/O}$ and V_{CC} are present).

7.1.4 Go-to-sleep command mode

The Go-to-sleep command mode is the controlled route for entering Sleep mode. In Go-to-sleep command mode the transceiver behaves as if in Standby mode, plus a Go-to-sleep command is issued to the transceiver. After remaining in Go-to-sleep command mode for the minimum hold time ($t_{h(min)}$), the transceiver will enter Sleep mode. The transceiver will not enter the Sleep mode if the state of pins $\overline{STB}$ or EN is changed or the UV_{BAT}, pwon or wake-up flag is set before $t_{h(min)}$ has expired.

7.1.5 Sleep mode

The Sleep mode is the second-level power saving mode of the transceiver. Sleep mode is entered via the Go-to-sleep command mode, and also when the undervoltage detection time on either V_{CC} or $V_{I/O}$ elapses before that voltage level has recovered. In Sleep mode the transceiver still behaves as described for Standby mode, but now pin INH is set floating. Voltage regulators controlled by pin INH will be switched off, and the current into pin V_{BAT} is reduced to a minimum. Waking up a node from Sleep mode is possible via the wake-up flag and (as long as the UV_{NOM} flag is not set) via pin $\overline{STB}$.

7.2 Internal flags

The TJA1041A makes use of seven internal flags for its fail-safe fallback mode control and system diagnosis support. Table 4 shows the relation between flags and operating modes of the transceiver. Five of the internal flags can be made available to the controller via pin $\overline{ERR}$. Table 5 shows the details on how to access these flags. The following sections describe the seven internal flags.

Table 5. Accessing internal flags via pin $\overline{ERR}$

Internal flag	Flag is available on pin $\overline{ERR}$[1]	Flag is cleared
UV_{NOM}	no	by setting the pwon or wake-up flag
UV_{BAT}	no	when V_{BAT} has recovered
pwon	in Pwon/Listen-only mode (coming from Standby mode, Go-to-sleep command mode, or Sleep mode)	on entering Normal mode
wake-up	in Standby mode, Go-to-sleep command mode, and Sleep mode (provided that $V_{I/O}$ and V_{CC} are present)	on entering Normal mode, or by setting the pwon or UV_{NOM} flag

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Table 5. Accessing internal flags via pin $\overline{ERR}$ *…continued*

Internal flag	Flag is available on pin $\overline{ERR}$[1]	Flag is cleared
wake-up source	in Normal mode (before the fourth dominant to recessive edge on pin TXD[2])	on leaving Normal mode, or by setting the pwon flag
bus failure	in Normal mode (after the fourth dominant to recessive edge on pin TXD[2])	on reentering Normal mode
local failure	in Pwon/Listen-only mode (coming from Normal mode)	on entering Normal mode or when RXD is dominant while TXD is recessive (provided that all local failures are resolved)

[1] Pin $\overline{ERR}$ is an active-LOW output, so a LOW-level indicates a set flag and a HIGH-level indicates a cleared flag. Allow pin $\overline{ERR}$ to stabilize for at least 8 µs after changing operating modes.

[2] Allow for a TXD dominant time of at least 4 µs per dominant-recessive cycle.

7.2.1 UV_{NOM} flag

UV_{NOM} is the V_{CC} and $V_{I/O}$ undervoltage detection flag. The flag is set when the voltage on pin V_{CC} drops below $V_{CC(sleep)}$ for longer than $t_{UV(VCC)}$ or when the voltage on pin $V_{I/O}$ drops below $V_{I/O(sleep)}$ for longer than $t_{UV(VI/O)}$. When the UV_{NOM} flag is set, the transceiver will enter Sleep mode to save power and not disturb the bus. In Sleep mode the voltage regulators connected to pin INH are disabled, avoiding the extra power consumption in case of a short circuit condition. After a waiting time (fixed by the same timers used for setting UV_{NOM}) any wake-up request or setting of the pwon flag will clear UV_{NOM} and the timers, allowing the voltage regulators to be reactivated at least until UV_{NOM} is set again.

7.2.2 UV_{BAT} flag

UV_{BAT} is the V_{BAT} undervoltage detection flag. The flag is set when the voltage on pin V_{BAT} drops below $V_{BAT(stb)}$. When UV_{BAT} is set, the transceiver will try to enter Standby mode to save power and not disturb the bus. UV_{BAT} is cleared when the voltage on pin V_{BAT} has recovered. The transceiver will then return to the operating mode determined by the logic state of pins $\overline{STB}$ and EN.

7.2.3 Pwon flag

Pwon is the V_{BAT} power-on flag. This flag is set when the voltage on pin V_{BAT} has recovered after it dropped below $V_{BAT(pwon)}$, particularly after the transceiver was disconnected from the battery. By setting the pwon flag, the UV_{NOM} flag and timers are cleared and the transceiver cannot enter Sleep mode. This ensures that any voltage regulator connected to pin INH is activated when the node is reconnected to the battery. In Pwon/Listen-only mode the pwon flag can be made available on pin $\overline{ERR}$. The flag is cleared when the transceiver enters Normal mode.

7.2.4 Wake-up flag

The wake-up flag is set when the transceiver detects a local or a remote wake-up request. A local wake-up request is detected when a logic state change on pin WAKE remains stable for at least t_{wake}. A remote wake-up request is detected after two bus dominant states of at least t_{BUSdom} (with each dominant state followed by a recessive state of at least t_{BUSrec}). The wake-up flag can only be set in Standby mode, Go-to-sleep command mode or Sleep mode. Setting of the flag is blocked during the UV_{NOM} flag waiting time. By setting the wake-up flag, the UV_{NOM} flag and timers are cleared. The wake-up flag is

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immediately available on pins $\overline{ERR}$ and RXD (provided that $V_{I/O}$ and V_{CC} are present). The flag is cleared at power-on, or when the UV_{NOM} flag is set or the transceiver enters Normal mode.

7.2.5 Wake-up source flag

Wake-up source recognition is provided via the wake-up source flag, which is set when the wake-up flag is set by a local wake-up request via pin WAKE. The wake-up source flag can only be set after the pwon flag is cleared. In Normal mode the wake-up source flag can be made available on pin $\overline{ERR}$. The flag is cleared at power-on or when the transceiver leaves Normal mode.

7.2.6 Bus failure flag

The bus failure flag is set if the transceiver detects a bus line short circuit condition to V_{BAT}, V_{CC} or GND during four consecutive dominant-recessive cycles on pin TXD, when trying to drive the bus lines dominant. In Normal mode the bus failure flag can be made available on pin $\overline{ERR}$. The flag is cleared when the transceiver reenters Normal mode.

7.2.7 Local failure flag

In Normal mode or Pwon/Listen-only mode the transceiver can recognize five different local failures and will combine them into one local failure flag. The five local failures are: TXD dominant clamping, RXD recessive clamping, a TXD-to-RXD short circuit, bus dominant clamping, and overtemperature. Nature and detection of these local failures is described in Section 7.3. In Pwon/Listen-only mode the local failure flag can be made available on pin $\overline{ERR}$. The flag is cleared when entering Normal mode or when RXD is dominant while TXD is recessive, provided that all local failures are resolved.

7.3 Local failures

The TJA1041A can detect five different local failure conditions. Any of these failures will set the local failure flag. In most cases the transmitter of the transceiver will be disabled. The following sections give the details.

7.3.1 TXD dominant clamping detection

A permanent LOW-level on pin TXD (due to a hardware or software application failure) would drive the CAN bus into a permanent dominant state, blocking all network communication. The TXD dominant time-out function prevents such a network lockup by disabling the transmitter of the transceiver if pin TXD remains at a LOW level for longer than the TXD dominant time-out $t_{dom(TXD)}$. The $t_{dom(TXD)}$ timer defines the minimum possible bit rate of 40 kbit/s. The transmitter remains disabled until the local failure flag is cleared.

7.3.2 RXD recessive clamping detection

An RXD pin clamped to HIGH-level will prevent the controller connected to this pin from recognizing a bus dominant state. So the controller can start messages at any time, which is likely to disturb all bus communication. RXD recessive clamping detection prevents this effect by disabling the transmitter when the bus is in dominant state without RXD reflecting this. The transmitter remains disabled until the local failure flag is cleared.

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7.3.3 TXD-to-RXD short-circuit detection

A short circuit between pins RXD and TXD would keep the bus in a permanent dominant state once the bus is driven dominant, because the low-side driver of RXD is typically stronger than the high-side driver of the controller connected to TXD. The TXD-to-RXD short circuit detection prevents such a network lockup by disabling the transmitter. The transmitter remains disabled until the local failure flag is cleared.

7.3.4 Bus dominant clamping detection

A CAN bus short circuit (to V_{BAT}, V_{CC} or GND) or a failure in one of the other network nodes could result in a differential voltage on the bus high enough to represent a bus dominant state. Because a node will not start transmission if the bus is dominant, the normal bus failure detection will not detect this failure, but the bus dominant clamping detection will. The local failure flag is set if the dominant state on the bus persists for longer than $t_{dom(bus)}$. By checking this flag, the controller can determine if a clamped bus is blocking network communication. There is no need to disable the transmitter. Note that the local failure flag does not retain a bus dominant clamping failure and is released as soon as the bus returns to recessive state.

7.3.5 Overtemperature detection

To protect the output drivers of the transceiver against overheating, the transmitter will be disabled if the virtual junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$. The transmitter remains disabled until the local failure flag is cleared.

7.4 Recessive bus voltage stabilization

In recessive state the output impedance of transceivers is relatively high. In a partially powered network (supply voltage is off in some of the nodes) any deactivated transceiver with a significant leakage current is likely to load the recessive bus to ground. This will cause a common-mode voltage step each time transmission starts, resulting in increased EME. Using pin SPLIT of the TJA1041A in combination with split termination (see Figure 5) will reduce this step effect. In Normal mode and Pwon/Listen-only mode pin SPLIT provides a stabilized $0.5V_{CC}$ DC voltage. In Standby mode, Go-to-sleep command mode and Sleep mode pin SPLIT is set floating.

7.5 I/O level adapter

The TJA1041A is equipped with a built-in I/O-level adapter. By using the supply voltage of the controller (to be supplied at pin $V_{I/O}$) the level adapter ratiometrically scales the I/O-levels of the transceiver. For pins TXD, $\overline{STB}$ and EN the digital input threshold level is adjusted, and for pins RXD and $\overline{ERR}$ the HIGH-level output voltage is adjusted. This allows the transceiver to be directly interfaced with controllers on supply voltages between 2.8 V and 5.25 V, without the need for glue logic.

7.6 Pin WAKE

Pin WAKE of the TJA1041A allows local wake-up triggering by a LOW-to-HIGH state change as well as a HIGH-to-LOW state change. This gives maximum flexibility when designing a local wake-up circuit. To keep current consumption at a minimum, after a t_{wake} delay the internal bias voltage of pin WAKE will follow the logic state of this pin. A HIGH level on pin WAKE is followed by an internal pull-up to V_{BAT}. A LOW level on pin WAKE is

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followed by an internal pull-down towards GND. To ensure EMI performance in applications not using local wake-up it is recommended to connect pin WAKE to pin V_{BAT} or to pin GND.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	DC voltage on pin V_{CC}	no time limit		–0.3	+6	V
		operating range		4.75	5.25	V
$V_{I/O}$	DC voltage on pin $V_{I/O}$	no time limit		–0.3	+6	V
		operating range		2.8	5.25	V
V_{BAT}	DC voltage on pin V_{BAT}	no time limit		–0.3	+40	V
		operating range		5	27	V
		load dump		-	40	V
V_{TXD}	DC voltage on pin TXD			–0.3	$V_{I/O}$ + 0.3	V
V_{RXD}	DC voltage on pin RXD			–0.3	$V_{I/O}$ + 0.3	V
V_{STB}	DC voltage on pin $\overline{STB}$			–0.3	$V_{I/O}$ + 0.3	V
V_{EN}	DC voltage on pin EN			–0.3	$V_{I/O}$ + 0.3	V
V_{ERR}	DC voltage on pin $\overline{ERR}$			–0.3	$V_{I/O}$ + 0.3	V
V_{INH}	DC voltage on pin INH			–0.3	V_{BAT} + 0.3	V
V_{WAKE}	DC voltage on pin WAKE			–0.3	V_{BAT} + 0.3	V
I_{WAKE}	DC current on pin WAKE			-	–15	mA
V_{CANH}	DC voltage on pin CANH	$0 < V_{CC} < 5.25$ V; no time limit		–27	+40	V
V_{CANL}	DC voltage on pin CANL	$0 < V_{CC} < 5.25$ V; no time limit		–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	$0 < V_{CC} < 5.25$ V; no time limit		–27	+40	V
V_{trt}	transient voltages on pins CANH, CANL, SPLIT and V_{BAT}	according to ISO 7637; see Figure 6		–200	+200	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM)	[1]			
		pins CANH, CANL and SPLIT		–6	+6	kV
		pins TXD, RXD, $V_{I/O}$ and $\overline{STB}$		–3	+3	kV
		all other pins		–4	+4	kV
		Machine Model (MM)	[2]	–200	+200	V
T_{vj}	virtual junction temperature		[3]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor (6 kV level with pin GND connected to ground).

[2] Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 10 Ω series resistor.

[3] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_{vj} = T_{amb} + P \times R_{th(vj-amb)}$, where $R_{th(vj-amb)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

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9. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient in SO14 package	in free air	120	K/W
$R_{th(j-s)}$	thermal resistance from junction to substrate of bare die	in free air	40	K/W

10. Characteristics

Table 8. Characteristics

V_{CC} = 4.75 V to 5.25 V; $V_{I/O}$ = 2.8 V to V_{CC}; V_{BAT} = 5 V to 27 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies (pins V_{BAT}, V_{CC} and $V_{I/O}$)						
$V_{CC(sleep)}$	V_{CC} undervoltage detection level for forced Sleep mode	V_{BAT} = 12 V (fail-safe)	2.75	3.3	4.5	V
$V_{I/O(sleep)}$	$V_{I/O}$ undervoltage detection level for forced Sleep mode		0.5	1.5	2	V
$V_{BAT(stb)}$	V_{BAT} voltage level for fail-safe fallback mode	V_{CC} = 5 V (fail-safe)	2.75	3.3	4.5	V
$V_{BAT(pwon)}$	V_{BAT} voltage level for setting pwon flag	V_{CC} = 0 V	2.5	3.3	4.1	V
I_{CC}	V_{CC} input current	normal mode; V_{TXD} = 0 V (dominant)	25	55	80	mA
		normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$ (recessive)	2	6	10	mA
		standby or sleep mode	-	1	10	µA
$I_{I/O}$	$V_{I/O}$ input current	normal mode; V_{TXD} = 0 V (dominant)	100	350	1000	µA
		normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$ (recessive)	15	80	200	µA
		standby or sleep mode	-	0	5	µA
I_{BAT}	V_{BAT} input current	normal or pwon/listen-only mode	15	30	40	µA
		standby mode; V_{CC} > 4.75 V; $V_{I/O}$ = 2.8 V; V_{INH} = V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
		sleep mode; V_{INH} = V_{CC} = $V_{I/O}$ = 0 V; V_{WAKE} = V_{BAT} = 12 V	10	20	30	µA
Transmitter data input (pin TXD)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	normal or pwon/listen-only mode; V_{TXD} = $V_{I/O}$	−5	0	+5	µA
I_{IL}	LOW-level input current	normal or pwon/listen-only mode; V_{TXD} = $0.3V_{I/O}$	−70	−250	−500	µA
C_i	input capacitance	not tested	-	5	10	pF

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Table 8. Characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; $V_{I/O}$ = 2.8 V to V_{CC}; V_{BAT} = 5 V to 27 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver data output (pin RXD)						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	−1	−3	−6	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; $V_{TXD} = V_{I/O}$; bus dominant	2	5	12	mA
Standby and enable control inputs (pins $\overline{STB}$ and EN)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	-	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{EN} = 0.7V_{I/O}$	1	4	10	µA
I_{IL}	LOW-level input current	$V_{STB} = V_{EN}$ = 0 V	-	0	−1	µA
Error and power-on indication output (pin $\overline{ERR}$)						
I_{OH}	HIGH-level output current	$V_{ERR} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	−4	−20	−50	µA
I_{OL}	LOW-level output current	V_{ERR} = 0.4 V	0.1	0.2	0.35	mA
Local wake-up input (pin WAKE)						
I_{IH}	HIGH-level input current	$V_{WAKE} = V_{BAT} - 1.9$ V	−1	−5	−10	µA
I_{IL}	LOW-level input current	$V_{WAKE} = V_{BAT} - 3.1$ V	1	5	10	µA
V_{th}	threshold voltage	V_{STB} = 0 V	$V_{BAT} - 3$	$V_{BAT} - 2.5$	$V_{BAT} - 2$	V
Inhibit output (pin INH)						
ΔV_H	HIGH-level voltage drop	I_{INH} = −0.18 mA	0.05	0.2	0.8	V
$\lvert I_L \rvert$	leakage current	sleep mode	-	0	5	µA
Bus lines (pins CANH and CANL)						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V				
		pin CANH	3	3.6	4.25	V
		pin CANL	0.5	1.4	1.75	V
$V_{O(dom)(m)}$	matching of dominant output voltage ($V_{CC} - V_{CANH} - V_{CANL}$)		−0.1	-	+0.15	V
$V_{O(dif)(bus)}$	differential bus output voltage ($V_{CANH} - V_{CANL}$)	V_{TXD} = 0 V (dominant); 45 Ω < R_L < 65 Ω	1.5	-	3.0	V
		$V_{TXD} = V_{I/O}$ (recessive); no load	−50	-	+50	mV
$V_{O(reces)}$	recessive output voltage	normal or pwon/listen-only mode; $V_{TXD} = V_{I/O}$; no load	2	$0.5V_{CC}$	3	V
		standby or sleep mode; no load	−0.1	0	+0.1	V
$I_{O(sc)}$	short-circuit output current	V_{TXD} = 0 V (dominant)				
		pin CANH; V_{CANH} = 0 V	−40	−70	−95	mA
		pin CANL; V_{CANL} = 40 V	40	70	95	mA
$I_{O(reces)}$	recessive output current	−27 V < V_{CAN} < 32 V	−2.5	-	+2.5	mA

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Table 8. Characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; $V_{I/O}$ = 2.8 V to V_{CC}; V_{BAT} = 5 V to 27 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{dif(th)}$	differential receiver threshold voltage	normal or pwon/listen-only mode (see Figure 7); −12 V < V_{CANH} < 12 V; −12 V < V_{CANL} < 12 V	0.5	0.7	0.9	V
		standby or sleep mode; −12 V < V_{CANH} < 12 V; −12 V < V_{CANL} < 12 V	0.4	0.7	1.15	V
$V_{hys(dif)}$	differential receiver hysteresis voltage	normal or pwon/listen-only mode (see Figure 7); −12 V < V_{CANH} < 12 V; −12 V < V_{CANL} < 12 V	50	70	100	mV
I_{LI}	input leakage current	V_{CC} = 0 V V_{CANH} = V_{CANL} = 5 V	100	170	250	µA
$R_{i(cm)}$	common-mode input resistance		15	25	35	kΩ
$R_{i(cm)(m)}$	common-mode input resistance matching	V_{CANH} = V_{CANL}	−3	0	+3	%
$R_{i(dif)}$	differential input resistance		25	50	75	kΩ
$C_{i(cm)}$	common-mode input capacitance	V_{TXD} = V_{CC}; not tested	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	V_{TXD} = V_{CC}; not tested	-	-	10	pF
$R_{sc(bus)}$	detectable short-circuit resistance between bus lines and V_{BAT}, V_{CC} and GND	normal mode	0	-	50	Ω
Common-mode stabilization output (pin SPLIT)						
V_o	output voltage	normal or pwon/listen-only mode; −500 µA < I_{SPLIT} < 500 µA	0.3V_{CC}	0.5V_{CC}	0.7V_{CC}	V
$\lvert I_L \rvert$	leakage current	standby or sleep mode; −22 V < V_{SPLIT} < 35 V	-	0	5	µA
Timing characteristics; see Figure 8) and 9						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	normal mode	25	70	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive	normal mode	10	50	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD	normal or pwon/listen-only mode	15	65	115	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD	normal or pwon/listen-only mode	35	100	160	ns
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	40	-	255	ns
$t_{UV(VCC)}$	undervoltage detection time on V_{CC}		5	10	12.5	ms
$t_{UV(VI/O)}$	undervoltage detection time on $V_{I/O}$		5	10	12.5	ms
$t_{dom(TXD)}$	TXD dominant time-out	V_{TXD} = 0 V	300	600	1000	µs
$t_{dom(bus)}$	bus dominant time-out	V_{dif} > 0.9 V	300	600	1000	µs
$t_{h(min)}$	minimum hold time of go-to-sleep command		20	35	50	µs

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Table 8. Characteristics *...continued*

V_{CC} = 4.75 V to 5.25 V; $V_{I/O}$ = 2.8 V to V_{CC}; V_{BAT} = 5 V to 27 V; R_L = 60 Ω; T_{vj} = −40 °C to +150 °C; unless otherwise specified; all voltages are defined with respect to ground; positive currents flow into the device [1].

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{BUSdom}	dominant time for wake-up via bus	standby or sleep mode; V_{BAT} = 12 V	0.75	1.75	5	µs
t_{BUSrec}	recessive time for wake-up via bus	standby or sleep mode; V_{BAT} = 12 V	0.75	1.75	5	µs
t_{wake}	minimum wake-up time after receiving a falling or rising edge	standby or sleep mode; V_{BAT} = 12 V	5	25	50	µs
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design, but only 100 % tested at T_{amb} = 125 °C for dies on wafer level and in addition to this, 100 % tested at T_{amb} = 125 °C for cased products, unless specified otherwise. For bare dies, all parameters are only guaranteed with the reverse side of the die connected to ground.

11. Application information

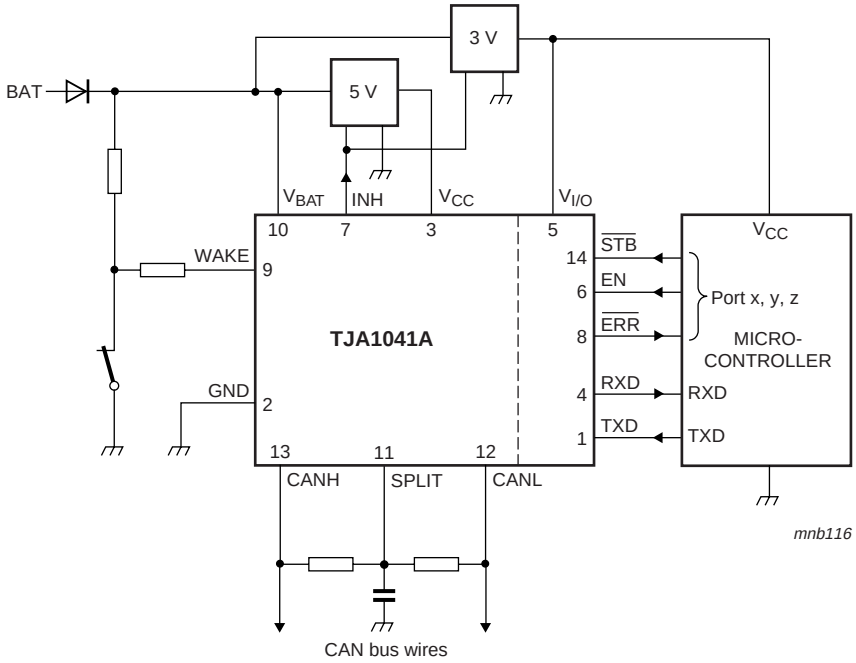


Fig 4. Typical application with 3 V microcontroller

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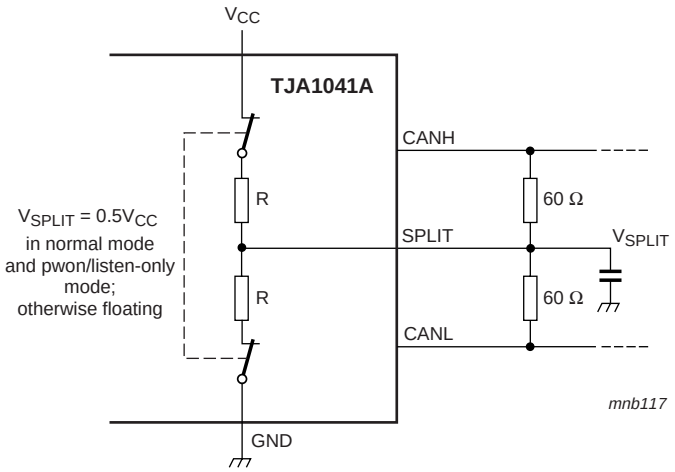
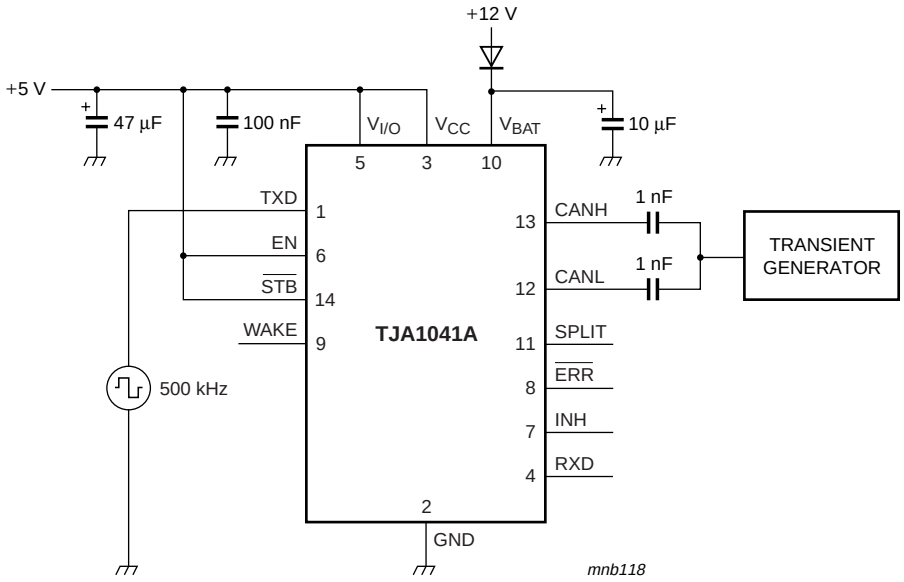


Fig 5. Stabilization circuitry and application

12. Test information



(1) The waveforms of the applied transients will be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, 5, 6 and 7.

Fig 6. Test circuit for automotive transients

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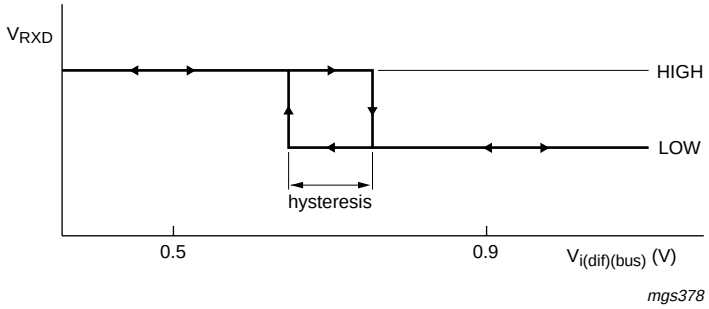


Fig 7. Hysteresis of the receiver

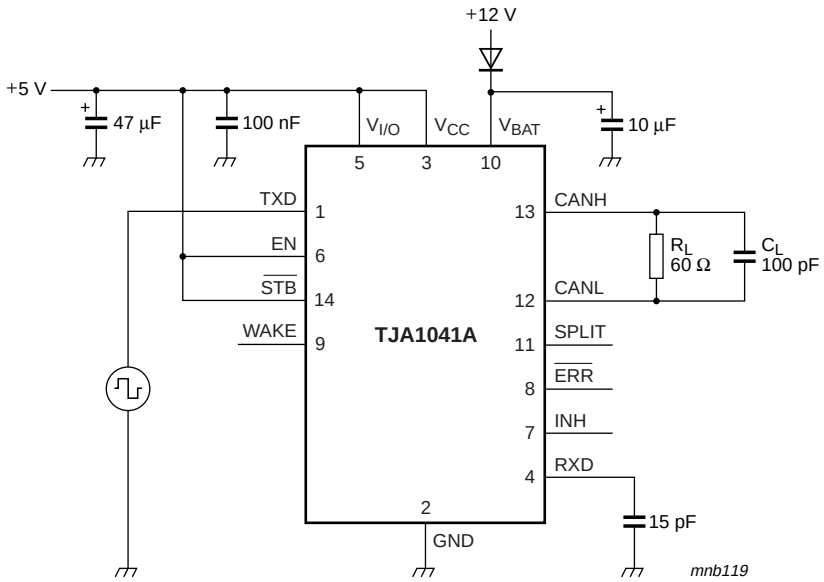
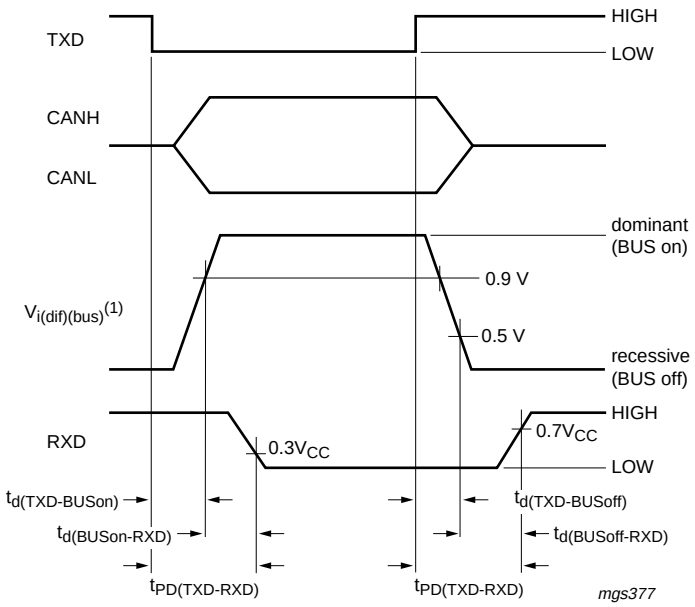


Fig 8. Test circuit for timing characteristics

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(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

Fig 9. Timing diagram

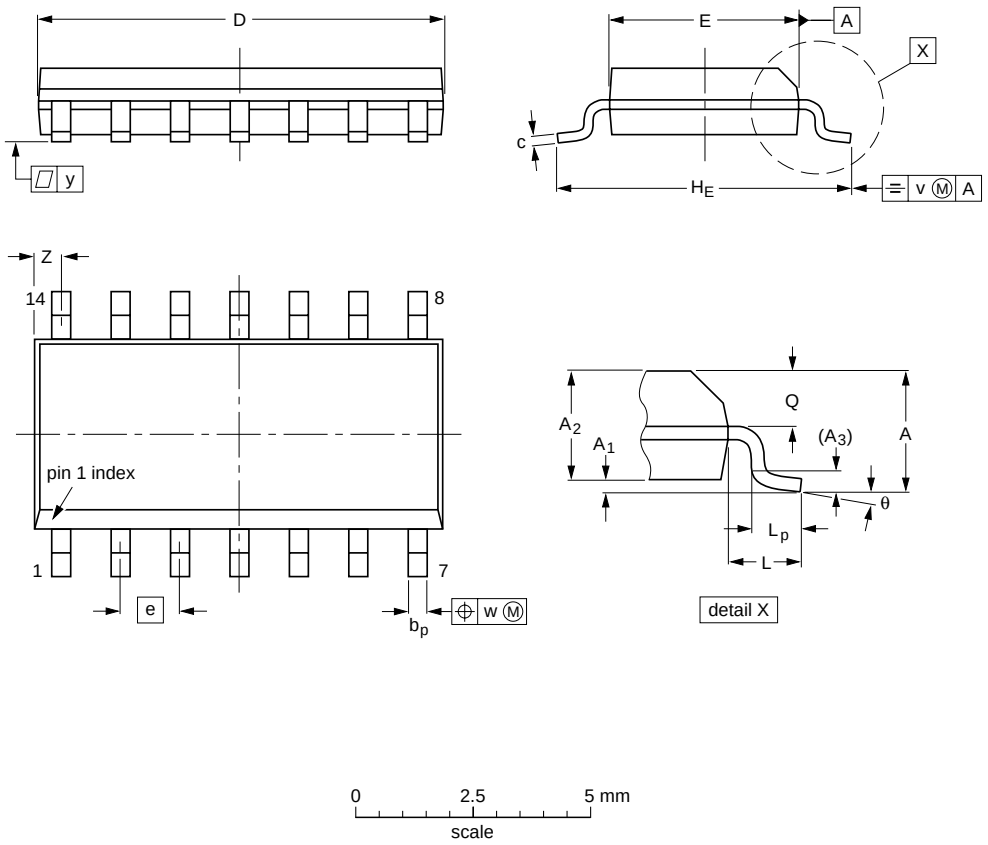
12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

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13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

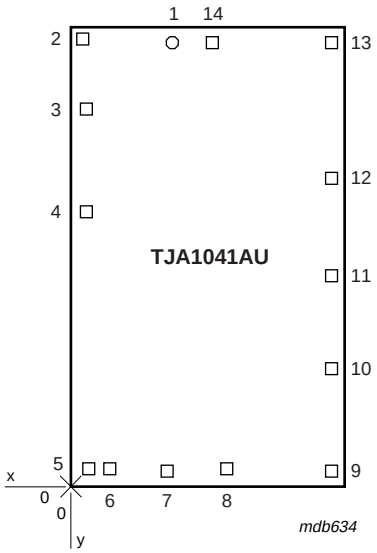
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT108-1 (SO14)

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14. Bare die outline



(1) The reverse side of the bare die must be connected to ground.

Fig 11. Bonding pad locations

Table 9. Bonding pad locations

Symbol	Pad	Coordinates[1]	
		x	y
TXD	1	664.25	3004.5
GND	2	75.75	3044.25
V_{CC}	3	115.5	2573
RXD	4	115.5	1862.75
$V_{I/O}$	5	115.5	115.5
EN	6	264.5	114
INH	7	667.75	85
$\overline{ERR}$	8	1076.75	115.5
WAKE	9	1765	85
V_{BAT}	10	1765	792.5
SPLIT	11	1765	1442.25
CANL	12	1765	2115
CANH	13	1751	3002.5
$\overline{STB}$	14	940.75	3004.5

[1] All x/y coordinates represent the position of the center of each pad (in μm) with respect to the left hand bottom corner of the top aluminium layer.

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15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

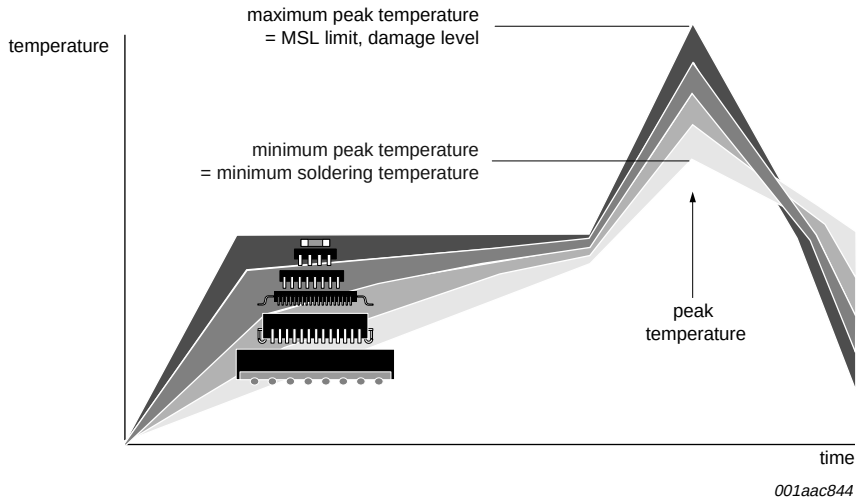
Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 12.

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MSL: Moisture Sensitivity Level

Fig 12. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1041A_4	20080729	Product data sheet	-	TJA1041A_3
Modifications:	• Table 8: corrected unit for I_{OH} - pin $\overline{ERR}$			
TJA1041A_3	20071204	Product data sheet	-	TJA1041A_2
TJA1041A_2	20040220	Product specification	-	TJA1041A_1
TJA1041A_1	20030929	Objective specification	-	-

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17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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