# TJA1042

## High-speed CAN transceiver with Standby mode

Rev. 10 — 24 November 2017 Product data sheet

## 1. General description

The TJA1042 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The TJA1042 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1040. It offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability
- TJA1042T/3 and TJA1042TK/3 can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

The TJA1042 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the TJA1042 an excellent choice for all types of HS-CAN networks, in nodes that require a low-power mode with wake-up capability via the CAN bus.

## 2. Features and benefits

### 2.1 General

- ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 compliant
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- $V_{IO}$ input on TJA1042T/3 and TJA1042TK/3 allows for direct interfacing with 3 V to 5 V microcontrollers
- SPLIT voltage output on TJA1042T for stabilizing the recessive bus level
- Available in SO8 package and leadless HVSON8 package (3.0 mm × 3.0 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- AEC-Q100 qualified

### 2.2 Predictable and fail-safe behavior

- Very low-current Standby mode with host and bus wake-up capability
- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)
- Transmit Data (TXD) dominant time-out function
- Bus-dominant time-out function in Standby mode
- Undervoltage detection on pins $V_{CC}$ and $V_{IO}$

### 2.3 Protections

- High ESD handling capability on the bus pins (±8 kV)
- High voltage robustness on CAN pins (±58 V)
- Bus pins protected against transients in automotive environments
- Thermally protected

## 3. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 4.5 | - | 5.5 | V |
| $V_{IO}$ | supply voltage on pin $V_{IO}$ | | 2.8 | - | 5.5 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | 3.5 | - | 4.5 | V |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin $V_{IO}$ | | 1.3 | 2.0 | 2.7 | V |
| $I_{CC}$ | supply current | Standby mode | - | 10 | 15 | µA |
| | | Normal mode; bus recessive | 2.5 | 5 | 10 | mA |
| | | Normal mode; bus dominant | 20 | 45 | 70 | mA |
| $I_{IO}$ | supply current on pin $V_{IO}$ | Standby mode; $V_{TXD} = V_{IO}$ | 5 | - | 14 | µA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD} = V_{IO}$ | 15 | 80 | 200 | µA |
| | | dominant; $V_{TXD} = 0$ V | - | 350 | 1000 | µA |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 at pins CANH and CANL | −8 | - | +8 | kV |
| $V_{CANH}$ | voltage on pin CANH | | −58 | - | +58 | V |
| $V_{CANL}$ | voltage on pin CANL | | −58 | - | +58 | V |
| $T_{vj}$ | virtual junction temperature | | −40 | - | +150 | °C |


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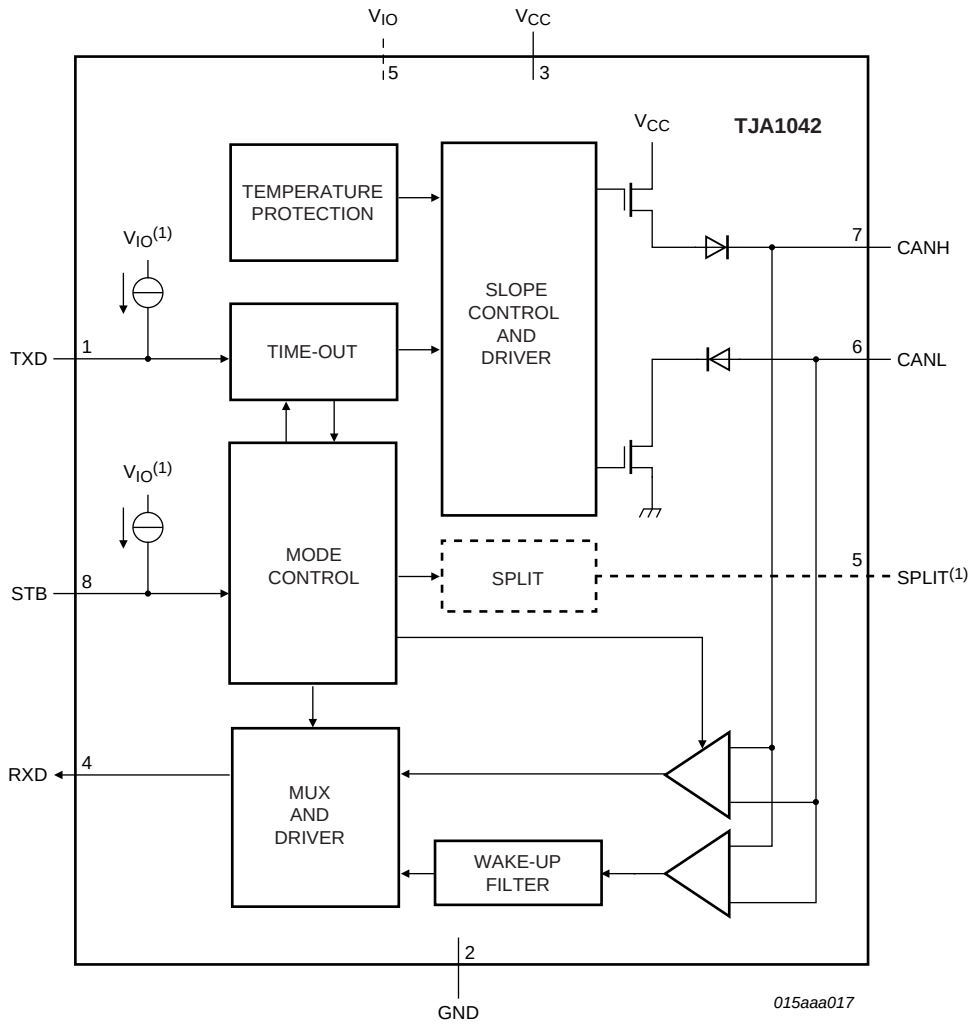
# 4. Ordering information

**Table 2. Ordering information**

| Type number[1] | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TJA1042T | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| TJA1042T/3 | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |
| TJA1042TK/3 | HVSON8 | plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm | SOT782-1 |

[1] TJA1042T with SPLIT pin; TJA1042T/3 and TJA1042TK/3 with $V_{IO}$ pin.

# 5. Block diagram




(1) In a transceiver with a SPLIT pin, the $V_{IO}$ input is internally connected to $V_{CC}$.

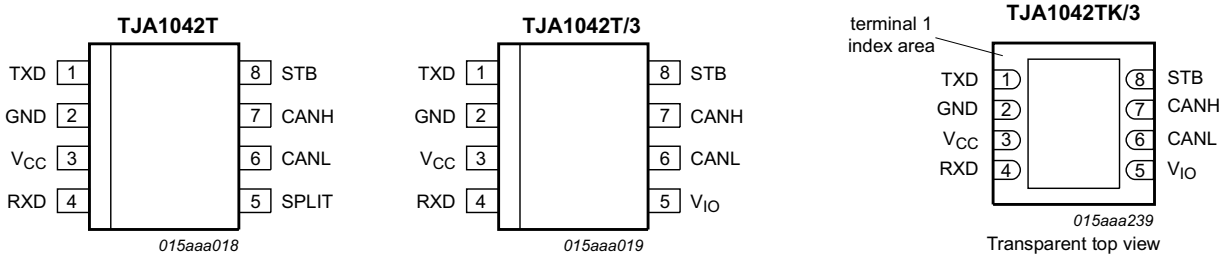
**Fig 1. Block diagram**


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# 6. Pinning information

## 6.1 Pinning




a. TJA1042T: SO8 b. TJA1042T/3: SO8 c. TJA1042TK/3: HVSON8

**Fig 2. Pin configuration diagrams**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| TXD | 1 | transmit data input |
| GND | 2[1] | ground supply |
| $V_{CC}$ | 3 | supply voltage |
| RXD | 4 | receive data output; reads out data from the bus lines |
| SPLIT | 5 | common-mode stabilization output; in TJA1042T version only |
| $V_{IO}$ | 5 | supply voltage for I/O level adapter; in TJA1042T/3 and TJA1042TK/3 versions only |
| CANL | 6 | LOW-level CAN bus line |
| CANH | 7 | HIGH-level CAN bus line |
| STB | 8 | Standby mode control input |

[1] HVSON8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.


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# 7. Functional description

The TJA1042 is a HS-CAN stand-alone transceiver with Standby mode. It combines the functionality of the PCA82C250, PCA82C251 and TJA1040 transceivers with improved EMC and ESD handling capability and quiescent current performance. Improved slope control and high DC handling capability on the bus pins provide additional application flexibility.

The TJA1042 is available in two versions, distinguished only by the function of pin 5:

- The TJA1042T is backwards compatible with the TJA1040 when used with a 5 V microcontroller, and also covers existing PCA82C250 and PCA82C251 applications
- The TJA1042T/3 and TJA1042TK/3 allow for direct interfacing to microcontrollers with supply voltages down to 3 V

## 7.1 Operating modes

The TJA1042 supports two operating modes, Normal and Standby, which are selected via pin STB. See Table 4 for a description of the operating modes under normal supply conditions.

**Table 4. Operating modes**

| Mode | Pin STB | Pin RXD | |
|---|---|---|---|
| | | LOW | HIGH |
| Normal | LOW | bus dominant | bus recessive |
| Standby | HIGH | wake-up request detected | no wake-up request detected |

### 7.1.1 Normal mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

### 7.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by $V_{IO}$, and is capable of detecting CAN bus activity even if $V_{IO}$ is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.


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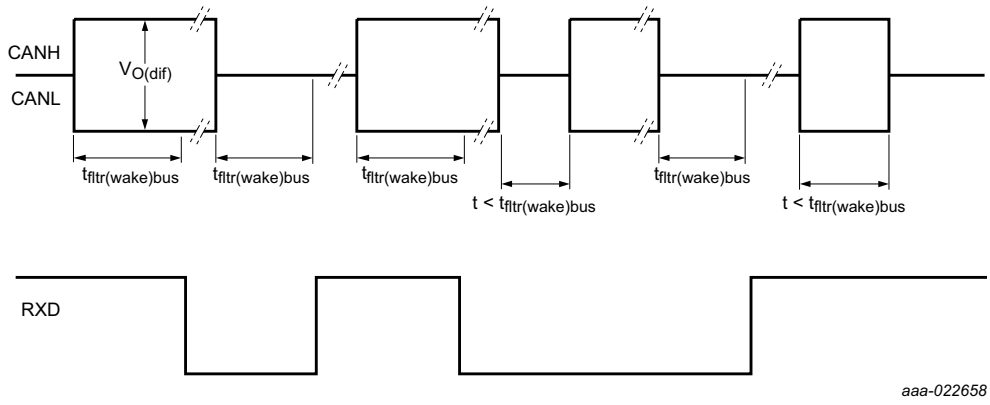



**Fig 3. Wake-up timing**

## 7.2 Fail-safe features

### 7.2.1 TXD dominant time-out function

A ‘TXD dominant time-out’ timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

### 7.2.2 Bus dominant time-out function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

### 7.2.3 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to $V_{IO}$ to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

### 7.2.4 Undervoltage detection on pins $V_{CC}$ and $V_{IO}$

Should $V_{CC}$ drop below the $V_{CC}$ undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until $V_{CC}$ has recovered.

Should $V_{IO}$ drop below the $V_{IO}$ undervoltage detection level, $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until $V_{IO}$ has recovered.


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### 7.2.5 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

## 7.3 SPLIT output pin and $V_{IO}$ supply pin

Two versions of the TJA1042 are available, only differing in the function of a single pin. Pin 5 is either a SPLIT output pin or a $V_{IO}$ supply pin.

### 7.3.1 SPLIT pin

Using the SPLIT pin on the TJA1042T in conjunction with a split termination network (see Figure 4 and Figure 7) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby mode or when $V_{CC}$ is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

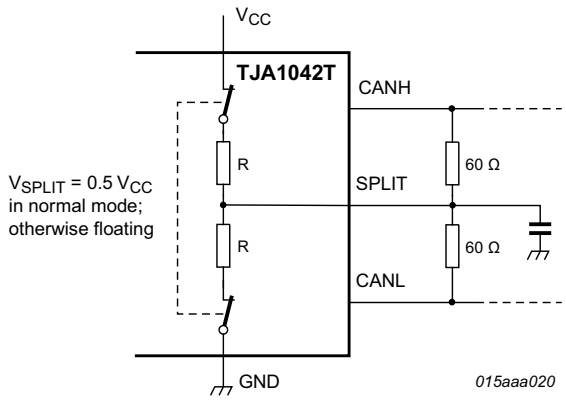



**Fig 4. Stabilization circuitry and application for version with SPLIT pin**

### 7.3.2 $V_{IO}$ supply pin

Pin $V_{IO}$ on the TTJA1042T/3 and TJA1042TK/3 should be connected to the microcontroller supply voltage (see Figure 8). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin $V_{IO}$ also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin $V_{CC}$.

For versions of the TJA1042 without a $V_{IO}$ pin, the $V_{IO}$ input is internally connected to $V_{CC}$. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V microcontrollers.


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# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_x$ | voltage on pin x[1] | on pins CANH, CANL and SPLIT | −58 | +58 | V |
| | | on any other pin | −0.3 | +7 | V |
| $V_{(CANH-CANL)}$ | voltage between pin CANH and pin CANL | | −27 | +27 | V |
| $V_{trt}$ | transient voltage | on pins CANH, CANL [2] | | | |
| | | pulse 1 | −100 | - | V |
| | | pulse 2a | - | 75 | V |
| | | pulse 3a | −150 | - | V |
| | | pulse 3b | - | 100 | V |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2 (150 pF, 330 Ω) [3] | | | |
| | | at pins CANH and CANL | −8 | +8 | kV |
| | | Human Body Model (HBM); 100 pF, 1.5 kΩ [4] | | | |
| | | at pins CANH and CANL | −8 | +8 | kV |
| | | at any other pin | −4 | +4 | kV |
| | | Machine Model (MM); 200 pF, 0.75 μH, 10 Ω [5] | | | |
| | | at any pin | −300 | +300 | V |
| | | Charged Device Model (CDM); field Induced charge; 4 pF [6] | | | |
| | | at corner pins | −750 | +750 | V |
| | | at any pin | −500 | +500 | V |
| $T_{vj}$ | virtual junction temperature | [7] | −40 | +150 | °C |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004-06.

[3] According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000-4-2.

[4] According to AEC-Q100-002.

[5] According to AEC-Q100-003.

[6] According to AEC-Q100-011 Rev-C1. The classification level is C4B.

[7] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of $T_{vj}$. The rating for $T_{vj}$ limits the allowable combinations of power dissipation (P) and ambient temperature ($T_{amb}$).

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

*According to IEC 60747-1.*

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | thermal resistance from virtual junction to ambient | SO8 package; in free air | 145 | K/W |
| | | HVSON8 package; in free air | 50 | K/W |


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# 10. Static characteristics

**Table 7. Static characteristics**

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.5 V to 5.5 V; $V_{IO}$ = 2.8 V to 5.5 V[1]; $R_L$ = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply; pin $V_{CC}$** | | | | | | |
| $V_{CC}$ | supply voltage | | 4.5 | - | 5.5 | V |
| $V_{uvd(VCC)}$ | undervoltage detection voltage on pin $V_{CC}$ | | 3.5 | - | 4.5 | V |
| $I_{CC}$ | supply current | Standby mode | | | | |
| | | TJA1042T; includes $I_{IO}$; $V_{TXD}$ = $V_{IO}$[3] | - | 10 | 15 | µA |
| | | TJA1042T/3 or TJA1042TK/3 | - | - | 5 | µA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD}$ = $V_{IO}$[3] | 2.5 | 5 | 10 | mA |
| | | dominant; $V_{TXD}$ = 0 V | 20 | 45 | 70 | mA |
| | | dominant; $V_{TXD}$ = 0 V; short circuit on bus lines; −3 V < ($V_{CANH}$ = $V_{CANL}$) < +18 V | 2.5 | 80 | 110 | mA |
| **I/O level adapter supply; pin $V_{IO}$[1]** | | | | | | |
| $V_{IO}$ | supply voltage on pin $V_{IO}$ | | 2.8 | - | 5.5 | V |
| $V_{uvd(VIO)}$ | undervoltage detection voltage on pin $V_{IO}$ | | 1.3 | 2.0 | 2.7 | V |
| $I_{IO}$ | supply current on pin $V_{IO}$ | Standby mode; $V_{TXD}$ = $V_{IO}$[3] | 5 | - | 14 | µA |
| | | Normal mode | | | | |
| | | recessive; $V_{TXD}$ = $V_{IO}$[3] | 15 | 80 | 200 | µA |
| | | dominant; $V_{TXD}$ = 0 V | - | 350 | 1000 | µA |
| **Standby mode control input; pin STB** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | [4] | 0.7$V_{IO}$[3] | - | $V_{IO}$[3] + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.3$V_{IO}$[3] | V |
| $I_{IH}$ | HIGH-level input current | $V_{STB}$ = $V_{IO}$[3] | −1 | - | +1 | µA |
| $I_{IL}$ | LOW-level input current | $V_{STB}$ = 0 V | −15 | - | −1 | µA |
| **CAN transmit data input; pin TXD** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | [4] | 0.7$V_{IO}$[3] | - | $V_{IO}$[3] + 0.3 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.3 | - | 0.3$V_{IO}$[3] | V |
| $I_{IH}$ | HIGH-level input current | $V_{TXD}$ = $V_{IO}$[3] | −5 | - | +5 | µA |
| $I_{IL}$ | LOW-level input current | $V_{TXD}$ = 0 V | −260 | −150 | −30 | µA |
| $C_i$ | input capacitance | [5] | - | 5 | 10 | pF |
| **CAN receive data output; pin RXD** | | | | | | |
| $I_{OH}$ | HIGH-level output current | $V_{RXD}$ = $V_{IO}$ − 0.4 V [3] | −8 | −3 | −1 | mA |
| $I_{OL}$ | LOW-level output current | $V_{RXD}$ = 0.4 V; bus dominant | 2 | 5 | 12 | mA |


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**Table 7. Static characteristics** *...continued*

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.5 V to 5.5 V; $V_{IO}$ = 2.8 V to 5.5 V[1]; $R_L$ = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Bus lines; pins CANH and CANL** | | | | | | |
| $V_{O(dom)}$ | dominant output voltage | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$ | | | | |
| | | pin CANH; $R_L$ = 50 Ω to 65 Ω | 2.75 | 3.5 | 4.5 | V |
| | | pin CANL; $R_L$ = 50 Ω to 65 Ω | 0.5 | 1.5 | 2.25 | V |
| $V_{dom(TX)sym}$ | transmitter dominant voltage symmetry | $V_{dom(TX)sym}$ = $V_{CC}$ − $V_{CANH}$ − $V_{CANL}$ | −400 | - | +400 | mV |
| $V_{TXsym}$ | transmitter voltage symmetry | $V_{TXsym}$ = $V_{CANH}$ + $V_{CANL}$; $f_{TXD}$ = 250 kHz, 1 MHz and 2.5 MHz; $C_{SPLIT}$ = 4.7 nF; $V_{CC}$ = 4.75 V to 5.25 V [5] [6] | 0.9$V_{CC}$ | - | 1.1$V_{CC}$ | V |
| $V_{O(dif)}$ | differential output voltage | dominant: Normal mode; $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$; $V_{CC}$ = 4.75 V to 5.25 V | | | | |
| | | $R_L$ = 45 Ω to 65 Ω | 1.5 | - | 3 | V |
| | | $R_L$ = 45 Ω to 70 Ω | 1.5 | - | 3.3 | V |
| | | $R_L$ = 2240 Ω | 1.5 | - | 5 | V |
| | | recessive; no load | | | | |
| | | Normal mode: $V_{TXD}$ = $V_{IO}$[3] | −50 | - | +50 | mV |
| | | Standby mode | −0.2 | - | +0.2 | V |
| $V_{O(rec)}$ | recessive output voltage | Normal mode; $V_{TXD}$ = $V_{IO}$[3]; no load | 2 | 0.5$V_{CC}$ | 3 | V |
| | | Standby mode; no load | −0.1 | - | +0.1 | V |
| $V_{th(RX)dif}$ | differential receiver threshold voltage | −30 V ≤ $V_{CANL}$ ≤ +30 V; −30 V ≤ $V_{CANH}$ ≤ +30 V | | | | |
| | | Normal mode | 0.5 | 0.7 | 0.9 | V |
| | | Standby mode [7] | 0.4 | 0.7 | 1.15 | V |
| $V_{rec(RX)}$ | receiver recessive voltage | −30 V ≤ $V_{CANL}$ ≤ +30 V; −30 V ≤ $V_{CANH}$ ≤ +30 V | | | | |
| | | Normal mode | −4 | - | 0.5 | V |
| | | Standby mode | −4 | - | 0.4 | V |
| $V_{dom(RX)}$ | receiver dominant voltage | −30 V ≤ $V_{CANL}$ ≤ +30 V; −30 V ≤ $V_{CANH}$ ≤ +30 V | | | | |
| | | Normal mode | 0.9 | - | 9.0 | V |
| | | Standby mode | 1.15 | - | 9.0 | V |
| $V_{hys(RX)dif}$ | differential receiver hysteresis voltage | −30 V ≤ $V_{CANL}$ ≤ +30 V; −30 V ≤ $V_{CANH}$ ≤ +30 V | 50 | 120 | 200 | mV |
| $I_{O(sc)dom}$ | dominant short-circuit output current | $V_{TXD}$ = 0 V; t < $t_{to(dom)TXD}$; $V_{CC}$ = 5 V | | | | |
| | | pin CANH; $V_{CANH}$ = −15 V to +40 V | −100 | −70 | −40 | mA |
| | | pin CANL; $V_{CANL}$ = −15 V to +40 V | 40 | 70 | 100 | mA |
| $I_{O(sc)rec}$ | recessive short-circuit output current | Normal mode; $V_{TXD}$ = $V_{IO}$[3] $V_{CANH}$ = $V_{CANL}$ = −27 V to +32 V | −5 | - | +5 | mA |
| $I_L$ | leakage current | $V_{CC}$ = $V_{IO}$ = 0 V or $V_{CC}$ = $V_{IO}$ = shorted to ground via 47 kΩ; $V_{CANH}$ = $V_{CANL}$ = 5 V | −5 | - | +5 | µA |
| $R_i$ | input resistance | −2 V ≤ $V_{CANL}$ ≤ +7 V; −2 V ≤ $V_{CANH}$ ≤ +7 V [5] | 9 | 15 | 28 | kΩ |


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**Table 7. Static characteristics** *...continued*

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.5 V to 5.5 V; $V_{IO}$ = 2.8 V to 5.5 V[1]; $R_L$ = 60 Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta R_i$ | input resistance deviation | 0 V ≤ $V_{CANL}$ ≤ +5 V; 0 V ≤ $V_{CANH}$ ≤ +5 V [5] | −1 | - | +1 | % |
| $R_{i(dif)}$ | differential input resistance | −2 V ≤ $V_{CANL}$ ≤ +7 V; −2 V ≤ $V_{CANH}$ ≤ +7 V [5] | 19 | 30 | 52 | kΩ |
| $C_{i(cm)}$ | common-mode input capacitance | [5] | - | - | 20 | pF |
| $C_{i(dif)}$ | differential input capacitance | [5] | - | - | 10 | pF |
| **Common mode stabilization output; pin SPLIT; only for TJA1042T** | | | | | | |
| $V_O$ | output voltage | Normal mode $I_{SPLIT}$ = −500 µA to +500 µA | 0.3$V_{CC}$ | 0.5$V_{CC}$ | 0.7$V_{CC}$ | V |
| | | Normal mode; $R_L$ = 1 MΩ | 0.45$V_{CC}$ | 0.5$V_{CC}$ | 0.55$V_{CC}$ | V |
| $I_L$ | leakage current | Standby mode $V_{SPLIT}$ = −58 V to +58 V | −5 | - | +5 | µA |
| **Temperature detection** | | | | | | |
| $T_{j(sd)}$ | shutdown junction temperature | [5] | - | 190 | - | °C |

[1] Only TJA1042T/3 and TJA1042TK/3 have a $V_{IO}$ pin. With TJA1042T, the $V_{IO}$ input is internally connected to $V_{CC}$.

[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] $V_{IO}$ = $V_{CC}$ for the non-$V_{IO}$ product variant TJA1042T.

[4] Maximum value assumes $V_{CC}$ < $V_{IO}$; if $V_{CC}$ > $V_{IO}$, the maximum value will be $V_{CC}$ + 0.3 V.

[5] Not tested in production; guaranteed by design.

[6] The test circuit used to measure the bus output voltage symmetry (which includes CSPLIT) is shown in Figure 10.

[7] For TJA1042T/3 and TJA1042TK/3: values valid when $V_{IO}$ = 4.5 V to 5.5 V; when $V_{IO}$ = 2.8 V to 4.5 V, values valid when −12 V ≤ $V_{CANL}$ ≤ +12 V, −12 V ≤ $V_{CANH}$ ≤ +12 V.

# 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.5 V to 5.5 V; $V_{IO}$ = 2.8 V to 5.5 V[1]; $R_L$ = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Transceiver timing; pins CANH, CANL, TXD and RXD; see Figure 5 and Figure 9** | | | | | | |
| $t_{d(TXD-busdom)}$ | delay time from TXD to bus dominant | Normal mode | - | 65 | - | ns |
| $t_{d(TXD-busrec)}$ | delay time from TXD to bus recessive | Normal mode | - | 90 | - | ns |
| $t_{d(busdom-RXD)}$ | delay time from bus dominant to RXD | Normal mode | - | 60 | - | ns |
| $t_{d(busrec-RXD)}$ | delay time from bus recessive to RXD | Normal mode | - | 65 | - | ns |
| $t_{d(TXDL-RXDL)}$ | delay time from TXD LOW to RXD LOW | version with SPLIT pin; Normal mode | 60 | - | 220 | ns |
| | | versions with $V_{IO}$ pin; Normal mode | 60 | - | 250 | ns |


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**Table 8. Dynamic characteristics** *...continued*

*$T_{vj}$ = −40 °C to +150 °C; $V_{CC}$ = 4.5 V to 5.5 V; $V_{IO}$ = 2.8 V to 5.5 V[1]; $R_L$ = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.[2]*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(TXDH-RXDH)}$ | delay time from TXD HIGH to RXD HIGH | version with SPLIT pin; Normal mode | 60 | - | 220 | ns |
| | | versions with $V_{IO}$ pin; Normal mode | 60 | - | 250 | ns |
| $t_{bit(bus)}$ | transmitted recessive bit width | $t_{bit(TXD)}$ = 500 ns [3] | 435 | - | 530 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 155 | - | 210 | ns |
| $t_{bit(RXD)}$ | bit time on pin RXD | $t_{bit(TXD)}$ = 500 ns [3] | 400 | - | 550 | ns |
| | | $t_{bit(TXD)}$ = 200 ns [3] | 120 | - | 220 | ns |
| $\Delta t_{rec}$ | receiver timing symmetry | $t_{bit(TXD)}$ = 500 ns | −65 | - | +40 | ns |
| | | $t_{bit(TXD)}$ = 200 ns | −45 | - | +15 | ns |
| $t_{to(dom)TXD}$ | TXD dominant time-out time | $V_{TXD}$ = 0 V; Normal mode [4] | 0.3 | 2 | 5 | ms |
| $t_{to(dom)bus}$ | bus dominant time-out time | Standby mode | 0.3 | 2 | 5 | ms |
| $t_{fltr(wake)bus}$ | bus wake-up filter time | version with SPLIT pin Standby mode | 0.5 | 1 | 3 | µs |
| | | versions with $V_{IO}$ pin Standby mode | 0.5 | 1.5 | 5 | µs |
| $t_{d(stb-norm)}$ | standby to normal mode delay time | | 7 | 25 | 47 | µs |

[1] Only TJA1042T/3 and TJA1042TK/3 have a $V_{IO}$ pin. With TJA1042T, the $V_{IO}$ input is internally connected to $V_{CC}$.

[2] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[3] See Figure 6.

[4] Minimum value of 0.8 ms required according to SAE J2284; 0.3 ms is allowed according to ISO11898-2:2016 for legacy devices.


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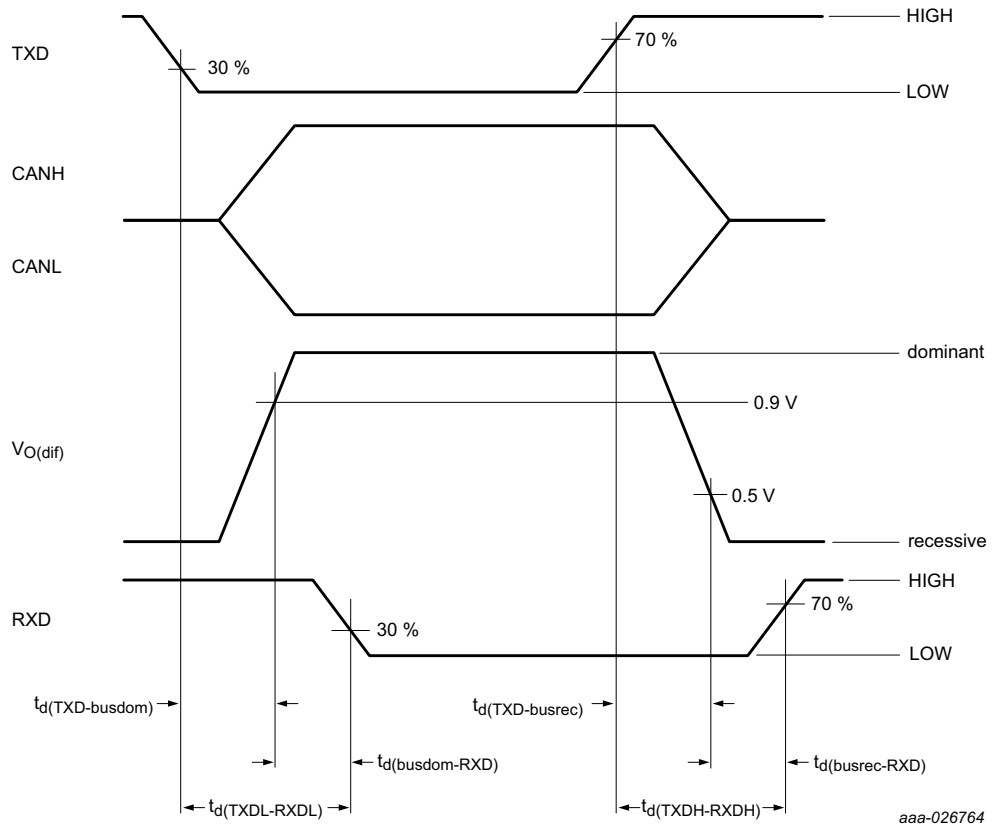



**Fig 5. CAN transceiver timing diagram**

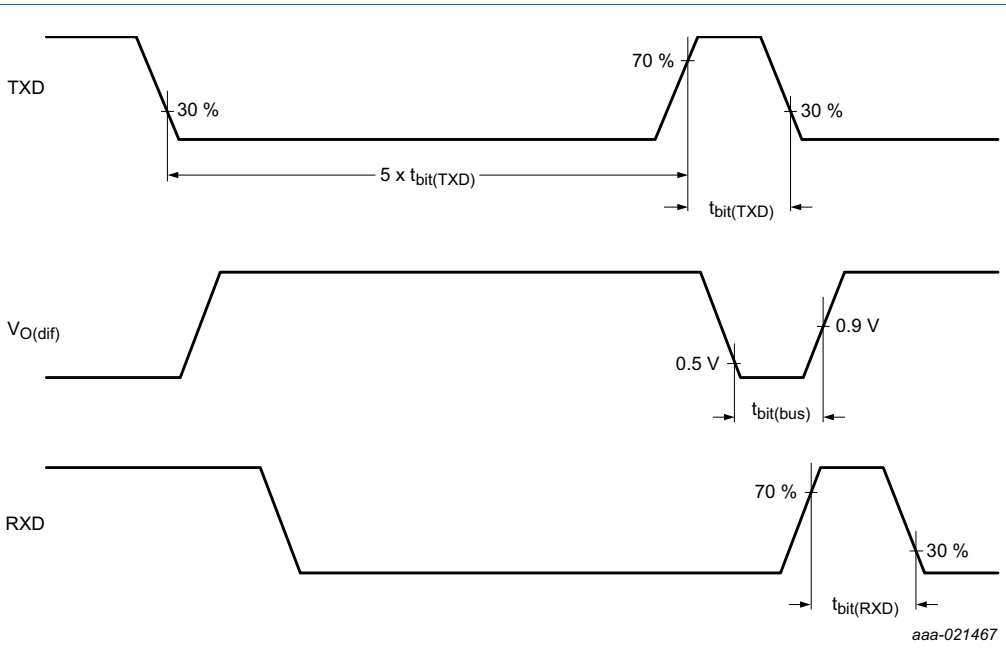


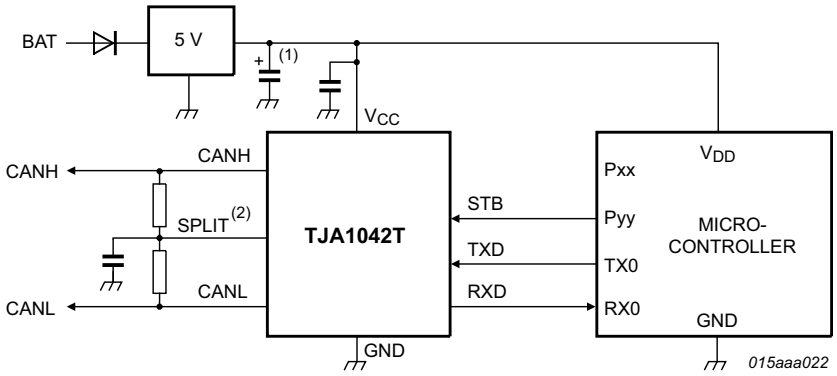

**Fig 6. CAN FD timing definitions according to ISO 11898-2:2016**


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# 12. Application information

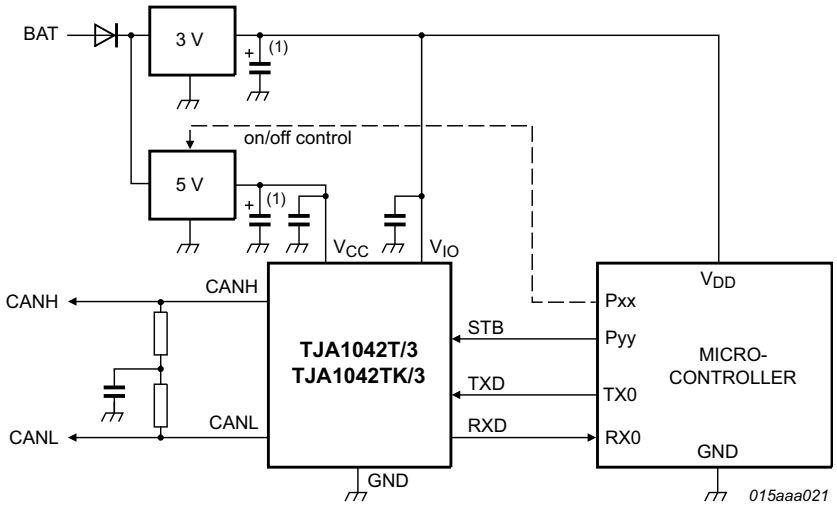
## 12.1 Application diagrams




(1) Optional, depends on regulator.

(2) Optional common mode stabilization by a voltage source of $V_{CC}/2$ at pin SPLIT.

**Fig 7. Typical application with TJA1042T and a 5 V microcontroller.**




(1) Optional, depends on regulator.

**Fig 8. Typical application with TJA1042T/3 or TJA1042TK/3 and a 3 V microcontroller.**

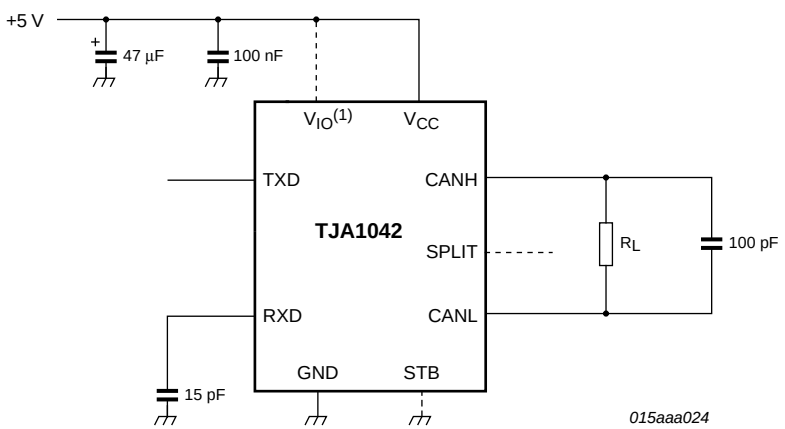
## 12.2 Application hints

Further information on the application of the TJA1042 can be found in NXP application hints *AH1014 'Application Hints - Standalone high speed CAN transceiver TJA1042/TJA1043/TJA1048/TJA1051'.*


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# 13. Test information




(1) For versions with a $V_{IO}$ pin (TJA1042T/3 and TJA1042TK/3), the $V_{IO}$ pin is connected to pin $V_{CC}$.

**Fig 9. Timing test circuit for CAN transceiver**

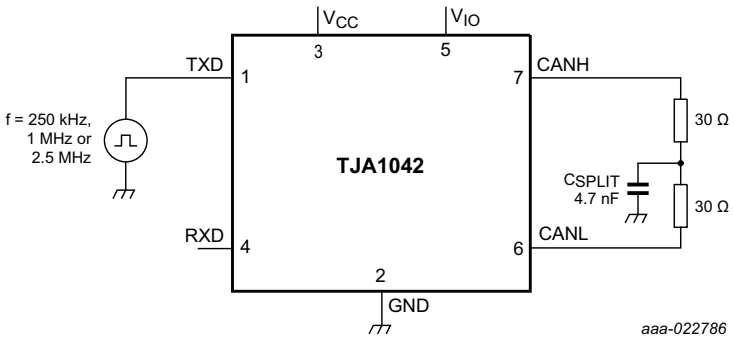



**Fig 10. Test circuit for measuring transceiver driver symmetry**

## 13.1 Quality information

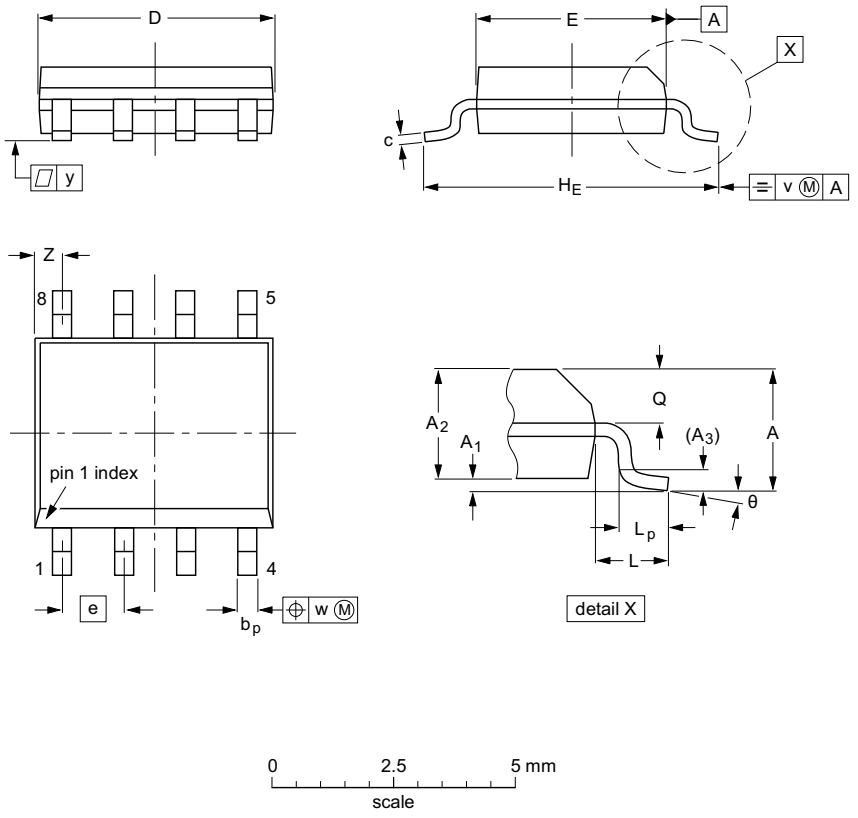
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.


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## 14. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

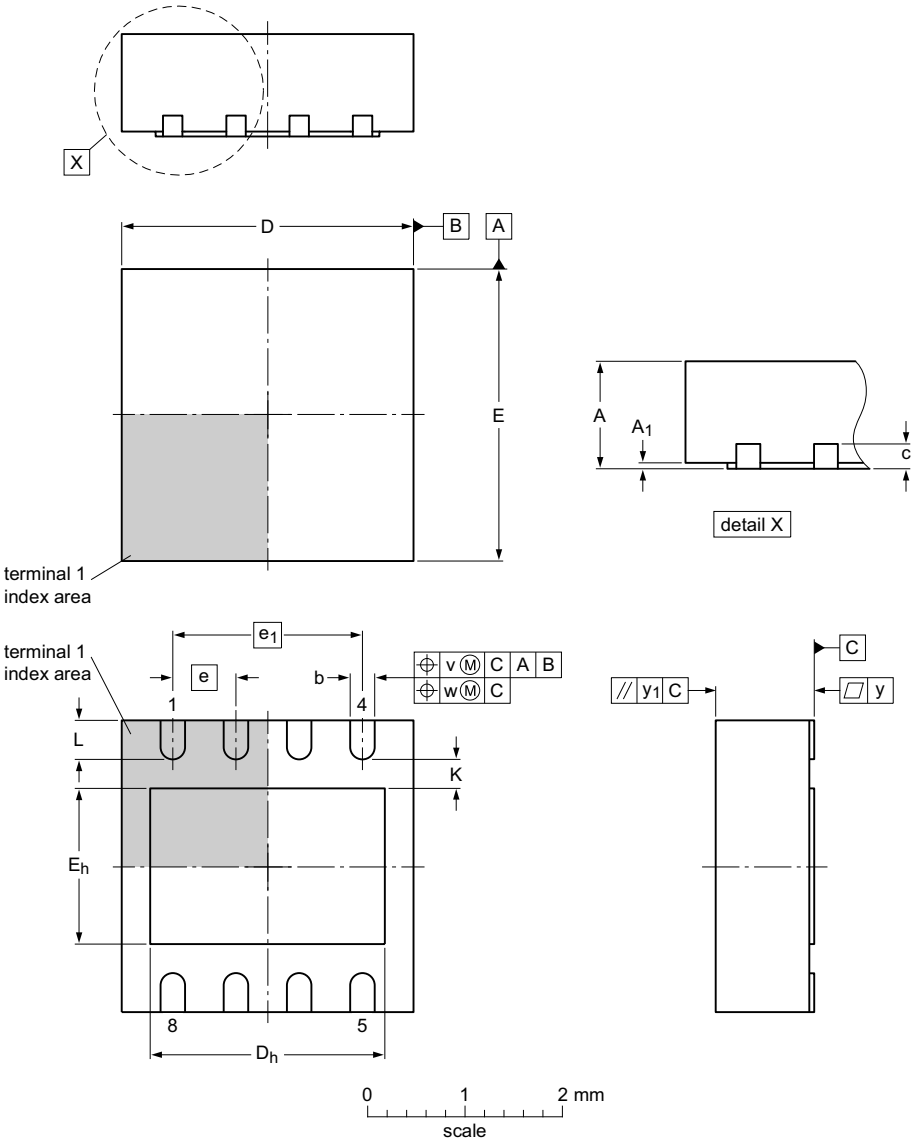
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig 11. Package outline SOT96-1 (SO8)**


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**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm** **SOT782-1**




Dimensions

| Unit(1) | | A | A1 | b | c | D | Dh | E | Eh | e | e1 | K | L | v | w | y | y1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.00 | 0.05 | 0.35 | | 3.10 | 2.45 | 3.10 | 1.65 | | | 0.35 | 0.45 | | | | |
| | nom | 0.85 | 0.03 | 0.30 | 0.2 | 3.00 | 2.40 | 3.00 | 1.60 | 0.65 | 1.95 | 0.30 | 0.40 | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | 0.80 | 0.00 | 0.25 | | 2.90 | 2.35 | 2.90 | 1.55 | | | 0.25 | 0.35 | | | | |

Note

1. Plastic or metal protrusions of 0.075 maximum per side are not included.

*sot782-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT782-1 | - - - | MO-229 | - - - | | | ~~09-08-25~~ 09-08-28 |

**Fig 12. Package outline SOT782-1 (HVSON8)**


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# 15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

# 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 16.3 Wave soldering

Key characteristics in wave soldering are:


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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

**Table 9. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 10. Lead-free process (from J-STD-020D)**

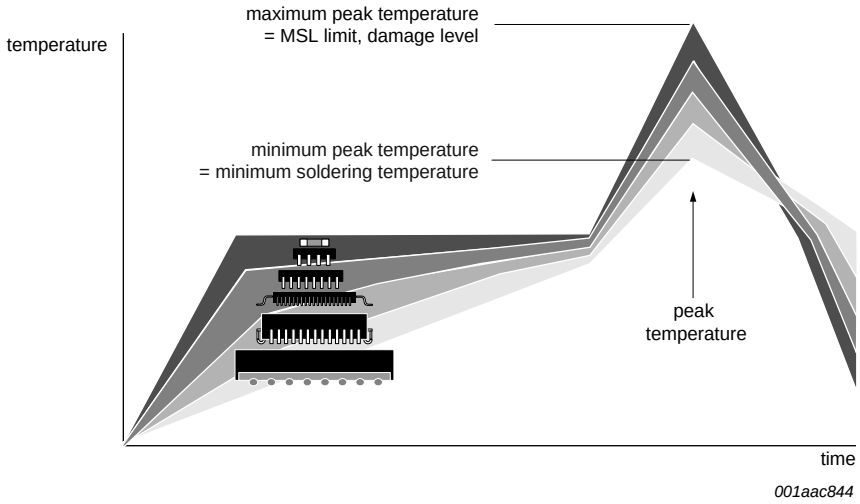
| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.


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MSL: Moisture Sensitivity Level

**Fig 13. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*


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# 18. Appendix: ISO 11898-2:2016 parameter cross-reference list

**Table 11. ISO 11898-2:2016 to NXP data sheet parameter conversion**

| ISO 11898-2:2016 | | NXP data sheet | |
|---|---|---|---|
| **Parameter** | **Notation** | **Symbol** | **Parameter** |
| **HS-PMA dominant output characteristics** | | | |
| Single ended voltage on CAN_H | $V_{CAN_H}$ | $V_{O(dom)}$ | dominant output voltage |
| Single ended voltage on CAN_L | $V_{CAN_L}$ | | |
| Differential voltage on normal bus load | $V_{Diff}$ | $V_{O(dif)}$ | differential output voltage |
| Differential voltage on effective resistance during arbitration | | | |
| Optional: Differential voltage on extended bus load range | | | |
| **HS-PMA driver symmetry** | | | |
| Driver symmetry | $V_{SYM}$ | $V_{TXsym}$ | transmitter voltage symmetry |
| **Maximum HS-PMA driver output current** | | | |
| Absolute current on CAN_H | $I_{CAN_H}$ | $I_{O(sc)dom}$ | dominant short-circuit output current |
| Absolute current on CAN_L | $I_{CAN_L}$ | | |
| **HS-PMA recessive output characteristics, bus biasing active/inactive** | | | |
| Single ended output voltage on CAN_H | $V_{CAN_H}$ | $V_{O(rec)}$ | recessive output voltage |
| Single ended output voltage on CAN_L | $V_{CAN_L}$ | | |
| Differential output voltage | $V_{Diff}$ | $V_{O(dif)}$ | differential output voltage |
| **Optional HS-PMA transmit dominant timeout** | | | |
| Transmit dominant timeout, long | $t_{dom}$ | $t_{to(dom)TXD}$ | TXD dominant time-out time |
| Transmit dominant timeout, short | | | |
| **HS-PMA static receiver input characteristics, bus biasing active/inactive** | | | |
| Recessive state differential input voltage range<br>Dominant state differential input voltage range | $V_{Diff}$ | $V_{th(RX)dif}$ | differential receiver threshold voltage |
| | | $V_{rec(RX)}$ | receiver recessive voltage |
| | | $V_{dom(RX)}$ | receiver dominant voltage |
| **HS-PMA receiver input resistance (matching)** | | | |
| Differential internal resistance | $R_{Diff}$ | $R_{i(dif)}$ | differential input resistance |
| Single ended internal resistance | $R_{CAN_H}$<br>$R_{CAN_L}$ | $R_i$ | input resistance |
| Matching of internal resistance | MR | $\Delta R_i$ | input resistance deviation |
| **HS-PMA implementation loop delay requirement** | | | |
| Loop delay | $t_{Loop}$ | $t_{d(TXDH-RXDH)}$ | delay time from TXD HIGH to RXD HIGH |
| | | $t_{d(TXDL-RXDL)}$ | delay time from TXD LOW to RXD LOW |
| **Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s up to 2 Mbit/s and above 2 Mbit/s up to 5 Mbit/s** | | | |
| Transmitted recessive bit width @ 2 Mbit/s / @ 5 Mbit/s, intended | $t_{Bit(Bus)}$ | $t_{bit(bus)}$ | transmitted recessive bit width |
| Received recessive bit width @ 2 Mbit/s / @ 5 Mbit/s | $t_{Bit(RXD)}$ | $t_{bit(RXD)}$ | bit time on pin RXD |
| Receiver timing symmetry @ 2 Mbit/s / @ 5 Mbit/s | $\Delta t_{Rec}$ | $\Delta t_{rec}$ | receiver timing symmetry |


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**Table 11. ISO 11898-2:2016 to NXP data sheet parameter conversion** *…continued*

| ISO 11898-2:2016 | | NXP data sheet | |
|---|---|---|---|
| **Parameter** | **Notation** | **Symbol** | **Parameter** |
| **HS-PMA maximum ratings of $V_{CAN_H}$, $V_{CAN_L}$ and $V_{Diff}$** | | | |
| Maximum rating $V_{Diff}$ | $V_{Diff}$ | $V_{(CANH-CANL)}$ | voltage between pin CANH and pin CANL |
| General maximum rating $V_{CAN_H}$ and $V_{CAN_L}$ | $V_{CAN_H}$ $V_{CAN_L}$ | $V_x$ | voltage on pin x |
| Optional: Extended maximum rating VCAN_H and VCAN_L | | | |
| **HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered** | | | |
| Leakage current on CAN_H, CAN_L | $I_{CAN_H}$ $I_{CAN_L}$ | $I_L$ | leakage current |
| **HS-PMA bus biasing control timings** | | | |
| CAN activity filter time, long | $t_{Filter}$ | $t_{wake(busdom)}$[1] | bus dominant wake-up time |
| CAN activity filter time, short | | $t_{wake(busrec)}$[1] | bus recessive wake-up time |
| Wake-up timeout, short | $t_{Wake}$ | $t_{to(wake)bus}$ | bus wake-up time-out time |
| Wake-up timeout, long | | | |
| Timeout for bus inactivity | $t_{Silence}$ | $t_{to(silence)}$ | bus silence time-out time |
| Bus Bias reaction time | $t_{Bias}$ | $t_{d(busact-bias)}$ | delay time from bus active to bias |

[1] $t_{fltr(wake)bus}$ - bus wake-up filter time, in devices with basic wake-up functionality


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## 19. Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TJA1042 v.10 | 20171124 | Product data sheet | - | TJA1042 v.9 |
| Modifications: | • Updated to comply with ISO 11898-2:2016 and SAE J22884-1 through SAE J2284-5 specifications:<br>– Section 1: text amended (2nd last paragraph)<br>– Section 2.1: text amended (1st entry)<br>– Table 7: values changed and/or measurements conditions amended/added for parameters $I_{CC}$, $V_{TXsym}$, $V_{O(dif)}$, $V_{rec(RX)}$, $V_{dom(RX)}$, $I_{O(sc)dom}$, $R_i$, $\Delta R_i$ and $R_{i(dif)}$<br>– Table 8: Table note 4 added<br>– Figure 5: thresholds clarified<br>– Figure 6: title changed<br>• Table 7: Table note 7 revised<br>• Figure 7, Figure 8, Figure 10: amended | | | |
| TJA1042 v.9 | 20160523 | Product data sheet | - | TJA1042 v.8 |
| TJA1042 v.8 | 20150115 | Product data sheet | - | TJA1042 v.7 |
| TJA1042 v.7 | 20120508 | Product data sheet | - | TJA1042 v.6 |
| TJA1042 v.6 | 20110323 | Product data sheet | - | TJA1042 v.5 |
| TJA1042 v.5 | 20110118 | Product data sheet | - | TJA1042 v.4 |
| TJA1042 v.4 | 20091006 | Product data sheet | - | TJA1042 v.3 |
| TJA1042 v.3 | 20090825 | Product data sheet | - | TJA1042 v.2 |
| TJA1042 v.2 | 20090708 | Product data sheet | - | TJA1042 v.1 |
| TJA1042 v.1 | 20090309 | Product data sheet | - | - |


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# 20. Legal information

## 20.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 20.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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## 22. Contents


**1 General description . . . . . 1**
**2 Features and benefits . . . . . 1**
2.1 General . . . . . 1
2.2 Predictable and fail-safe behavior . . . . . 2
2.3 Protections . . . . . 2
**3 Quick reference data . . . . . 2**
**4 Ordering information . . . . . 3**
**5 Block diagram . . . . . 3**
**6 Pinning information . . . . . 4**
6.1 Pinning . . . . . 4
6.2 Pin description . . . . . 4
**7 Functional description . . . . . 5**
7.1 Operating modes . . . . . 5
7.1.1 Normal mode . . . . . 5
7.1.2 Standby mode . . . . . 5
7.2 Fail-safe features . . . . . 6
7.2.1 TXD dominant time-out function . . . . . 6
7.2.2 Bus dominant time-out function . . . . . 6
7.2.3 Internal biasing of TXD and STB input pins . . . 6
7.2.4 Undervoltage detection on pins $V_{CC}$ and $V_{IO}$ . . 6
7.2.5 Overtemperature protection . . . . . 7
7.3 SPLIT output pin and $V_{IO}$ supply pin . . . . . 7
7.3.1 SPLIT pin . . . . . 7
7.3.2 $V_{IO}$ supply pin . . . . . 7
**8 Limiting values . . . . . 8**
**9 Thermal characteristics . . . . . 8**
**10 Static characteristics . . . . . 9**
**11 Dynamic characteristics . . . . . 11**
**12 Application information . . . . . 14**
12.1 Application diagrams . . . . . 14
12.2 Application hints . . . . . 14
**13 Test information . . . . . 15**
13.1 Quality information . . . . . 15
**14 Package outline . . . . . 16**
**15 Handling information . . . . . 18**
**16 Soldering of SMD packages . . . . . 18**
16.1 Introduction to soldering . . . . . 18
16.2 Wave and reflow soldering . . . . . 18
16.3 Wave soldering . . . . . 18
16.4 Reflow soldering . . . . . 19
**17 Soldering of HVSON packages . . . . . 20**
**18 Appendix: ISO 11898-2:2016 parameter cross-reference list . . . . . 21**
**19 Revision history . . . . . 23**
**20 Legal information . . . . . 24**
20.1 Data sheet status . . . . . 24
20.2 Definitions . . . . . 24
20.3 Disclaimers . . . . . 24
20.4 Trademarks . . . . . 25
**21 Contact information . . . . . 25**
**22 Contents . . . . . 26**


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